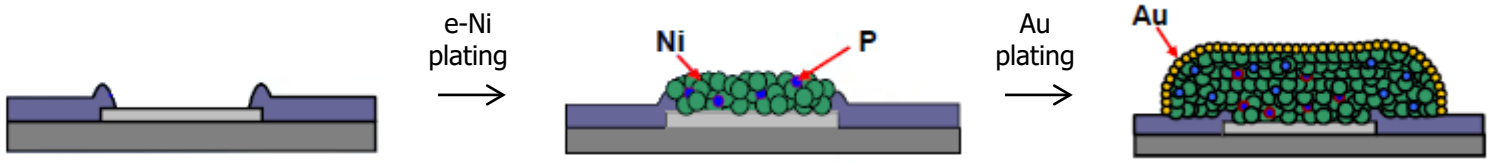
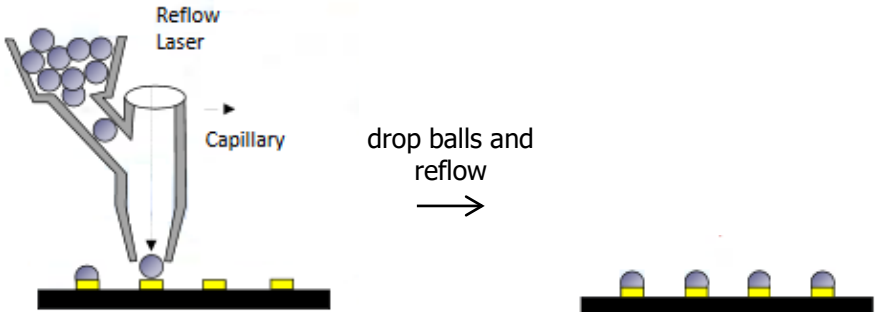
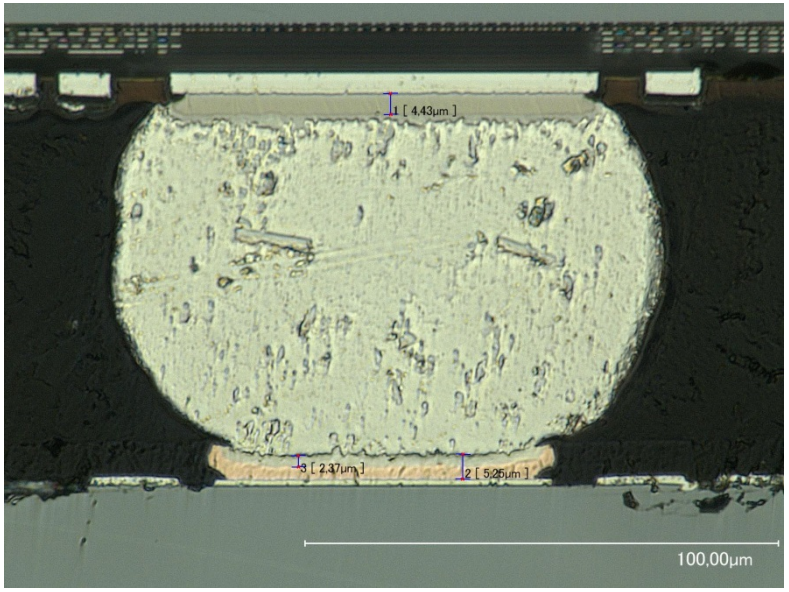
Bumping at PacTech – SwitcherBv2.0

▷ ENIG process: Electroless Nickel Immersion Gold → UBM



▷ Solder ball jetting



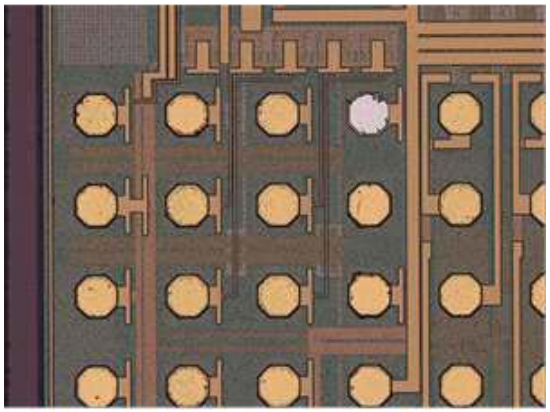


▷ Fully Qualified with SwitcherB18v2.0

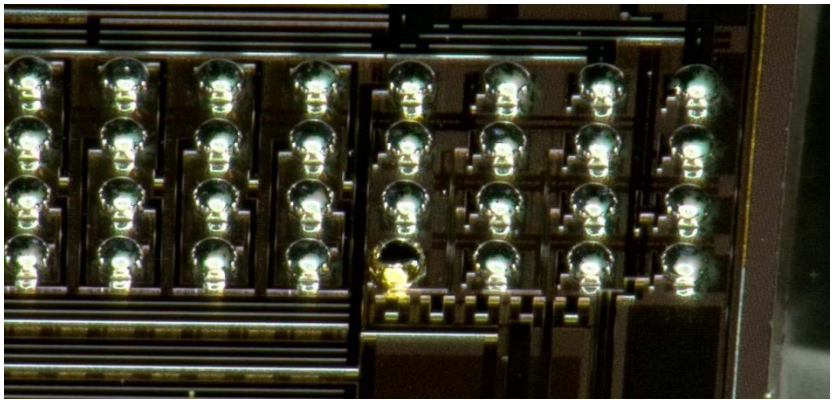
- ↳ Test production
- ↳ X-sections, shear tests, test assemblies … all ok!
- ↳ Assembly of EMCMs, pilot modules, Desy test..

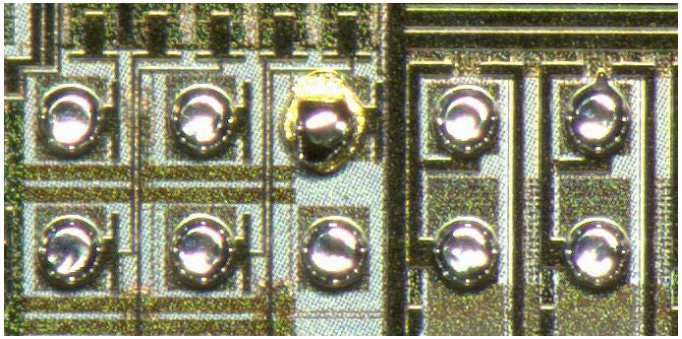
SwitcherBv2.1 bumping

- Bumping (UBM process) causes problems with the new Switcher
- On one pad – the substrate pad – and only on this pad
  - Very little or no Nickel deposition



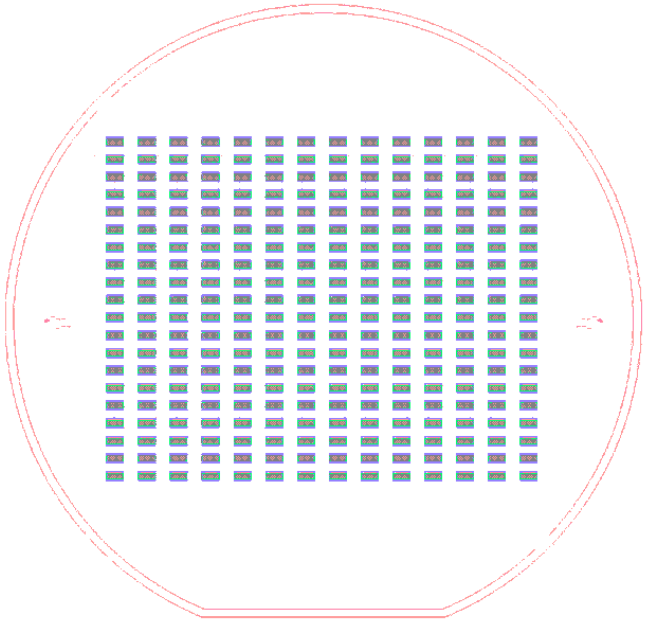
- Main difference to old Switcher
  - Different passivation (1µm Nitride/Oxide <-> PI)
  - Guard ring of the chip exposed, connected to bulk
- Different electrochemical potential causes reduced Ni growth on substrate
- **Trials** with isolated edge **failed** in batch process, workaround(s) **failed/not reliable**

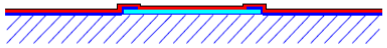




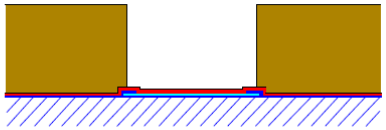
Bumping on “wafer level” at IZM

- Assemble a “wafer” by pick-and-place of Switchers to support with alignment marks
  - Accuracy good enough for 150µm pitch, subsequent wafer level lithography possible
  - Possibility to apply standard technology bumping by electro-plating

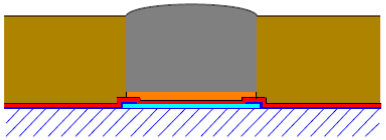




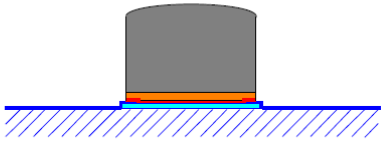
Sputter Etching and Sputtering of the Plating Base / UBM



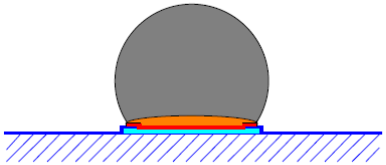
Spin Coating and Printing of Photoresist



Electroplating of Cu and PbSn



Resist Stripping and wet Etching of the Plating Base



Reflow

From the IZM quotation – it's complicated..

Prozesschritte bei IZM:

- Design des Carrierwafers mit Alignmentmarken
- Design des Rekonfigurierten Wafers mit Bumpingmaske
- 2x 9" Lithographiemaske (external vendor)

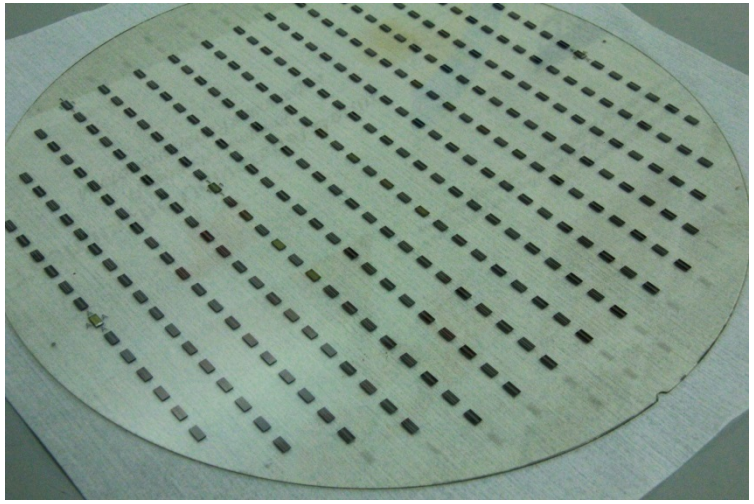
- Strukturierung der Alignmentmarken auf dem Carrierwafer
- Assembly der Chips auf dem Carrierwafer
- Sputtern der Platingbase
- Resist-Lithographie
- Galvanische Abscheidung von UBM oder UBM+SnAg-Bumps (max. 20µm Gesamthöhe)
- Entfernen von Resist und Platingbase
- Reflow
- Ablösen der Chips vom Carrierwafer
- Reinigung und Sortieren in Gel Packs

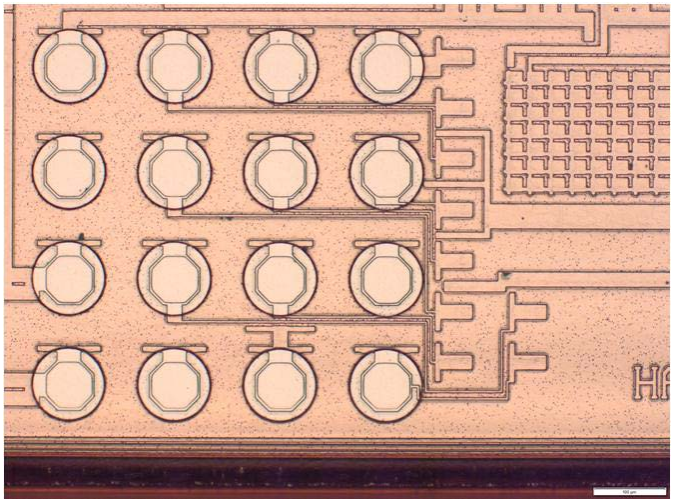
Task 1: Setupbatch mit ca. 30 Chips
Prozessierungsdauer: voraussichtlich 10 Wochen
Fixed Price: 15000, - €

Task 2: Folgebatch nach erfolgreichem Abschluss von Task 1 (Design+Masken aus Task1):
Prozessierungsdauer: voraussichtlich 8 Wochen
Fixed Price (500 Chips): ca. 16000, - €

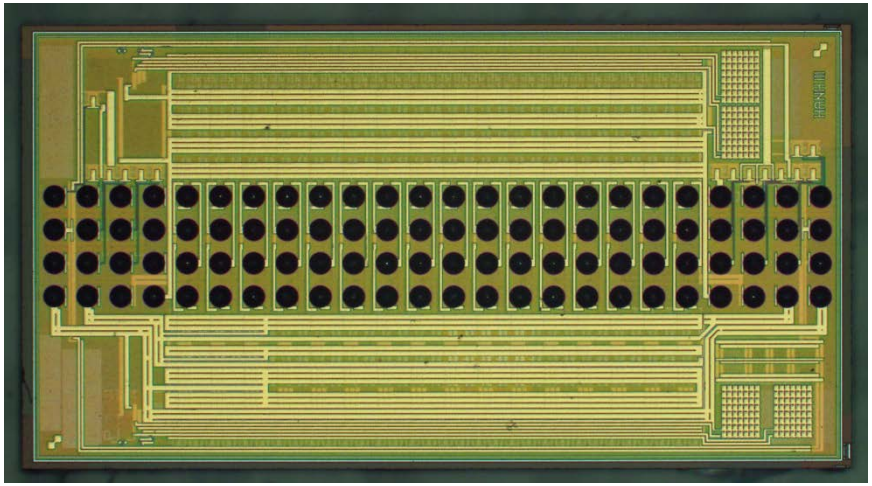
SwitcherBv2.1 bumped at IZM

- Reconfigured Wafer and after seed layer deposition and lithography





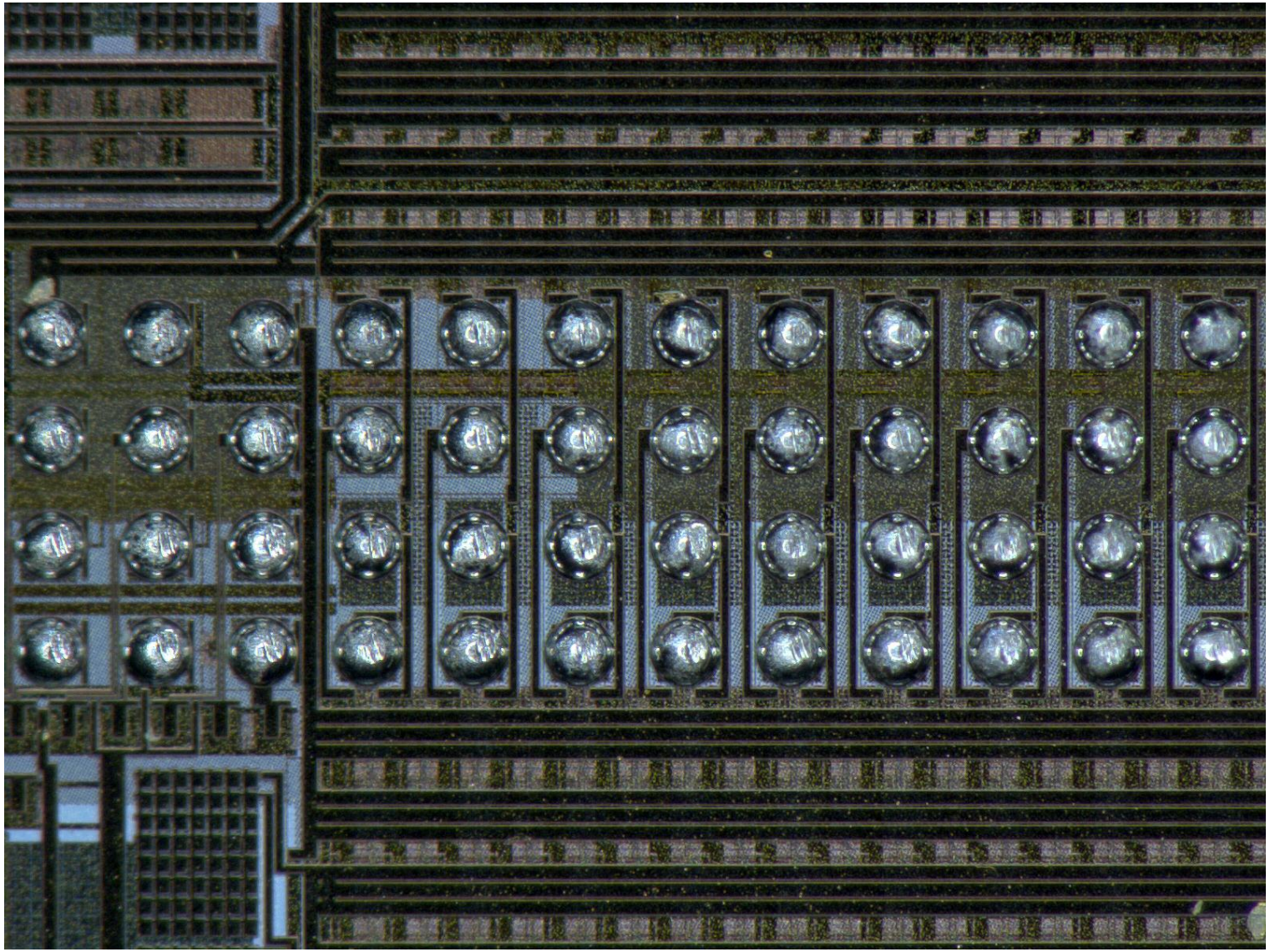
- The bumped chip after reflow



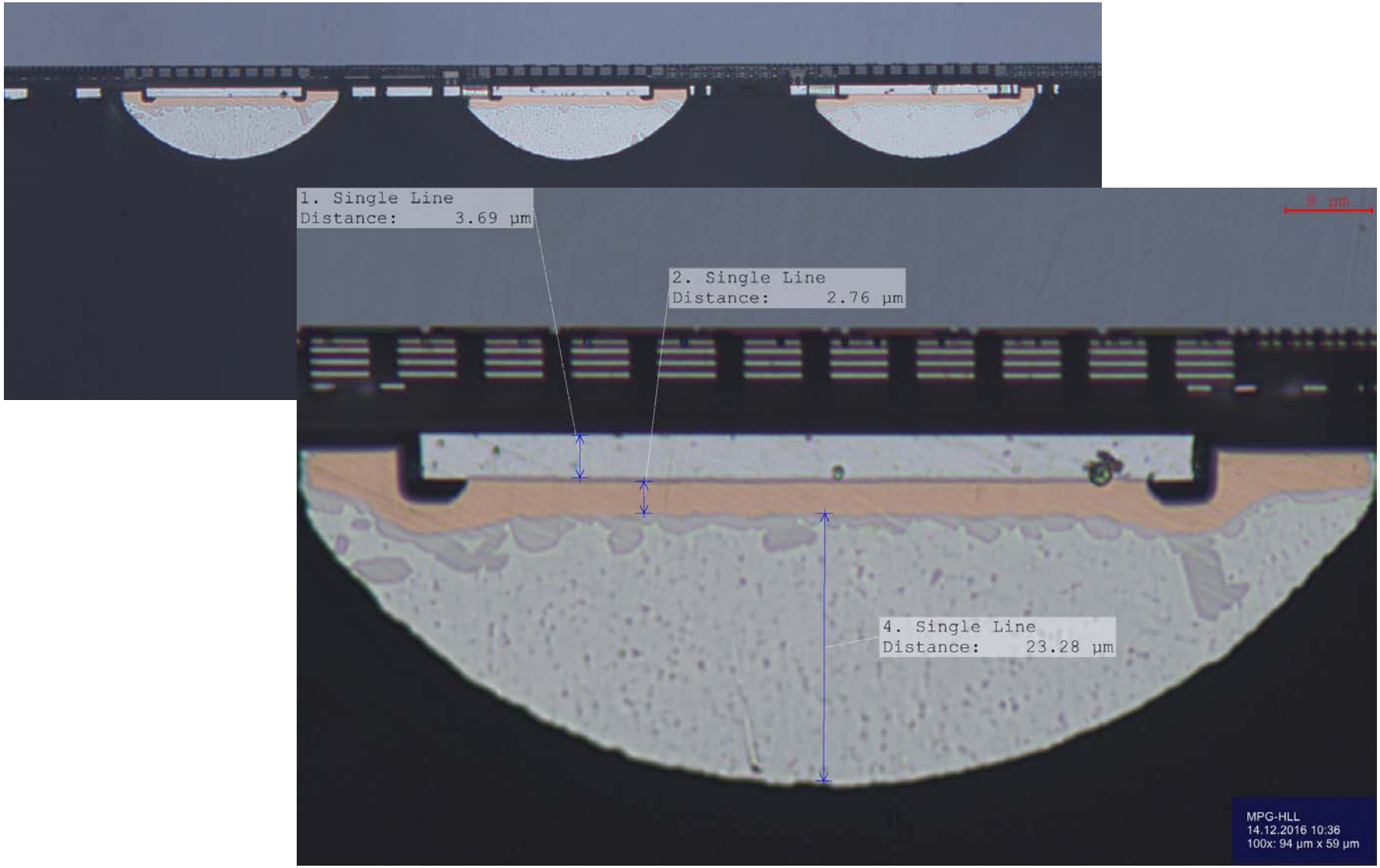
BELLE II- Switcher tests

Switcher Chips	Read JTAG ID	Bias Current	Boost Current	64 HV-channels
18	✓	✓	✓	✓
1	✓	✓	✓	✗
5	✗	✗	✗	✗

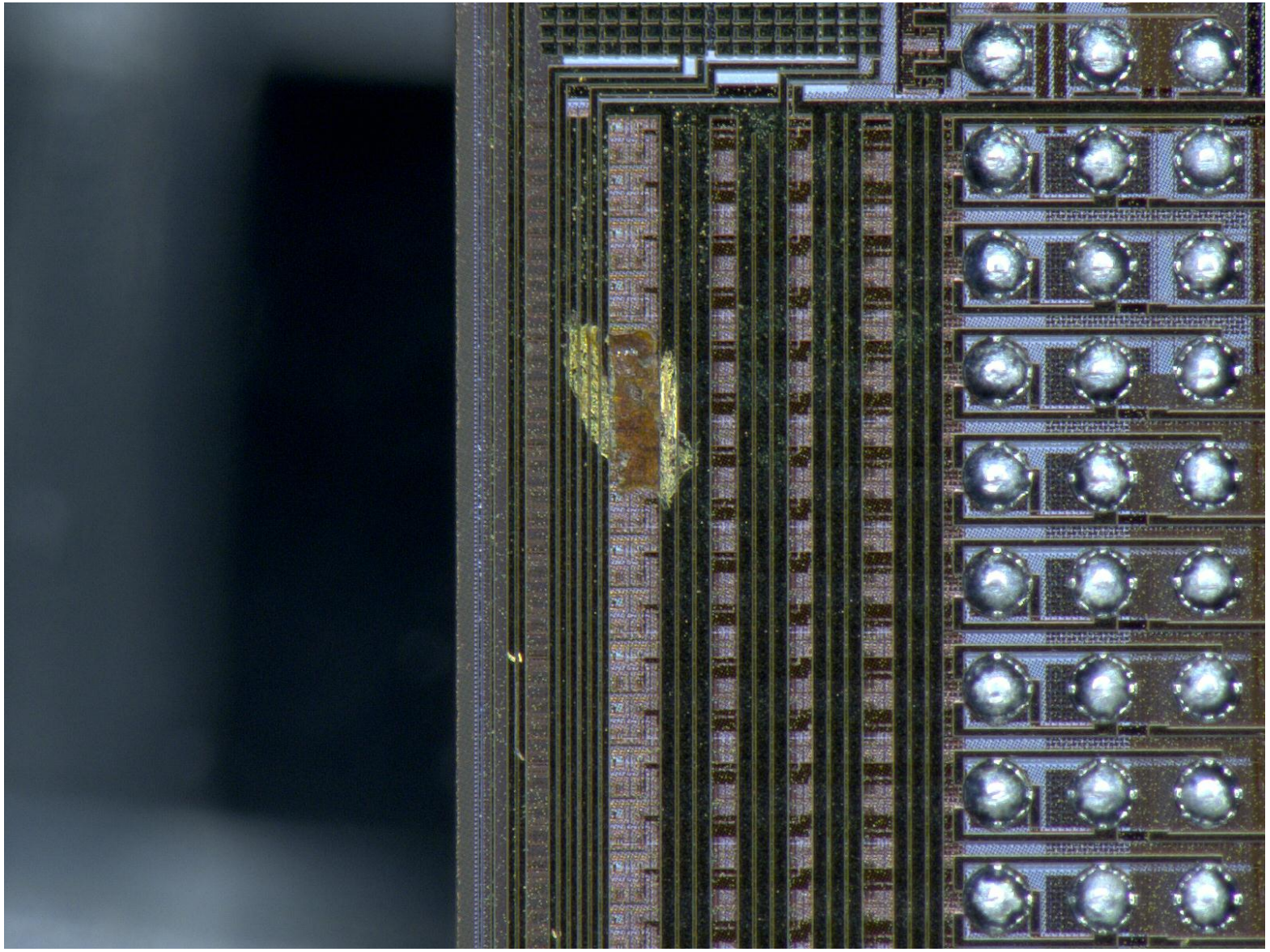
Traces from probe card testing at KIT



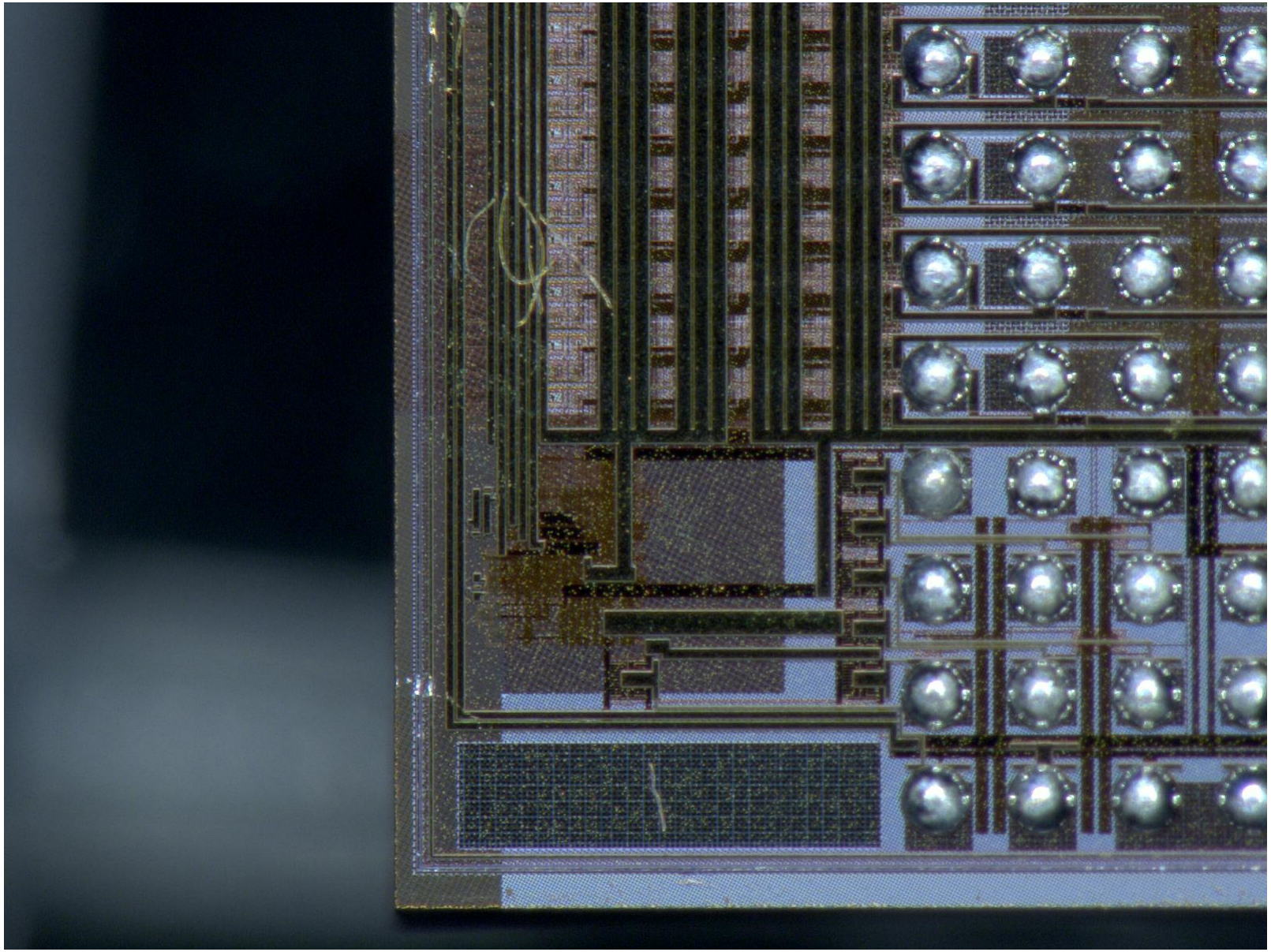
Cross section of IZM bumps



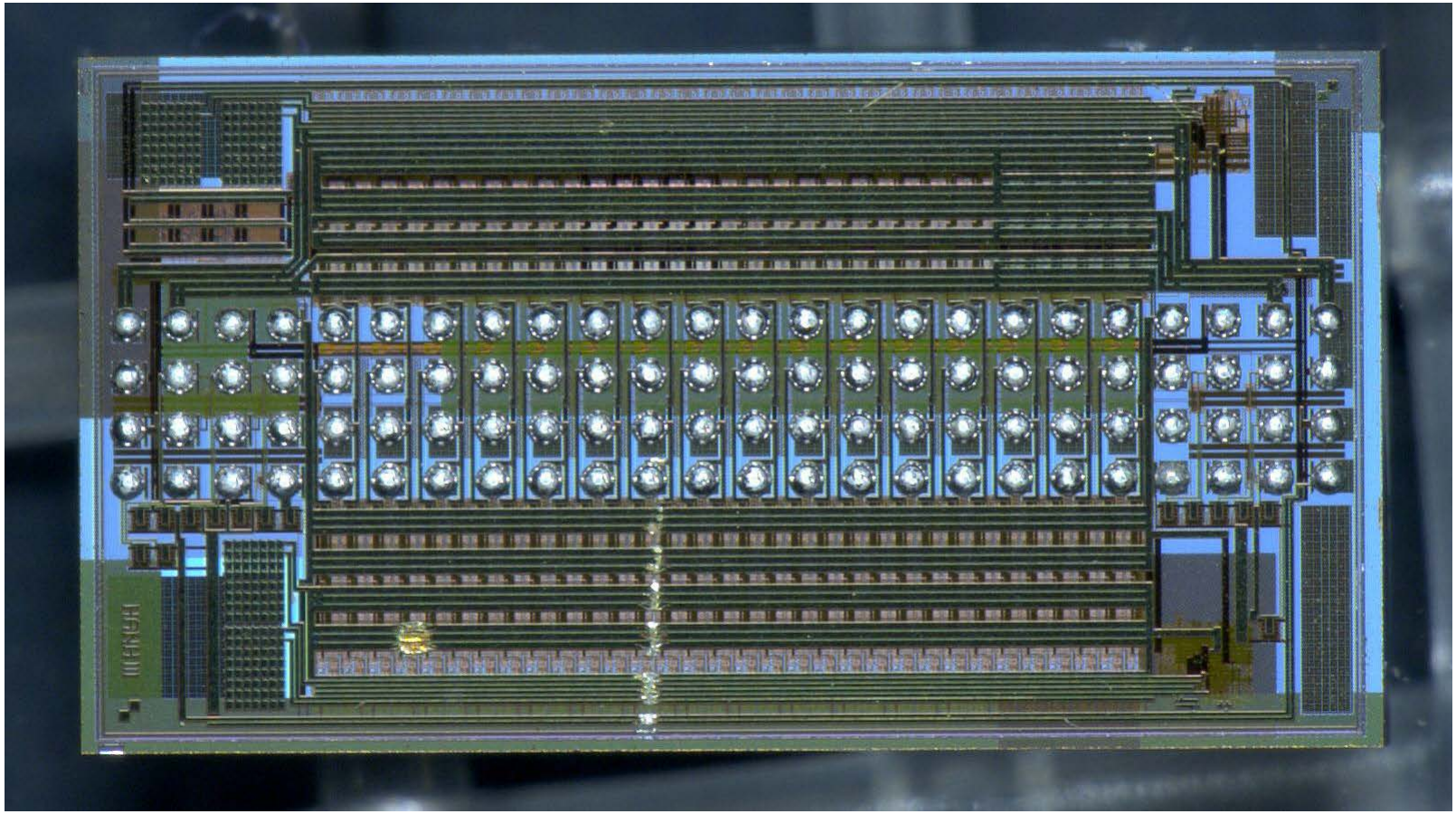
Residues from electro-plating?



Not clear, under investigation



Chip handling



- Scratches from tweezers,
- most likely from our side
  - ↳ Re-packing, probing…
- **Needs improvement, is probably the main yield killer**

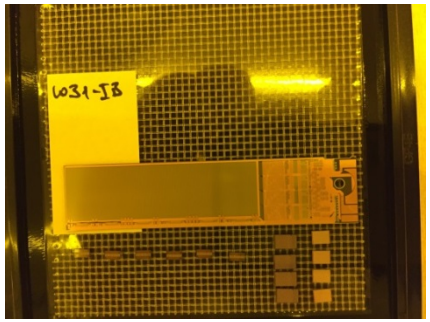
Next steps

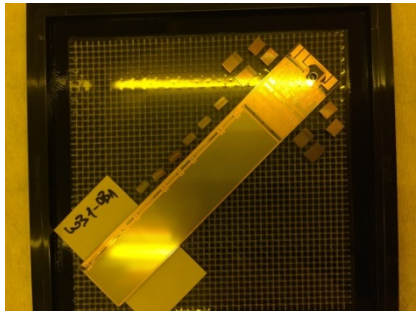
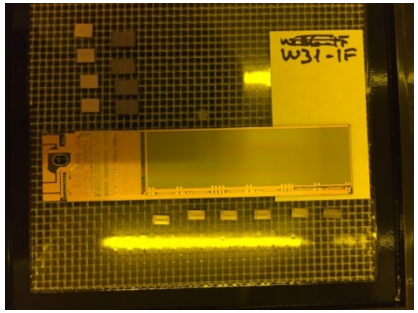
- Flip chip trials at HLL with IZM bumped SWBs
  - Shear tests, cross sections …
- New modules being prepared
  - DCDB4.2, DHPT1.1, SWB2.1 from the IZM pilot batch
  - W37-IB, W31-OB2
  - Expected back from flip chip in 2nd week of January
    - SMD and Kapton till end of January
- 439 unbumped chips now at IZM
  - For reassembly of 8 wafers, then bumping…
  - Handle wafer preps started
  - Aggressive time schedule: chips hopefully available till end of February
- Fall back
  - If flip chip trials or new modules show problems, stop processing → problem!
  - New wafers with SWB2.1 ordered (?)
  - Important: try to get them on wafers, **needs negotiations with broker/ams**
- If all goes well, start production mid/end March (time scale of DHPT1.2b)

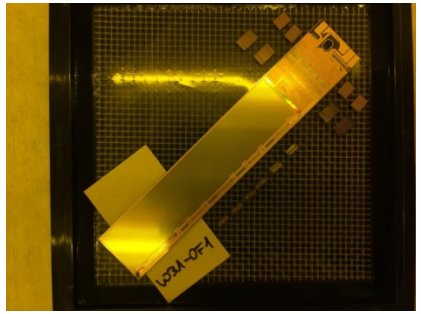
The recently assembled modules

4 modules assembled

- W31-IB, W31-OB, W31-OF
  - DCDB4.2 (final), SWB2.1 (final, repaired bump), DHPT1.1
- W31-IF
  - DCDB4.2 (final), SWB2.0 (last samples of the old version), DHPT1.1





- Flip Chip without any anomalies
  - Switcher generally not prime grade due to problems with bumping (see next slide)
- SMD, Kapton attachment as usual

Status of the modules as of today

- **… n.b.: this is work in progress**

- W31-IB and W31-OB:
  - JTAG configuration fails as soon as the Switchers are in the chain

- W31-IF:
  - JTAG configuration okay,
  - functional so far, see effect of bad substrate bump on the Switchers (3/6 SWBs)

- W31-OF (with SWB2.0):
  - JTAG okay
  - Functional so far, under test and optimization

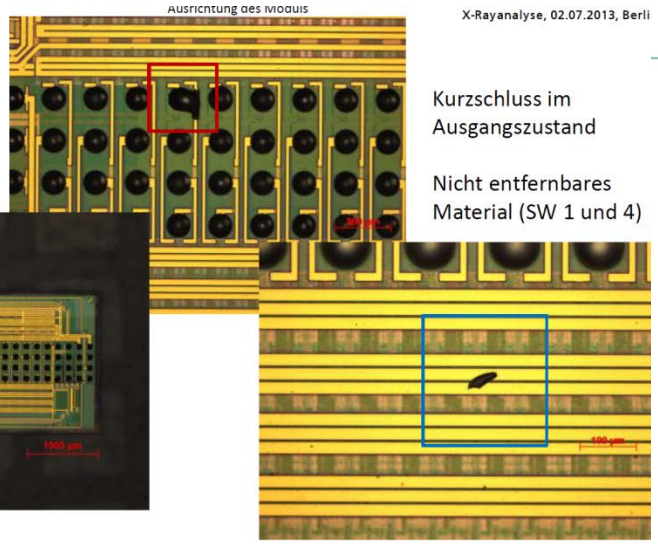
- There is no completely clear picture what went wrong with these modules
  - Many new components on the modules
    - SWBs, DCDB4.2, new kapton, new patch panel and cables, new firmware
    - Many suspects …

- **Tests and debugging is ongoing!!**

“fishy” Switchers, though tested okay

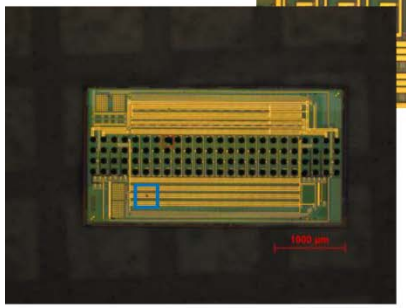
Modul W31-IB

Switcher 1



Kurzschluss im Ausgangszustand

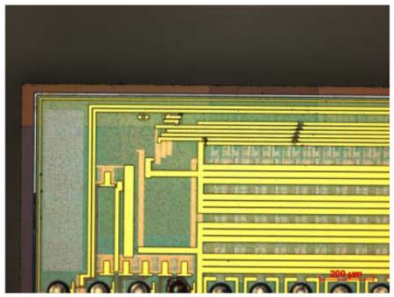
Nicht entfernbares Material (SW 1 und 4)



Belle Pixeldetektor

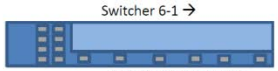
Modul W31-IF

Switcher 5

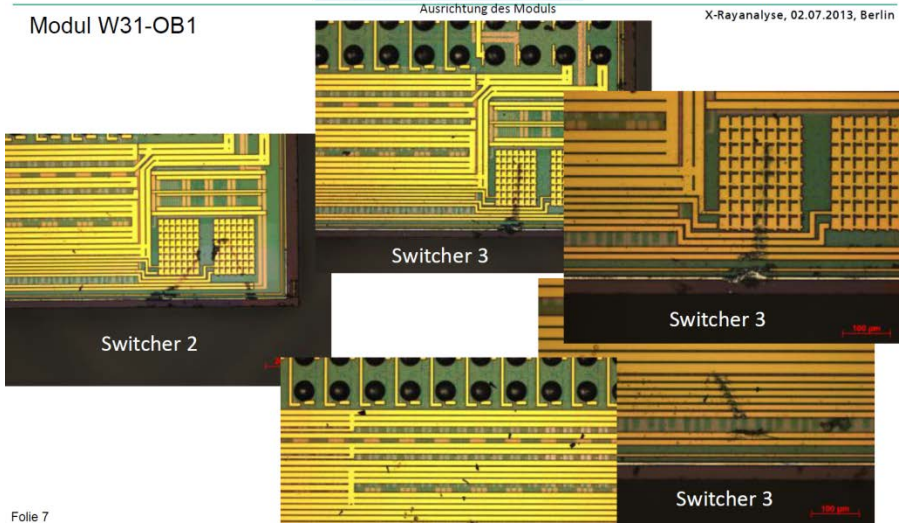


Leiterbahn beschädigt

Belle Pixeldetektor



Modul W31-OB1



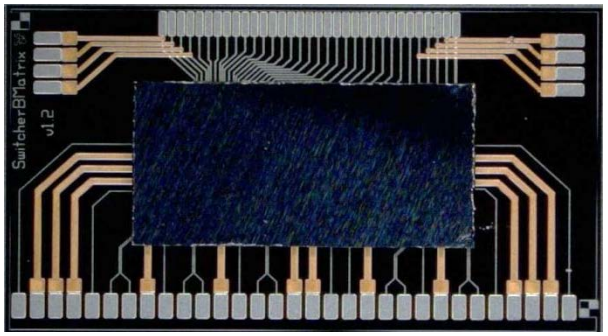
:- SWBs show imperfections, scratches

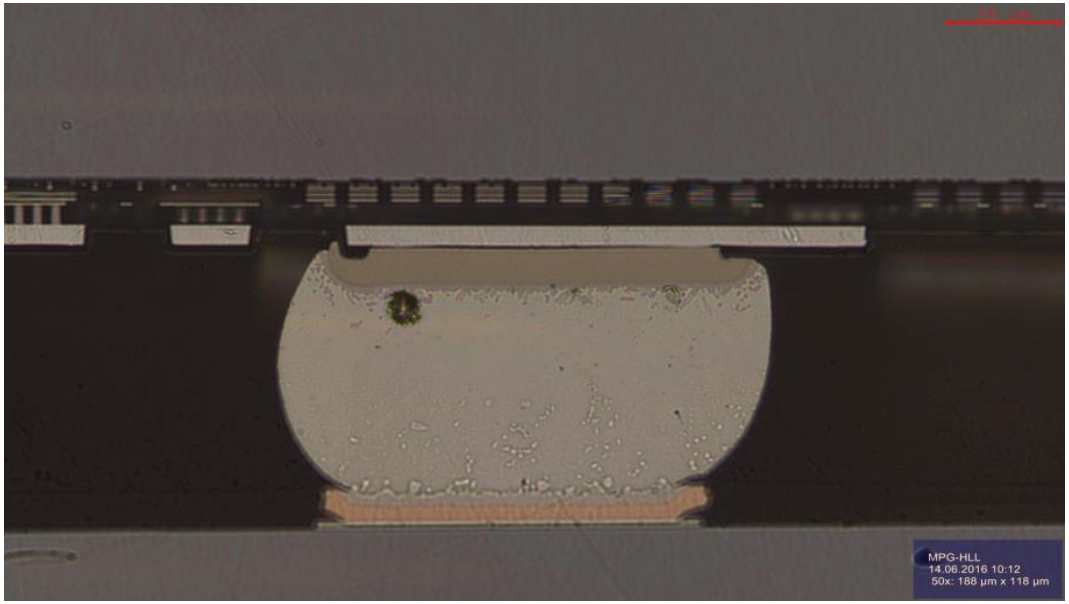
:- flip chip was done, since the tests on chip level were positive

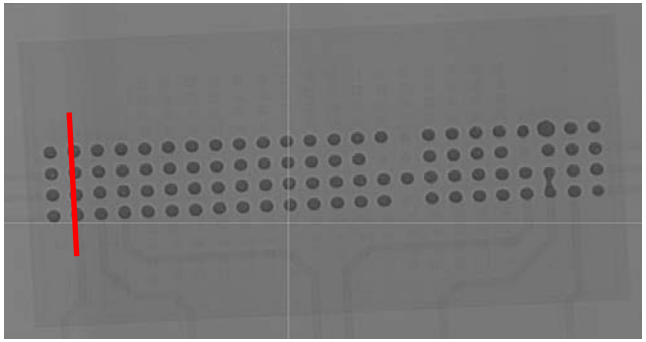
:- detailed xray inspection after FC showed no anomalies (apart from the Au stud bump)

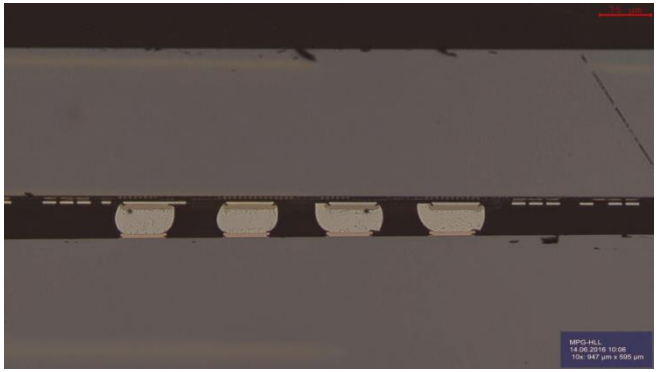
Test Assembly of SWBs to bond adapter

- Adapters assembled for SWB testing on hybrid level
  - Three adapters assembled
  - One assembly done with bad chip (bumping problems)
- Cross-section









- Delamination between SWB Alu and Ni?
  - Not certain that is this real
  - Could be due to contamination before UBM….

Test Assembly of SWBs to bond adapter