PXD DAQ – Status and News

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6th DEPFET Workshop, Bonn, Feb 7-9, 2011

Outline

- ATCA System
  - 1. Test of ROI Algorithm
  - 2. RAM Test on Compute Node
- PC-based system (Higuchi-san)
- Remarks on load balancing
- Schedule and Timeline

DHH

→ see talk by Igor Konorov

New compute node

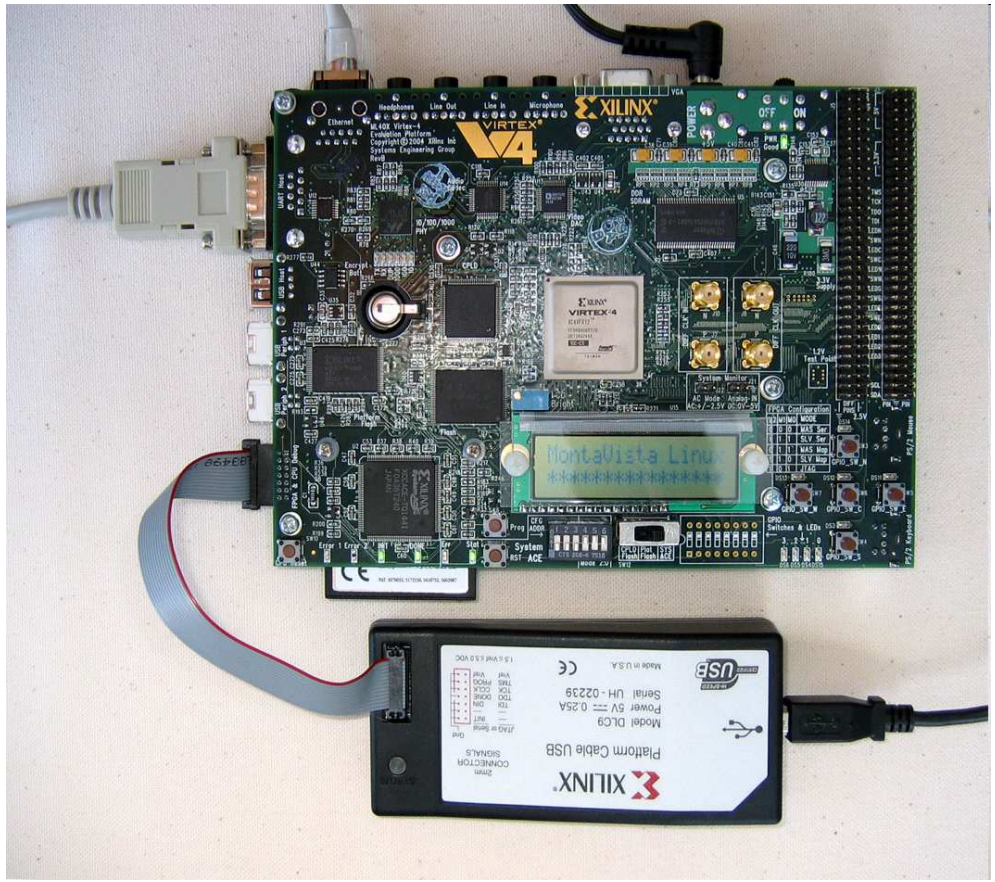
→ see talk by Zhen-An Liu

SVD data concentrator

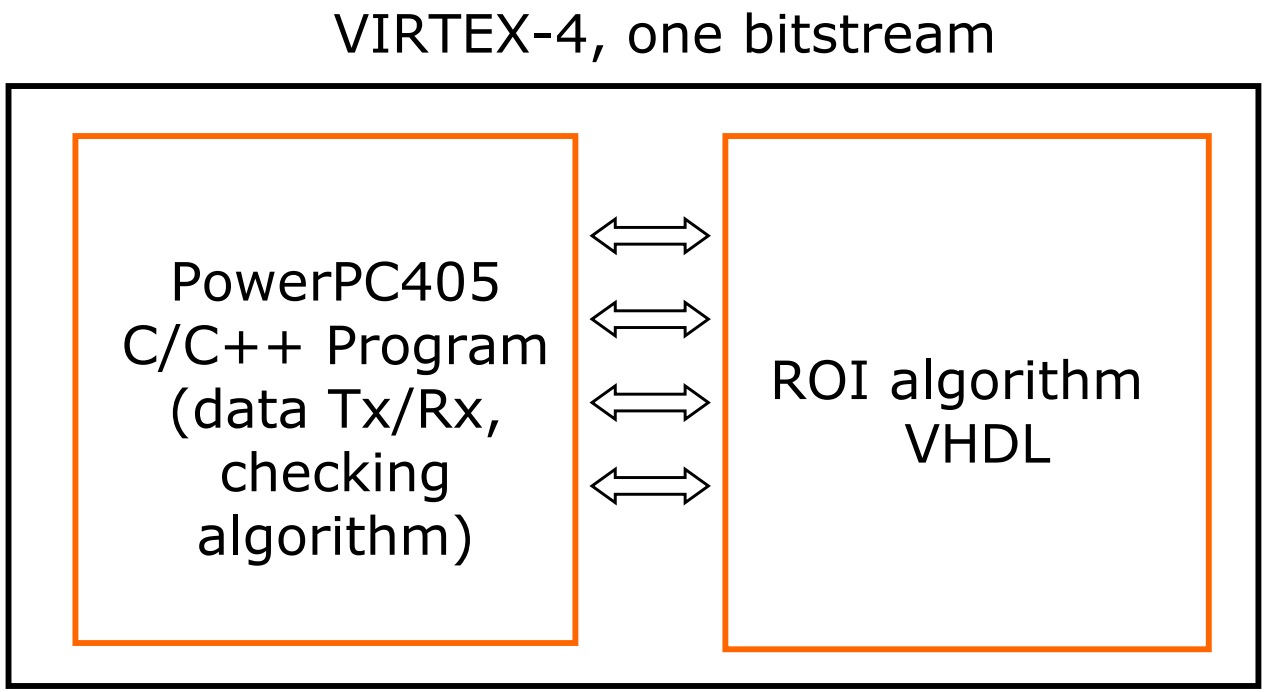
→ see talk by Carlos Marinas

David Münchow

Status of ROI algorithm on ML403 board (XC4VFX12-FF668-10C)



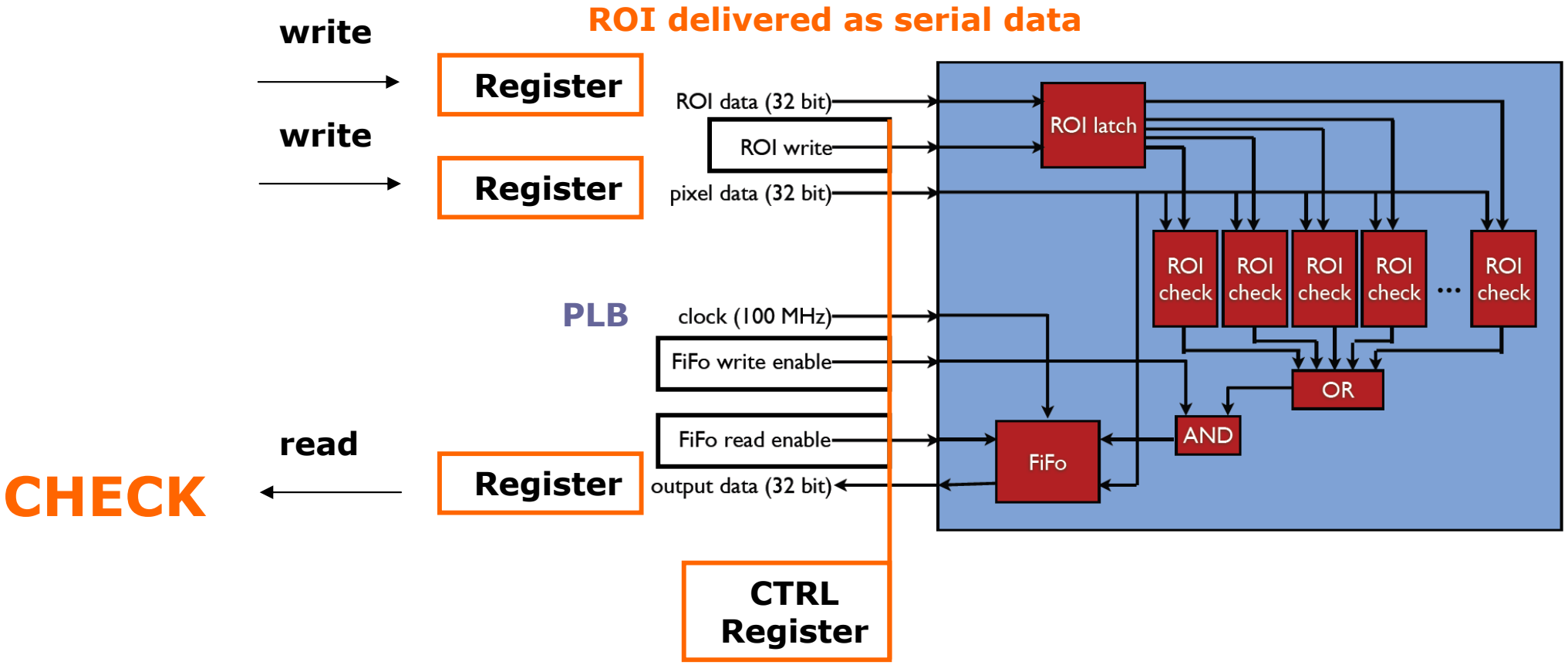
ROI Algorithm



- Handshaking and data Rx/Tx by 4 registers (32-bit)
  THIS IS THE ONLY INTERFACE.
- PowerPC is external data source
  (will be changed later to e.g. optical link core)
- PowerPC runs our self cross-compiled Linux
  (NFS, C/C++ compiler, etc.)

ROI Algorithm

parallel in ROI



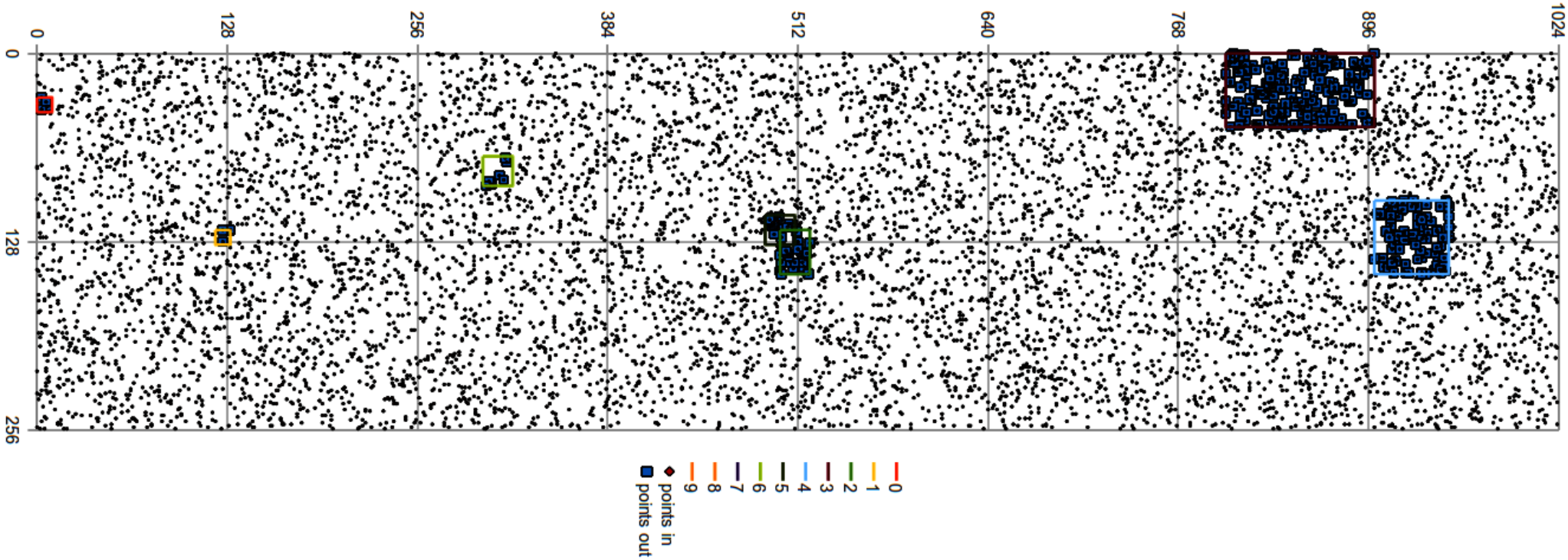
Register #5 (write ACK, read ACK) is not needed anymore (removed now)

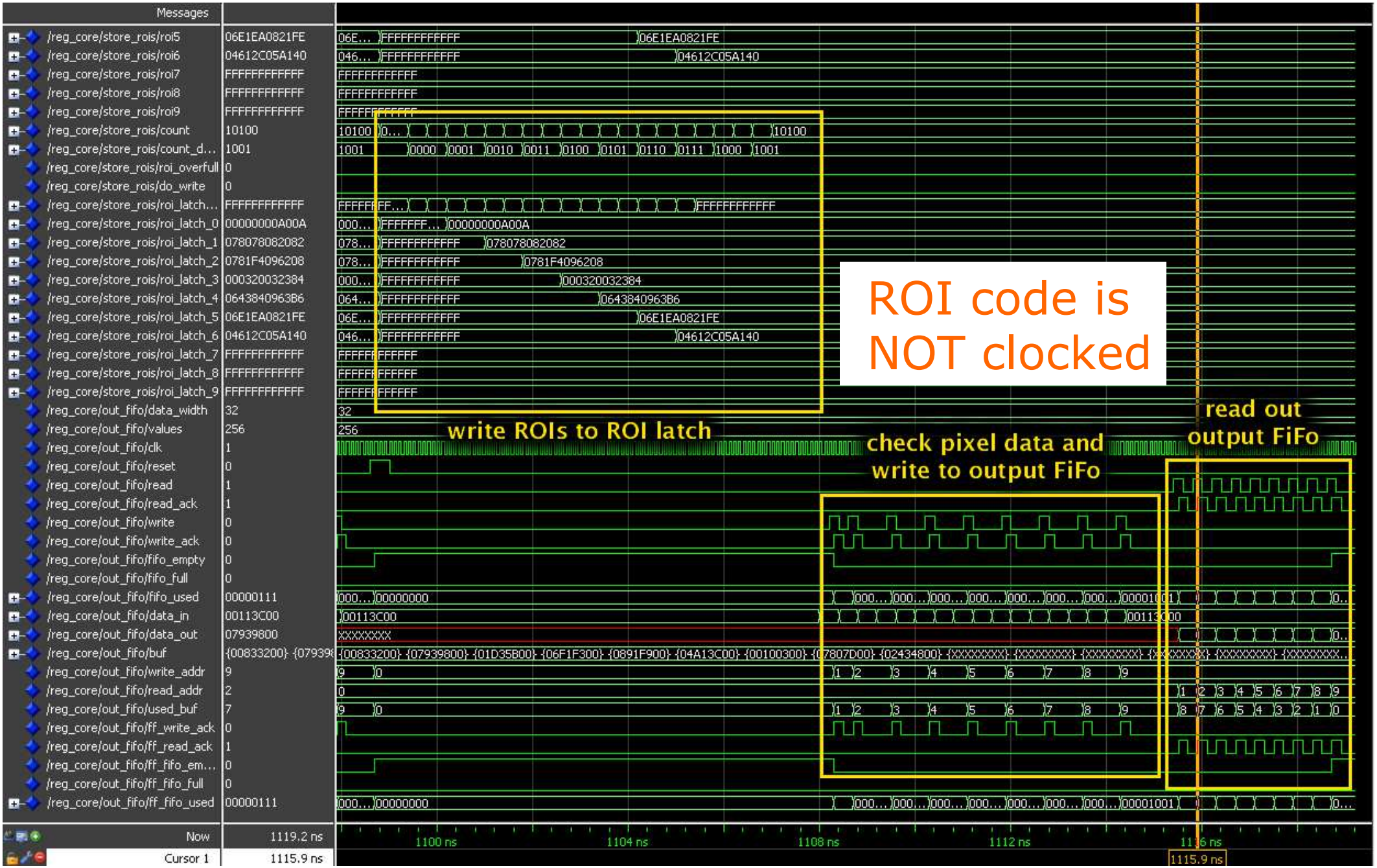
Event Example, 1 Half-Module

1024 x 256 space
(reality: 768 x 250, but address space needs to be bit aligned anyway, -> 10 bit x 8 bit)

3% occupancy

9 ROIs

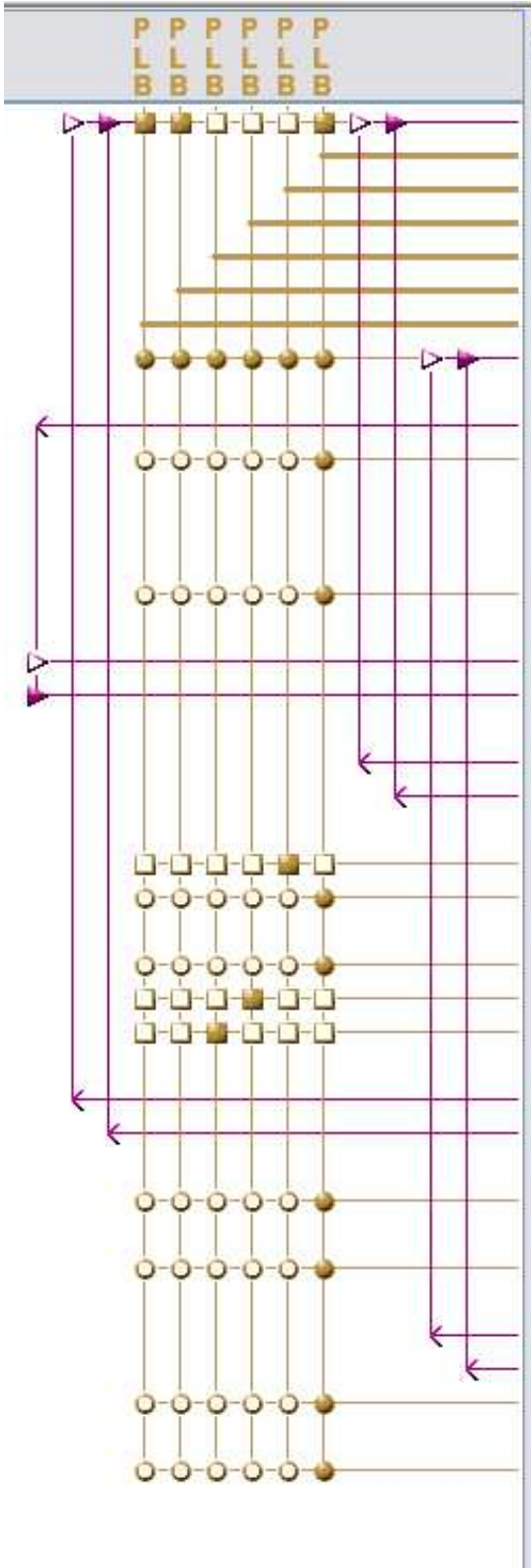



Messages
/reg_core/store_rois/roi5
/reg_core/store_rois/roi6
/reg_core/store_rois/roi7
/reg_core/store_rois/roi8
/reg_core/store_rois/roi9
/reg_core/store_rois/count
/reg_core/store_rois/count_d...
/reg_core/store_rois/roi_overfull
/reg_core/store_rois/do_write
/reg_core/store_rois/roi_latch...
/reg_core/store_rois/roi_latch_0
/reg_core/store_rois/roi_latch_1
/reg_core/store_rois/roi_latch_2
/reg_core/store_rois/roi_latch_3
/reg_core/store_rois/roi_latch_4
/reg_core/store_rois/roi_latch_5
/reg_core/store_rois/roi_latch_6
/reg_core/store_rois/roi_latch_7
/reg_core/store_rois/roi_latch_8
/reg_core/store_rois/roi_latch_9
/reg_core/out_fifo/data_width
/reg_core/out_fifo/values
/reg_core/out_fifo/clk
/reg_core/out_fifo/reset
/reg_core/out_fifo/read
/reg_core/out_fifo/read_ack
/reg_core/out_fifo/write
/reg_core/out_fifo/write_ack
/reg_core/out_fifo/fifo_empty
/reg_core/out_fifo/fifo_full
/reg_core/out_fifo/fifo_used
/reg_core/out_fifo/data_in
/reg_core/out_fifo/data_out
/reg_core/out_fifo/buf
/reg_core/out_fifo/write_addr
/reg_core/out_fifo/read_addr
/reg_core/out_fifo/used_buf
/reg_core/out_fifo/ff_write_ack
/reg_core/out_fifo/ff_read_ack
/reg_core/out_fifo/ff_fifo_em...
/reg_core/out_fifo/ff_fifo_full
/reg_core/out_fifo/ff_fifo_used
Now
1119.2 ns
Cursor 1
1115.9 ns
1100 ns
1104 ns
1108 ns
1112 ns
1116 ns
write ROIs to ROI latch
check pixel data and
write to output FiFo
read out
output FiFo
ROI code is
NOT clocked

Stability Test

```
count events:   1758620 correct        0 with error  (rate 0.000000  ROIs(8):  ) 195010 195780 194950 195468 194624 195459 196079 195484 195766
count events:   1758630 correct        0 with error  (rate 0.000000  ROIs(4):  ) 195012 195781 194952 195469 194625 195459 196080 195485 195767
count events:   1758640 correct        0 with error  (rate 0.000000  ROIs(6):  ) 195014 195781 194953 195471 194626 195461 196080 195485 195769
count events:   1758650 correct        0 with error  (rate 0.000000  ROIs(1):  ) 195016 195784 194953 195472 194626 195463 196081 195486 195769
count events:   1758660 correct        0 with error  (rate 0.000000  ROIs(6):  ) 195017 195785 194954 195474 194626 195466 196082 195486 195770
count events:   1758670 correct        0 with error  (rate 0.000000  ROIs(6):  ) 195017 195787 194955 195475 194629 195469 196082 195486 195770
count events:   1758680 correct        0 with error  (rate 0.000000  ROIs(1):  ) 195018 195788 194956 195476 194629 195470 196085 195488 195770
count events:   1758690 correct        0 with error  (rate 0.000000  ROIs(3):  ) 195019 195789 194957 195478 194629 195471 196085 195490 195772
count events:   1758700 correct        0 with error  (rate 0.000000  ROIs(4):  ) 195020 195792 194957 195479 194630 195471 196085 195492 195774
count events:   1758710 correct        0 with error  (rate 0.000000  ROIs(6):  ) 195020 195793 194957 195480 194632 195473 196086 195494 195775
count events:   1758720 correct        0 with error  (rate 0.000000  ROIs(1):  ) 195022 195795 194960 195482 194632 195473 196086 195494 195776
count events:   1758730 correct        0 with error  (rate 0.000000  ROIs(7):  ) 195023 195797 194960 195482 194635 195474 196088 195495 195776
count events:   1758740 correct        0 with error  (rate 0.000000  ROIs(5):  ) 195026 195799 194960 195482 194636 195475 196088 195498 195776
count events:   1758750 correct        0 with error  (rate 0.000000  ROIs(8):  ) 195026 195799 194960 195487 194636 195477 196089 195499 195777
count events:   1758760 correct        0 with error  (rate 0.000000  ROIs(7):  ) 195027 195800 194960 195489 194637 195477 196090 195500 195780
count events:   1758770 correct        0 with error  (rate 0.000000  ROIs(8):  ) 195028 195800 194961 195489 194639 195479 196091 195503 195780
count events:   1758780 correct        0 with error  (rate 0.000000  ROIs(7):  ) 195029 195801 194962 195491 194640 195480 196093 195504 195780
count events:   1758790 correct        0 with error  (rate 0.000000  ROIs(5):  ) 195030 195802 194964 195492 194643 195481 196093 195505 195780
count events:   1758800 correct        0 with error  (rate 0.000000  ROIs(9):  ) 195031 195803 194965 195493 194645 195482 196093 195505 195783
count events:   1758810 correct        0 with error  (rate 0.000000  ROIs(7):  ) 195032 195806 194965 195493 194645 195483 196096 195506 195784
count events:   1758820 correct        0 with error  (rate 0.000000  ROIs(7):  ) 195034 195807 194965 195494 194645 195485 196097 195508 195785
count events:   1758830 correct        0 with error  (rate 0.000000  ROIs(6):  ) 195035 195807 194967 195496 194646 195487 196097 195509 195786
count events:   1758840 correct        0 with error  (rate 0.000000  ROIs(6):  ) 195037 195809 194968 195496 194647 195490 196097 195510 195786
count events:   1758850 correct        0 with error  (rate 0.000000  ROIs(4):  ) 195037 195810 194968 195499 194648 195490 196099 195512 195787
count events:   1758860 correct        0 with error  (rate 0.000000  ROIs(8):  ) 195037 195811 194970 195500 194649 195490 196101 195513 195789
count events:   1758870 correct        0 with error  (rate 0.000000  ROIs(9):  ) 195038 195811 194971 195501 194650 195492 196101 195514 195792
count events:   1758880 correct        0 with error  (rate 0.000000  ROIs(4):  ) 195040 195811 194971 195502 194650 195494 196104 195515 195793
count events:   1758890 correct        0 with error  (rate 0.000000  ROIs(8):  ) 195041 195811 194971 195502 194651 195496 196105 195518 195795
count events:   1758900 correct        0 with error  (rate 0.000000  ROIs(5):  ) 195042 195813 194972 195503 194653 195496 196107 195519 195795
count events:   1758910 correct        0 with error  (rate 0.000000  ROIs(7):  ) 195042 195816 194972 195503 194653 195497 196109 195520 195798
```

<=10 random ROIs, variable number of ROI, variable ROI size
random data, 3% occupancy
>3 days
>11 x 10^6 events
output data re-checked on PowerPC side



Bus Interfaces | Ports | Addresses

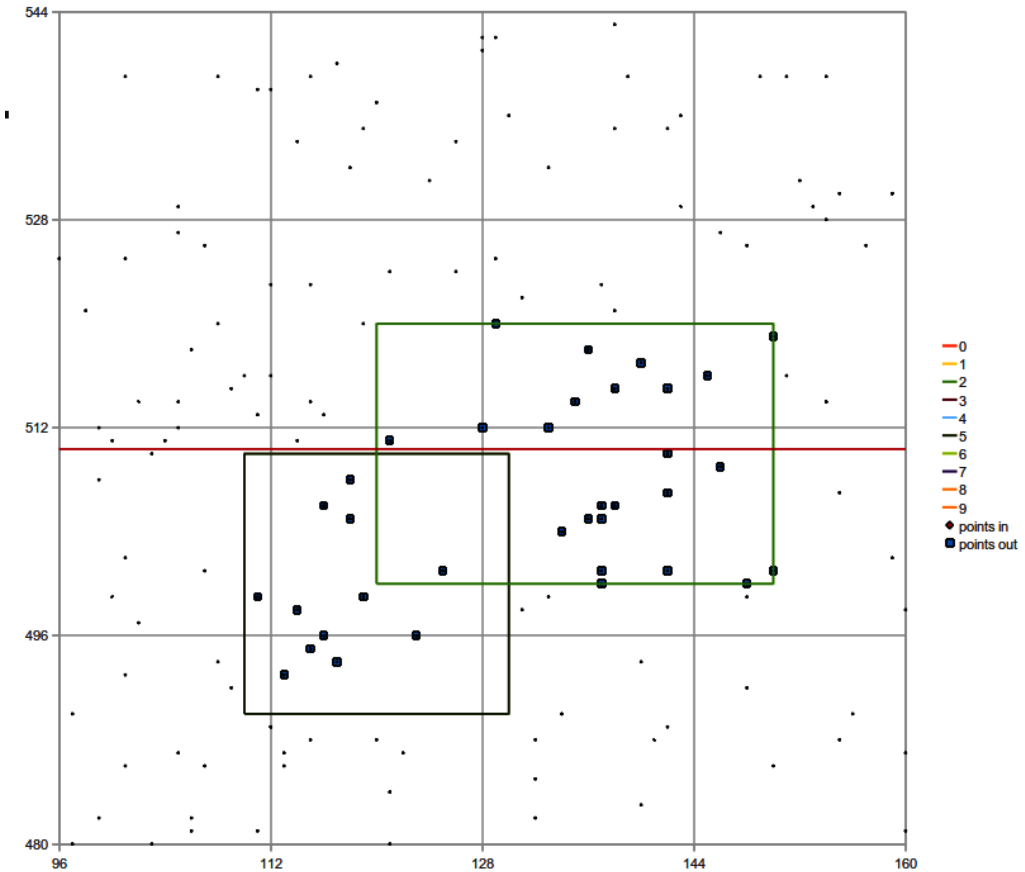
Name	Bus Connection	IP Type	IP Version
ppc405_0		ppc405_virtex4	2.01.a
plb		plb_v46	1.03.a
plb_v46_0		plb_v46	1.03.a
plb_v46_1		plb_v46	1.03.a
plb_v46_2		plb_v46	1.03.a
ppc405_0_dplb1		plb_v46	1.03.a
ppc405_0_iplb1		plb_v46	1.03.a
DDR2_SDRAM_W1D32M72R...		mpmc	4.03.a
xps_bram_if_cntlr_1		xps_bram_if_cntlr	1.00.a
PORTA	xps_bram_if_cntlr_1_port		
SPLB	plb		
FLASH		xps_mch_emc	2.00.a
MCH1	No Connection		
MCH0	No Connection		
SPLB	plb		
plb_bram_if_cntlr_1_bram		bram_block	1.00.a
PORTB	No Connection		
PORTA	xps_bram_if_cntlr_1_port		
jtagppc_cntlr_0		jtagppc_cntlr	2.01.c
JTAGPPC1	jtagppc_cntlr_0_JTAGPPC1		
JTAGPPC0	jtagppc_cntlr_0_0		
ll_plb_optical_0		ll_plb_optical	1.00.a
MPLB	plb_v46_0		
SPLB	plb		
plt_test2_fifo_0		plt_test2_fifo	1.00.a
SPLB	plb		
MPLB2	plb_v46_1		
MPLB	plb_v46_2		
proc_sys_reset_0		proc_sys_reset	2.00.a
RESETPPC1	proc_sys_reset_0_RESETPPC1		
RESETPPC0	ppc_reset_bus		
roi_core_test_0		roi_core_test	3.00.a
SPLB	plb		
xps_intc_0		xps_intc	1.00.a
SPLB	plb		
Hard_Ethernet_MAC		xps_ll_temac	1.01.b
LLINK1	Hard_Ethernet_MAC_LLINK1		
LLINK0	Hard_Ethernet_MAC_LLINK0		
SPLB	plb		
RS232		xps_uartlite	1.00.a
SPLB	plb		
clock_generator_0		clock_generator	2.01.a
FLASH_util_bus_split_0		util_bus_split	1.00.a

interfaces to RAM and optical link already in the bitstream

Overlapping ROIs

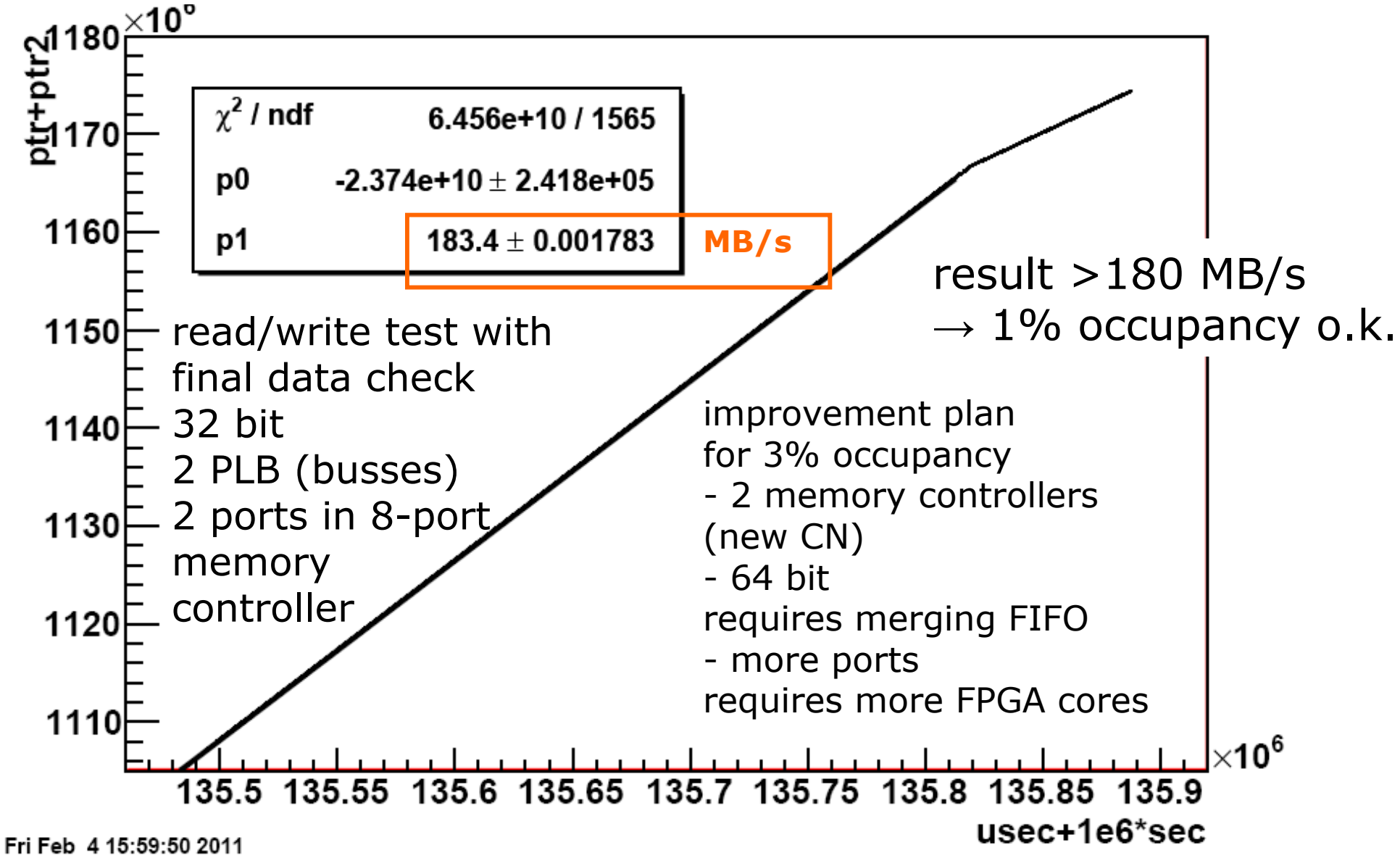
ROI selection => OR

i.e. if ROI overlap, these output data are only written 1x



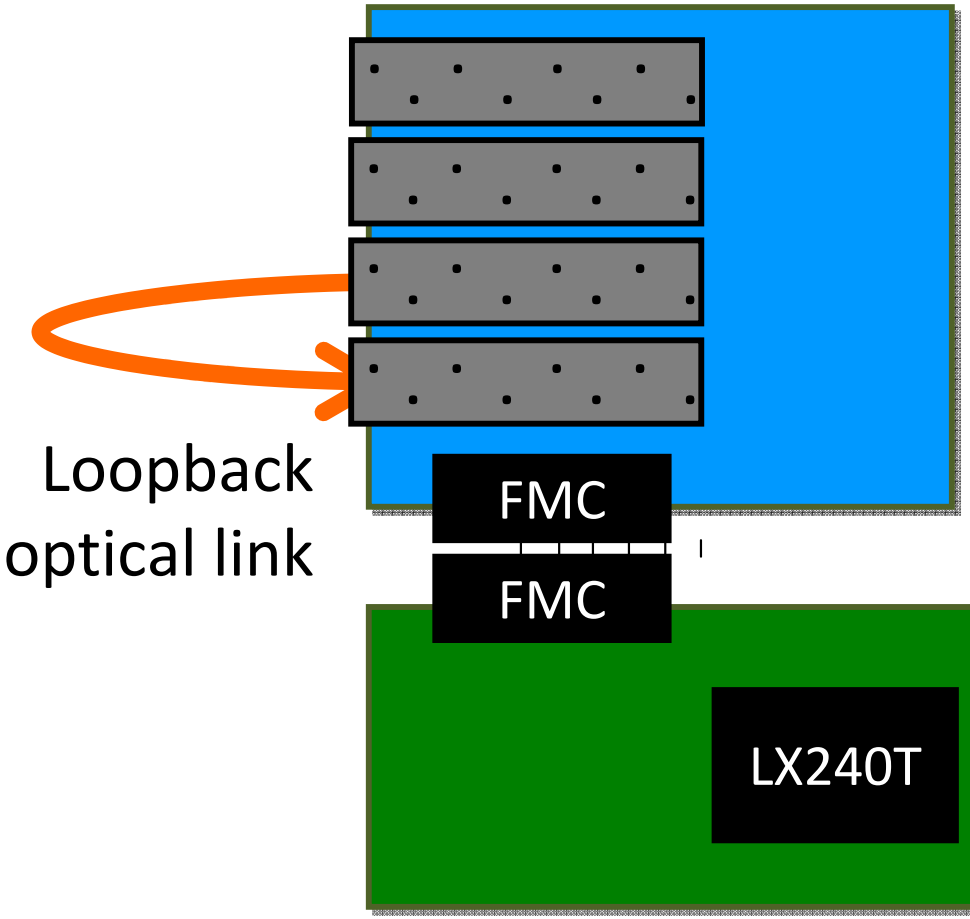
ATCA System
RAM Test on Compute Node (Vers. #2)

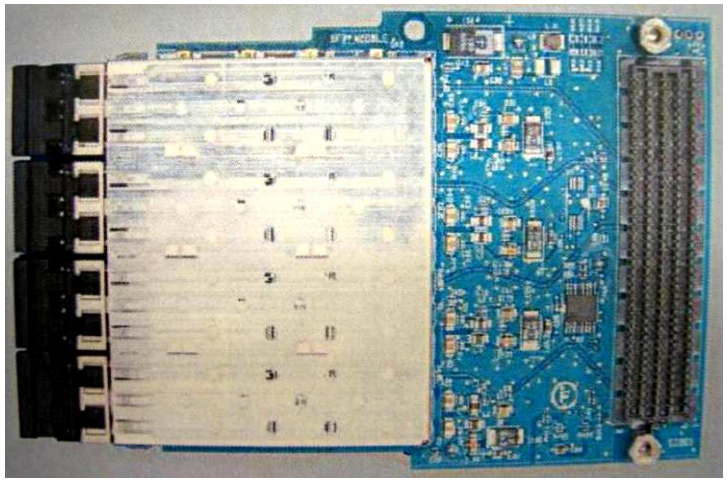
Björn Spruck



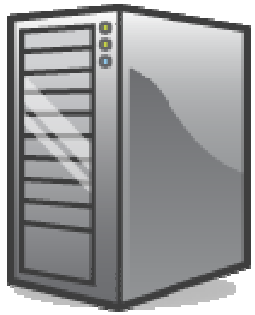
PC-based System

Takeo Higuchi
(for details see his talk at Beijing Belle-II DAQT Workshop)





PCIe Gen2 (x4)
<2 GB/s



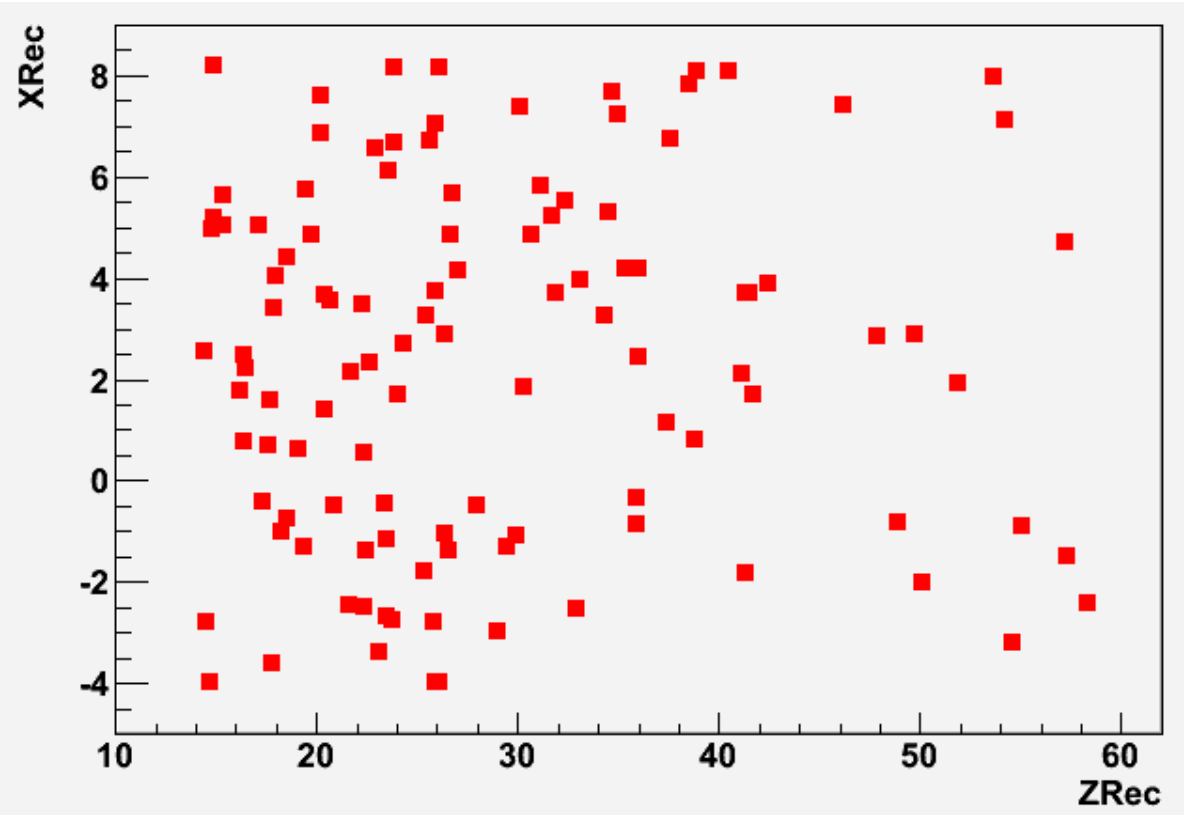
PCIe server

progress on device driver and firmware (FMC)
discussion of contracts with companies

Load balancing with QED background

MC data by Zbynek Drasal, Prague

1 event, 1 half-module in inner layer



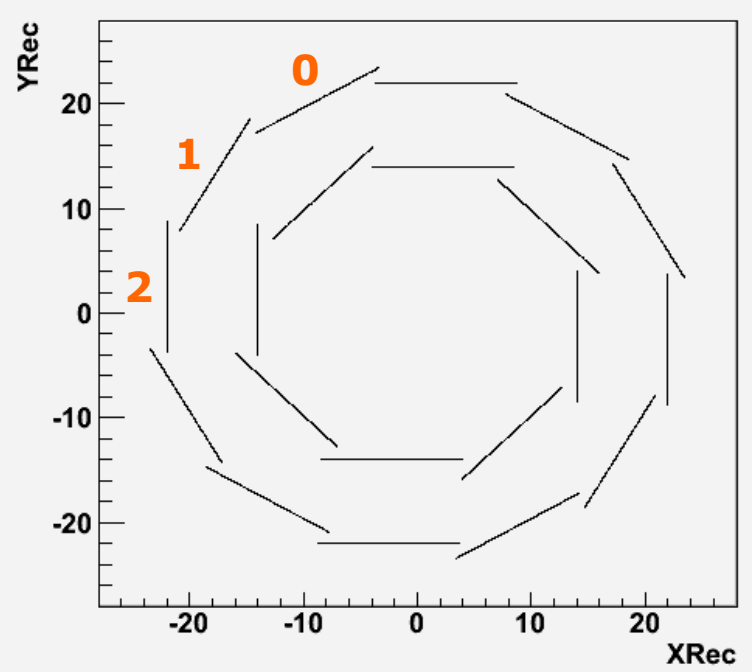
Preparation for FPGA ongoing
(coordinate transformation, rotation etc.)

Load balancing: inner vs. outer

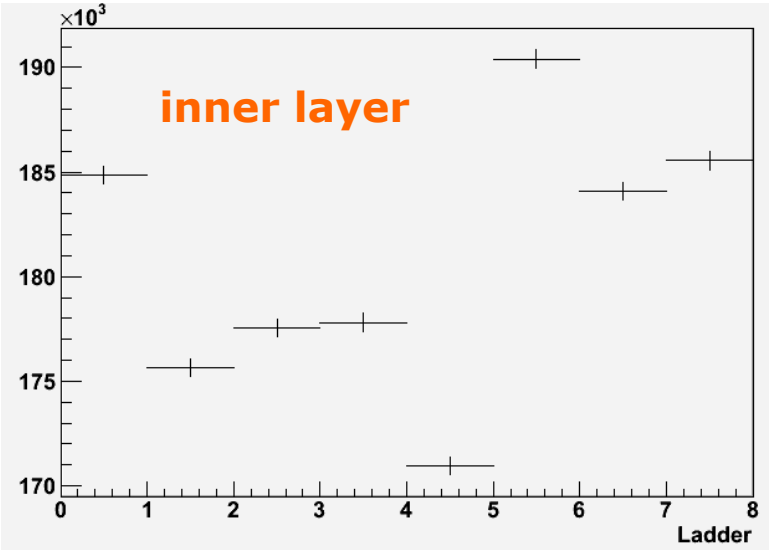
MC data by Zbynek Drasal, Prague

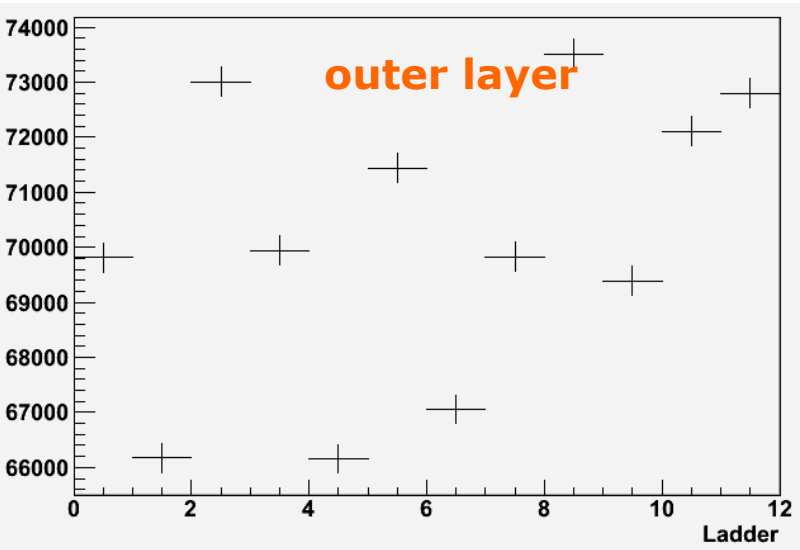
- Example:
  charged pions, p=1 GeV/c
  uniform in ϕ, ϑ
- QED background, KoralW

# of hits in inner layer:
~70% more integrated
but 8 vs. 12 modules
>150% higher occupancy per 1 module



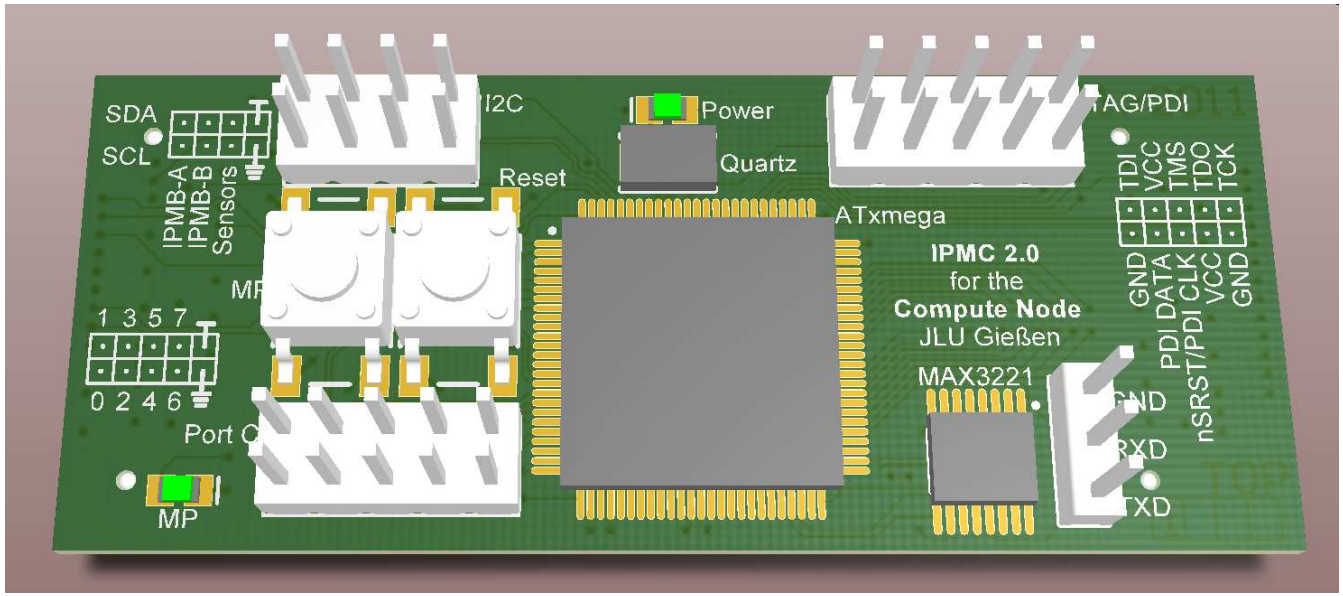
fluctuations much larger than statistical (material?)





New IPMI PCB

- negociation to ATCA „shelf manager“
  (e.g. request of compute node „give me 180 W power“)
- New CN addon card: Microcontroller ATMEGA1280 -> XMEGA A1
  - internal I2C
    (-> 4 external chips can be skipped)
  - PCBs are delivered (01.02.)
    chip placement and soldering is ongoing

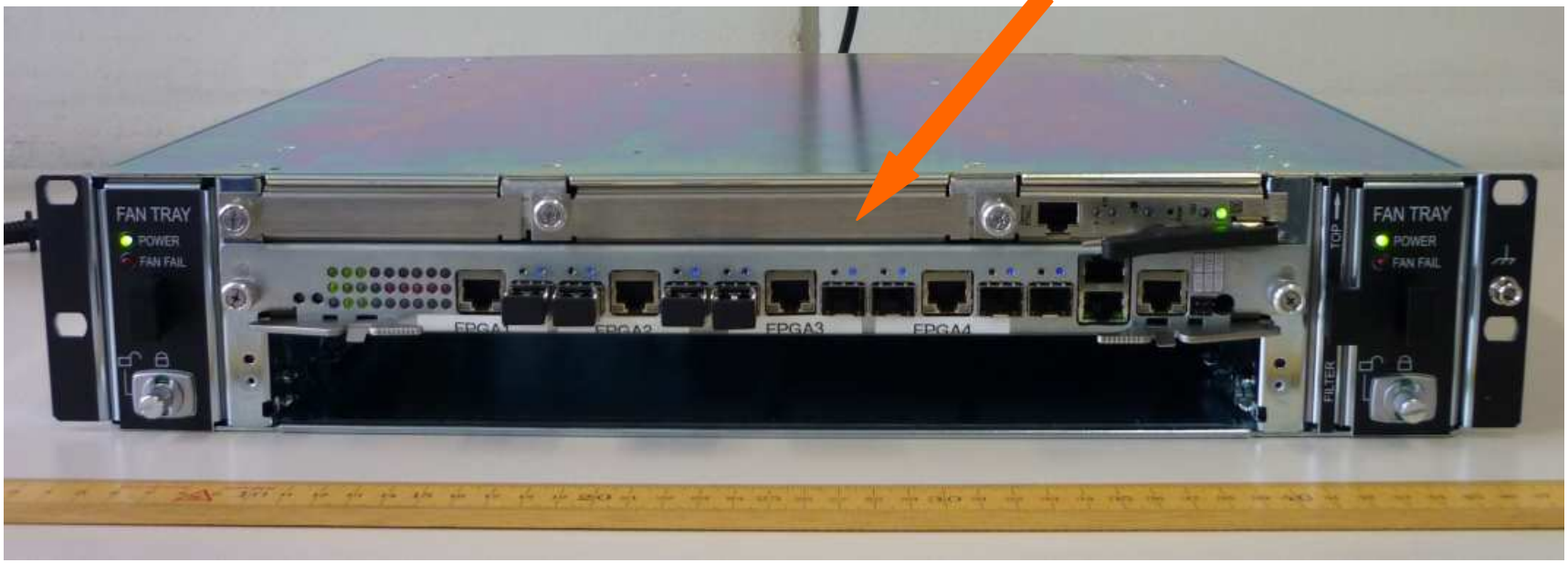


Next steps

- All developers will move from development (XC4VFX12, XC4VFX20) boards to CN (XC4VFX60)
  - 10 new CN will come soon from IHEP
    (2 CN for Belle-2 from german ministry funding)
  - 1 large (14-slot) scheduled 28.03.
  - 4 mini-ATCA shelfs (2-slot) delivered 26.01.

  everybody will have a mini-system in the office which he can reboot as often as needed

Compute Node Vers. #2



Next steps

- Move ROI algorithm to CN – ongoing (David Münchow)
  with read/write clock: o.k. ~10^5 events
  w/o read/write clock: timing problem
  (only on CN, not on ML403)
- Connect ROI algorithm to optical link

- Feb 02 - Meeting of Bonn and Gießen Groups
  (Bonn Group of Jochen Dingfelder)
  - data concentrator, interfaces to ATCA, possible test systems etc.
  - cancelled (snow)
    new tentative date TUE Feb 15
- Feb 21,22 - Meeting in Munich
  (organized by Andreas Moll)
  - HLT interface

Timeline

- Proposed schedule until decision ATCA vs. PC based system

- April 6-10
  Presentation of status of both systems at B2GM
  -> identify open issues
- May 9-11
  Ringberg Workshop
  -> short update of important issues
- June 9 (THU) and 10 (FRI)
  PXD DAQ Workshop in Germany (location not fixed yet)
  -> decision
- July 6-9
  B2GM
  -> announcement of decision

Backup Slides

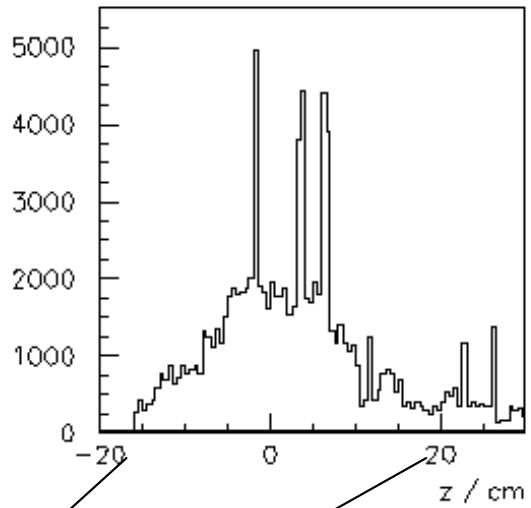
ROI Algorithm

Details:

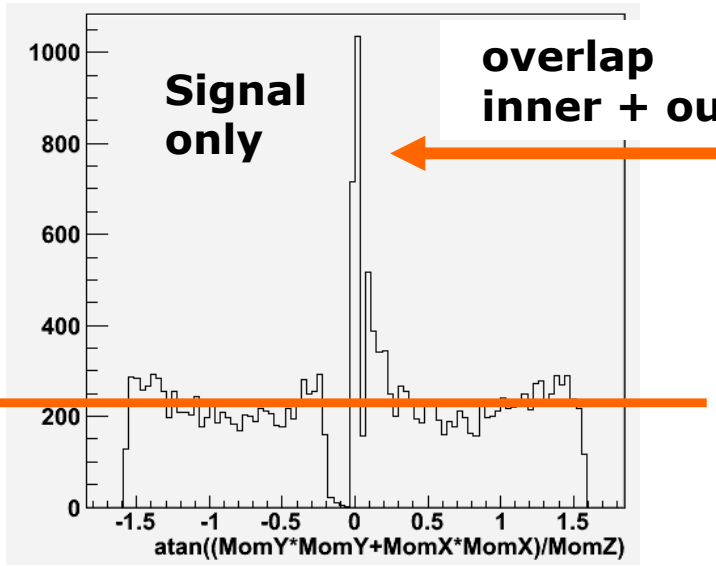
- Only 1 FIFO (output)
  (FIFO config: write/read enable with full clock speed)
  no input FIFO, not needed (just consumes FPGA resources)
- Code for ROI checker is NOT clocked
- Data Tx/Rx not by PLB
  bus is not used (avoids arbitration)
- n (n<=10) ROIs -> code is parallel x n
  n is variable event-by-event
- Next step: combine with „shared memory" concept
  (developed further meanwhile by Björn Spruck)
  new: 2 master busses
  -> registers have adresses (to RAM), not data

Load balancing: forward vs. backward

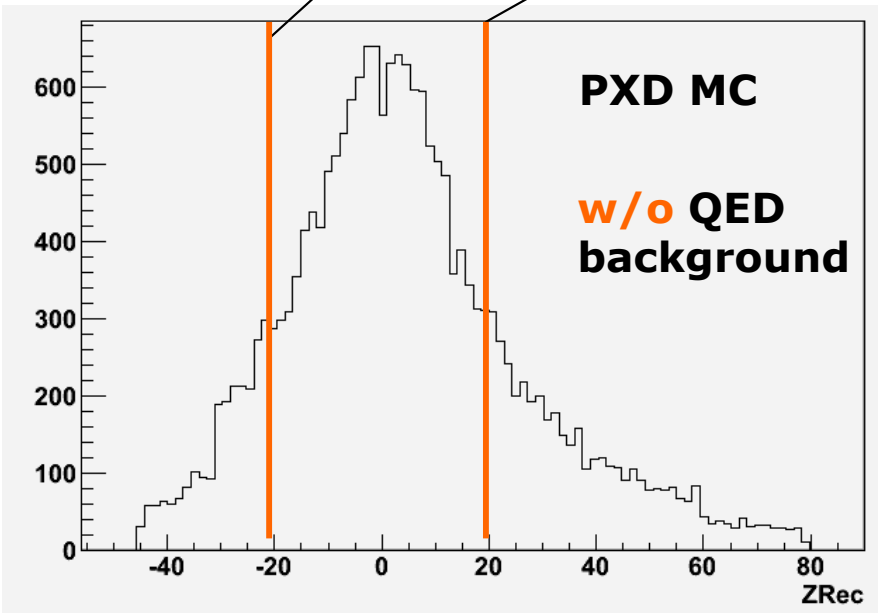
SVD z hits
exp. 69
run 1203
17. Jun 2009
14:20-17:25
L= 21.083 x 10^{33}
- highest Belle peak luminosity

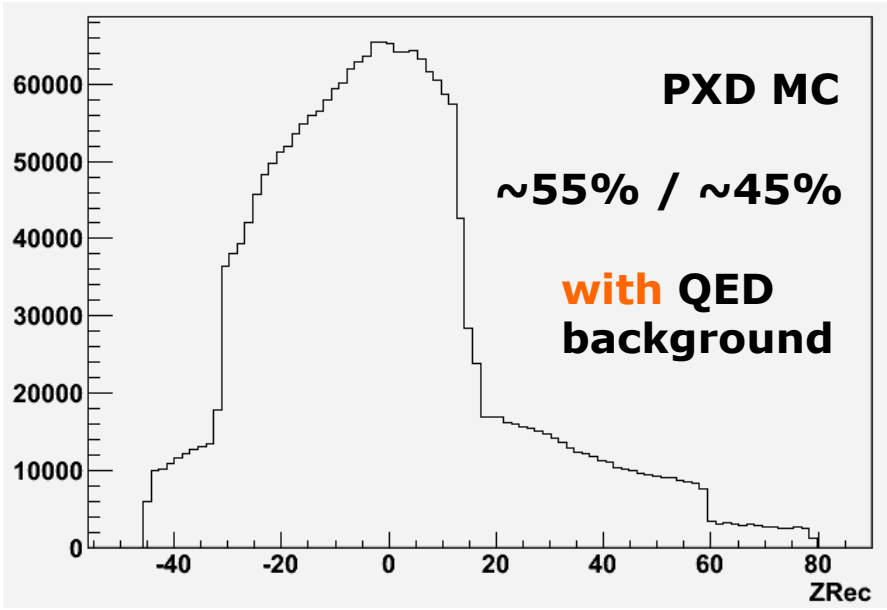


MC data by Zbynek Drasal, Prague



flat

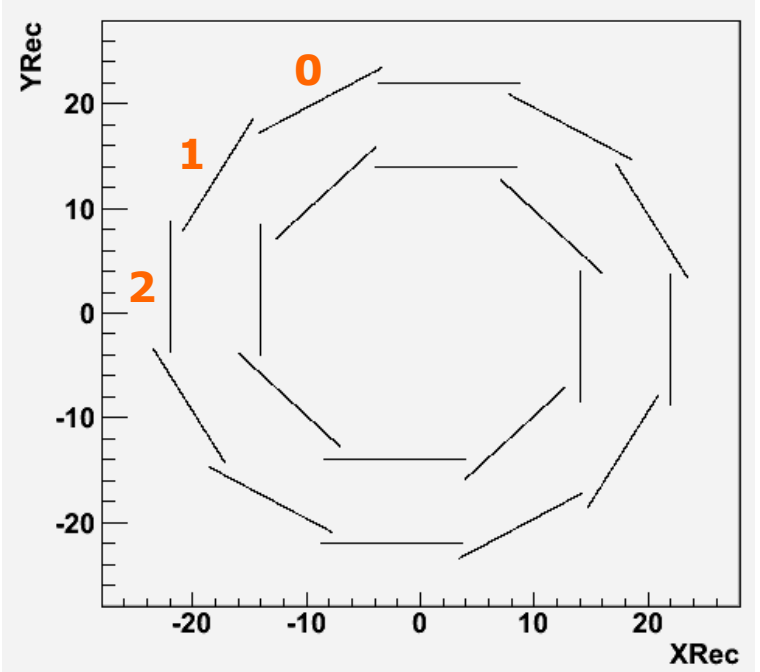




Load balancing: inner vs. outer

MC data by Zbynek Drasal, Prague

- Example:
  charged pions, p=1 GeV/c
- signal only, 0% background
- uniform in ϑ



# of hits 10275 vs. 9767 → almost same
but 8 vs. 12 modules

inner layer >~50% more occupancy

~10% fluctuations (material?)