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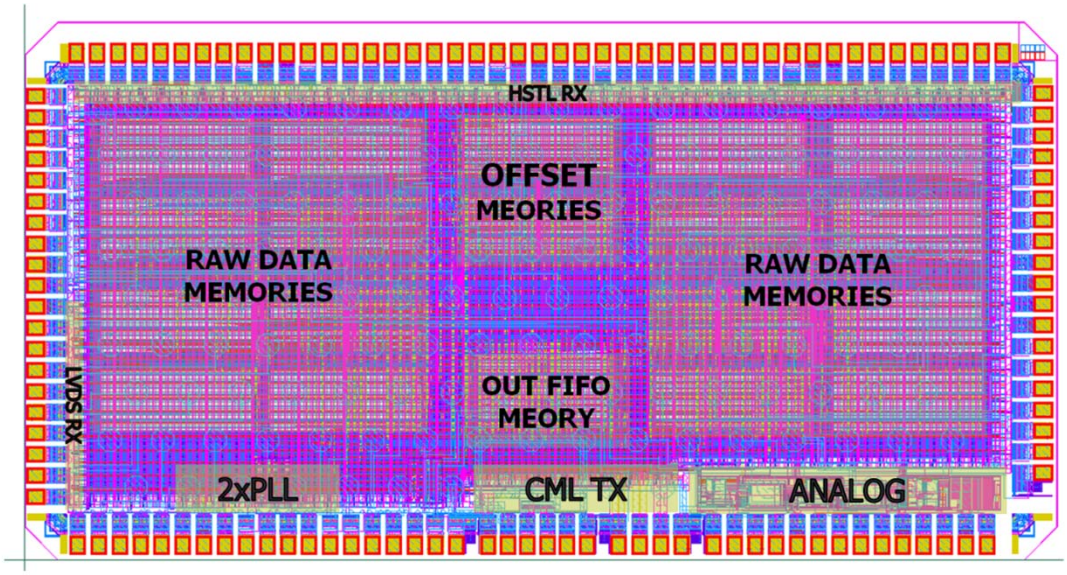
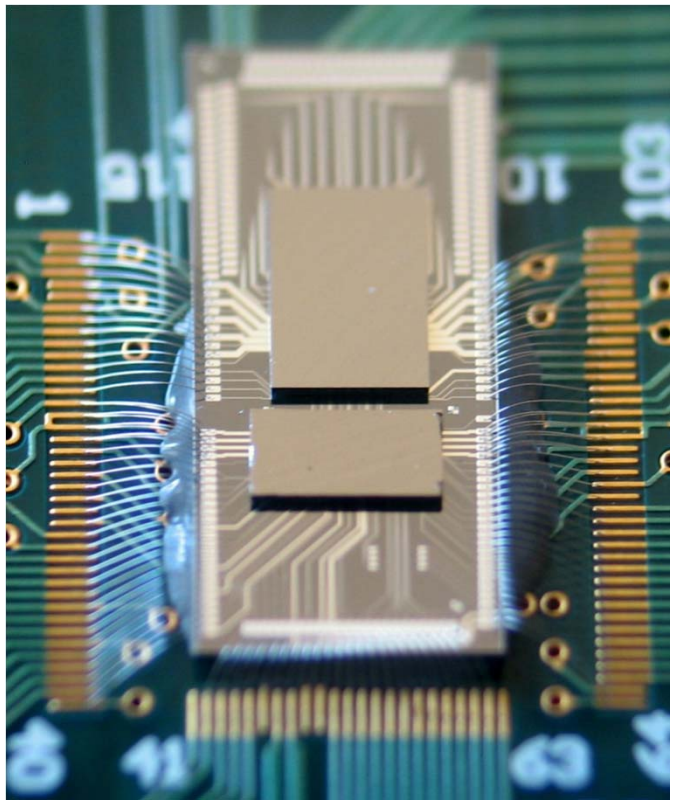
SI LAB
Silizium Labor Bonn

Data Handling Processor Status/Plans

Tomasz Hemperek

DHP 0.1


HSTL RX
OFFSET
MEORIES
RAW DATA
MEMORIES
RAW DATA
MEMORIES
OUT FIFO
MEORY
LVDS RX
2xPLL
CML TX
ANALOG



DHP 0.1 - Status

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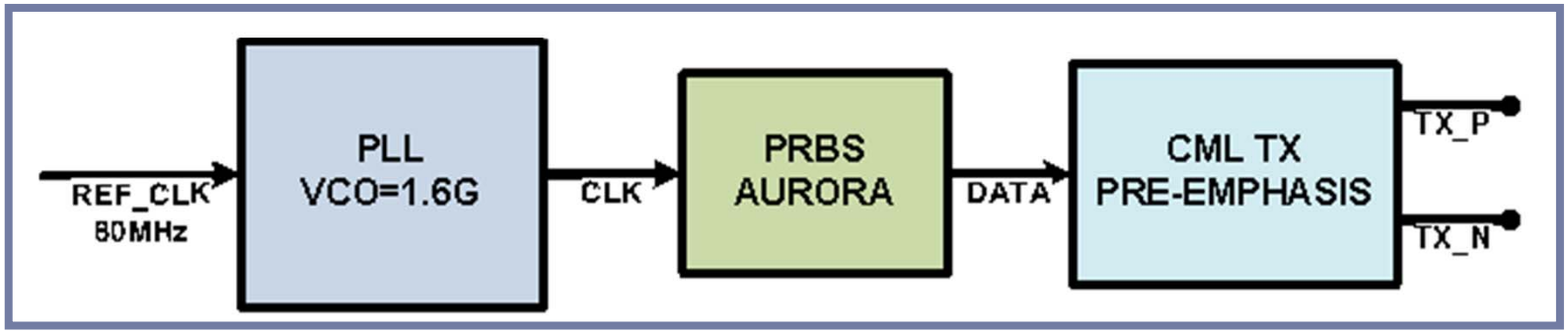
Working:

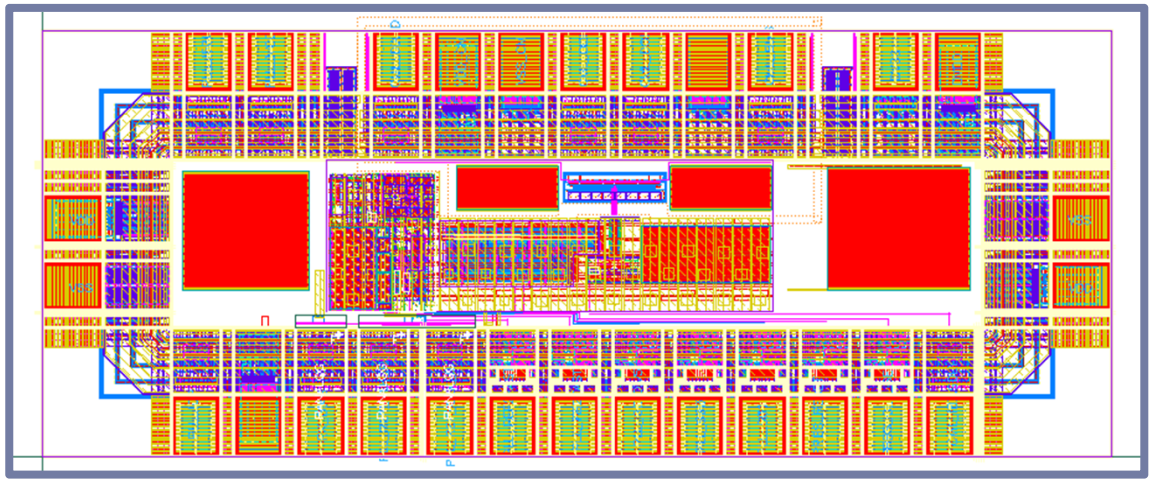
- LVDS Input
- HSTL like Input
- Slow control (JTAG)
- Memories read/write
- Input readout
- Patter generator
- DAC
- Band Gap
- Processing (*need DCD)
- High Speed TX testing

To Do:

- DCD communication and synchronization
- More Processing
- Radiation test

DhpTxTest Chip





- **Design ready: December 2010 - MPW canceled**
- **Resubmission: February 2011 - MPW canceled**

DHP 0.2 - Changes

- Fixes
  - Input routing
  - signed/unsigned convention
  - PRBS
- Digital improvements/changes
  - Fix to static pedestal
  - Pedestal during acquisition update – JTAG
  - Improved common mode correction
  - Common mode readback
  - …
- New combined PLL+Ser+TX
- New I/O cells
- Improved DACs/ADC

DHP 0.2 - Processing

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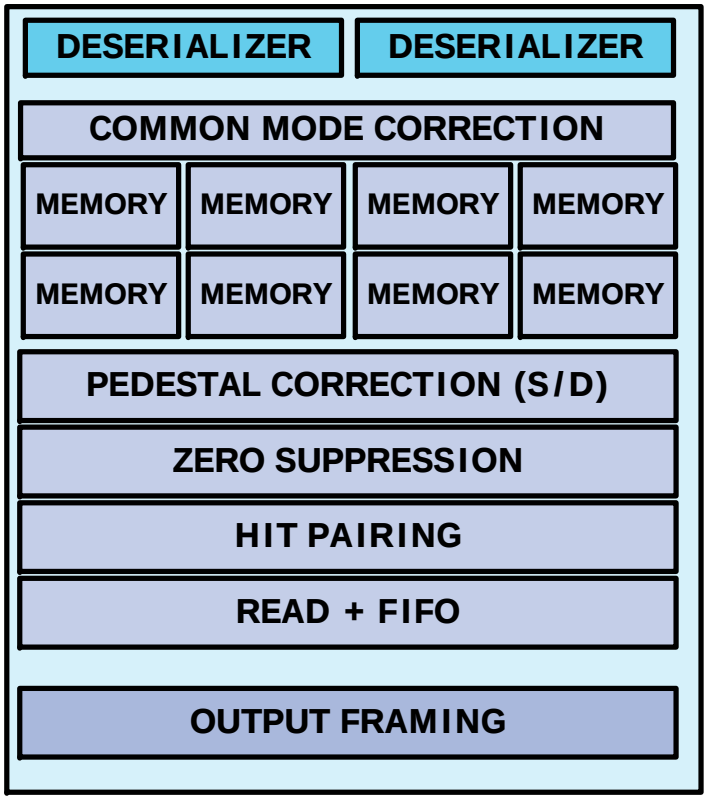
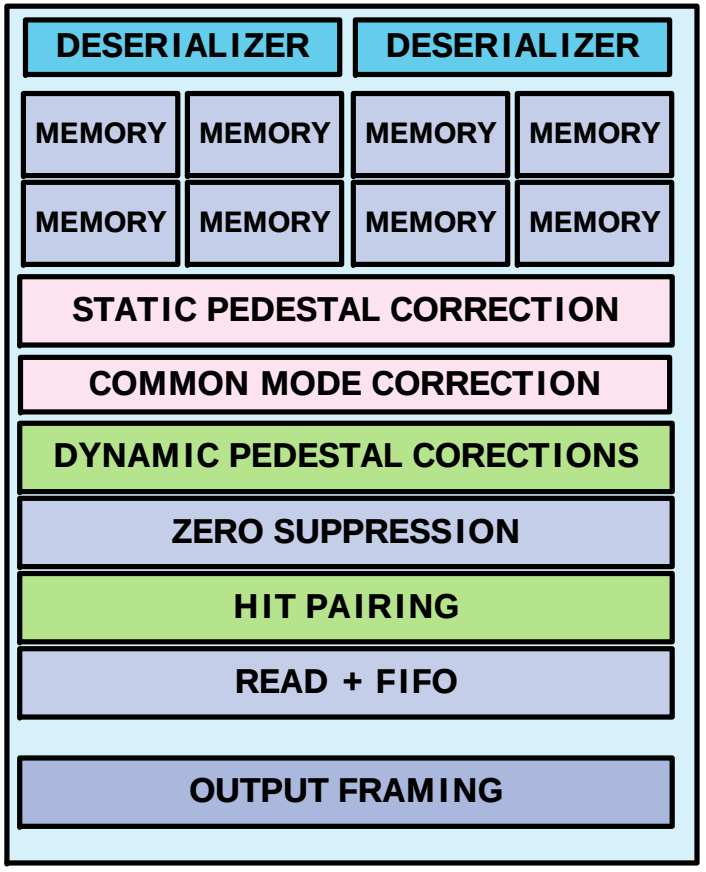
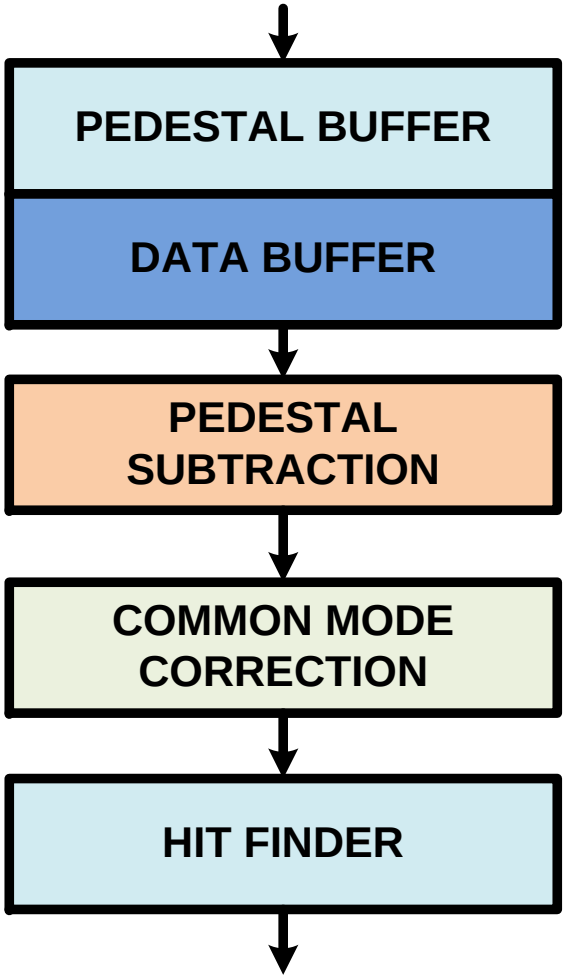
DHP 0.1



DHP 0.2



DHP 0.2 - Data Processing



- 1024 rows buffer for data and for pedestals and offsets
- 8 bit static pedestal subtraction
- 2 pass common mode correction (signal rejection)

DHP 0.2 - Interface

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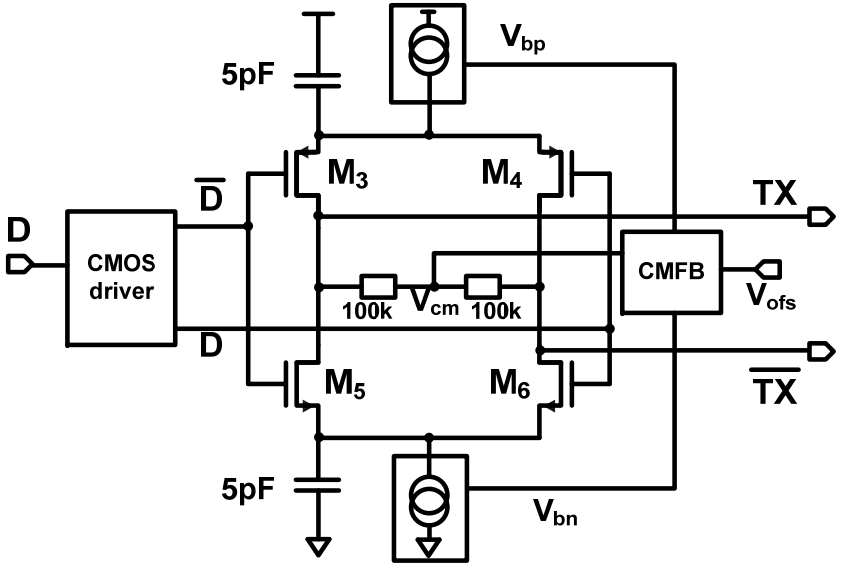
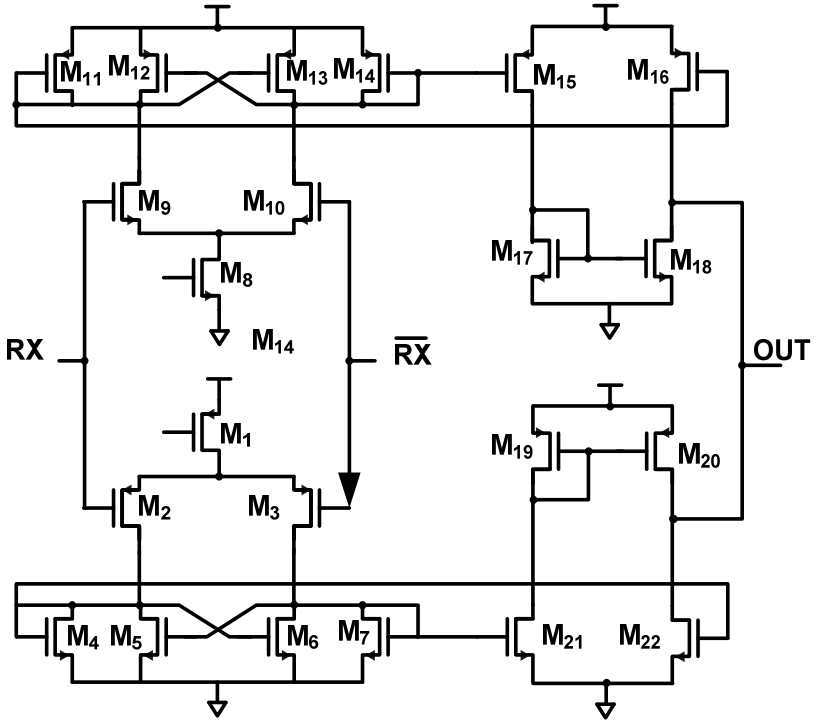
LVDS TX



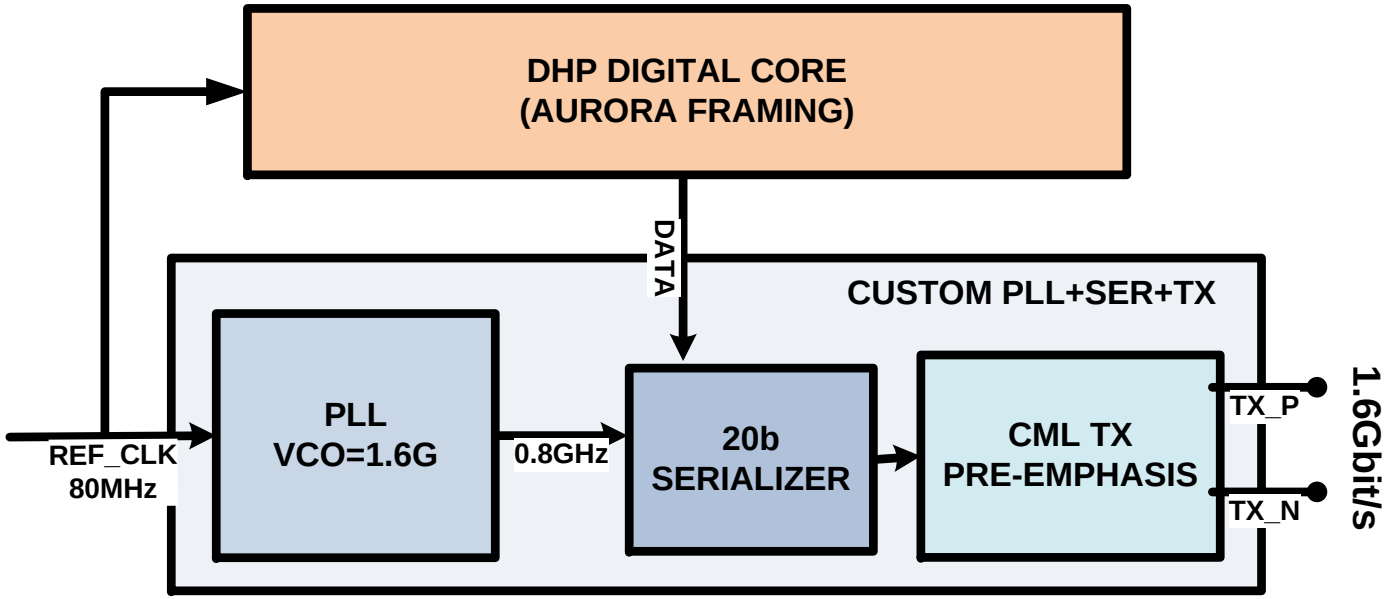
Rail-to-Rail LVDS RX



- **+ Custom Area I/O Pads**

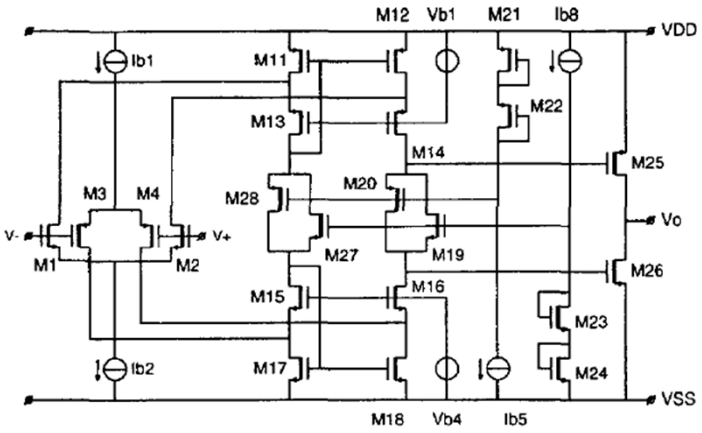
DHP 0.2 – PLL+Ser+TX

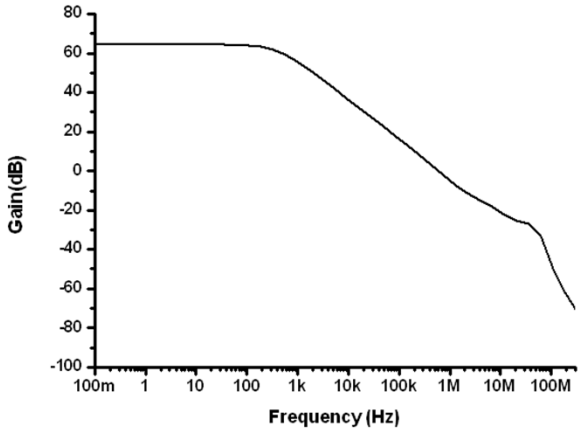
- Integrated PLL, Serializer and CML TX
- Separate power domain

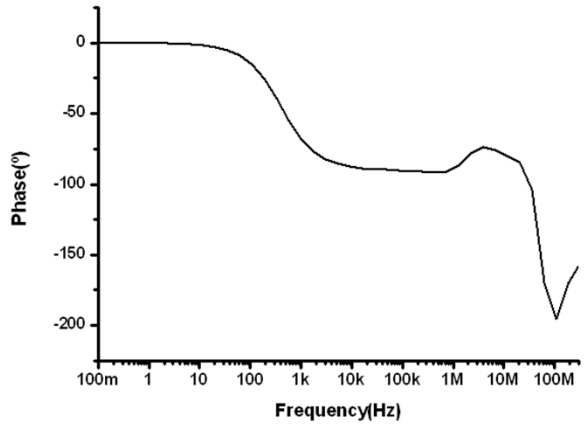


8-bits DAC redesign

- **DHP 0.1 tests showed that the 8-bits DAC and 10-bits ADC had to be redesigned in order to have a rail-to-rail output.**
- **8-bits DAC has been redesigned (schematic level).**
- **New op-amp with Avo=64 dB, PM=88.46º and a rail-to-rail output range.**



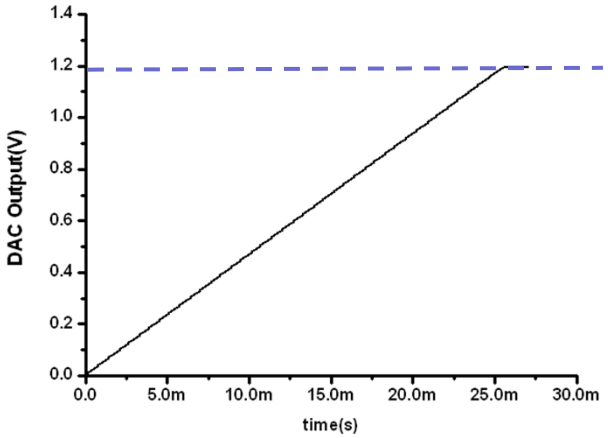




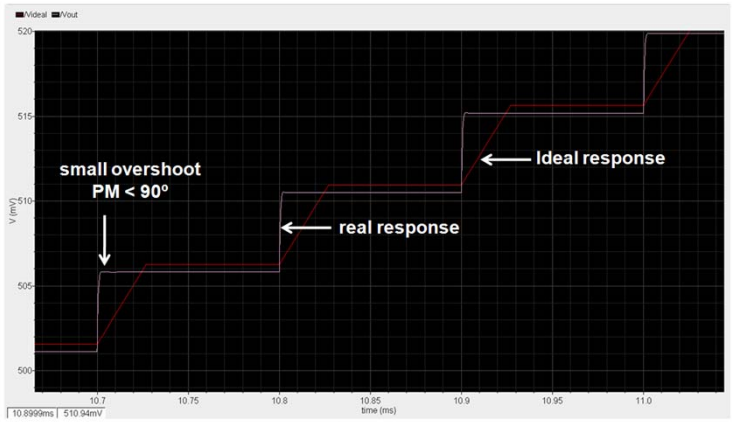
R. Hogervorst, et. al.,"A Compact Power-Efficient 3 V CMOS Rail-to-Rail Input/Output Operational Amplifier for VLSI Cell Libraries", JSCC, vol. 29, no. 12, pp. 1505-1513, Dec. 1994.

8-bits DAC redesign

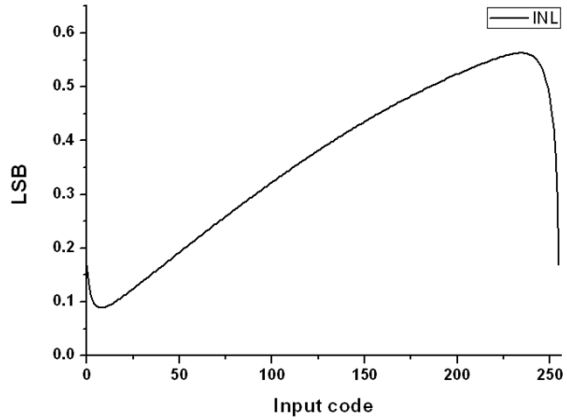
Rail to rail 8-bits DAC

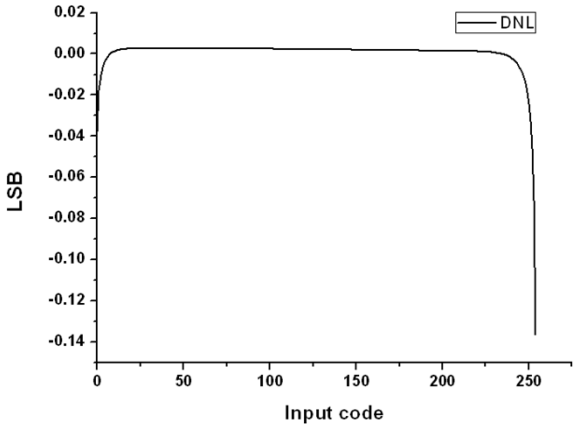


Dynamic response

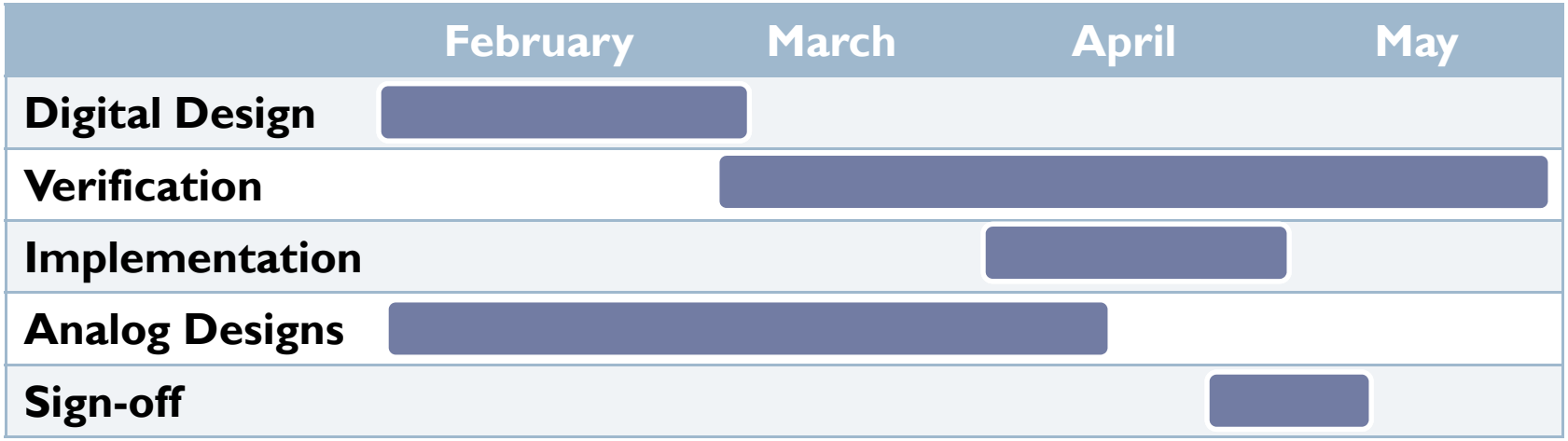


•Op-amp PM = 88.46 º < 90º ➡ small overshoot.





DHP 0.2 Timetable



- **Want to be ready for May 2011 Submission**