SVD → PXD Data Concentrator (DC)

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Outline

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1.- Why do we need a Data Concentrator?

2.- Expected data rates

3.- Options under study

Commercial board
ATCA based

Data sizes

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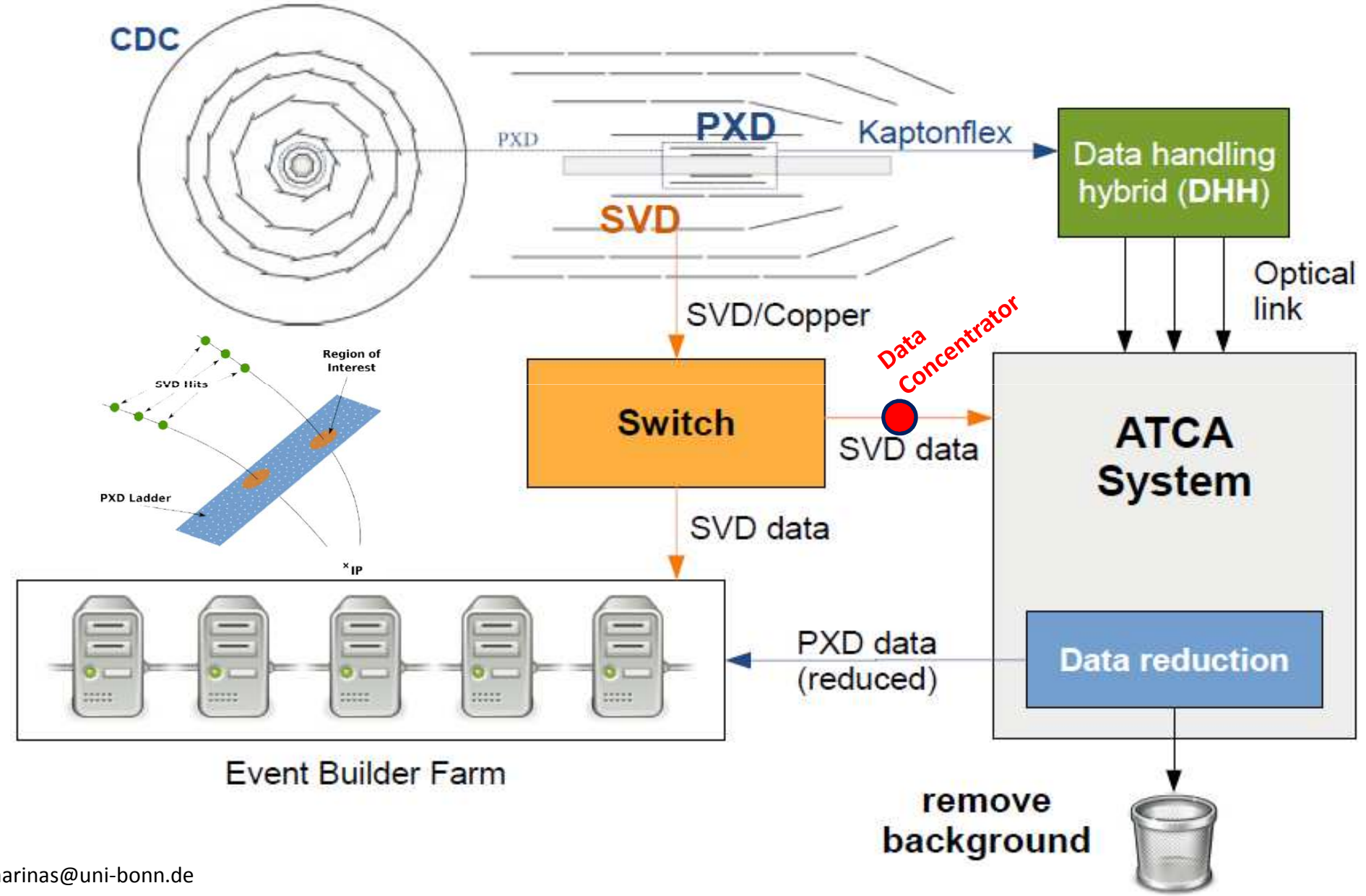
	#ch	occ. [%]	#link	/link [B/s]	#COPPER	ch size [B]	ev size [B]	total [B/s]	/COPPER [B/s]
PXD	8M	1	40	182M	—	4	320k	7.2G	—
SVD	243456	1.9	80	6.9M	80	4	18.5k	555M	6.9M
CDC	15104	10	300	0.6M	75	4	6k	175M	2.3M
BPID	8192	2.5	128	7.5M	8	16	4k	120M	15M
EPID	77760	1.3	138	0.87M	35	0.5	4k	120M	15M
ECL	8736	33	52	7.7M	13	4	12k	360M	30M
BKLM	21696	1	86	9.7M	6	8	2K	60M	10M
EKLM	16800	2	66	19.5M	5	4	1.4k	42M	8.4M

The expected data rate produced in the PXD is higher than the sum of the other subdetectors together!

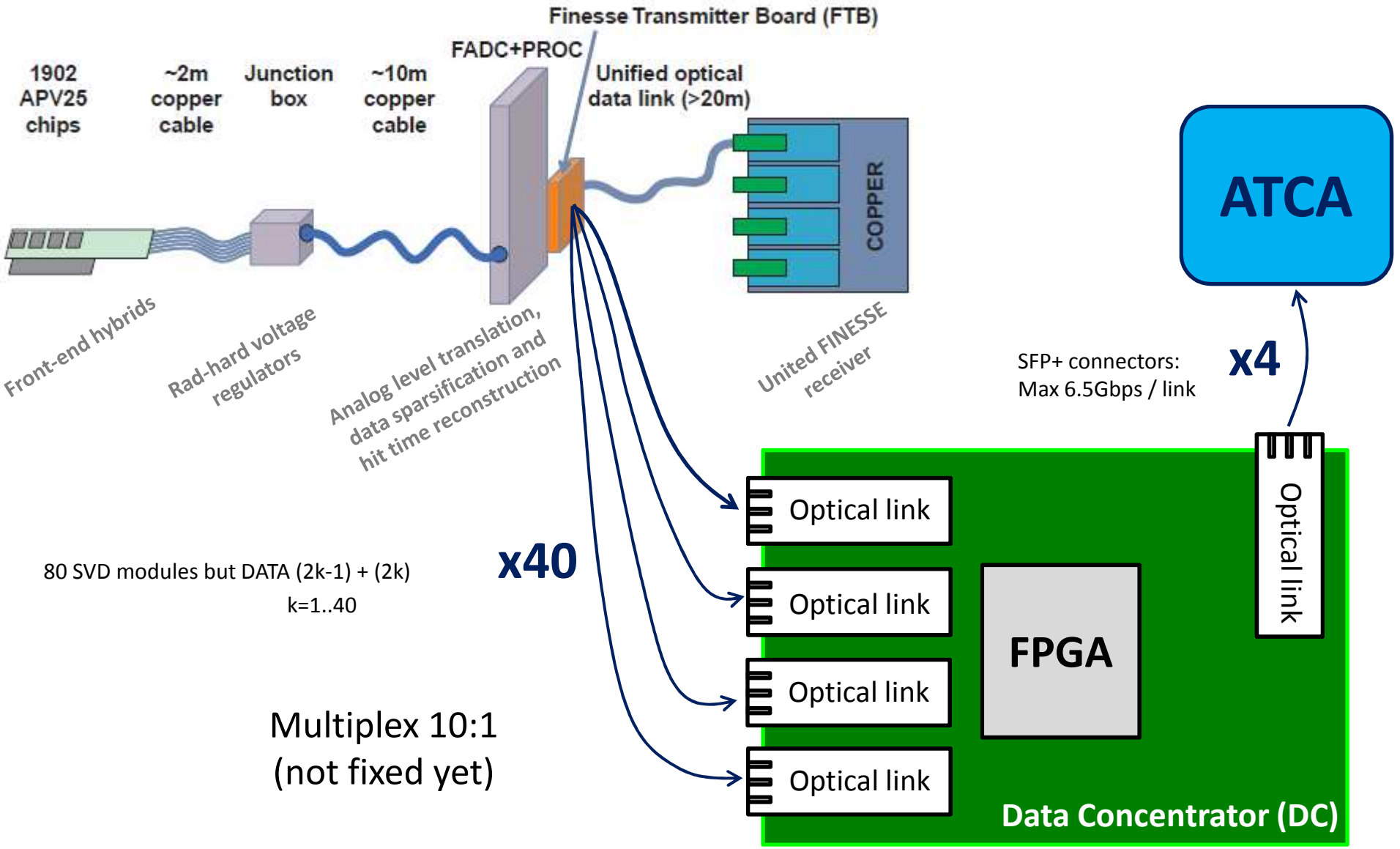
(even just with a 1% of occupancy)

The most part is coming from background → no interesting physics events there!

Data reduction



In short…



80 SVD modules but DATA (2k-1) + (2k)
k=1..40

Multiplex 10:1
(not fixed yet)

Expected SVD data rates

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Using an instantaneous luminosity of $8 \cdot 10^{35}$ cm^{-2} s^{-1} and an average trigger rate of 30kHz

Layer	Radius (mm)	Occupancy	RO chips	RO strips	Hit strips
6	140	0.9%	850	108800	967
5	115	1.3%	560	71680	944
4	80	2.7%	300	38400	1045
3	38	6.7%	192	24576	1647
Average / Sum		1.9%	1902	243456	4602

Depending on the level of online data processing (if 80 lines; if 40, multiply the numbers by 2):

Case	Average occupancy	Data size/ channel (B)	Event size (B)	Total data rate (B/s)	Data rate/ link (B/s)
1	1.9%	12	53.9k	1.54G	19.7M
2	1.9%	4	18.0k	527M	6.6M
3	0.4%	12	10.8k	316M	3.9M
4	0.4%	4	3.6k	105M	1.3M

4Byte containing Strip ID+Data

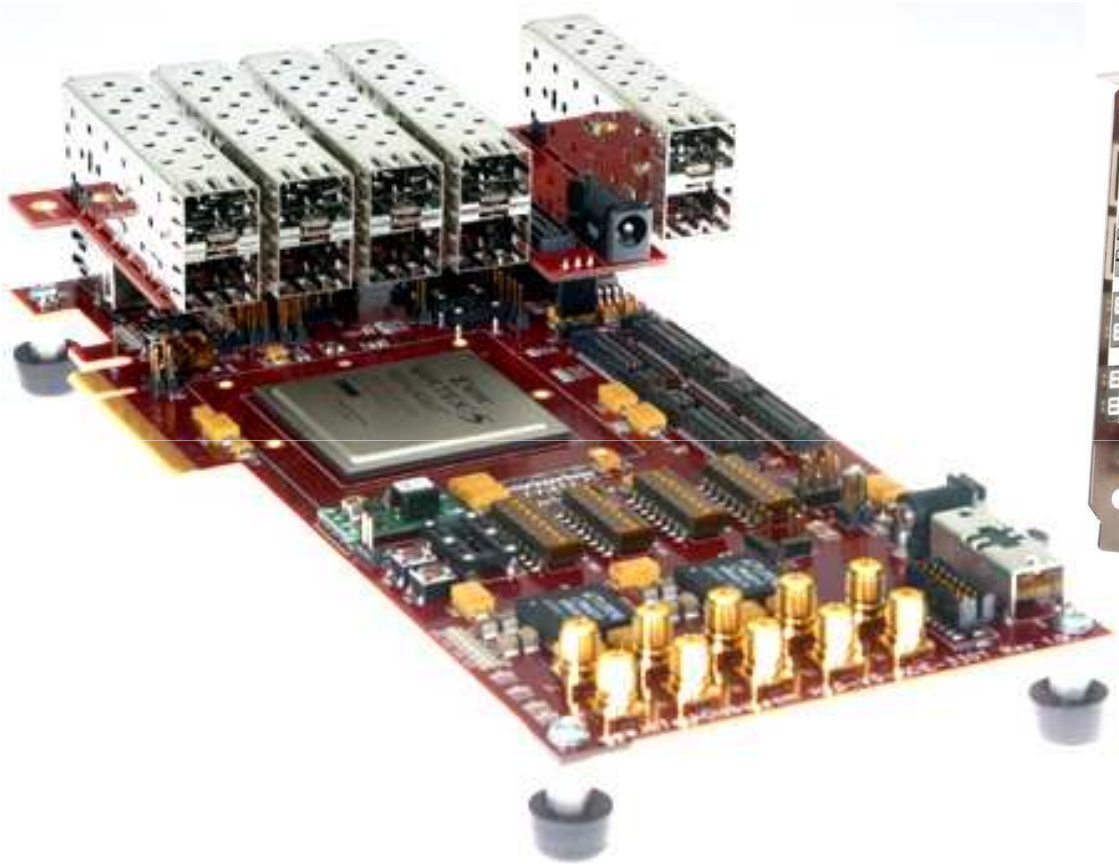
We consider four levels of data processing related to hit time finding:

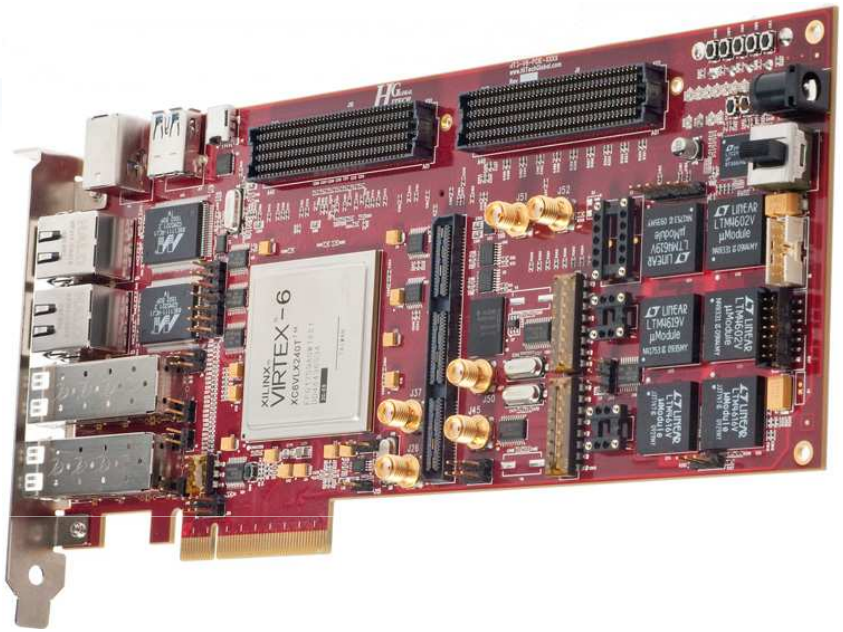
1. no hit time finding, 6 samples per hit
2. no hit time finding, 1 sample per hit
3. online reduction by hit time finding, 6 samples per hit
4. online reduction by hit time finding, 1 sample per hit

For security reasons, we set the expected occupancy into a **7%** (max. occupancy)

→ This translates in data rates in the order of hundreds of Mbits/s/link

First option: Commercial solution





- Produce an add on card with SFP connected to RocketIO
- Do the programming

Pros: Can be close to the Finesse Transmitter Boards. Only a few long optical fibers to the ATCA

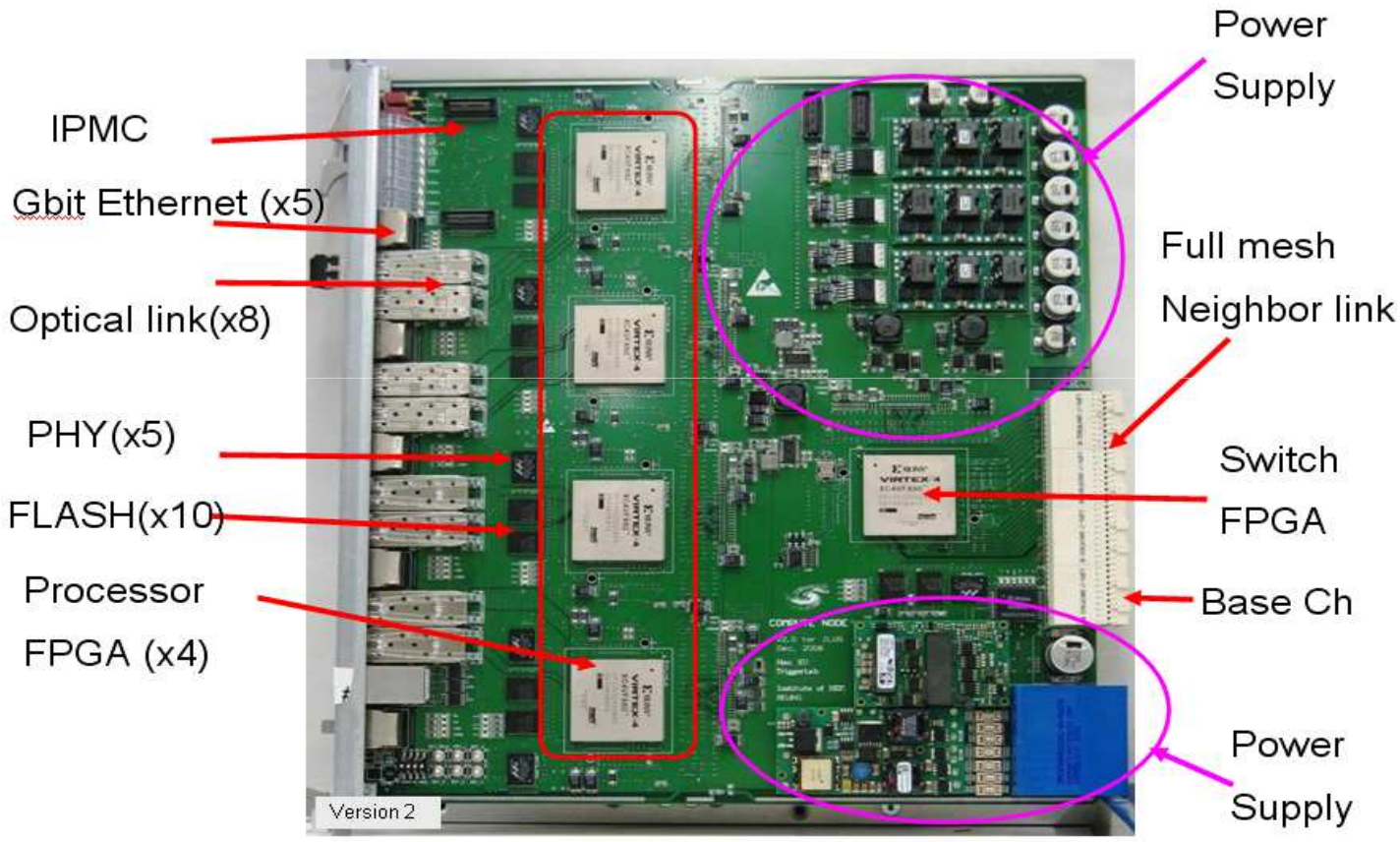
Cons: Price? Complexity?

Second option: ATCA based

Using the Compute Nodes of the ATCA system

Adapted to our needs?

Up to 8 SFP+ connected to RocketIOs



Pros: Already integrated in the ATCA system

Cons: Long optical fibers from Finesse Transmitter Boards?

Open questions

➢ Technical details:

- 40 input links from the SVD
- 500Mbps is the expected bandwidth of each link (7% occupancy)
- SFP+ connectors
- Encoding: 8B10B
- Aurora protocol. Wizard version 1.6

- In case of commercial solution: Can the Data Concentrator do a part of the data reduction?
  Virtex 6 with a lot of memory and computational power availiable

- In case of ATCA based: Can another ATCA crate be used as a DC with minor modifications?
  Virtex 4 adapted with several SFP connectors?

Summary

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- New project already started in Bonn
- Working in the definition of the requirements with Krakow and Giessen
  - ➢ Meeting next week in Giessen
- Two solutions are on the table:

  Commercial FPGA board
  ATCA based
  Any other? Ideas are welcome

- Decision will be taken soon

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THANK YOU VERY MUCH!

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► **Features:**

- **Xilinx Virtex 6** LX550T, LX365T, LX240T, SX475T, or SX315T in different speed grades
- x8 PCI Express Gen 2 Edge Connector
- PCI Express Jitter Attenuator for cleaning PC clock and generating different PCIe clocks (100MHz, 250MHz, etc.)
- DDR3 SO-DIMM (up to 4GB)
- One USB 2.0 & 3.0 Host port
- One USB 2.0 & 3.0 Device port
- Two SFP ports (4 additional SFP and two SFP+ connectors are available through HTG-FMC-4SFP-4SATA and HTG-FMC-SFP-PLUS modules)
- Four SMA connectors for one GTX serial transceiver port (8 additional SMA ports are available through HTG-FMC-8SMA module)
- Two SMA connectors for external differential clock
- Two 10/100/1000 Ethernet ports with SGMII, RGMII, and GMII support using Marvell 88E111 PHY (4 additional SGMII ports are available through HTG-FMC-RJ45 module)
- FMC Vita 57 compliant Connectors with :
  - Connecter #1:
    160 Single Ended IOs (or 80 LVDS), & ten Data-Rate-Adjustable GTX transceivers with the LX550T, LX365T, LX240T, SX475T, or SX315T models
  - Connecter #2:
    126 Single Ended IOs (or 63 LVDS) with the LX550T, LX365T, LX240T, SX475T, or SX315T models
    160 Single Ended IOs (or 80 LVDS), & ten Data-Rate-Adjustable GTX transceivers with the LX550 and SX475 models
- Auxiliary FMC Super Clock for board-to-board communication
- Samtec QSE High-speed connectors with 32 pairs of LVDS IOs
- IP Protection Chipset
- Power Management Bus for all voltage rails
- Size: 9.5" x 4.25"
- **Support for both PCI Express and stand alone operation modes**
- Standard ATX and wall power supply connectors

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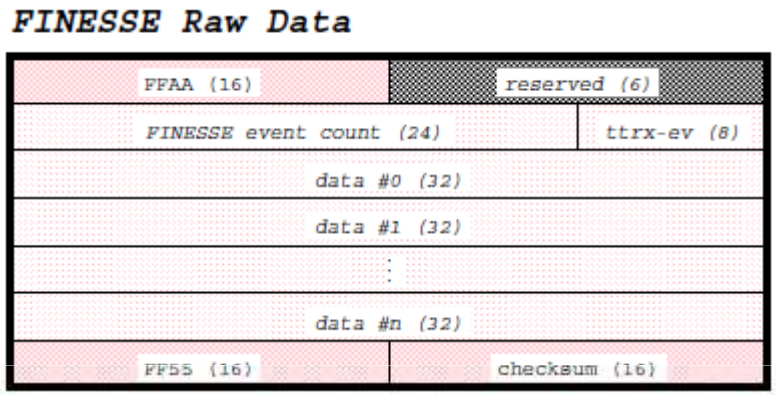
Raw data format output from the FINESSE card:



Unified high speed Belle2Link: Belle-II DAQ system uses the RocketIO GTP technology over optical fibers for the data transmission between the front-end electronics (FEE) and the backend system.

GTP is a cost-effective version of the RocketIO which can handle up to 3.125Gbps line rate on LXT series of the Xilinx Virtex5, Virtex6 and Spartan6 FPGA.

Belle2Link is an unified high speed link that has been defined for use in all connections between each of the subsystems.

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Features:

- **Xilinx Virtex-5** LX330T, FX200T, or SX240T FPGA (FF1738 package)
- 8-Lane PCI Express End-Point (upstream) Connector - Gen 1 with LXT/SXT and Gen 2 with FXT
- Up to 2 GB of SO-DIMM DDR2 Memory (the SO-DIMM socket is populated on the flip side of the board)
- 2 RocketIO GTP (3.128 Gbps) /GTX (6.5 Gbps) Ports accessible through 8 SMA connectors (4 Rx & 4 Tx with SMA for external clock)
- 10 datarate-adjustable RocketIO GTP/GTX Ports accessible through high speed Samtec QSE connectors
- 68 Pairs of LVDS (2.5V) or 136 Single-Ended (3.3V) IOs accessible through high speed Samtec connectors
- 2 SATA Ports (I/II)
- 2 Gigabit Ethernet Ports (both with SGMII support)
- PCI Express Jitter Attenuator with adjustable outputs
- Super Clocks with adjustable outputs for the SATA and RocketIO GTP ports
- External Clock input
- 256 Mb Intel Flash Memory (for FPGA configuration and additional Flash storage)
- ATX and Standard 5 V Power Connectors (supporting stand alone operation)
- Jumper for Stand Alone mode
- Jumper for FPGA configuration via PCIe bus
- Size: 8.75 " x 4.25 "
- Linear Technology FPGA/RocketIO Power Regulators LTM4601EV and LTC3026 (Linear Technology Power Management Solution for Xilinx devices)

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First prototype

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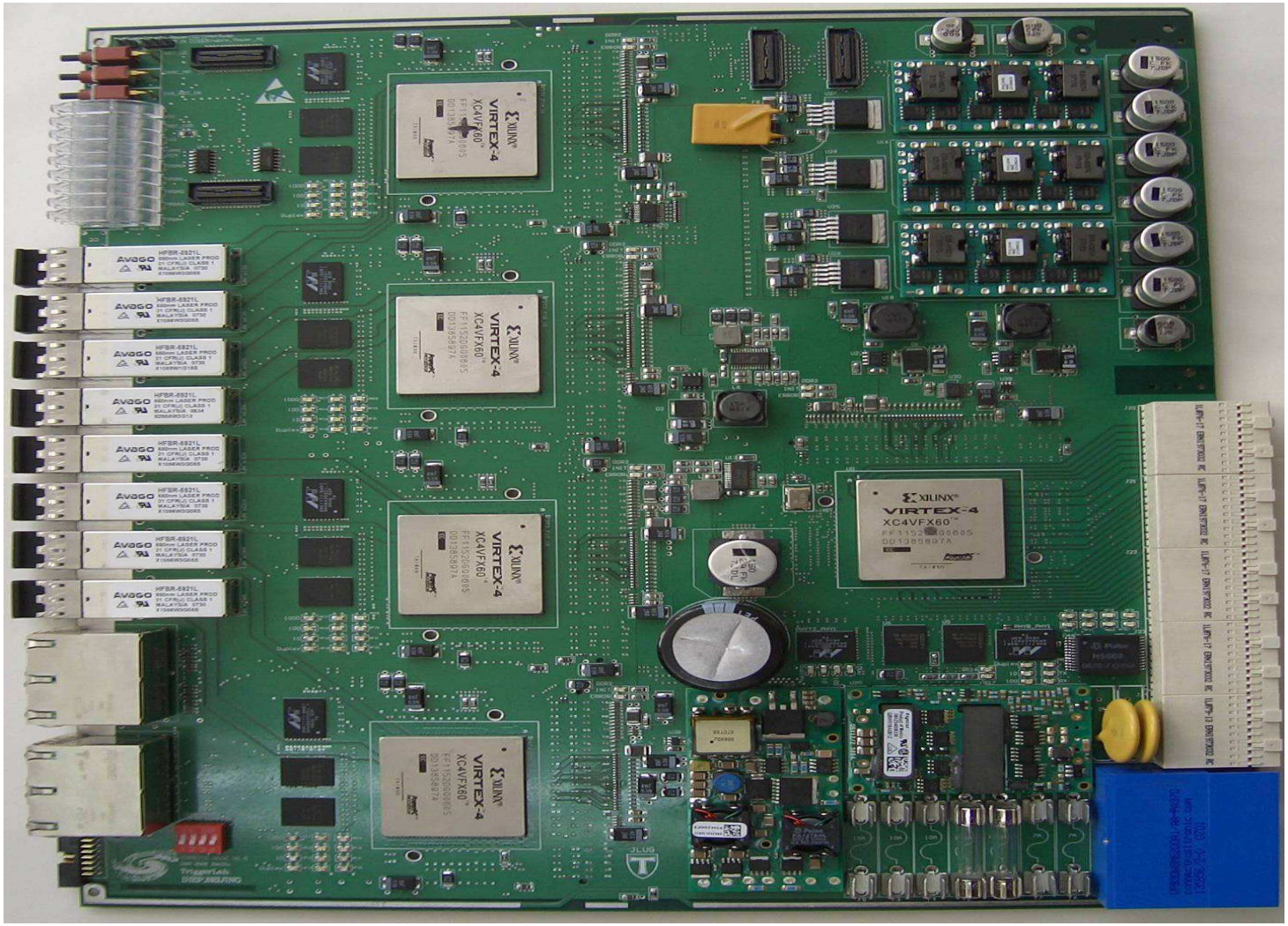

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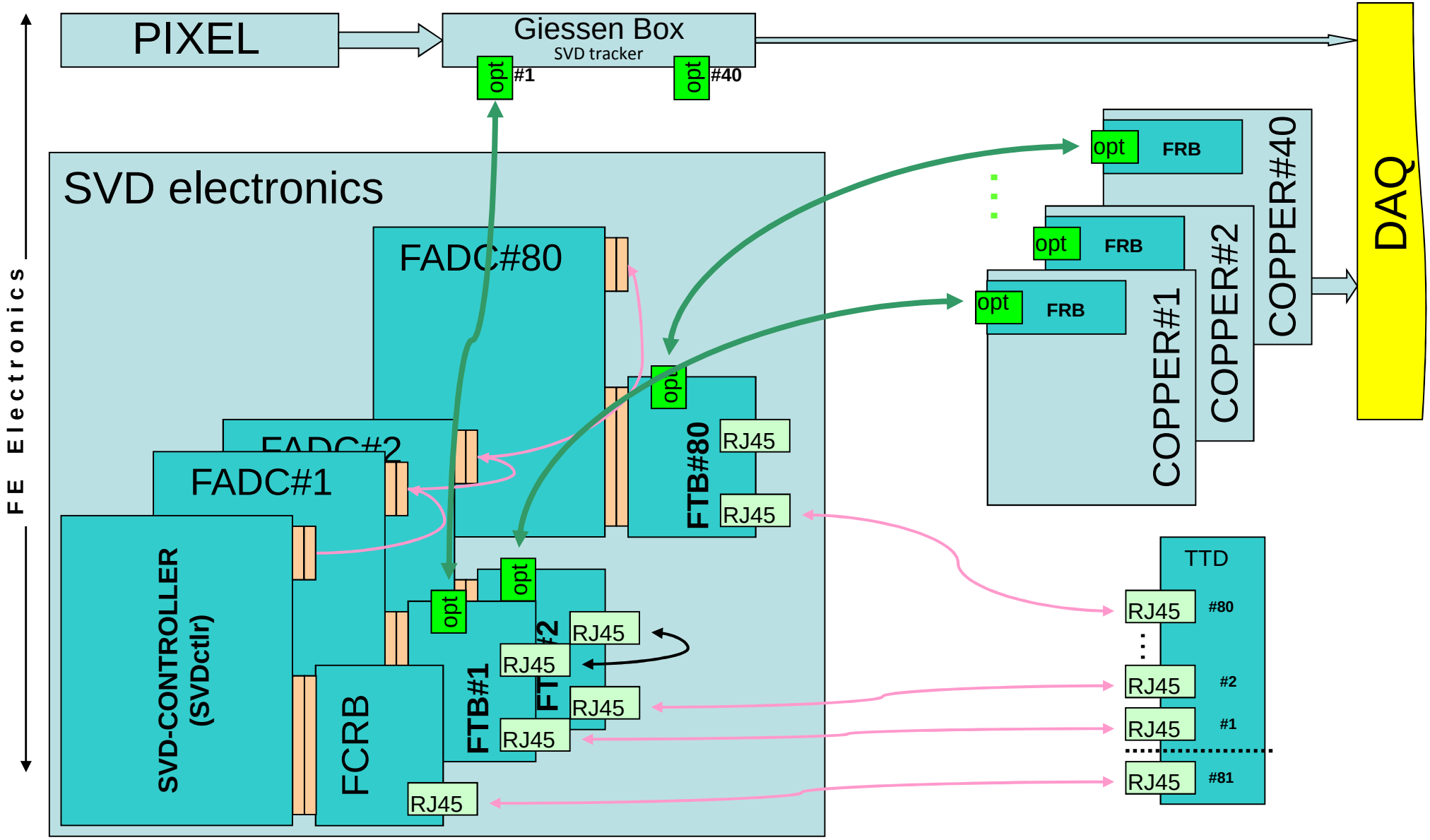
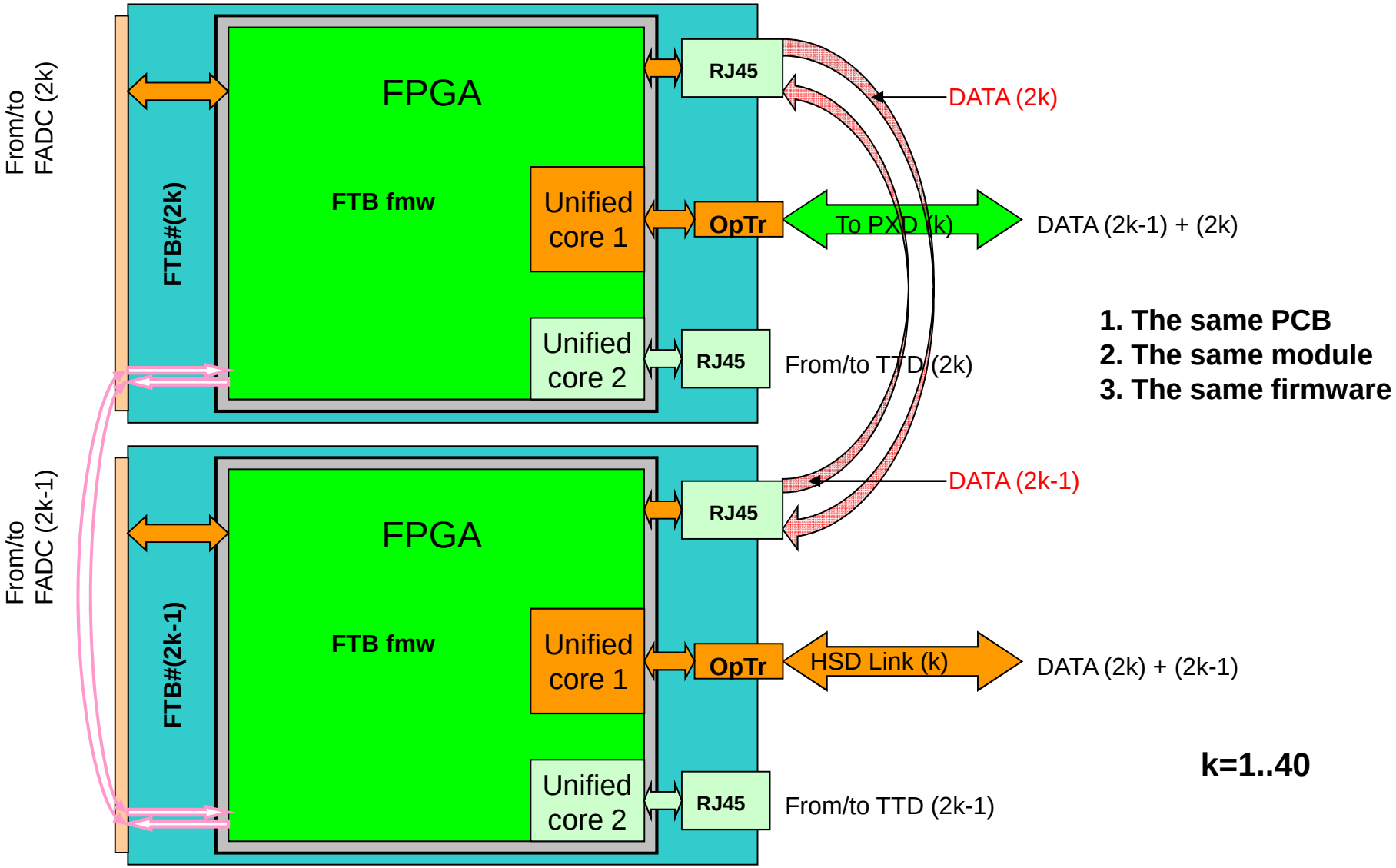
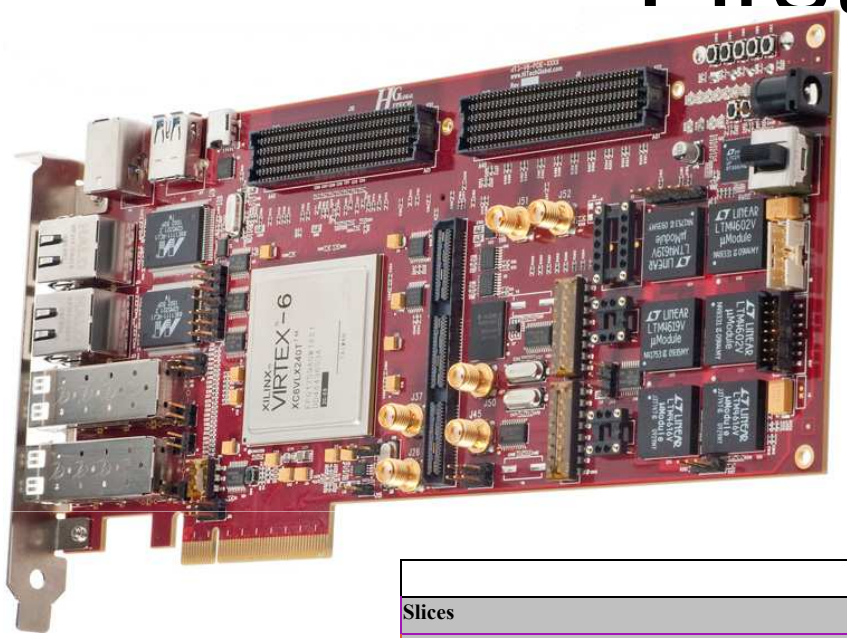
General view – 40 sets of two boards



Two boards - one set



First option



Design an *ad hoc* board with SFP transceivers to connect to the FMC connectors

- How many RocketIO availiable in the FMC?
- Lines characteristics FMC to FPGA

	XC6VLX240T	XC6VLX365T	XC6VLX550T	XC6VSX475T	XC6VSX315T
Slices	37,680	56,880	**85,920**	74,400	49,200
Logic Cells	241,152	364,032	**549,888**	476,160	314,880
CLB Flip-Flops	301,440	455,040	**687,360**	595,200	393,600
Maximum Distributed RAM (Kbits)	3,650	4,130	**6,200**	7,640	5,090
Block RAM/FIFO w/ ECC (36Kbits each)	416	416	**632**	1,064	704
Total Block RAM (Kbits)	14,976	14,976	**22,752**	38,304	25,344
Mixed Mode Clock Managers (MMCM)	12	12	**18**	18	12
Maximum Single-Ended I/O	720	720	**1200**	840	720
Maximum Differential I/O Pairs	360	360	**600**	420	360
DSP48E1 Slices	768	576	**864**	2,016	1,344
PCI Express® Interface Blocks	2	2	**2**	2	2
10/100/1000 Ethernet MAC Blocks	4	4	**4**	4	4
GTX Low-Power Transceivers	24	24	**36**	36	24
Commercial	-L1, -1, -2, -3	-L1, -1, -2, -3	**-L1, -1, -2**	-L1, -1, -2	-L1, -1, -2, -3
Configuration Memory (Mbits)	70.4	91.6	**137.4**	149.4	99.6

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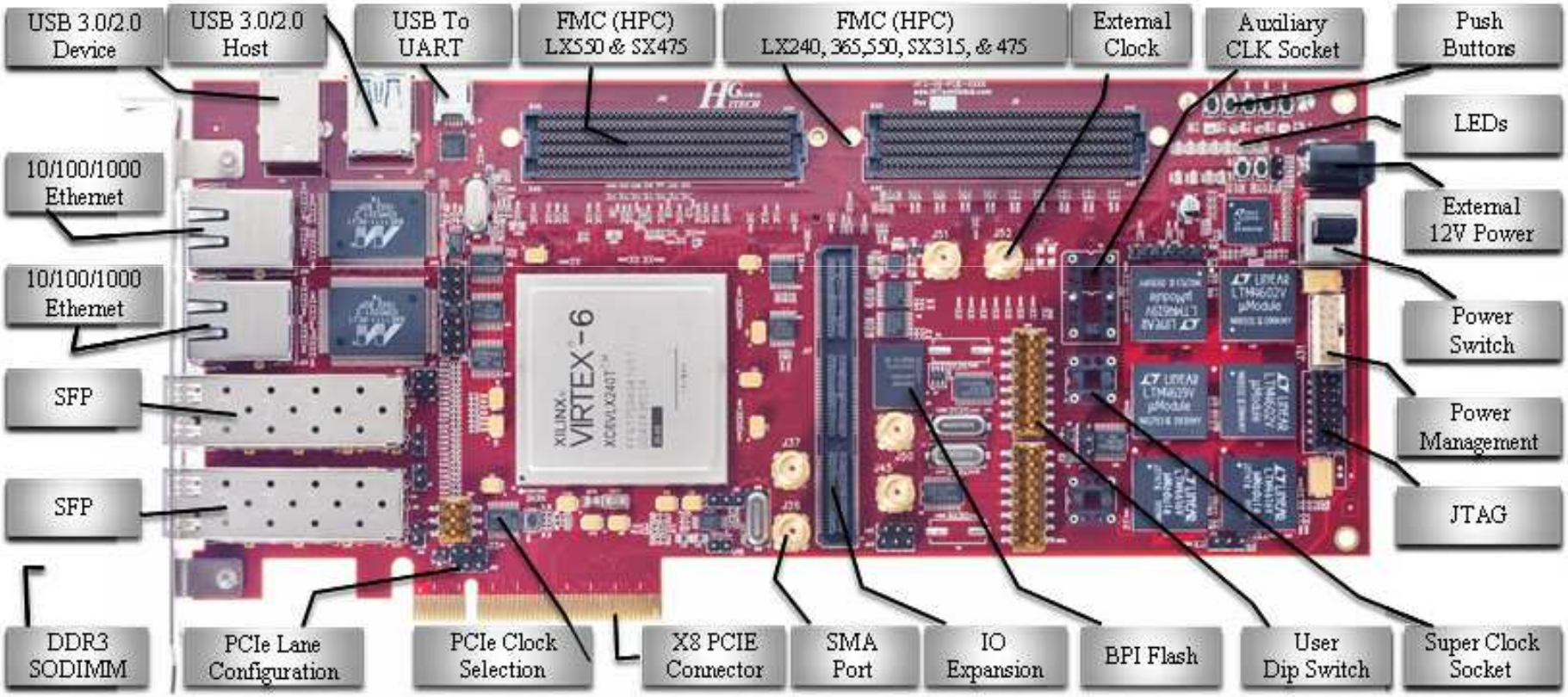
Detailed view



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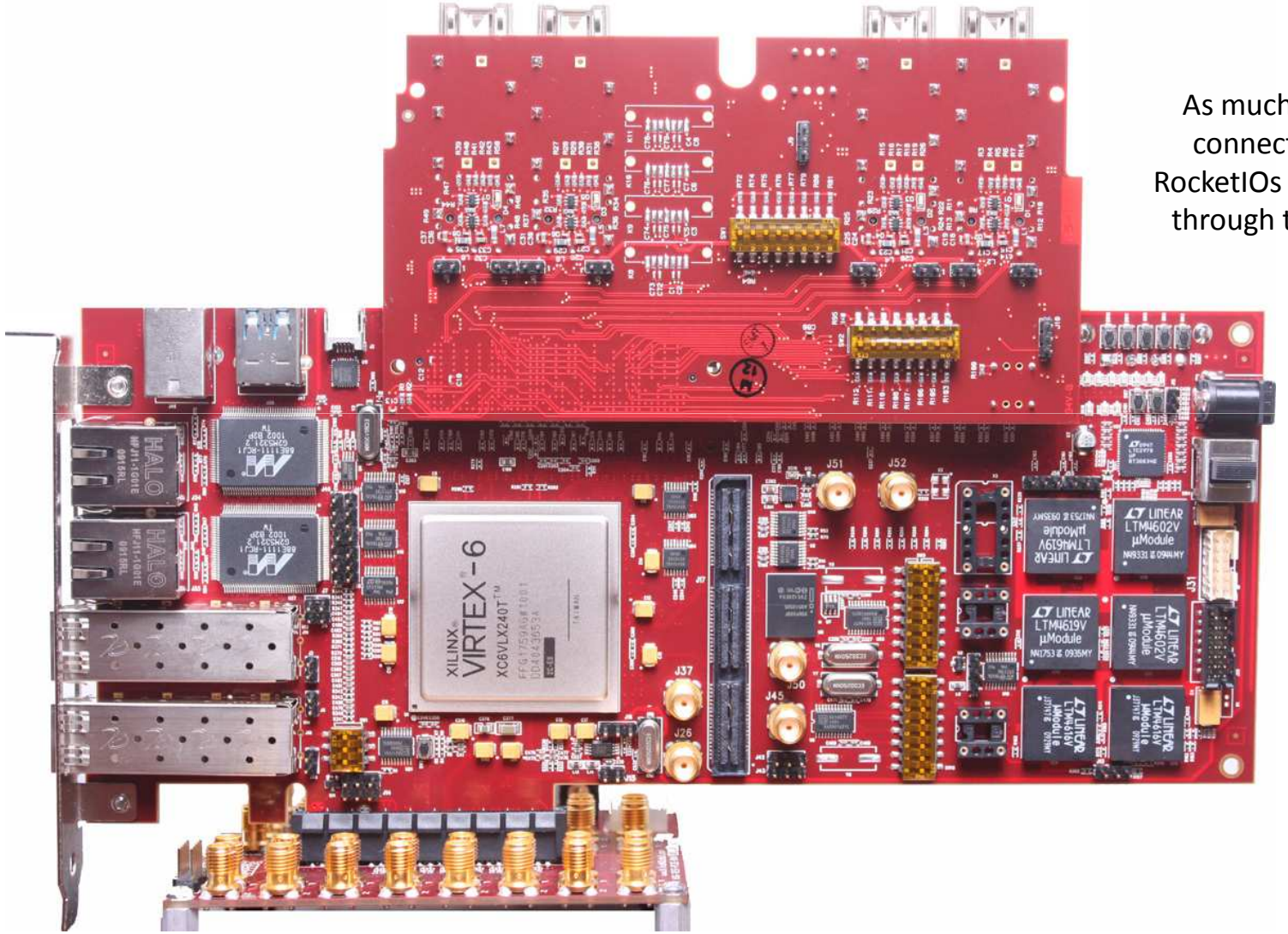
Somehow the idea…



As much as SPF connectors as RocketIOs availiable through the FMC

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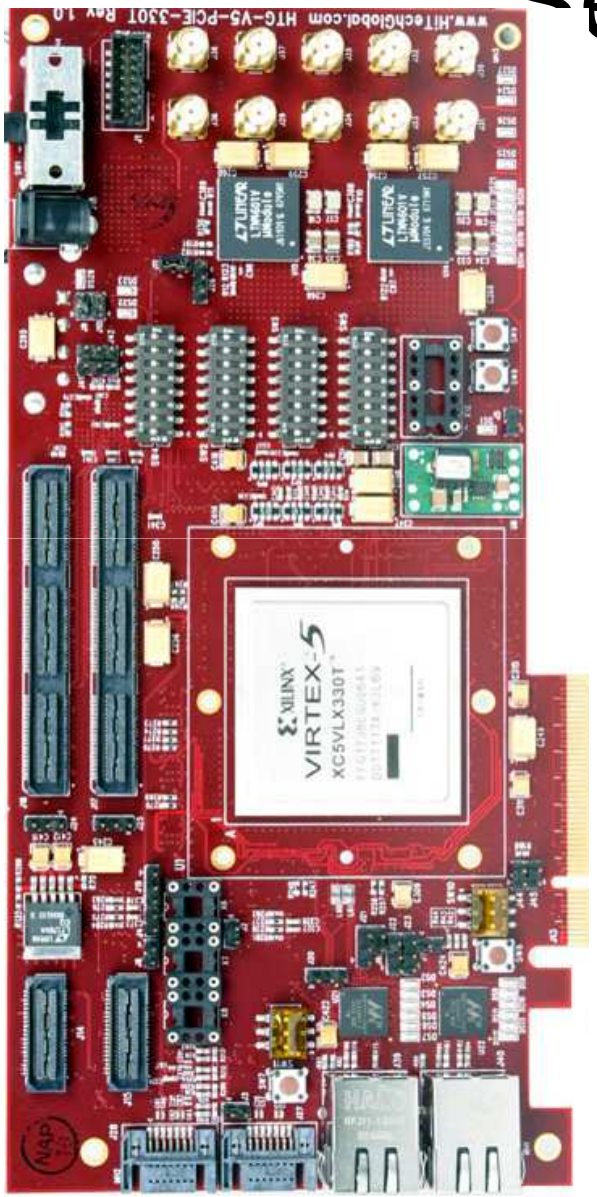
Second option



- Less number of GTP transceivers
- A comercial add on card already availiable

Part Number	XC5VLX330T	XC5VSX240T	XC5VFX200T
Slices	51,840	37,440	30,720
Logic Cells	331,776	239,616	196,608
CLB Flip-Flops	207,360	149,760	122,880
Maximum Distributed RAM (Kbits)	3,420	4,200	2,280
Block RAM/FIFO w/ECC (36Kbits each)	324	516	456
Total Block RAM (Kbits)	11,664	18,576	16,416
Digital Clock Managers (DCM)	12	12	12
Phase Locked Loop (PLL)/PMCD	6	6	6
Maximum Single-Ended Pins	960	960	960
Maximum Differential I/O Pairs	480	480	480
DSP48E Slices	192	1,056	384
PowerPC® 440 Processor Blocks	—	—	2
PCI Express Endpoint Blocks	1	1	4
10/100/1000 Ethernet MAC Blocks	4	4	8
RocketIO GTP Low -Power Transceivers	24	24	—
RocketIO GTX High -Power Transceivers	—	—	24
Configuration Memory (Mbits)	82.7	79.6	70.9

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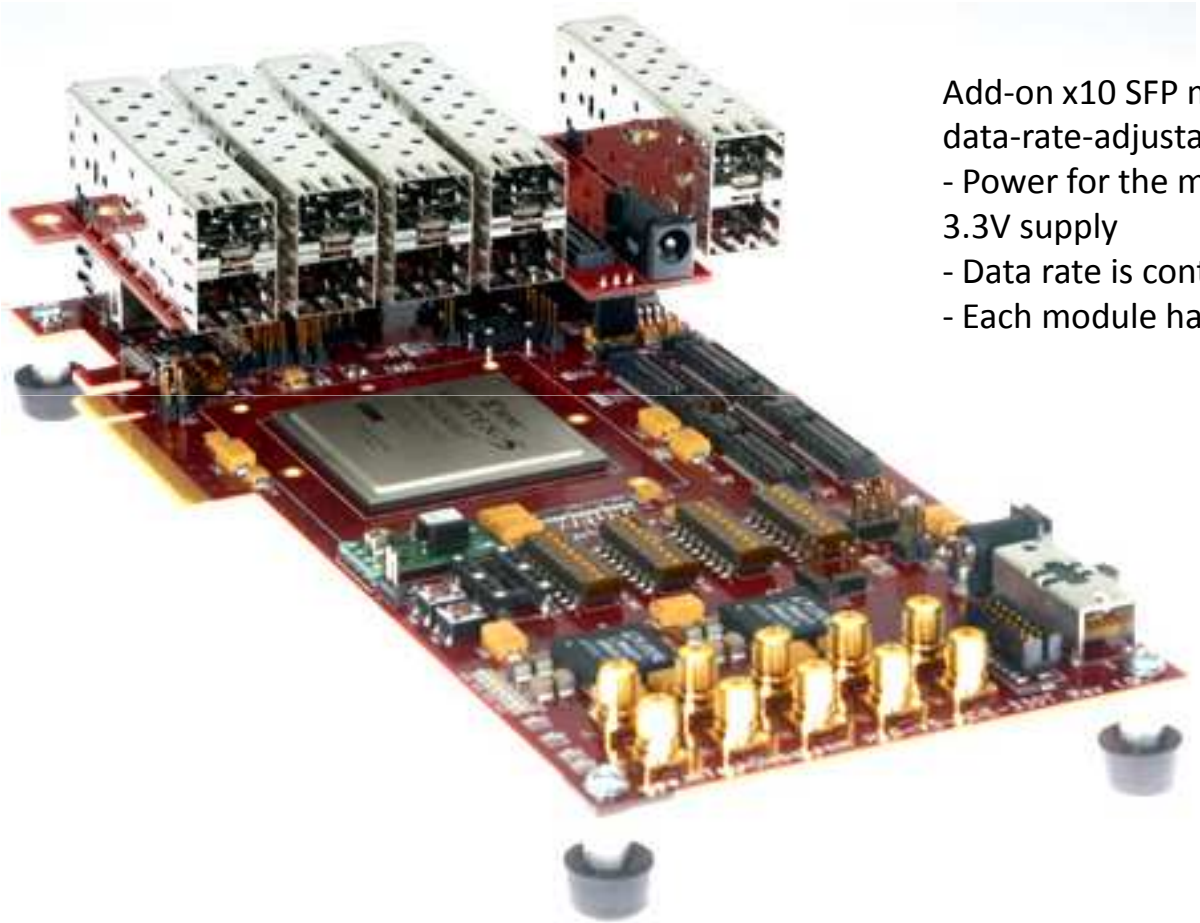
Fully equiped board



Add-on x10 SFP module used in conjunction with the on-board data-rate-adjustable RocketIO GTP transceivers
- Power for the module is supplied by external and/or on-board 3.3V supply
- Data rate is controlled by the on-board super clock
- Each module has its own power filter and control switch

≈ 5 cards needed

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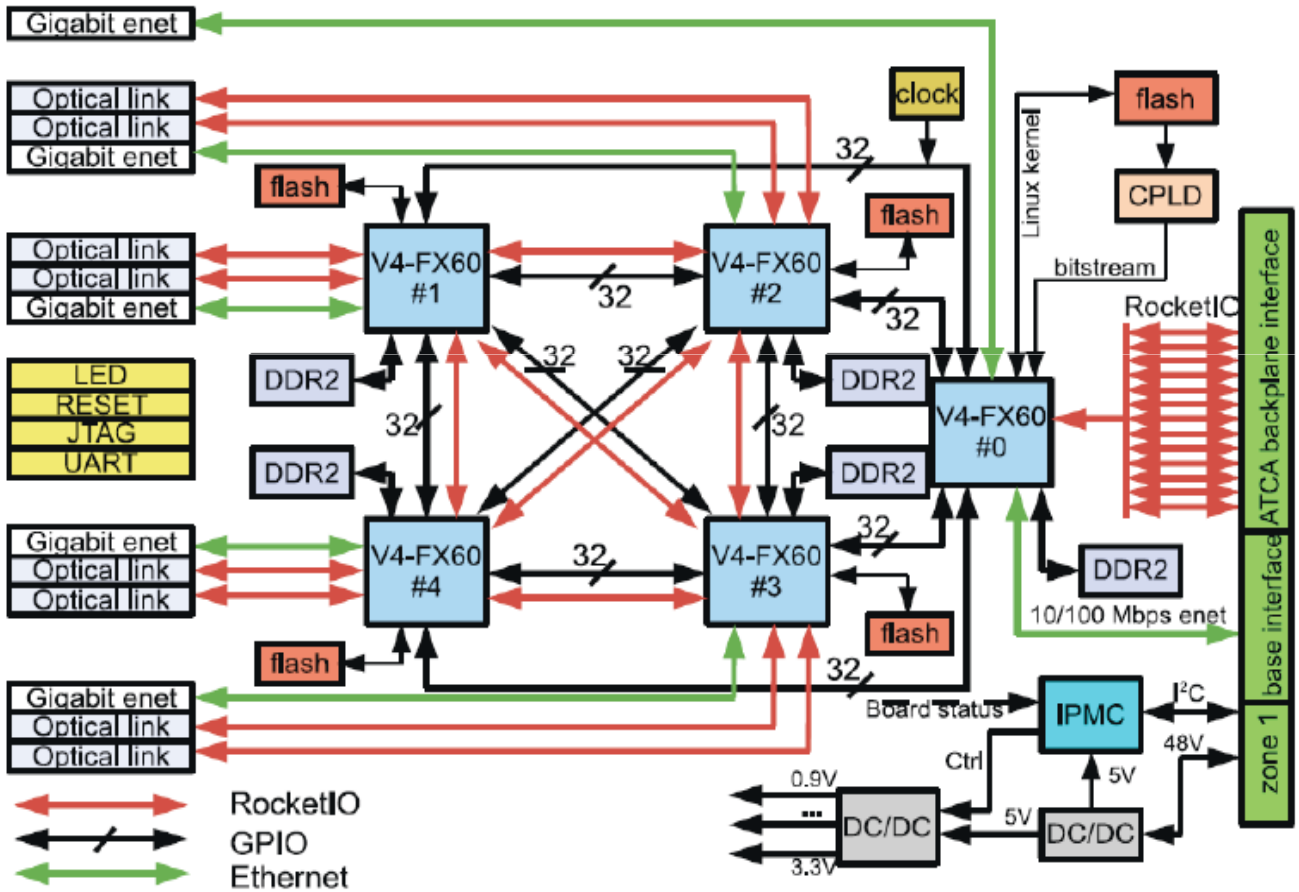
Third option

Using the Compute Nodes of the ATCA system

- High Performance Compute Power/resources:
  - 5 Virtex-4 FX60 FPGA
  - 10Gb DDR2 RAM (2G/FPGA)
- ~32Gbps Bandwidth
  - 8x panel Optical Link (3Gbps each)
  - 13x RocketIO to backplane
  - 5x Gigabit Ethernet
  - 1x GBit Ethernet to backplane



Belle-II DAQ Overview

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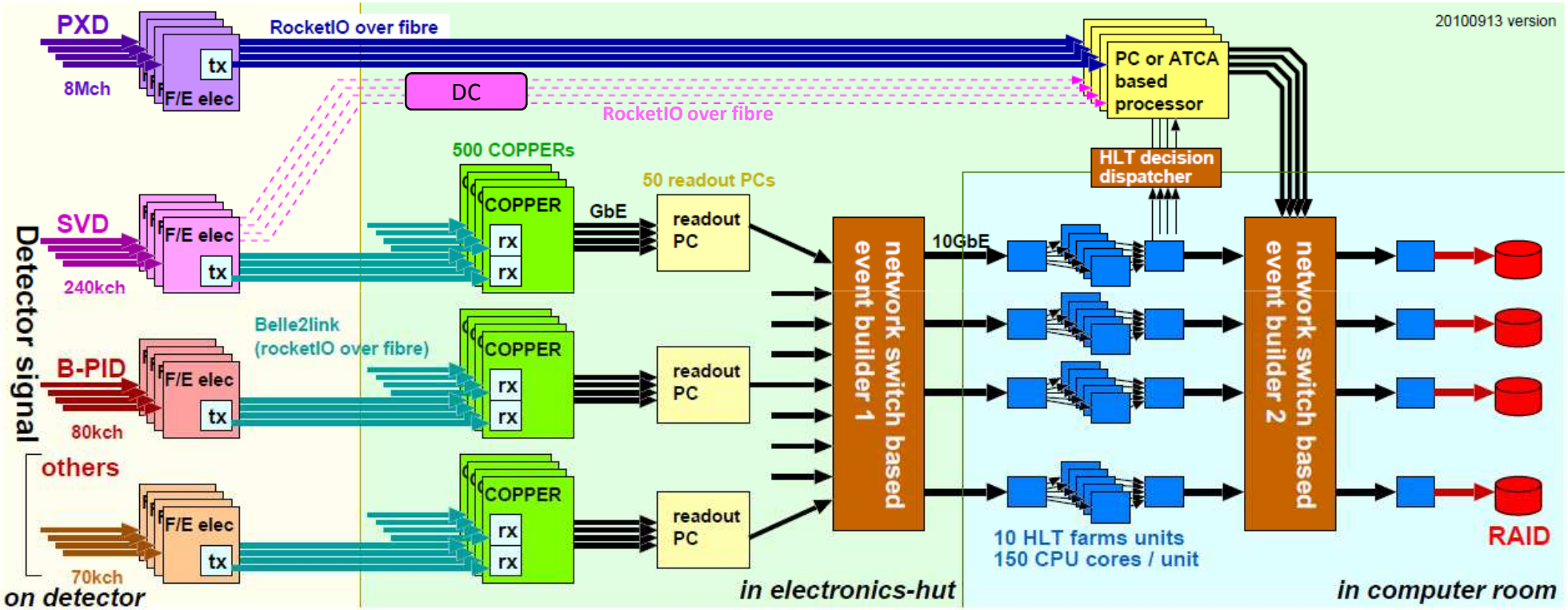

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