Hybrids: Status report

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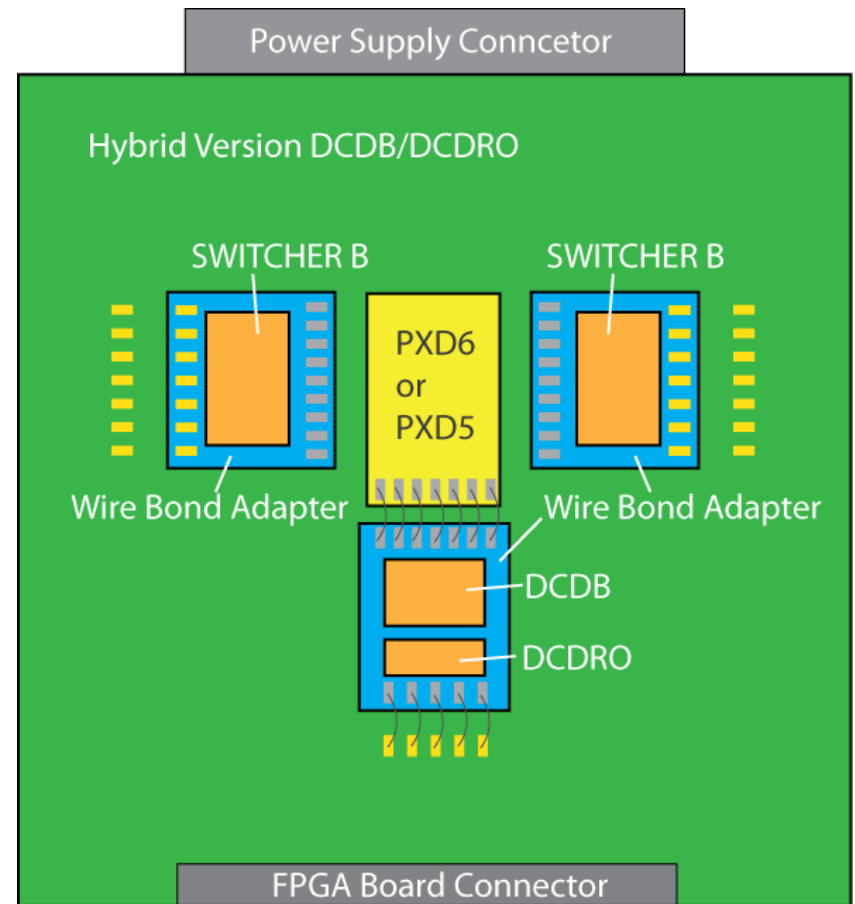
Overview

Hybrid 4.1.x

- Functionality of the Hybrid 4.1.x

- Bring-up of the Hybrid 4.1.x Boards

- Hybrids 4.1.x Overview

- Preparations for the assembly of PXD6

Mini Matrices

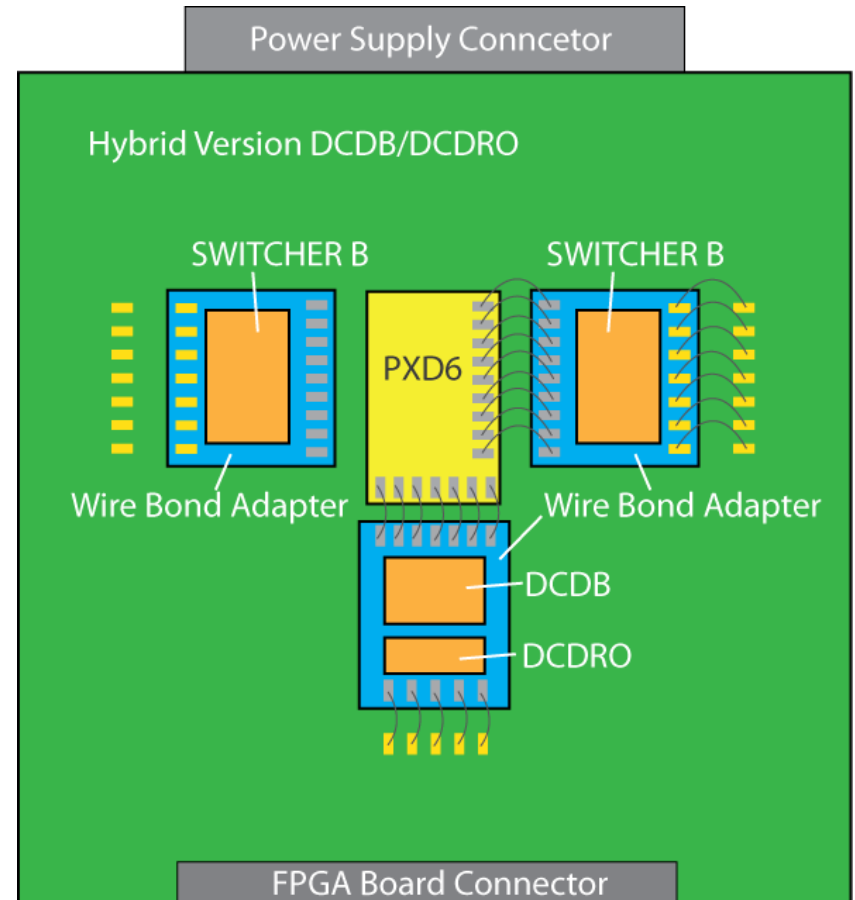- Preparations for the assembly of PXD6

PXD6/PXD5 Hybrid Board H4.1

- 2 x **SwitcherB** to address
  - either a full PXD6 matrix (small matrix 128 x 16)
  - or a part of a PXD5 matrix (128 x 128)

- DCD-B/DCDRO read out

- DEPFET Matrix directly bonded to ASICs/wire bond adapters

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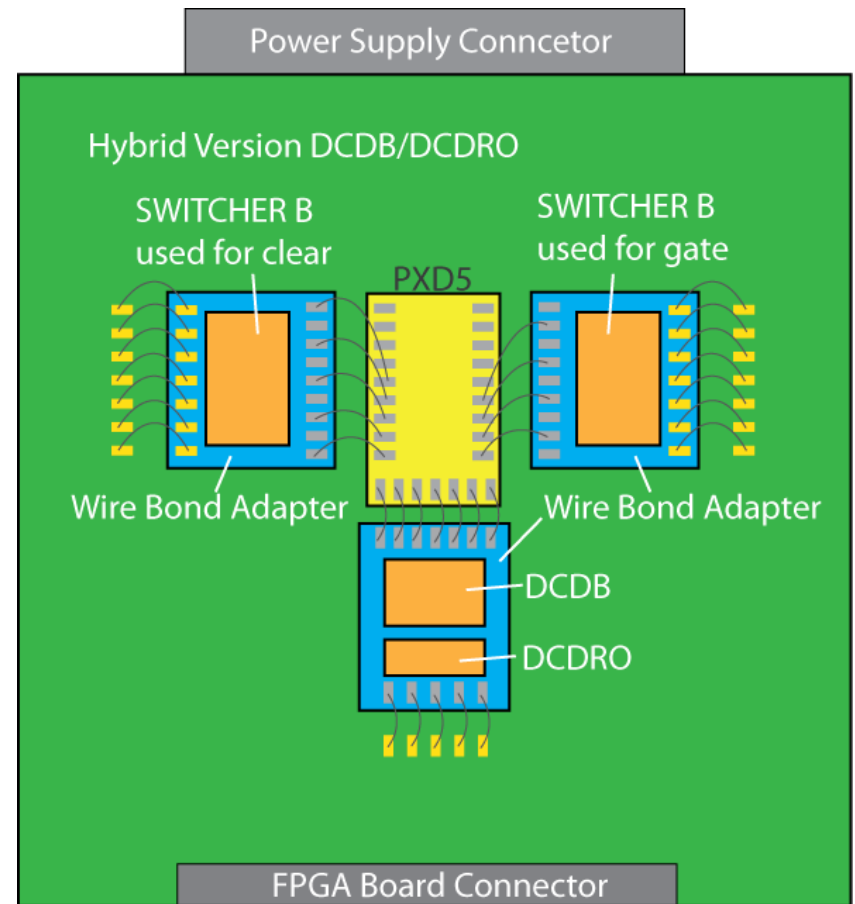- DEPFET Matrix directly bonded to ASICs/wire bond adapters

Power Supply Conncetor

Hybrid Version DCDB/DCDRO

SWITCHER B   SWITCHER B

PXD6

Wire Bond Adapter   Wire Bond Adapter

DCDB

DCDRO

FPGA Board Connector

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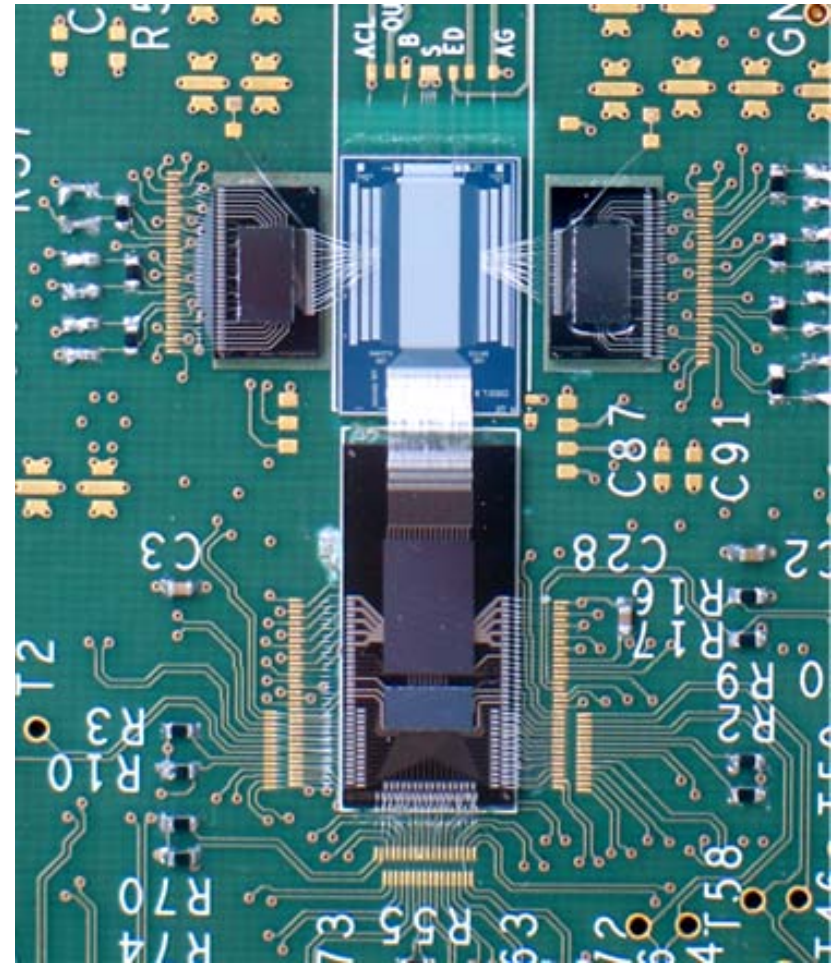- DEPFET Matrix directly bonded to ASICs/wire bond adapters

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# PXD6/PXD5 Hybrid Board H4.1

Issues during the bring-up:

- PCB had to be re-work
  - One via wrongly connects power planes and GND
  - Repair was done at HLL and the PCB manufacture

- Clear Switcher
  - On three hybrid boards the clear switcher is not functional
  - JTAG programming not working
  - Further analysis needed (as mentioned by Ivan)
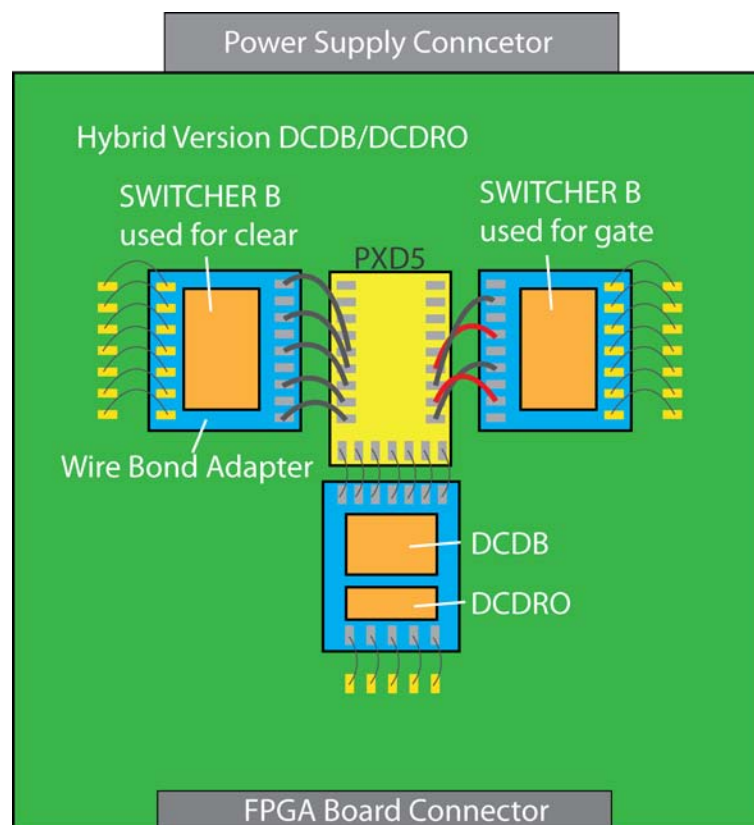
PXD6/PXD5 Hybrid Board H4.1

Issues during the bring-up:

- DCD-B
  - ➤ ADCs characteristic distorted
  - ➤ Link between FPGA and DCDRO broken
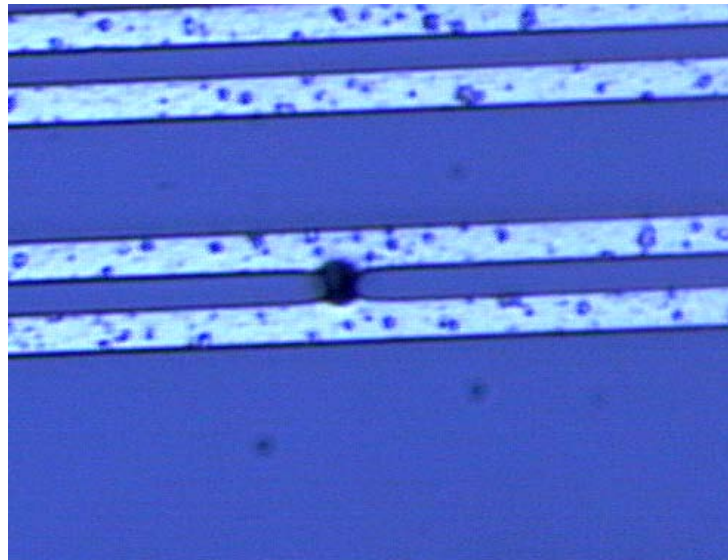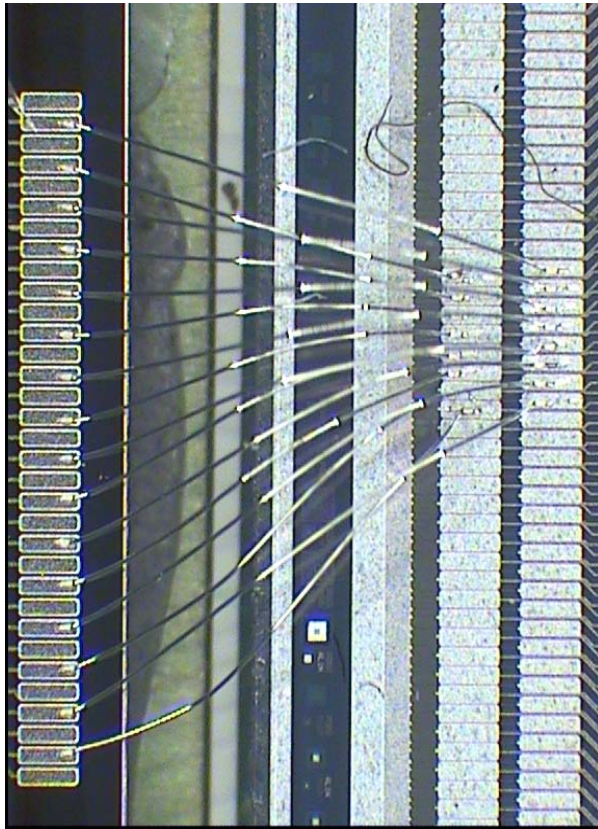
Hybrid Board H4.1.01

Issues during the bring-up Hybrid 4.1.01:
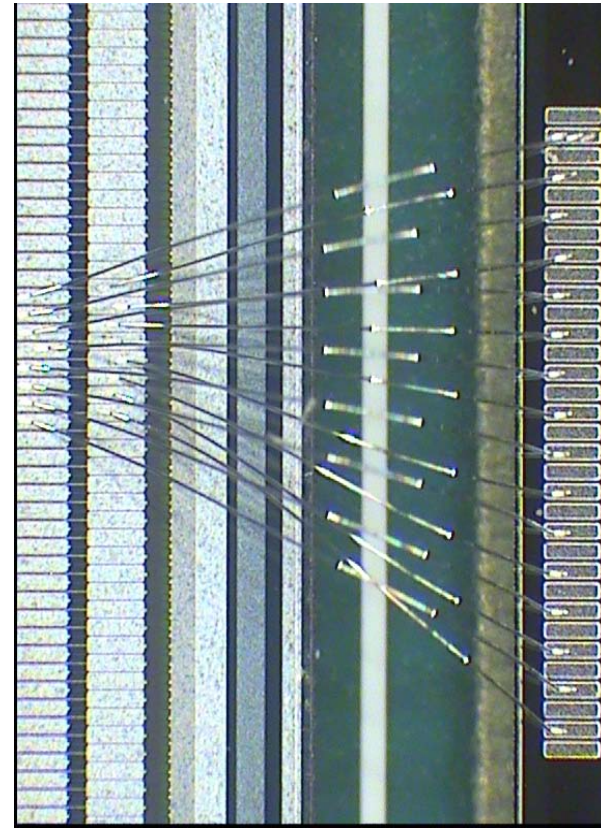
- Bond-wire Connection between Gate and Matrix

Hybrid Board H4.1.01

Clear Switcher   Gate Switcher

Hybrid4.1.01: Read/Clear Sequence

Step	Sequence
0	switch on Switcher Channel gate 0 -> read signals from Matrix double row 1 switch on Switcher Channel clear 0 -> clear Matrix double row 0
1	switch on Switcher Channel gate 1 -> read signals from Matrix double row 0 switch on Switcher Channel clear 1 -> clear Matrix double row 1

→ No matrix channel was operated in its normal mode of operation during the TB2010!

→ Explains effects we see in the TB data:

  ➢ Clear inefficiency

  ➢ Gain difference between odd and even rows
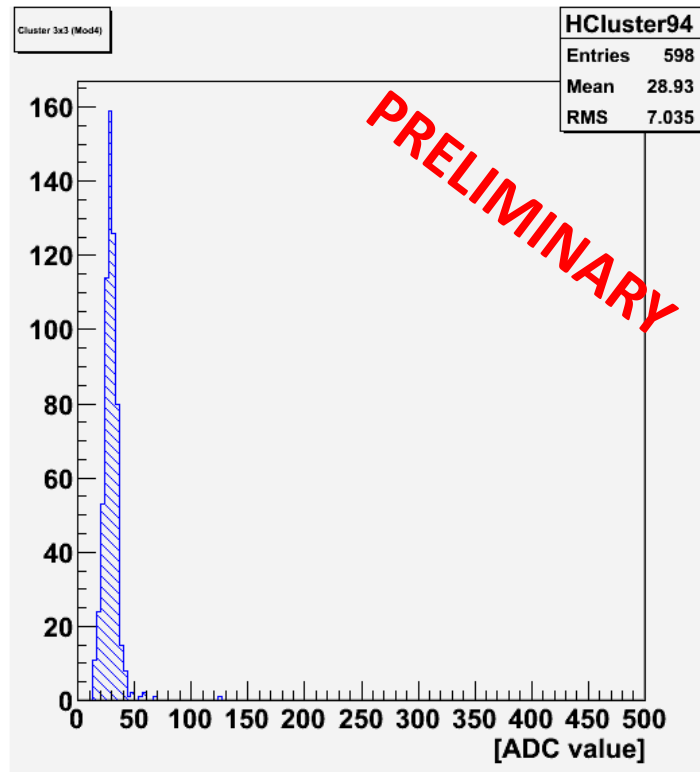

Gates   PXD 5 Double Rows   Clears
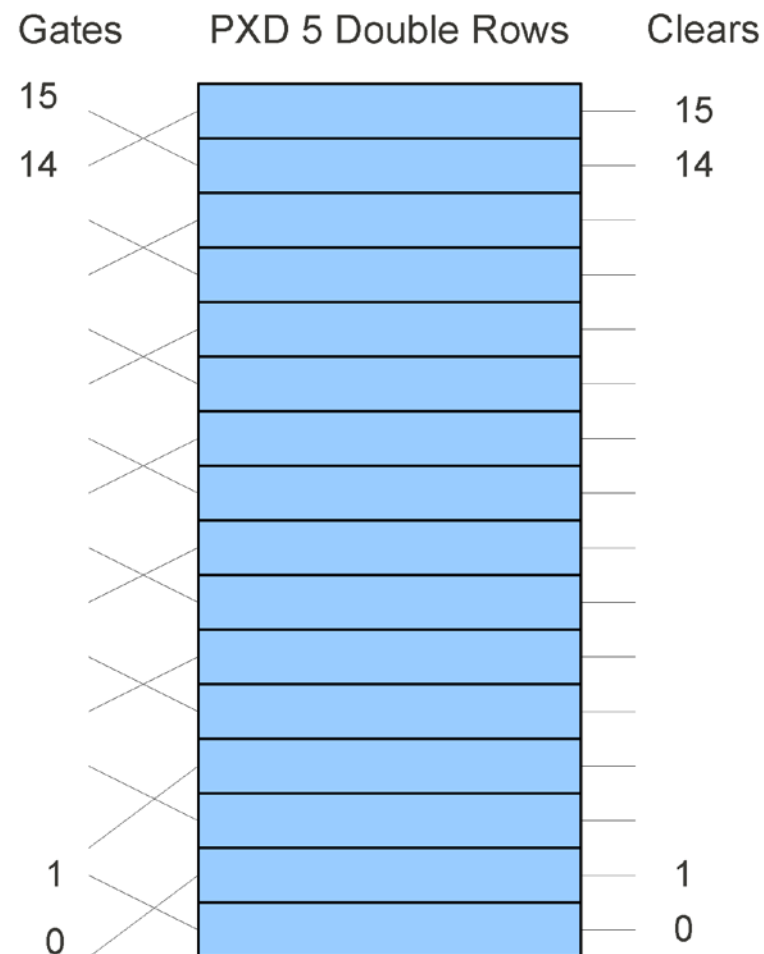
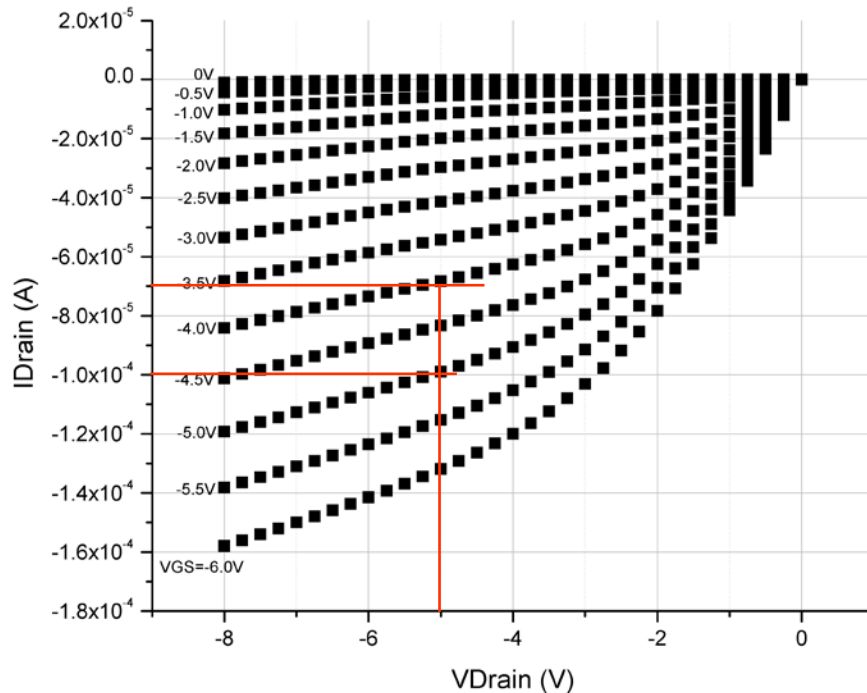# Re-bonding of Hybrid 4.1.01

Gate Switcher re-bonded in CW4:
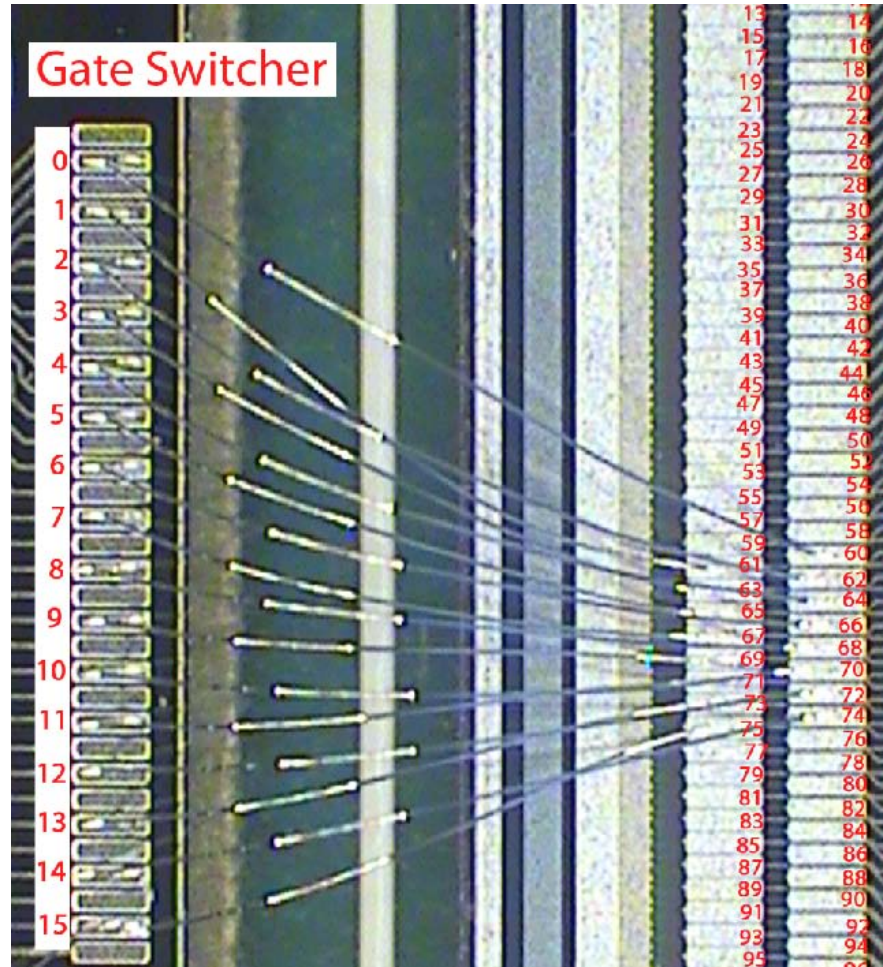
First results after re-bonding Gate Switcher

- Noise and Common Mode are smaller as in the beam test
- A very preliminary number for gq = 280 pA/e-
  → some very new results will be shown by Benjamin tomorrow!
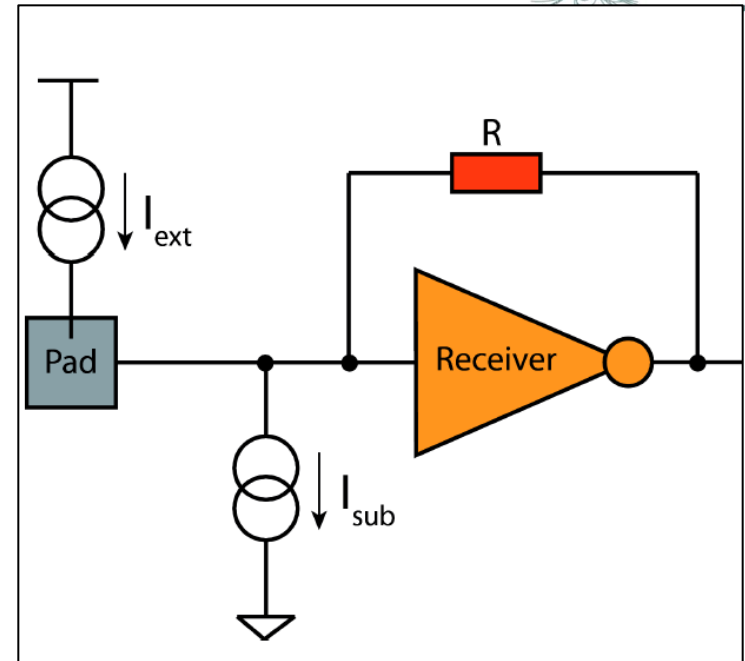

Further source measurements will be done!

PXD5/PXD6 Drain Current

PXD5 - characteristic

Simplified Input of the DCD-B

- PXD5 and PXD6 drain current are expected to be around 100µA (same W/L) without irradiation
- DCD-B internal current source is designed for 70µA and thus limits the DEPFET drain current – TC1 is designed for 140µA
- gq is proportional to Drain current

Hybrid 4.1.x

| Hybrid Number	Components Mounted	Status	Location
H4.1.00	DCDB/DCDRO, SWB x 2	DCDB not working	Mannheim
H4.1.01	DCDB/DCDRO, SWB x 2, PXD5 Matrix COCG LB	DUT Beam Test 2010	HLL
H4.1.02	DCDB/DCDRO, SWB x 2, PXD5 Matrix COCG LB	Clear Switcher did not work right after assembly	Mannheim
H4.1.03	DCDB/DCDRO, SWB x 2, assembled in Bonn	DCDB & SWB, no PXD yet	Bonn
H4.1.04	DCDB/DCDRO, SWB x 2	DCDB & SWB, no PXD yet	HLL
H4.1.05	DCDB/DCDRO, SWB x 2	DCDB & SWB, no PXD yet	HLL
H4.1.06	DCDB/DCDRO, SWB x 2	DCDB/DCRO: Digital Injection Test failed - communication problem between FPAG and DCDB	HLL

Preparations for PXD6

- Mechanical dummies are ready since CW5

- Assembly tests have been started:

  - set parameters for bonding
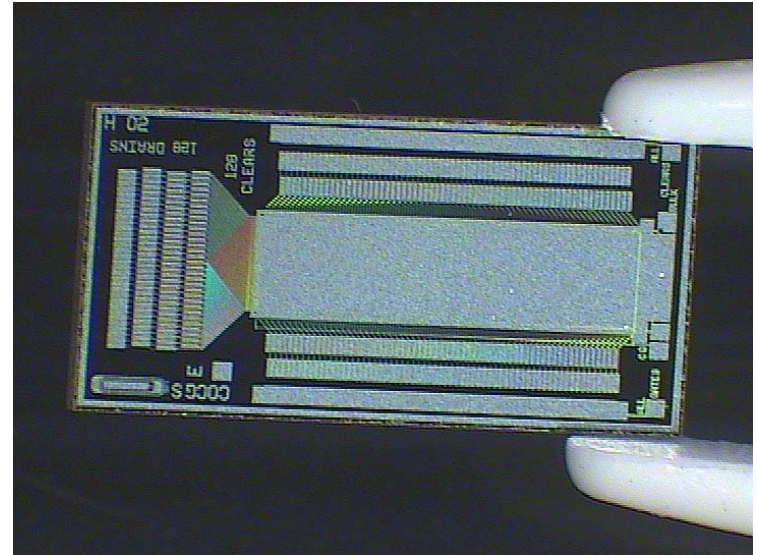
Mini Matrix Preparations for PXD6
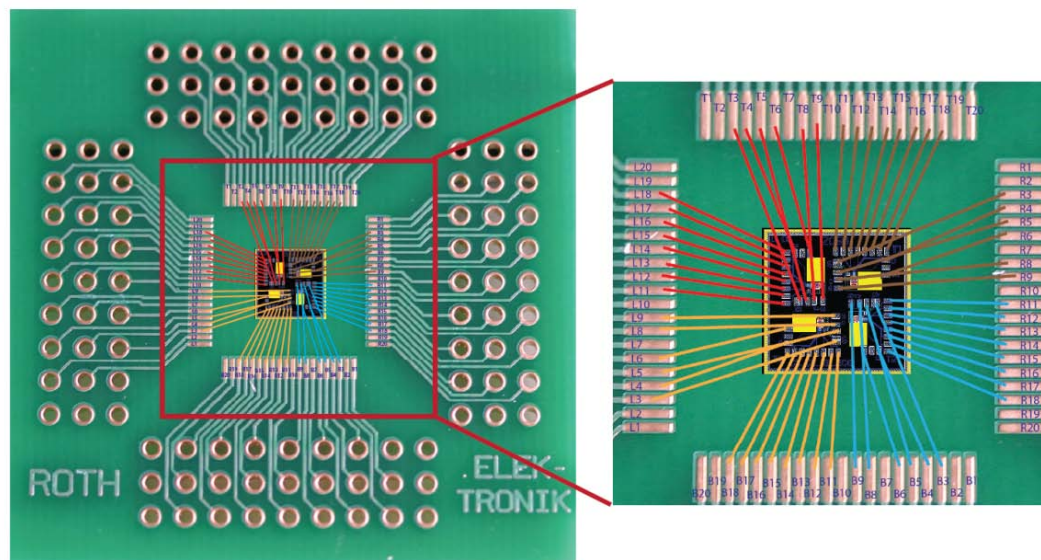
- PCBs for PXD6 Mini-Matrices are available
- Dummy Matrices are also available
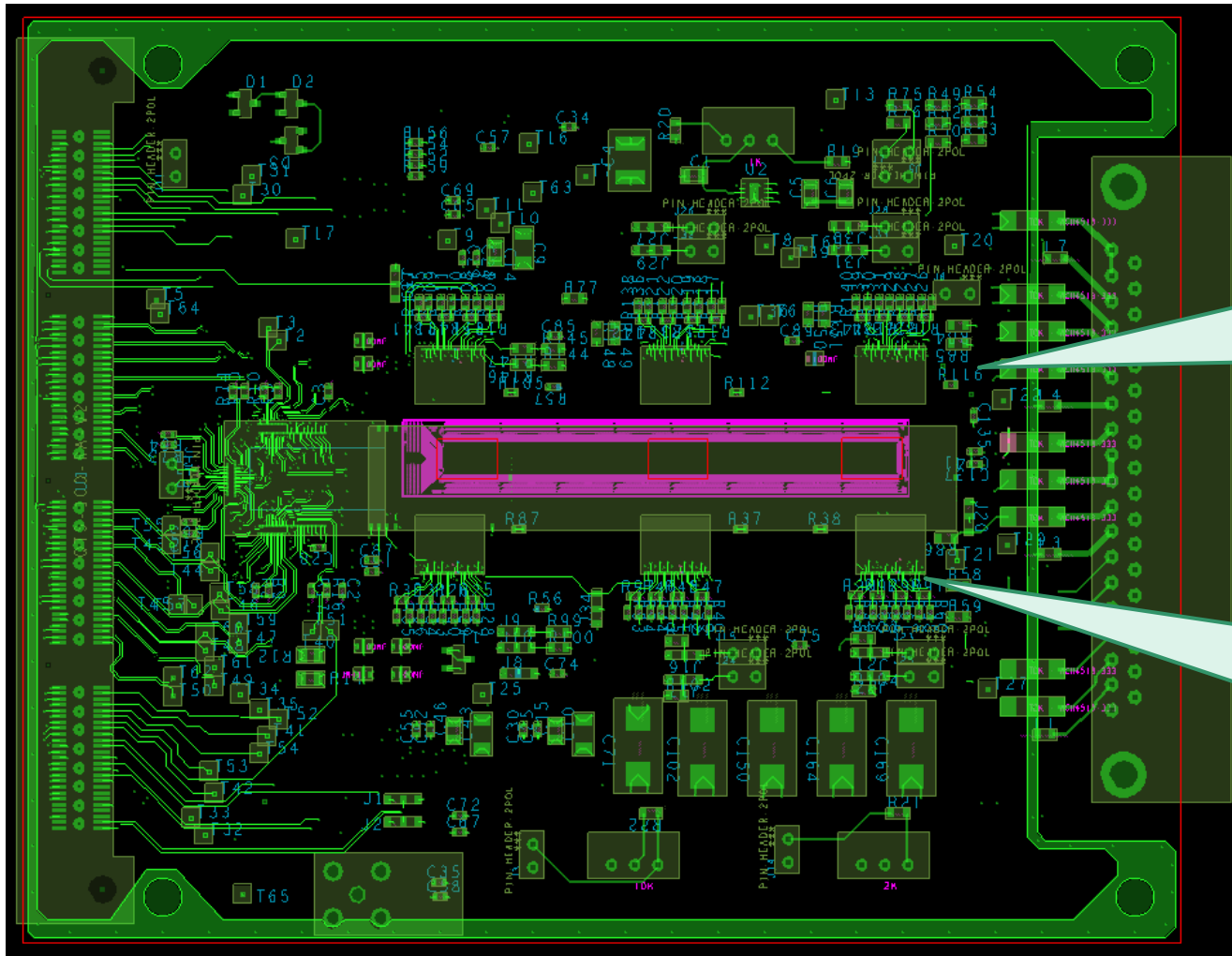- Assembly tests will be started soon

Summary

- Hybrid 4.1.x
  - Lot's of things learned
  - First read-out of PXD5 Matrix with DCDB and SwitcherB as steering chips
  - Assembly and test of further hybrid boards is ongoing (in Bonn, Mannheim and Munich)

- Preparation for PXD6 is started using dummy matrices

Thank you!

Hybrid 4.2.x

SwitcherB Wirebond Adapter for Clear

SwitcherB Wirebond Adapter for Gate