PXD6 Production Status and other issues

PXD6 Production Status

Early Backside Breakdown on SOI wafer

Operation safety

PXD6 production status - Batch 1

Short reminder:

Split of PXD6 in 2 parts

Status Valencia-Meeting:

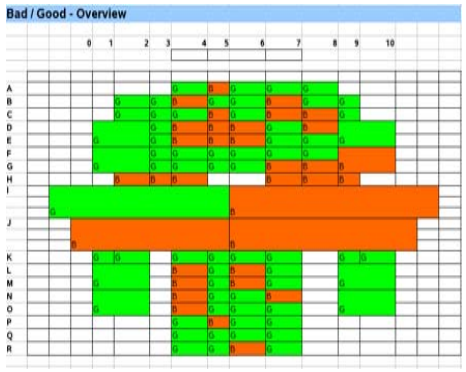
PXD6 – I: front side production finished -

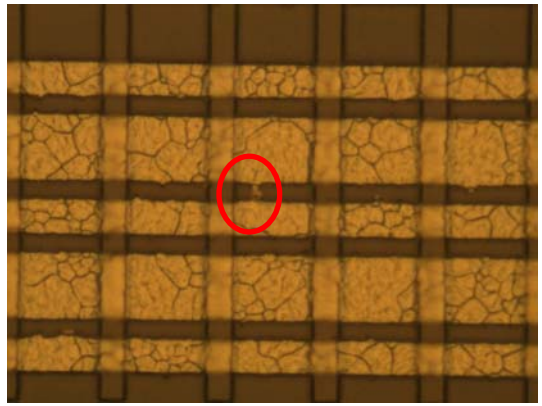
yield problems in the first Aluminum layer – identified but not reparable

- batch continued
- backside processing finished
- 4 wafer (3SOI, 1 Standard)

ready for cutting

first static measurements -> Jelena





PXD6 production status – batch 2

Batch 2 (6 wafer) was stopped before aluminization

reserved as safety option and accomodate the DHP (not ready)

forced to be continue early

- correction of some minor design bugs,
- testability features improved to spot technology problems already after metal 1

further split necessary

2 wafers are stopped before metal1/metal 2 contact

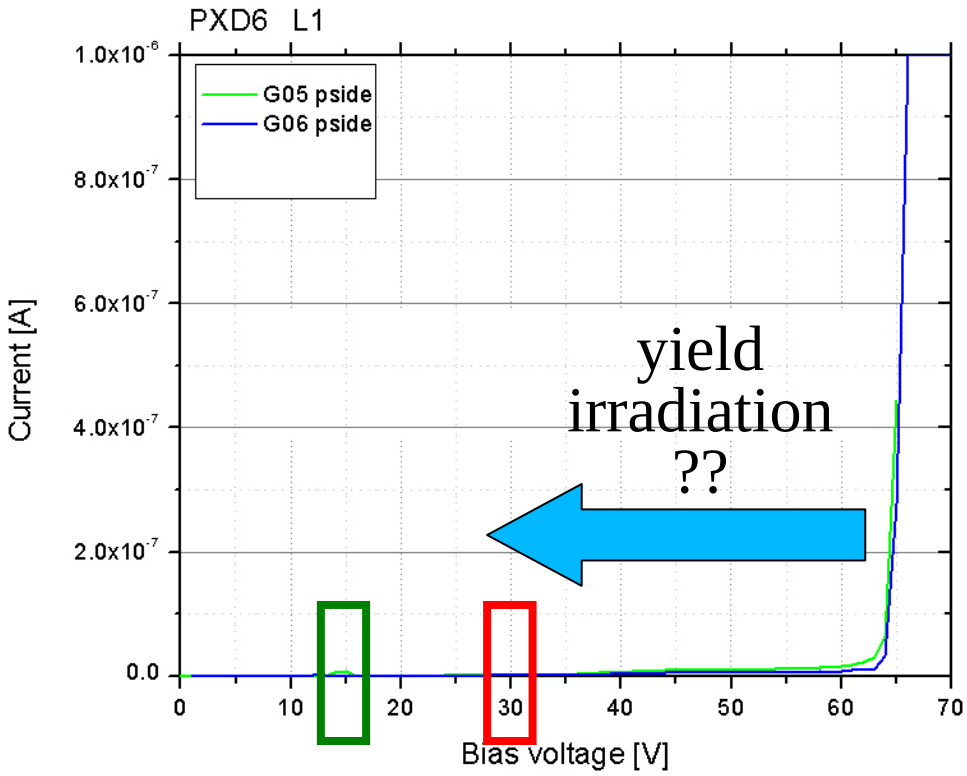
waiting for DHP foot print and UBM (copper)

current status

pause if two weeks due to sputter problem

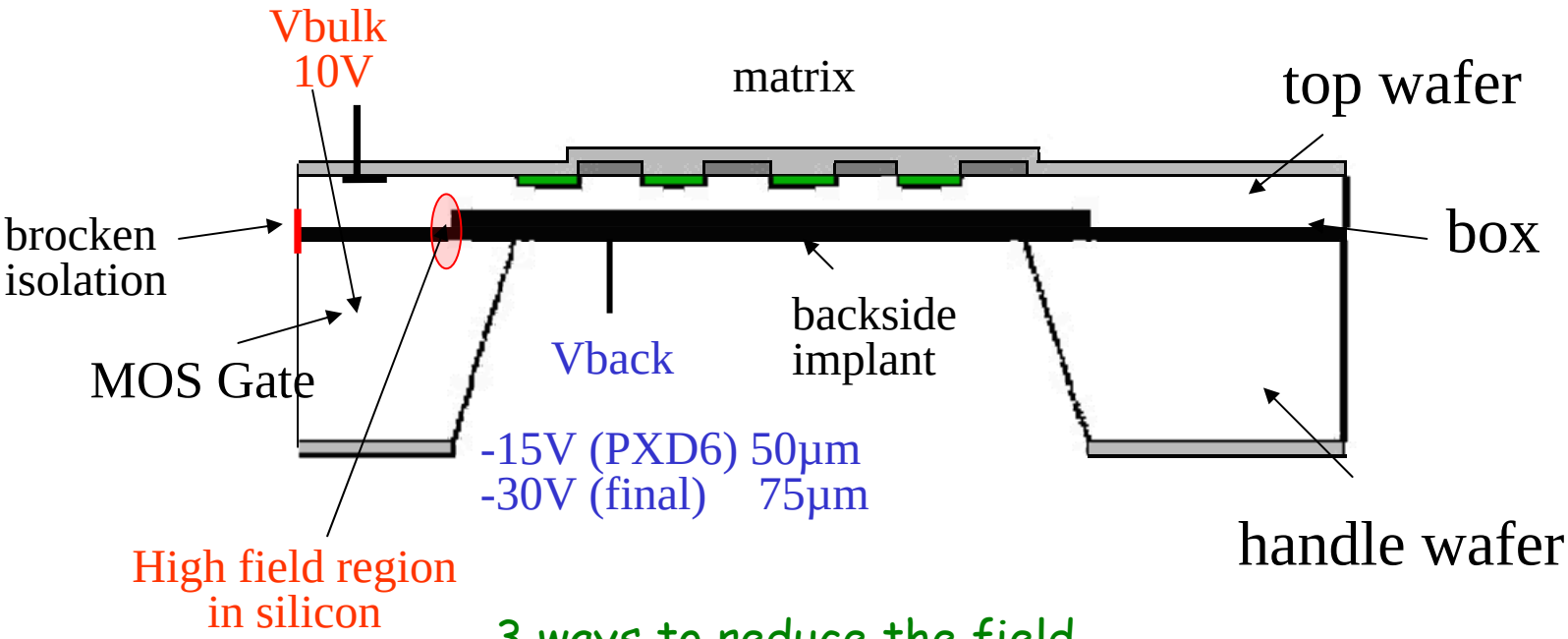
Batch 2 continues this week, ready for backside etching by end of Feb.

SOI Backside diodes I



more curves in Jelena‘s talk

SOI Backside diodes II



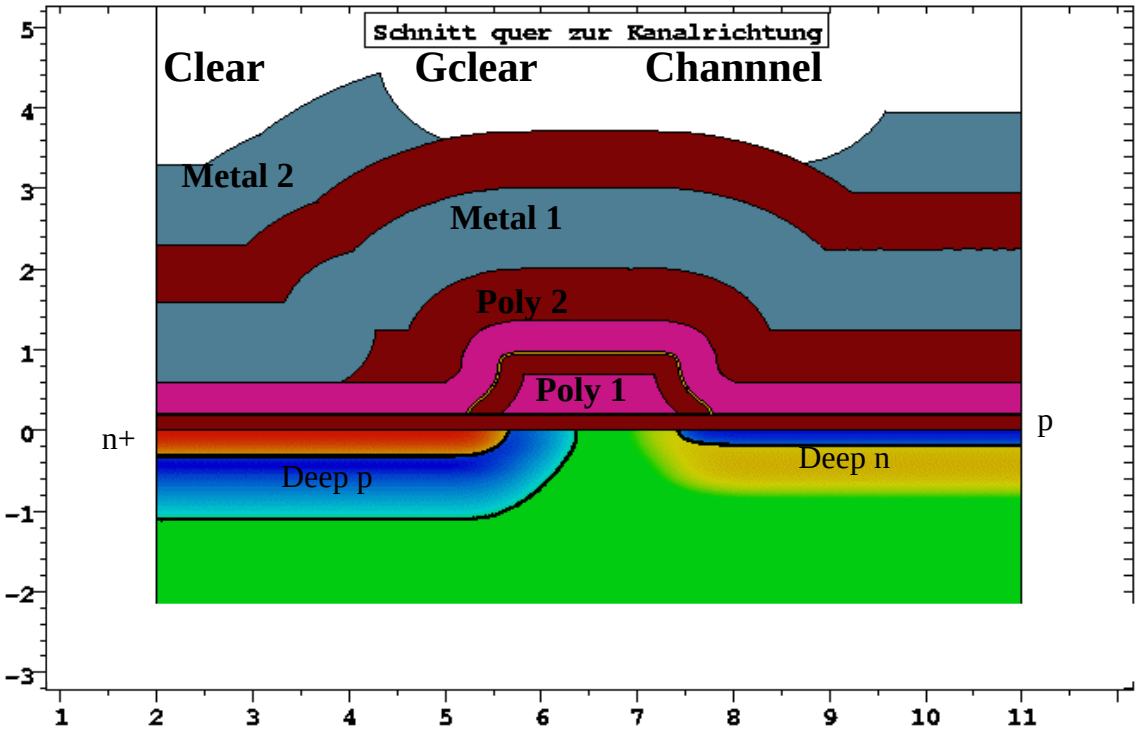
3 ways to reduce the field

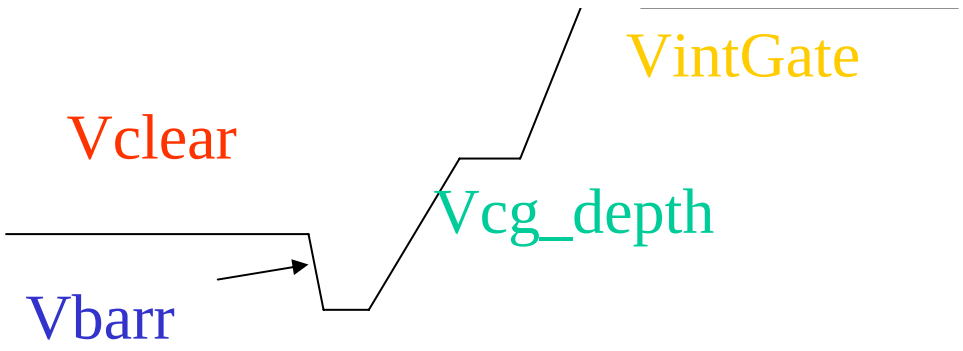
A) Thicker box oxide to reduce the penetration of the handle wafer 'gate'

B) Special multi guard rings

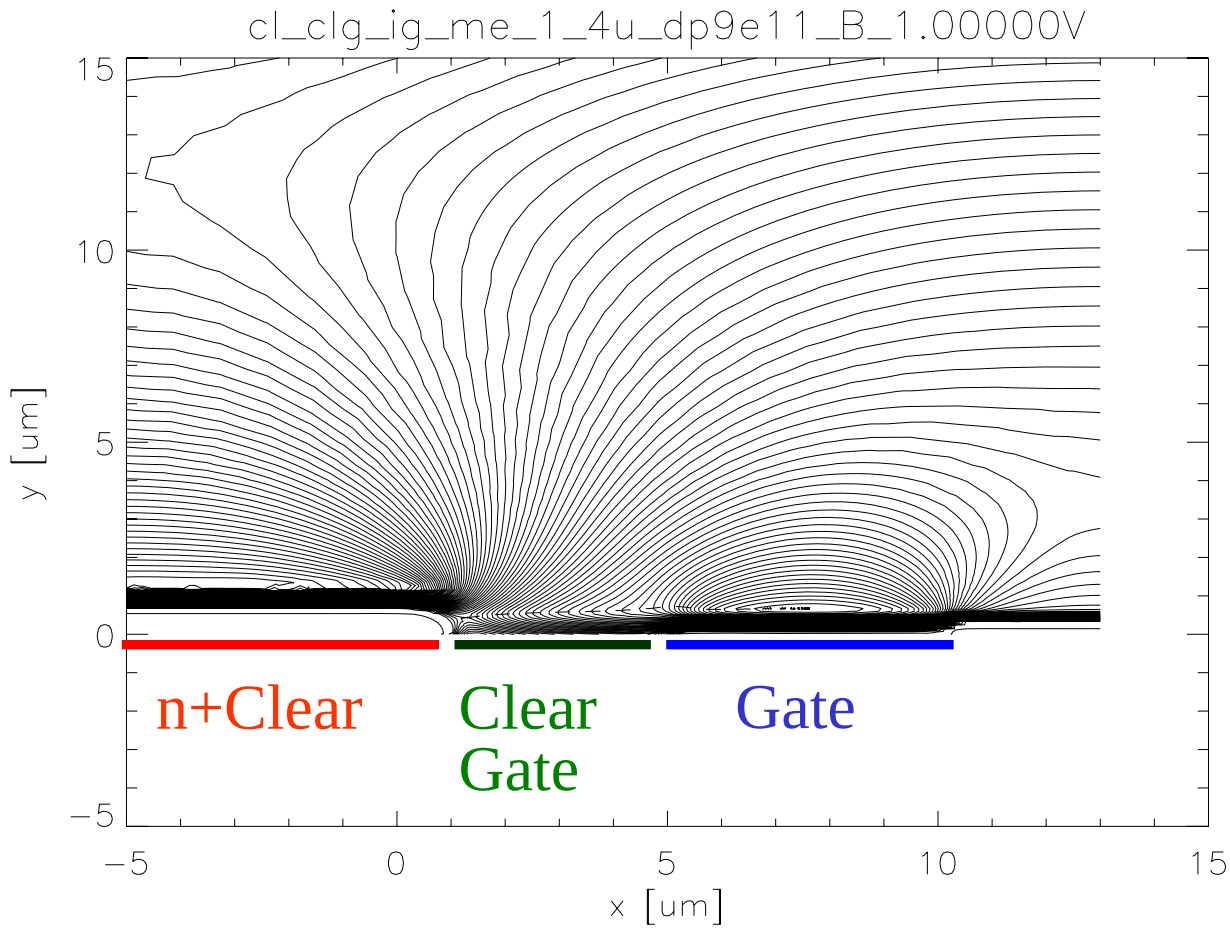
C) Isolation of the chip edge from the bulk potential

Read/Collection

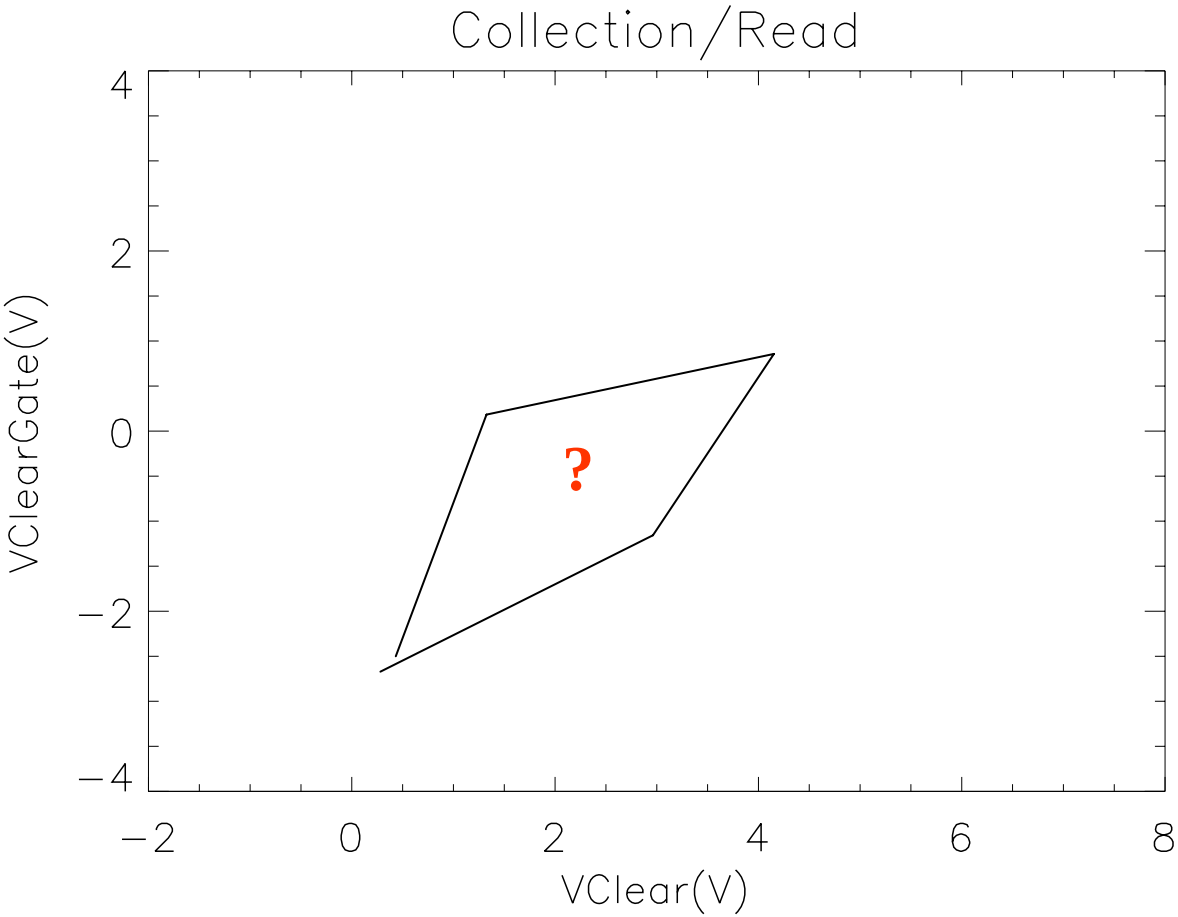




Potential distribution during charge collection

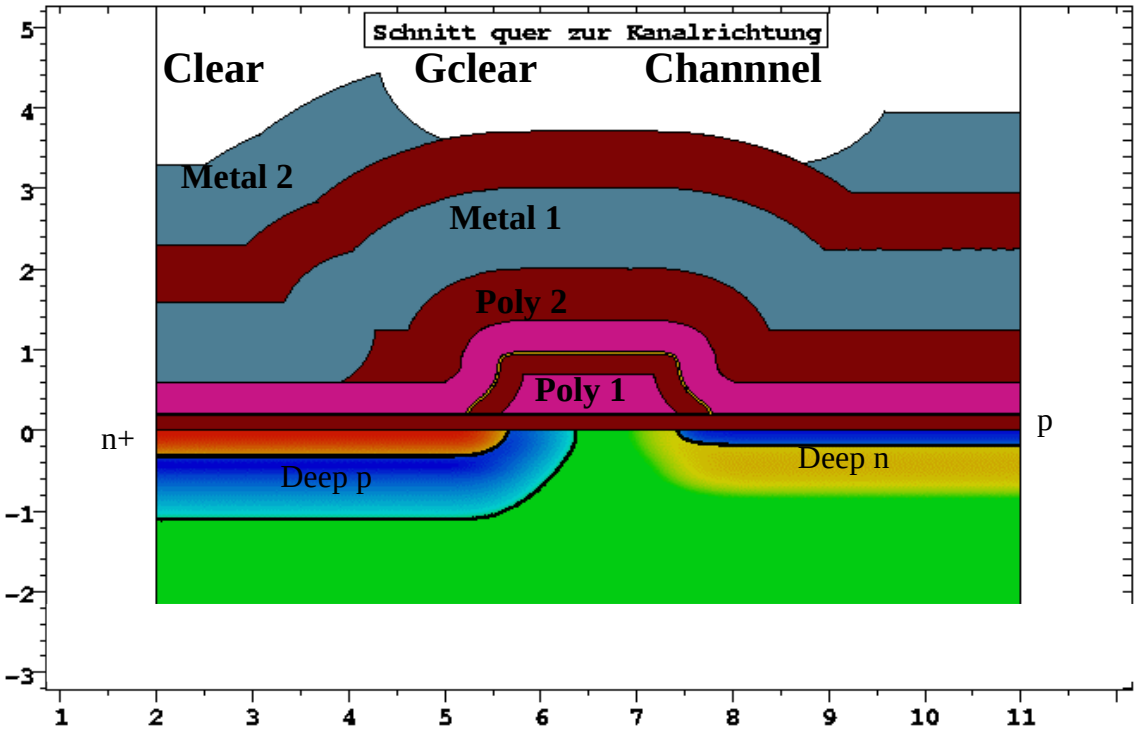


Which Clear and ClearGate voltages ensure a safe operation?



The larger the window the safer the operation !
What are the limiting mechanismens ?

Back Emission of electrons from the Clear into the Internal Gate



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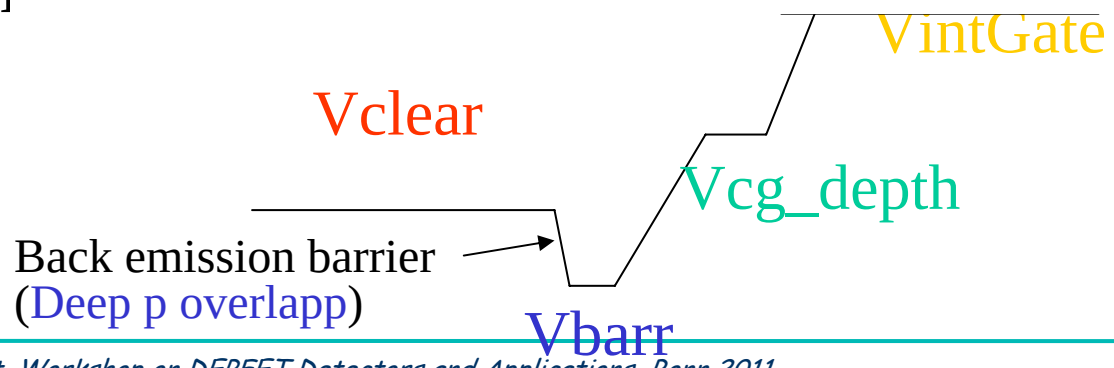

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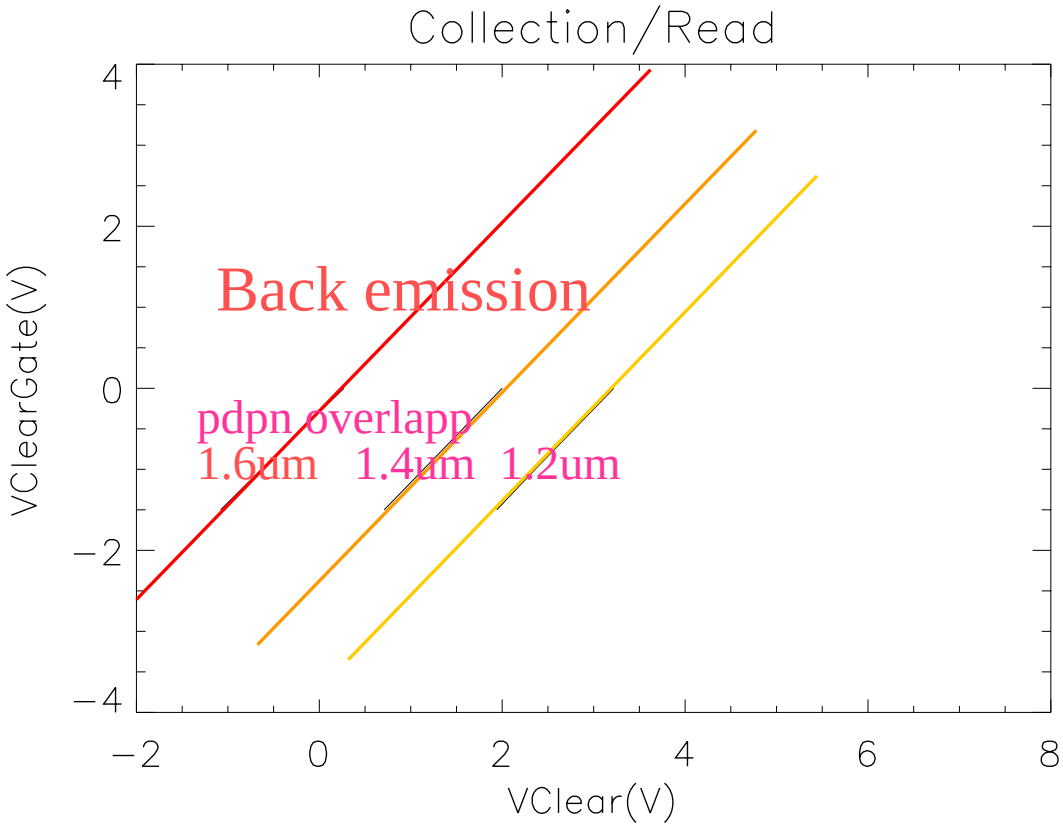
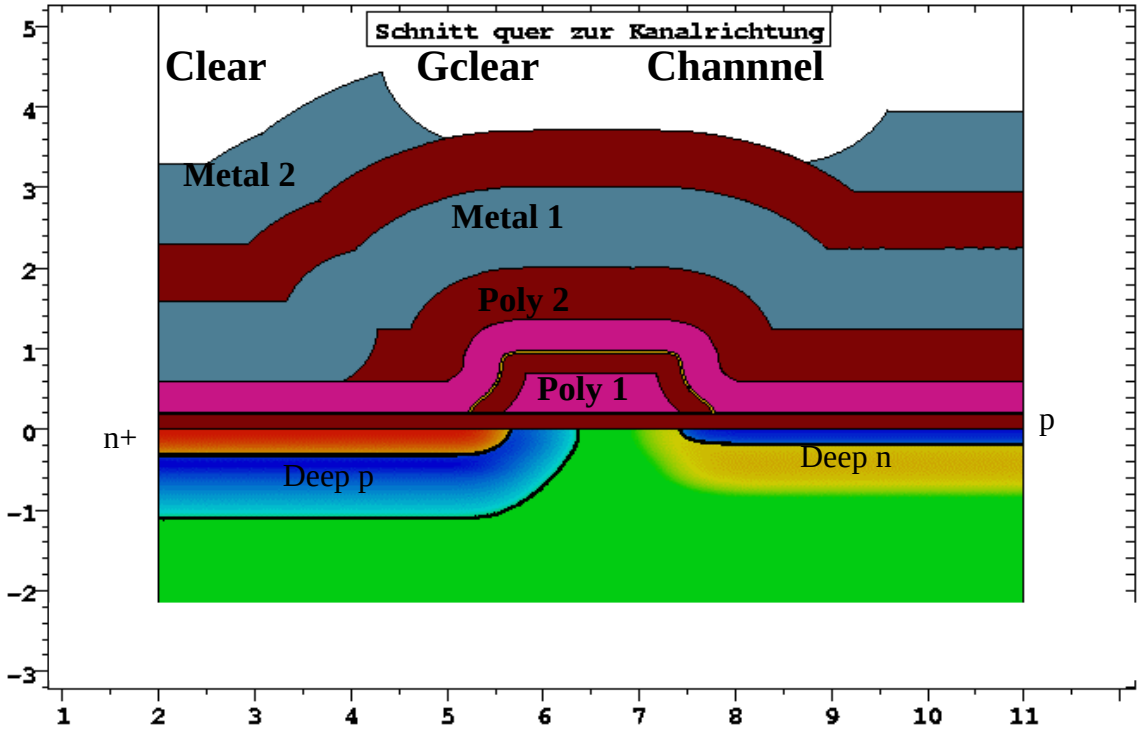


Hole Inversion beneath ClearGate



Parasitic hole channel along ClearGate
-> shorts Source and Drain (linear designs)
-> shorts Source – Deep p – Backside (all designs)

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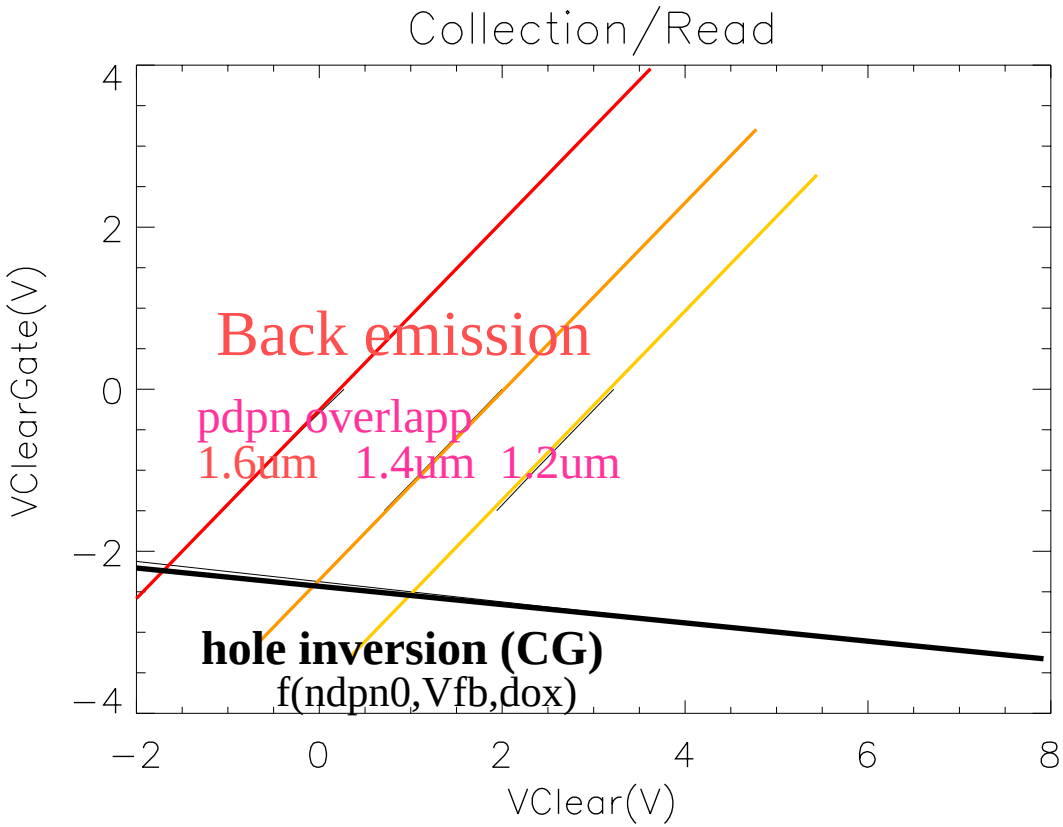
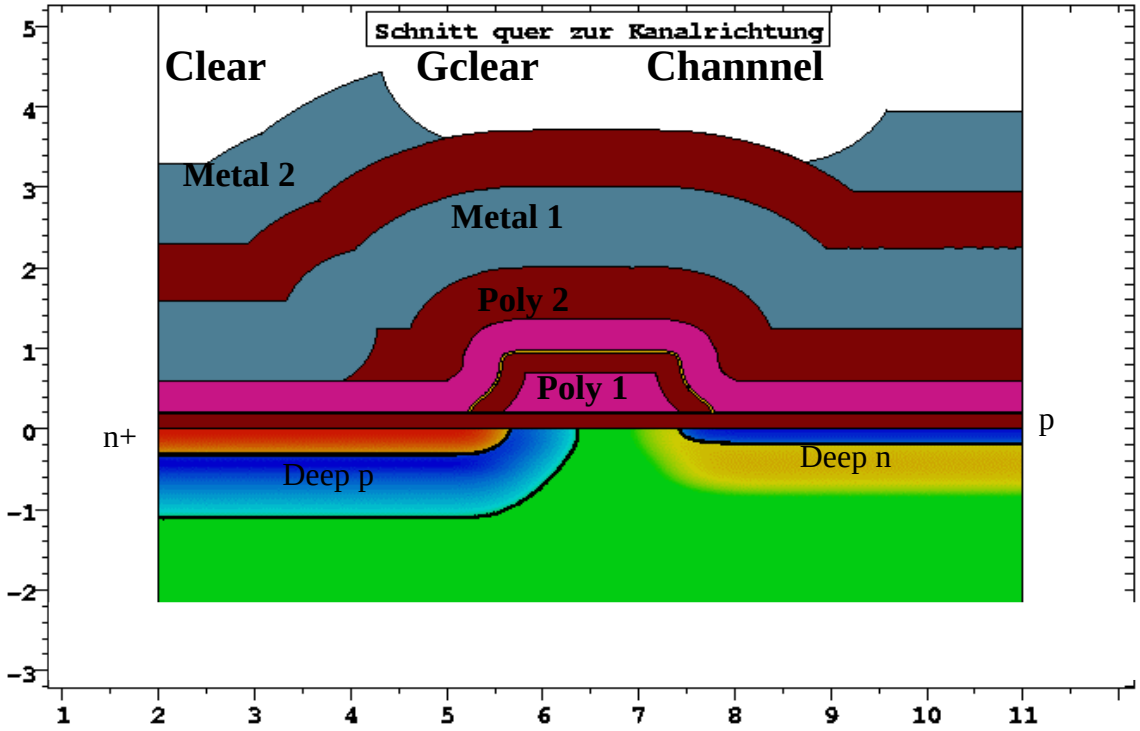
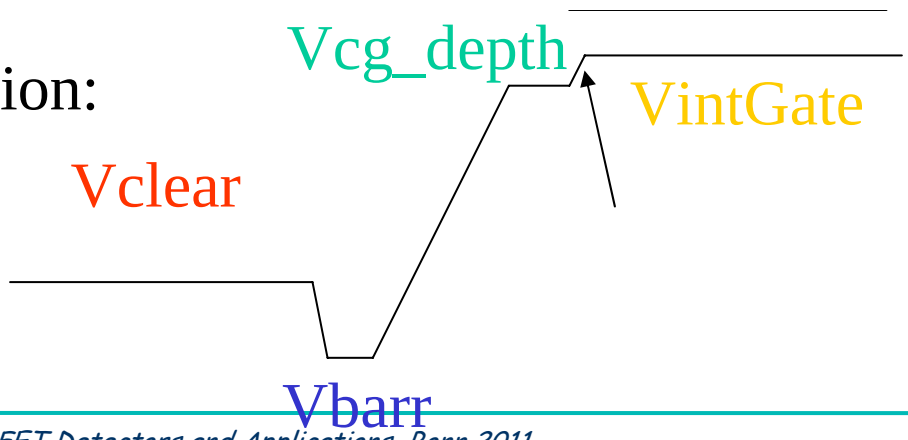


Charge Loss from Internal Gate to ClearGate region



Read/Collection:



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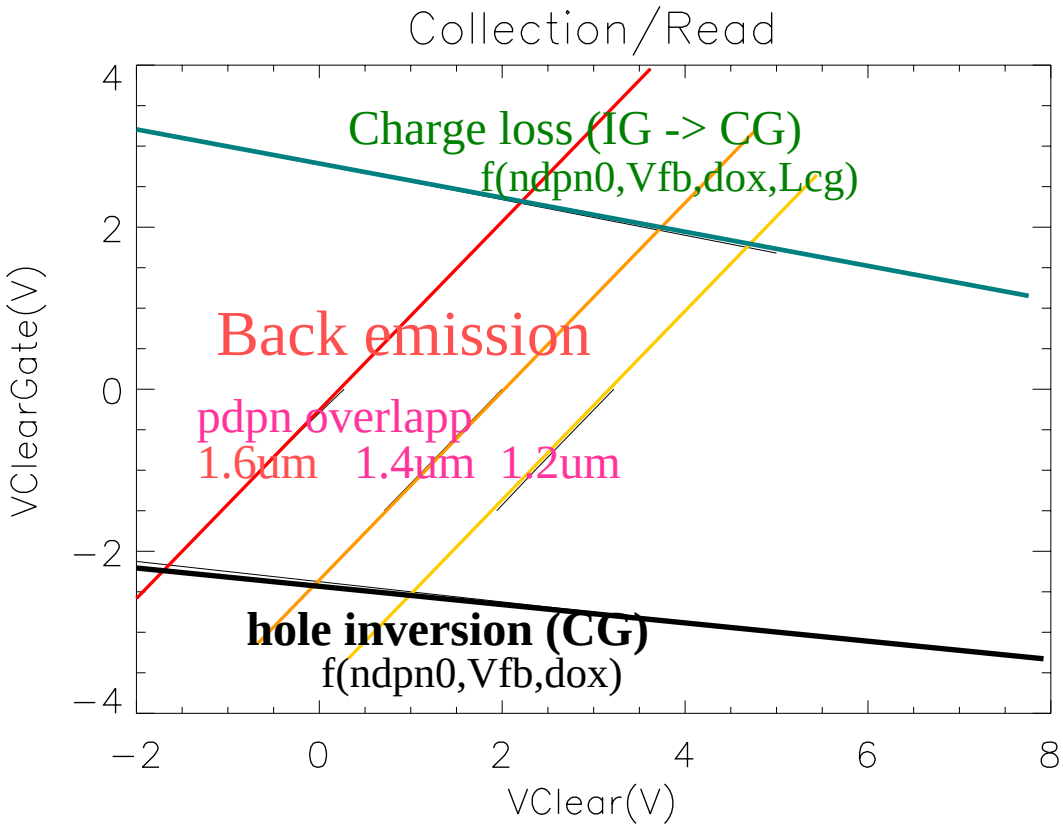
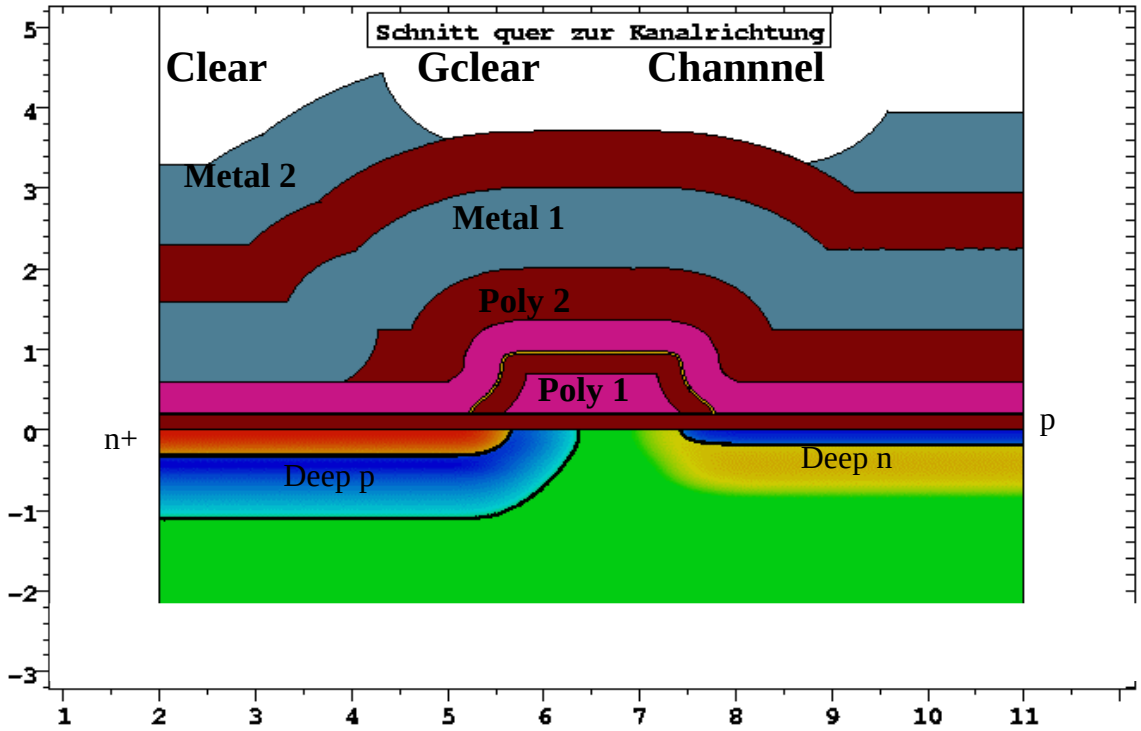


Charge Loss during Charge Collection into Clear

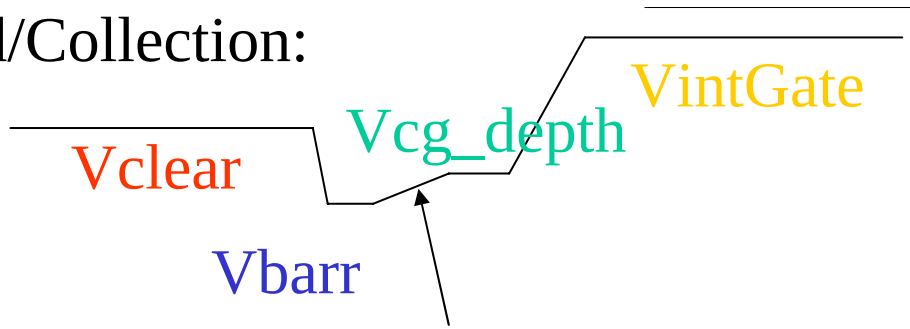


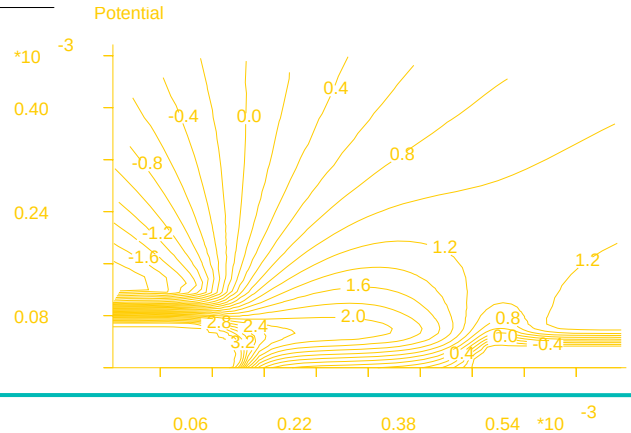
Difficult to describe generally

C-CG-S section more critical than C-CG-IG section

C-CG-S section

Read/Collection:





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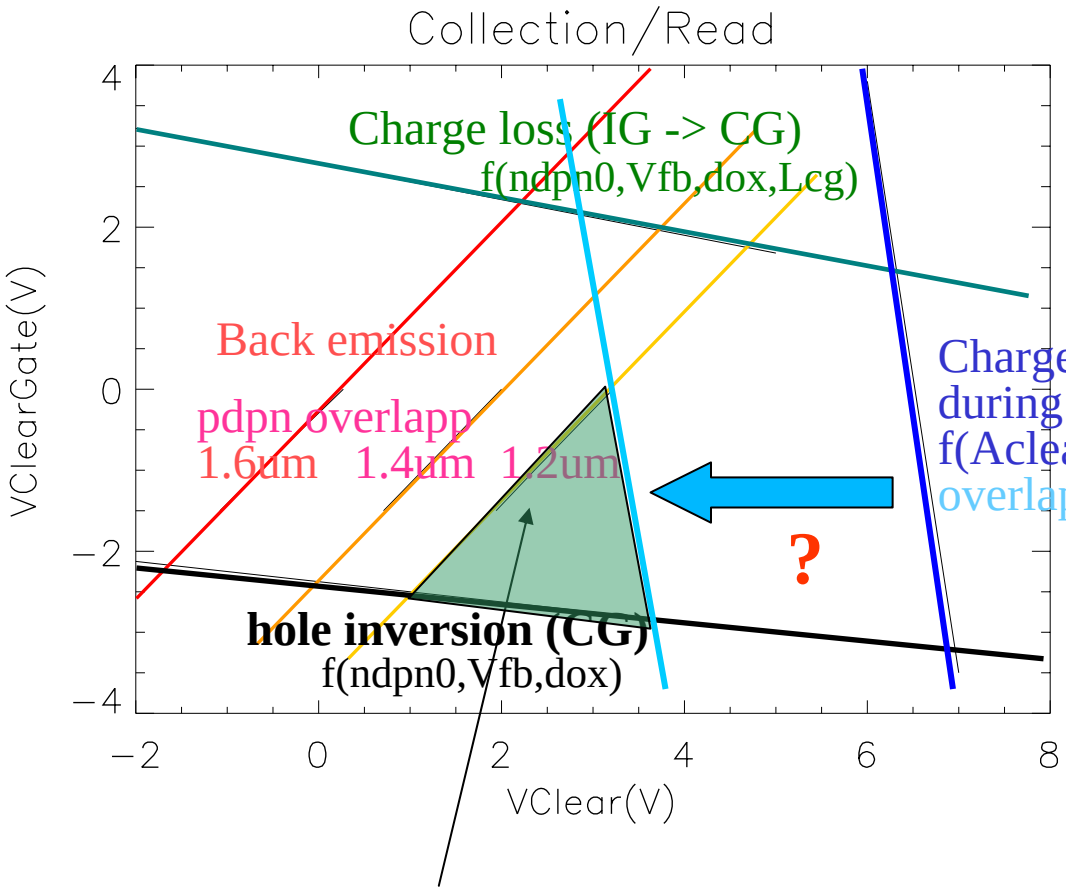
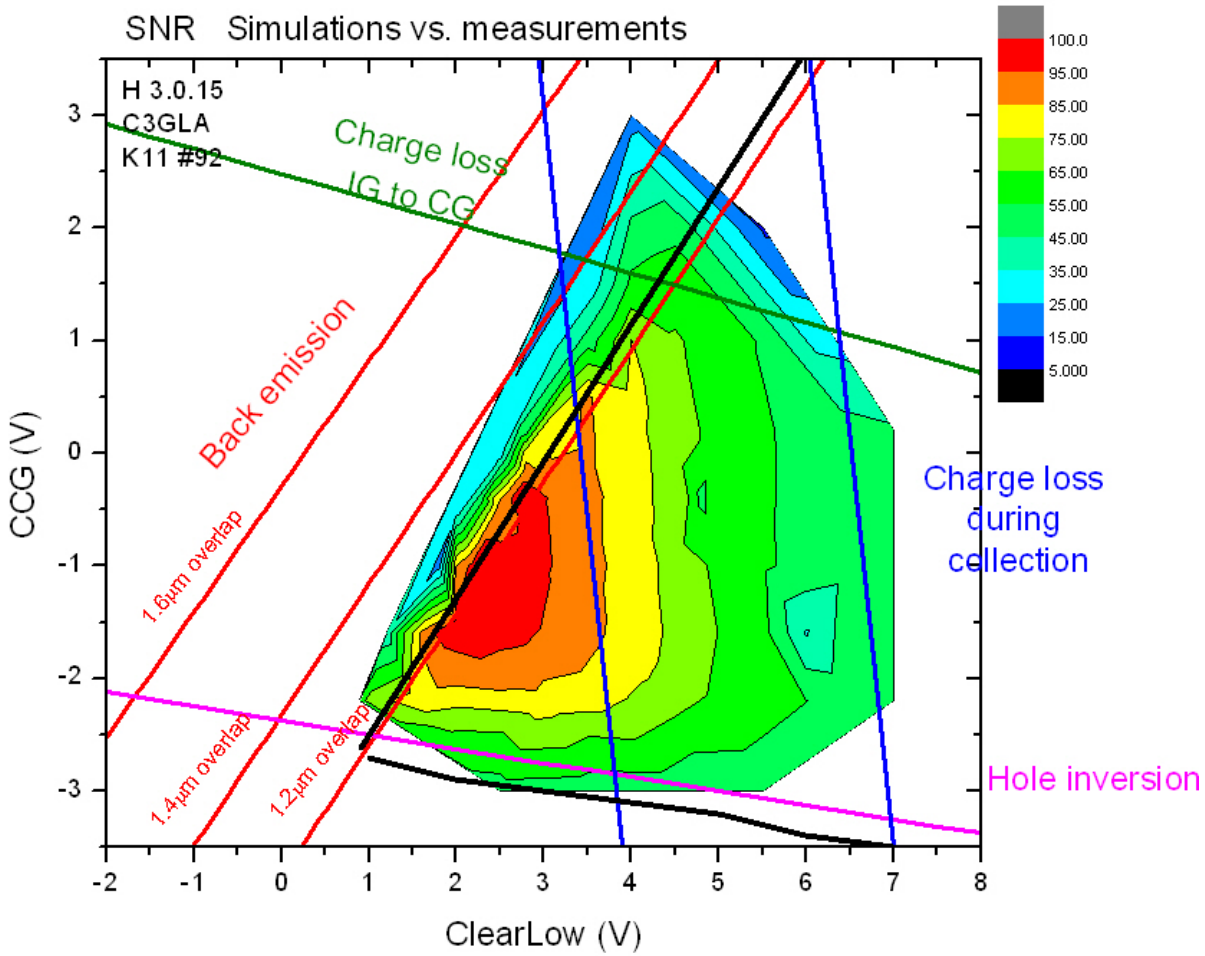


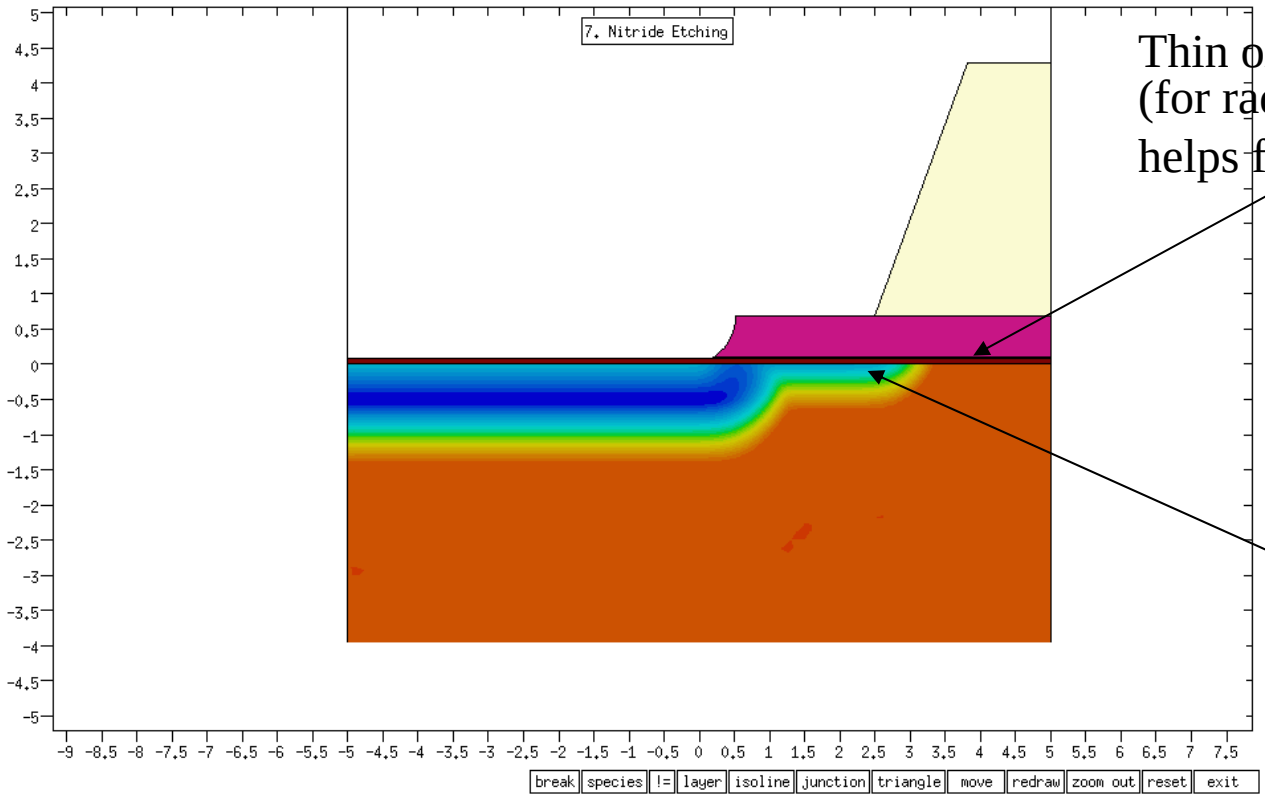
Operation triangles

Comparison with measurements



Deep p - shield implantation

Masked by Poly1
Reduction of Boron impl. energy from 650keV to 200keV

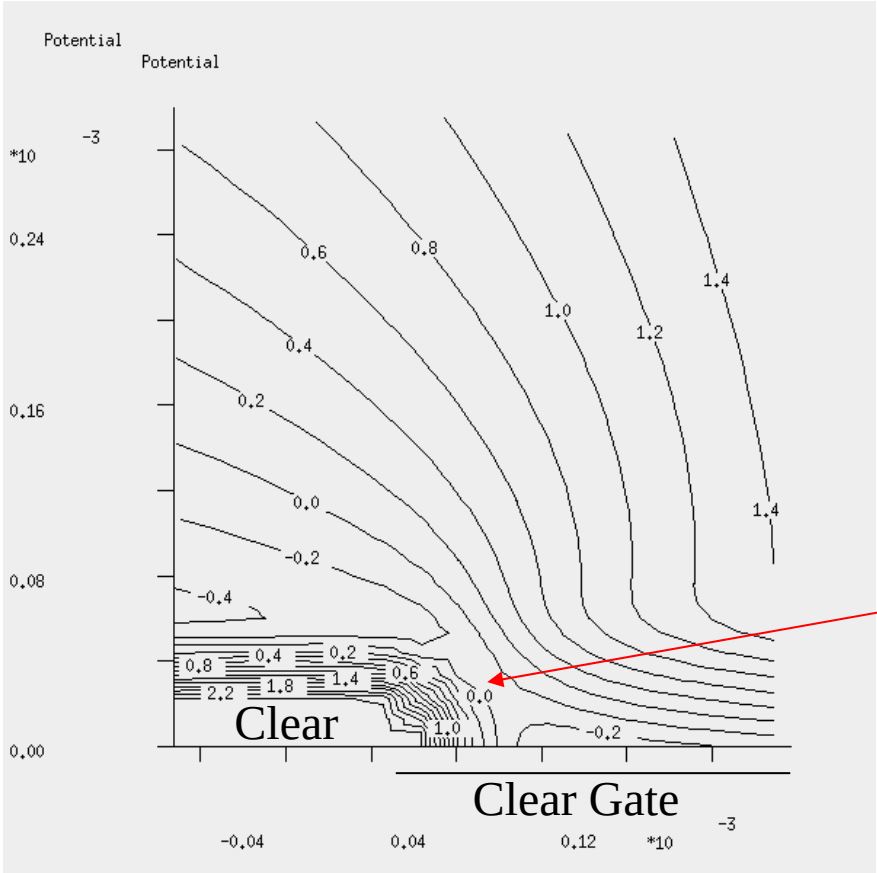


Thin oxide
(for radiation hardness)
helps for As implantation

neglible dose

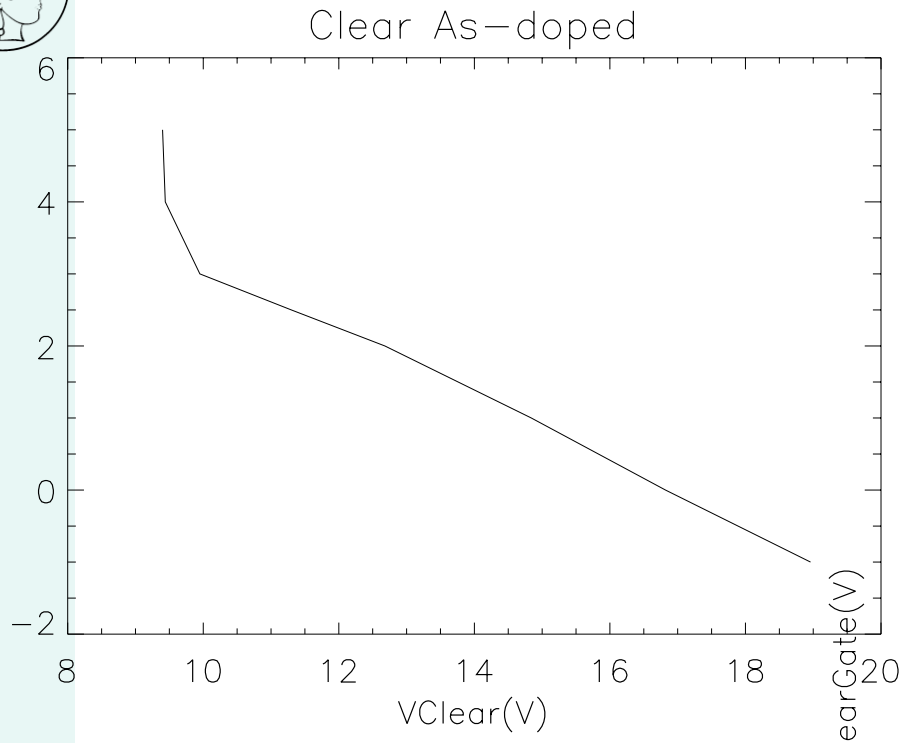
Barrier during READ

Vclear = 2V, VclearGate=-1V



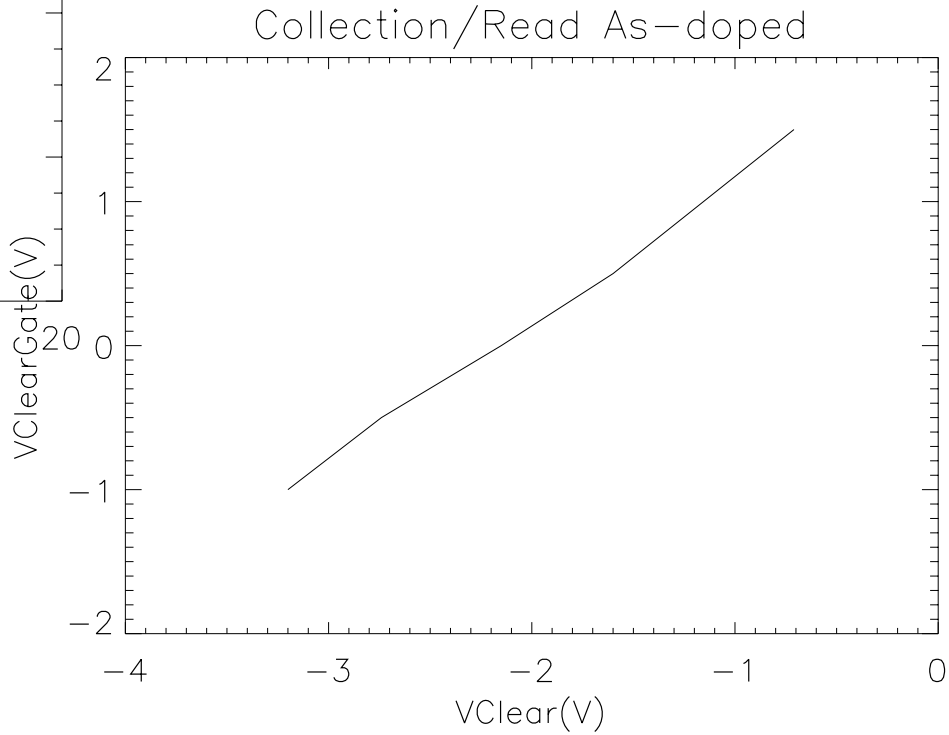
Vbarr > 2V
☺

Very first Simulations (prelimenary)



Clear conditions:
for 1 remaining electron

Collection conditions:
1 back emitted electron
within 0.5µs



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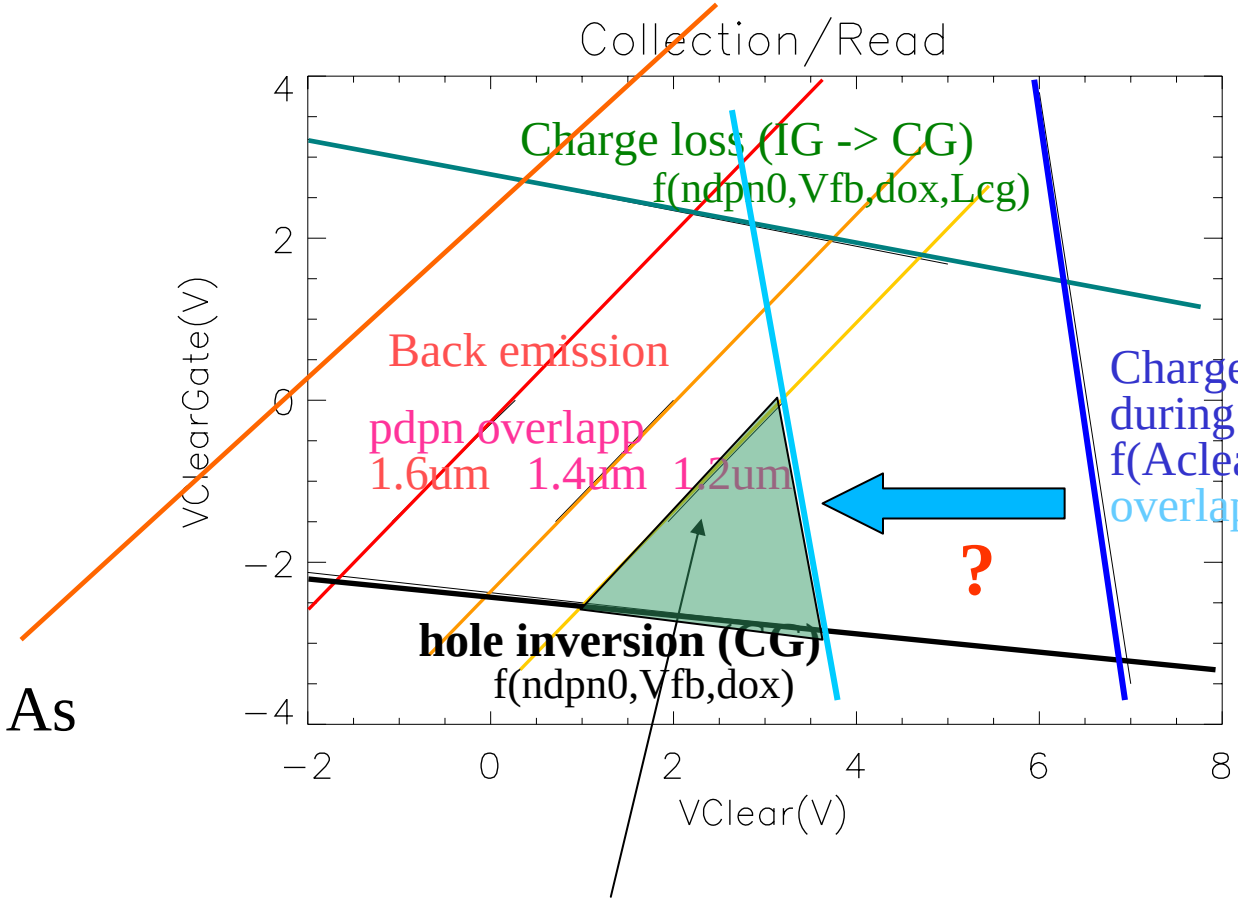
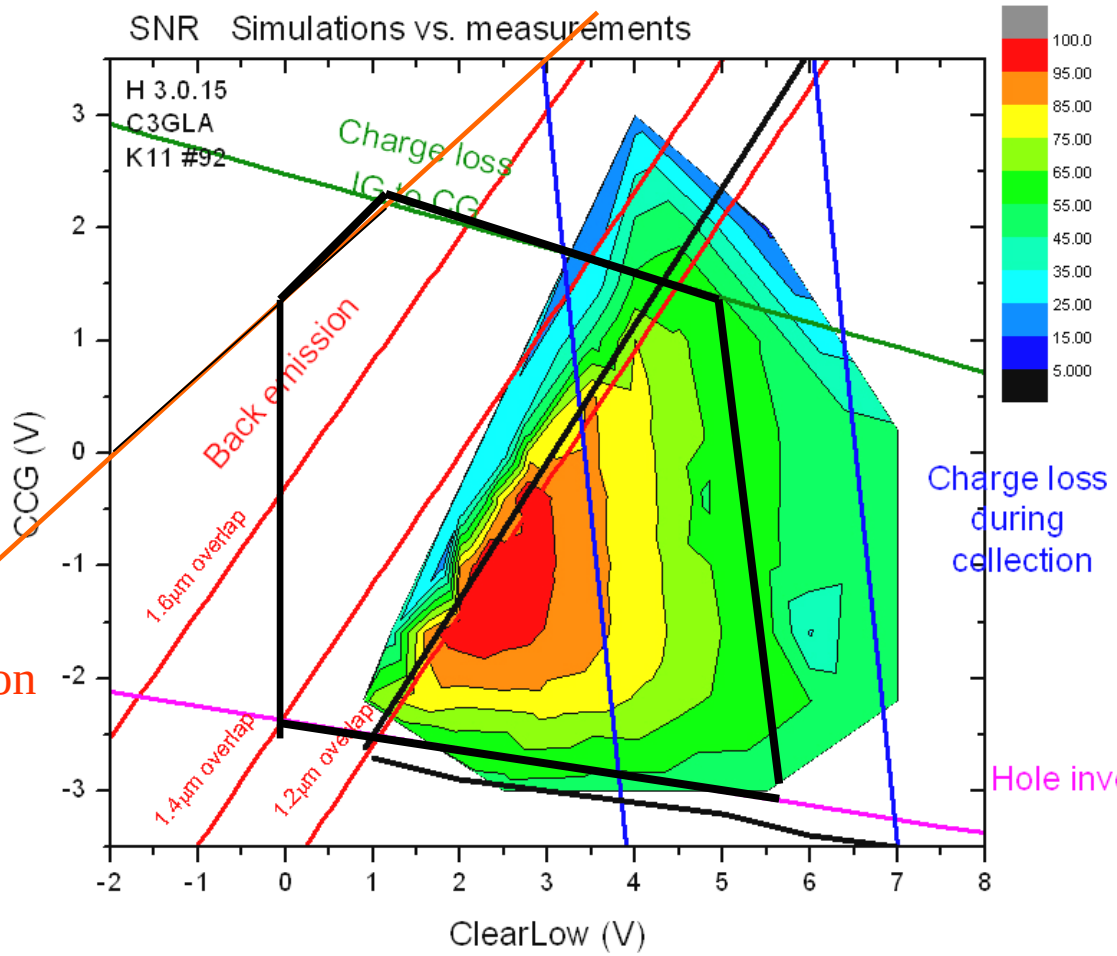


As

Operation triangle

Comparison with measurements



Back emission self aligned technology

Charge loss during collection

Hole inversion

Summary

We will have cut (small) matrices from PXD6 Batch I by end of February.

More matrices (also big ones) about 6 weeks later.

2 wafer are reserved for the DHP and copper UBM.

Our SOI concept leads to reduced breakdown voltages of back diodes
-> improvement necessary

Arsenic doped clear regions allow a fully self aligned technology for all implanations and a safer detector operation