Lab 13: A parametrised N-bit adder

Goal of this lab exercise is to design an N-bit adder, similar to the one designed in lab 6, using VHDL `generics` and `generate` features.

The design ports are

Port	Direction	Width	Type
A	IN	N	std_logic_vector
B	IN	N	std_logic_vector
SUM	OUT	N + 1	std_logic_vector

A testbench is provided to test the design.

Exercise

1. Design the N-bit adder

Go to `~/labs/labs15/` and open `src/nbitadder.vhd` with a text editor.

```
kate src/nbitadder.vhd &
```

- Implement the N-bit adder module with a generic parameter `N`, that defines the width of the input/output vectors
- Use the `for generate` statement within the architecture to instantiate N full adders.
- Connect the carry-out signal of each full-adder to the carry-in of the next in the `for generate`
- Connect the carry-out signal of the last full-adder to the MSB of the output `S`

A symlink to the fulladder module you designed in Lab5 is available in `src/fulladder.vhd`

2. Run the simulation

Run the provided simulation, to test your module.

```
./run_sim.sh
```