Lab 5: Combinatorial Logic - Design a Full Adder

In this lab, we will design a simple Full Adder block, to test our knowledge of concurrent signal assignments, and simple VHDL operators.

A. Design A Full Adder

The port interface of the adder are:

Port	Direction	Type
A	IN	std_logic
B	IN	std_logic
Ci	IN	std_logic
S	OUT	std_logic
Co	OUT	std_logic

The functionalities of the full adder are summarised in the following table

	Function
S	A XOR B XOR Ci
Co	(A AND B) or (A AND Ci) or (B AND Ci)

Simulating the project

A testbench `tb_fulladder.vhd` is provided inside the `sim/` folder. It initialises all inputs to zero, and explores all possible combinations. Finally, it compares the results against the expectation as in the following table.

A	B	Ci	S	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Exercise 1.

1. Open a terminal and go to 1. Go to `~/labs/lab05`.
2. Open the source file `src/fulladder.vhd`, using `kate` or your favorite editor

```
kate src/fulladder.vhd &
```

3. Implement the functionalities as in the above truth table.
4. Run the provided simulation script to check that your design is working correctly

```
./run_sim.sh
```

To run the simulation in GUI mode launch

```
./run_sim.sh -g
```

Exercise 2. Add signals

1. Define a new `std_logic` signal `TMP` in the FullAdder Architecture
2. Implement the following functionalities using the new defined signal

	Function
TMP	A XOR B
S	TMP XOR Ci
Co	(A AND B) or (TMP AND Ci)

3. Run again the simulation and check the results