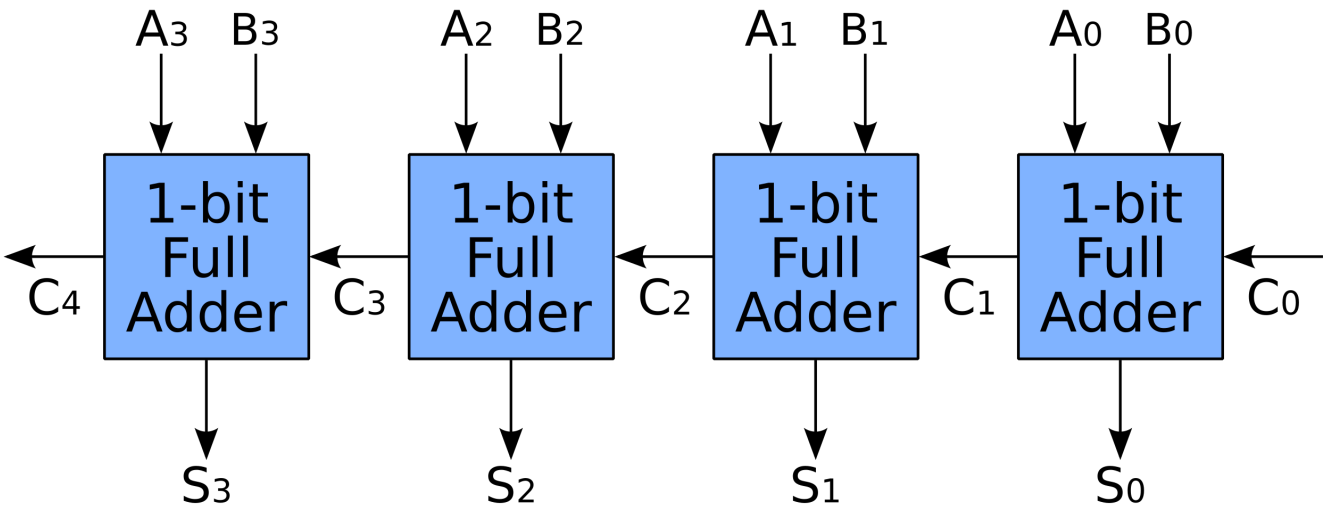
Lab 6: Combinatorial Logic - Design a Ripple Carry Adder

In this lab, we will design a simple 4-bit Full Adder block, purely combinatorial, using the ripple Carry adder (RCA) scheme.

A block diagram of the design is shown below.



The design

Port	Direction	Width	Type
ENABLE	IN	1	std_logic
C0	IN	1	std_logic
A	IN	4	std_logic_vector
B	IN	4	std_logic_vector
S	OUT	4	std_logic_vector
C4	OUT	1	std_logic

A testbench is provided to check the outputs and prints a summary message at the end.

The functionality of the block can be summarised as,

```
S = A + B
```

Exercise

1. Hierarchical Design

Implement the 4-bit RCA in file `~/labs/lab06/src/rca.vhd`, instantiating the fulladder block that you designed in Lab 5. A symlink to `fulladder.vhd` is also available in `~/labs/lab06/src/`.

N.B. You can access the individual bits of a `std_logic_vector` using round parenthesis

```
A(4); -- Get bit 4 of signal A
A(3 downto 1) -- Returns a std_logic vector of size 3, taking the bits (3)(2)(1) of signal A
```

2. Run the simulation and investigate the design

Run the simulation using the `run_sim.sh` script. Once you pass the simulation, run the script in GUI mode and investigate the hierarchical design.

```
./run_sim -g
```

3. Enabling/Disabling

Enhance the design to add an enable signal which zeros the `S` output when is set to `1`, and calculates the sum when set to `0`.

4. Increase the width

Increase the length of the adder to 8 bits.