

INTRODUCTION TO FPGA PROGRAMMING

LESSON 10: IP BLOCKS

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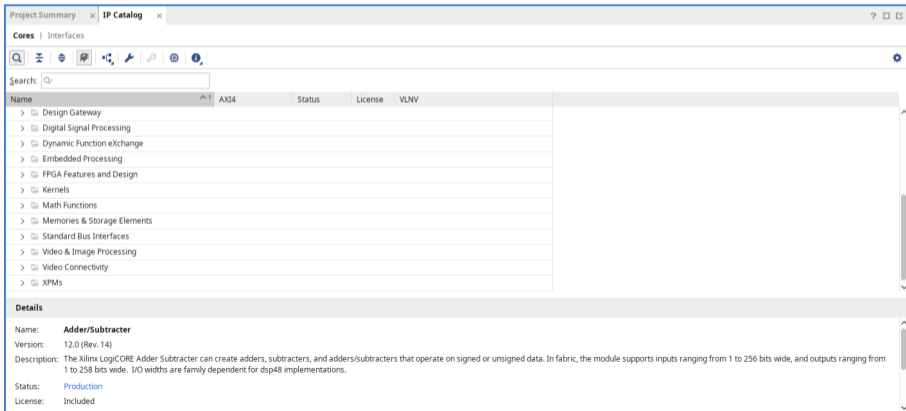
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WHAT ARE IP BLOCKS

- IP (Intellectual Property) blocks or IPs are a collection of pre-built configurable blocks provided by the FPGA vendor or third-parties
- Encrypted synthesised blocks with full simulation models



The screenshot shows the Xilinx IP Catalog interface. At the top, there are tabs for 'Project Summary' and 'IP Catalog'. Below the tabs, there are navigation icons and a search bar. The main area displays a list of IP blocks with columns for Name, AXI4, Status, License, and VLNW. The 'Adder/Subtractor' IP block is selected, and its details are shown in the bottom panel.

Name	AXI4	Status	License	VLNV
> Design Gateway				
> Digital Signal Processing				
> Dynamic Function eXchange				
> Embedded Processing				
> FPGA Features and Design				
> Kernels				
> Math Functions				
> Memories & Storage Elements				
> Standard Bus Interfaces				
> Video & Image Processing				
> Video Connectivity				
> XPMs				

Details

Name: **Adder/Subtractor**

Version: 12.0 (Rev. 14)

Description: The Xilinx LogiCORE Adder Subtractor can create adders, subtractors, and adders/subtractors that operate on signed or unsigned data. In fabric, the module supports inputs ranging from 1 to 256 bits wide, and outputs ranging from 1 to 258 bits wide. I/O widths are family dependent for dsp48 implementations.

Status: [Production](#)

License: Included

IP GENERATION

Customize IP

Adder/Subtractor (12.0)

Documentation IP Location Switch to Defaults

IP Symbol Information

Show disabled ports

Component Name

Basic Control

Implement using

S = **A** +/- **B**

Input Type

Input Width [2,256] [2,256]

Add Mode

Output Width [15 - 16]

Latency Configuration

Latency [0 - 15]

Constant Input

Constant Value (Bin)


OK Cancel

Xilinx Documentation Navigator - file:///home/dcieri/Documents/XilinxDocs/IP/support/documents/ip_documentation/addsub/v12_0/pg120-c-addsub.pdf

Catalog View Design Hub View X pg120-c-addsub.pdf X

LogiCORE IP Adder/Subtractor v12.0 Product Guide Up to Date

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IP Facts

Introduction

The Xilinx LogiCORE™ IP Adder/Subtractor core provides LUT and single DSP slice add/sub implementations. The Adder/Subtractor module can create adders (A+B), subtracters (A-B), and dynamically configurable adder/subtracters that operate on signed or unsigned data. The function can be implemented in a single DSP slice or LUTs (but currently not a hybrid of both). The module can be pipelined.

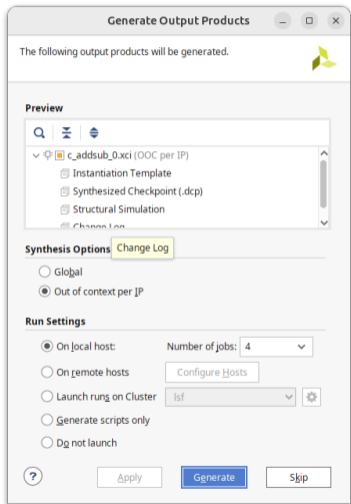
Features

- Generates adder, subtracter and adder/subtractor functions
- Supports two's complement-signed and unsigned operations

Core Specifics	
Supported Device Family ⁽¹⁾	Versal™ ACAP UltraScale+™ Families UltraScale™ Architecture Zynq®-7000 SoC 7 Series
Supported User Interfaces	N/A
Resources	Performance and Resource Utilization web page
Provided with Core	
Design Files	Encrypted RTL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	N/A
Simulation Model	Encrypted VHDL
Supported S/W Driver	N/A

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IP GENERATED FILES



- Generated products of the IP includes:
 - Instantiation Template to add IP to your design (next slide)
 - Synthesis Checkpoint
 - Structural Simulation, to allow simulation of IP
 - Changelog
- IP Synthesis options
 - Out-of-context: IP is synthesised as a standalone module
 - Global: IP is synthesised within your design. Any change to the design will require to resynthesise the IP as well. Not recommended.

IP INSTANTIATION IN VHDL

```
c_addsub_0.vho
/home/dcieri/Work/fpga-course-tum/labs/lab01/project_1/project_1.gen/sources_1/ip/c_addsub_0/c_addsub_0.vho
Read-only

49 -- IP Revision: 14
50
51 -- The following code must appear in the VHDL architecture header.
52
53 ----- Begin Cut here for COMPONENT Declaration ----- COMP_TAG
54 COMPONENT c_addsub_0
55   PORT (
56     A : IN STD_LOGIC_VECTOR(14 DOWNTO 0);
57     B : IN STD_LOGIC_VECTOR(14 DOWNTO 0);
58     CLK : IN STD_LOGIC;
59     CE : IN STD_LOGIC;
60     S : OUT STD_LOGIC_VECTOR(14 DOWNTO 0)
61   );
62 END COMPONENT;
63 -- COMP_TAG_END ----- End COMPONENT Declaration -----
64
65 -- The following code must appear in the VHDL architecture
66 -- body. Substitute your own instance name and net names.
67
68 ----- Begin Cut here for INSTANTIATION Template ----- INST_TAG
69 your_instance_name : c_addsub_0
70   PORT MAP (
71     A => A,
72     B => B,
73     CLK => CLK,
74     CE => CE,
75     S => S
76   );
77 -- INST_TAG_END ----- End INSTANTIATION Template -----
78
79 -- You must compile the wrapper file c_addsub_0.vhd when simulating
80 -- the core c_addsub_0. When compiling the wrapper file, be sure to
```

ANOTHER EXAMPLE: BLOCK RAM

The screenshot shows the 'Block Memory Generator (8.4)' IP configuration window. The window title is 'Customize IP'. On the left, there are tabs for 'IP Symbol' and 'Power Estimation'. Under 'IP Symbol', there is a checkbox for 'Show disabled ports' and a diagram of a block with two ports labeled 'BRAM_PORTA' and 'BRAM_PORTB'. The main configuration area on the right is titled 'Component Name' and 'blk_mem_gen_0'. It has several tabs: 'Basic', 'Port A Options', 'Port B Options', 'Other Options', and 'Summary'. The 'Basic' tab is active and contains the following settings:

- Interface Type: Native (dropdown)
- Memory Type: True Dual Port RAM (dropdown)
- Generate address interface with 32 bits:
- Common Clock:

Below these are 'ECC Options':

- ECC Type: No ECC (dropdown)
- Error Injection Pins: Single Bit Error Injection (dropdown)

Next is 'Write Enable':

- Byte Write Enable:
- Byte Size (bits): 9 (dropdown)

Finally, 'Algorithm Options':

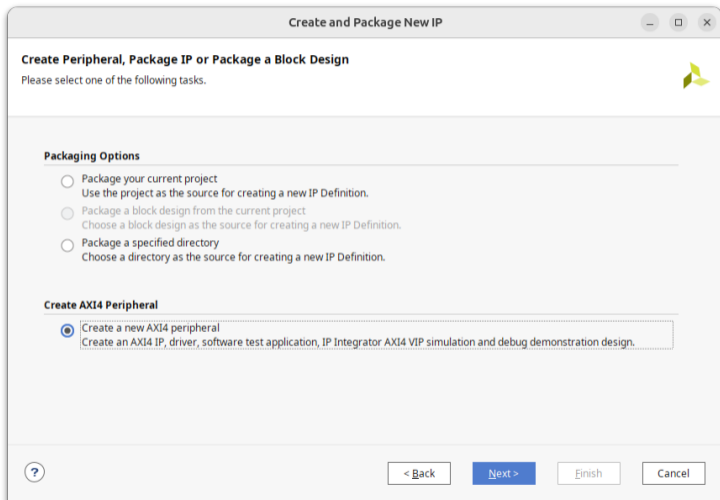
- Algorithm: Minimum Area (dropdown)
- Primitive: 8kx2 (dropdown)

At the bottom right, there are 'OK' and 'Cancel' buttons.

USER IPS

- You can pack your design into an IP that can be later placed in a repository
- User IP can be parametrised thanks to generics/generate
- You can include documentation, instantiation templates, and constraint files (even pin locations)
- Include a test-bench or design example
- Customise the IP generation GUI

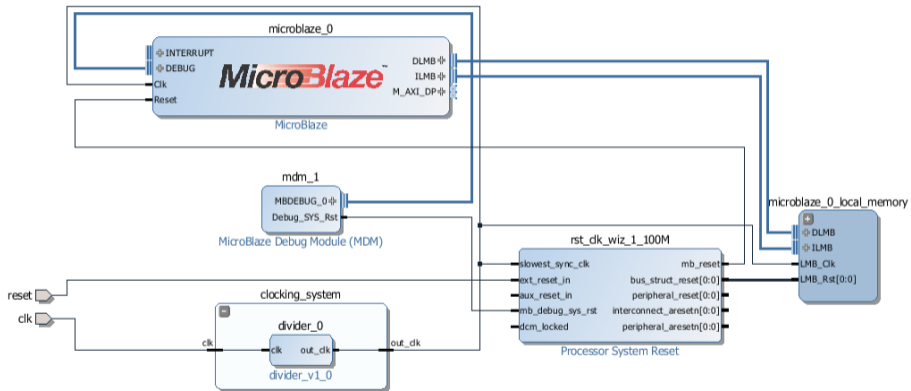
USER IP CREATION



IP INTEGRATOR

- Vivado provides a smart schematic editor to connect IPs together into a Block Design
 - Including user IPs
- Legal connections are highlighted
- Designs are validated
- Block Designs can be auto wrapped into a VHDL file
 - Wrapper can be used as top level of your design
- Alternatively, they can be instantiated as a normal component

BLOCK DESIGN EXAMPLE



LAB 16: USING IPS

The figures in these slides are taken from:

- Digital Design: Principles and Practices, Fourth Edition, John F. Wakerly, ISBN 0-13- 186389-4.
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- allaboutfpga.com
- nandland.com
- docs.amd.com
- <https://www.symmetryelectronics.com/>
- <https://www.edn.com/>
- Stephen A. Edwards, Columbia University, Fundamentals of Computer Systems, Spring 2012
- <https://medium.com/well-red/state-machines-for-everyone-part-1-introduction-b7ac9aaf482e>