INTRODUCTION TO FPGA PROGRAMMING

Lesson 12: Hardware Debug

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September 2024

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HARDWARE DEBUGGING ON FPGA

- Simulation and Verification tools provide an optimal way to debug an HDL design
- It is unavoidable sometimes to debug the design directly on hardware
  - E.g. when dealing with data from external sources that cannot be simulated
- Hardware Debugging is done using a set of data collecting IP provided by AMD

HARDWARE DEBUG WITH AMD FPGAS

- Hardware Debug using Vivado Hardware Manager
- It requires a JTAG connection to the FPGA
  - Platform USB cable I or II
  - Digilent cables
  - Our board has already the JTAG interface on board
- N.B. Adding hardware debug IPs alter your design!

AVAILABLE HARDARE DEBUG TOOLS

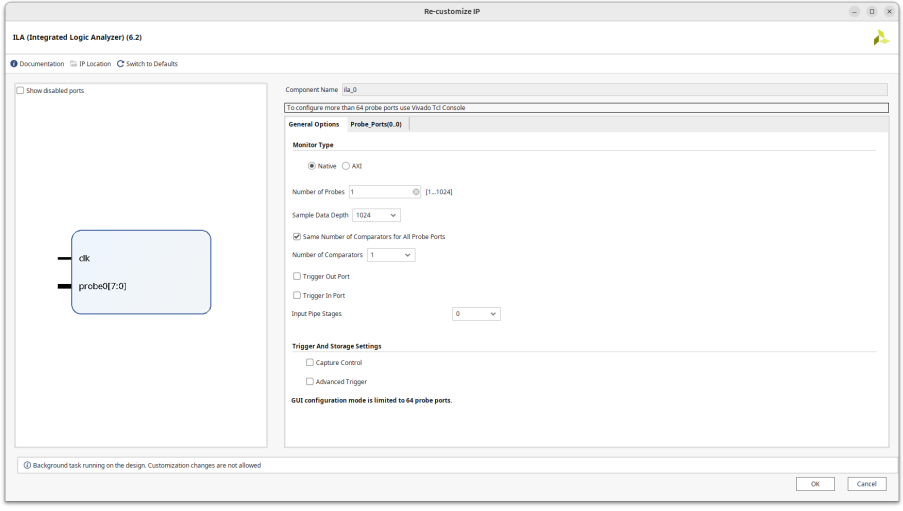
- Integrated Logic Analyzer (ILA): monitors the internal signals of a design for sampling time
- Virtual Input/Output (VIO): monitors and drive internal signals in real time
- Integrated Bit Error Ratio Tester: Evaluates and monitors the data quality of a transceiver
- JTAG to AXI Master: Emulates to AXI transactions and drives the internal AXI signals[1]

[1] AXI is a common standard communication protocol, widely used in computing and FPGA. More in another lecture

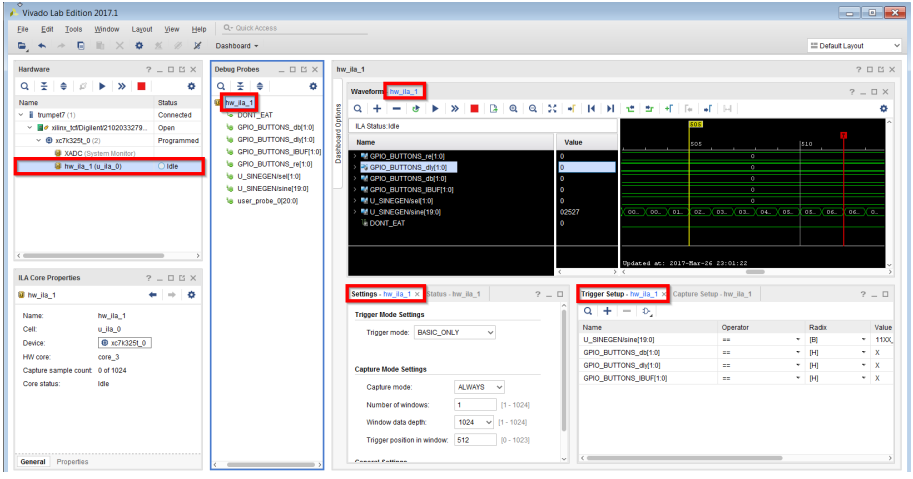
ILA

- ILA records the value of internal signals
- Stores values in FPGA memory
  - Signals to monitors and Sample data depth can be configured
- Signal sampling is driven by trigger signals
  - Triggers can be setup also at run time
- Number of samples captured is based on an input clock
- Storage Requirements = no. samples * total bits of sampled signals

ILA IP


Re-customize IP
ILA (Integrated Logic Analyzer) (6.2)
Documentation
IP Location
Switch to Defaults
Show disabled ports
clk
probe0[7:0]
Component Name
ila_0
To configure more than 64 probe ports use Vivado Tcl Console
General Options
Probe_Ports(0..0)
Monitor Type
Native
AXI
Number of Probes
1
[1..1024]
Sample Data Depth
1024
Same Number of Comparators for All Probe Ports
Number of Comparators
1
Trigger Out Port
Trigger In Port
Input Pipe Stages
0
Trigger And Storage Settings
Capture Control
Advanced Trigger
GUI configuration mode is limited to 64 probe ports.
Background task running on the design. Customization changes are not allowed
OK
Cancel

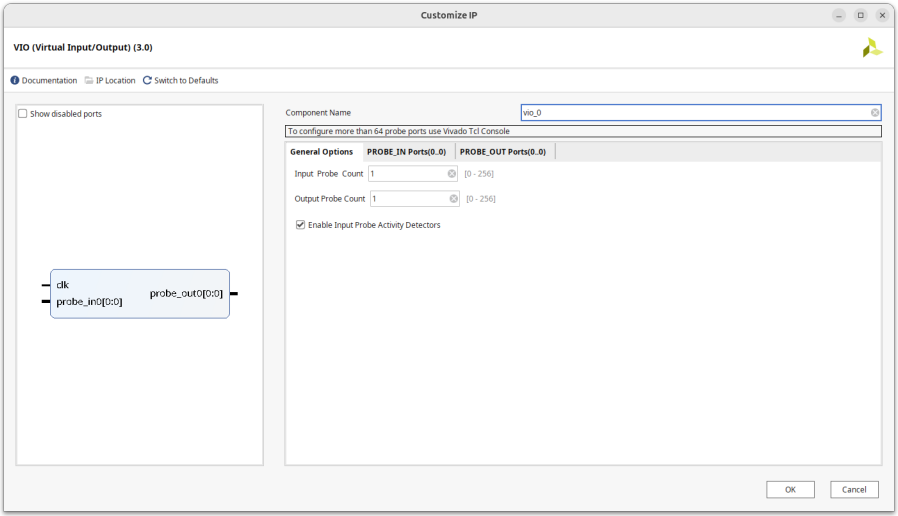
ILA IP


Vivado Lab Edition 2017.1
File Edit Tools Window Layout View Help
Quick Access
Dashboard
Default Layout
Hardware
Name
Status
trumpet7 (1)
Connected
xilinx_tcf/Digilent/2102033279...
Open
xc7k325t_0 (2)
Programmed
XADC (System Monitor)
hw_ila_1 (u_ila_0)
Idle
ILA Core Properties
hw_ila_1
Name: hw_ila_1
Cell: u_ila_0
Device: xc7k325t_0
HW core: core_3
Capture sample count: 0 of 1024
Core status: Idle
General
Properties
Debug Probes
hw_ila_1
DONT_EAT
GPIO_BUTTONS_db[1:0]
GPIO_BUTTONS_dly[1:0]
GPIO_BUTTONS_IBUF[1:0]
GPIO_BUTTONS_re[1:0]
U_SINEGEN/sel[1:0]
U_SINEGEN/sine[19:0]
user_probe_0[20:0]
hw_ila_1
Waveform - hw_ila_1
ILA Status: Idle
Dashboard Options
Name
Value
GPIO_BUTTONS_re[1:0]
GPIO_BUTTONS_dly[1:0]
GPIO_BUTTONS_db[1:0]
GPIO_BUTTONS_IBUF[1:0]
U_SINEGEN/sel[1:0]
U_SINEGEN/sine[19:0]
DONT_EAT
002527
Updated at: 2017-Mar-26 23:01:22
Settings - hw_ila_1
Status - hw_ila_1
Trigger Mode Settings
Trigger mode: BASIC_ONLY
Capture Mode Settings
Capture mode: ALWAYS
Number of windows: 1 [1 - 1024]
Window data depth: 1024 [1 - 1024]
Trigger position in window: 512 [0 - 1023]
Trigger Setup - hw_ila_1
Capture Setup - hw_ila_1
Name
Operator
Radix
Value
U_SINEGEN/sine[19:0]
GPIO_BUTTONS_db[1:0]
GPIO_BUTTONS_dly[1:0]
GPIO_BUTTONS_IBUF[1:0]

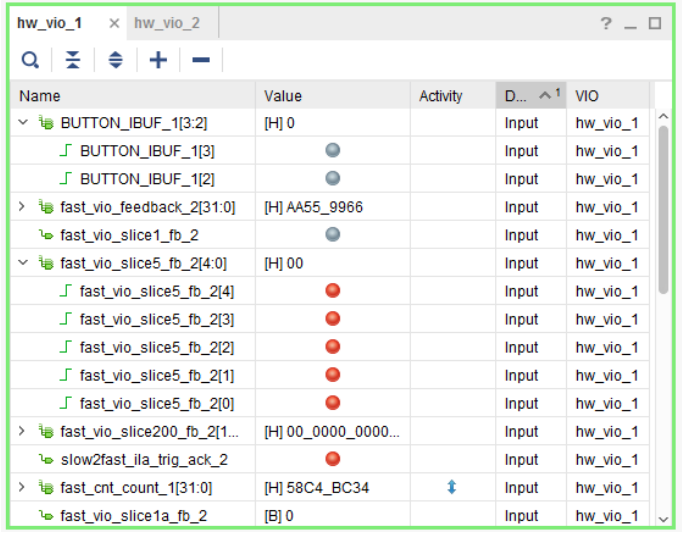
VIO

- VIO blocks is used to manually drive values to signals in the design
- It can monitor real-time signals

VIO IP


Customize IP
VIO (Virtual Input/Output) (3.0)
Documentation
IP Location
Switch to Defaults
Show disabled ports
clk
probe_in0[0:0]
probe_out0[0:0]
Component Name
vio_0
To configure more than 64 probe ports use Vivado Tcl Console
General Options
PROBE_IN Ports(0..0)
PROBE_OUT Ports(0..0)
Input Probe Count
1
[0 - 256]
Output Probe Count
1
[0 - 256]
Enable Input Probe Activity Detectors
OK
Cancel

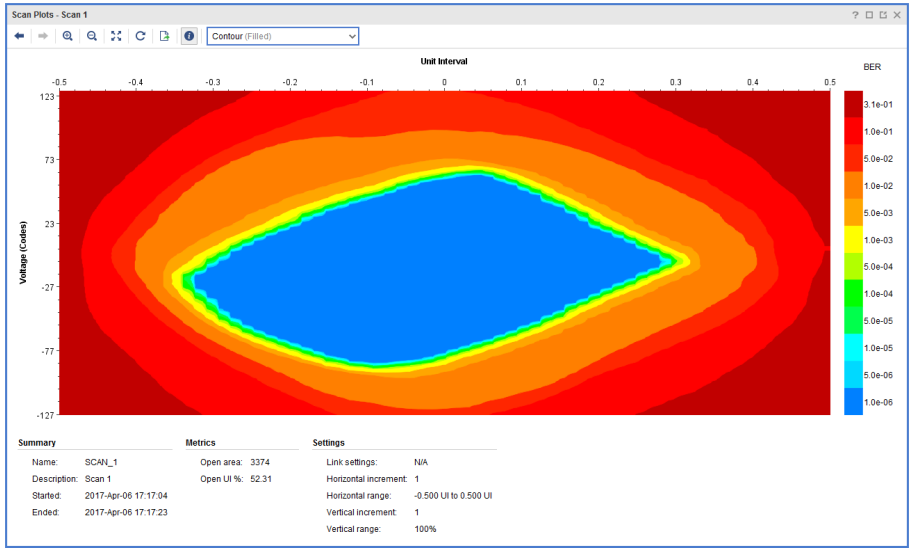
VIO IP


hw_vio_1
hw_vio_2
Name
Value
Activity
D...
VIO
BUTTON_IBUF_1[3:2]
[H] 0
Input
hw_vio_1
BUTTON_IBUF_1[3]
Input
hw_vio_1
BUTTON_IBUF_1[2]
Input
hw_vio_1
fast_vio_feedback_2[31:0]
[H] AA55_9966
Input
hw_vio_1
fast_vio_slice1_fb_2
Input
hw_vio_1
fast_vio_slice5_fb_2[4:0]
[H] 00
Input
hw_vio_1
fast_vio_slice5_fb_2[4]
Input
hw_vio_1
fast_vio_slice5_fb_2[3]
Input
hw_vio_1
fast_vio_slice5_fb_2[2]
Input
hw_vio_1
fast_vio_slice5_fb_2[1]
Input
hw_vio_1
fast_vio_slice5_fb_2[0]
Input
hw_vio_1
fast_vio_slice200_fb_2[1...
[H] 00_0000_0000...
Input
hw_vio_1
slow2fast_ila_trig_ack_2
Input
hw_vio_1
fast_cnt_count_1[31:0]
[H] 58C4_BC34
Input
hw_vio_1
fast_vio_slice1a_fb_2
[B] 0
Input
hw_vio_1

IBERT

- Integrated Bit Error Ratio Tester
- Determines the quality of a serial link, measuring the Bit Error Ratio and plotting Eye Diagrams
- The IP transmits pre-defined bit patterns to the transceiver and reads back the results
- If bits are different it increases the Bit Error Count (BEC)
- Eventually, calculates the total Bit Error Ratio (BER)
- BER can be plotted against time and voltage variation over many sample to produce the so called Eye Diagram
  - The more open the eye, the better is the link

EYE DIAGRAM


Scan Plots - Scan 1
Contour (Filled)
Unit Interval
-0.5
-0.4
-0.3
-0.2
-0.1
0
0.1
0.2
0.3
0.4
0.5
Voltage (Codes)
123
73
23
-27
-77
-127
BER
3.1e-01
1.0e-01
5.0e-02
1.0e-02
5.0e-03
1.0e-03
5.0e-04
1.0e-04
5.0e-05
1.0e-05
5.0e-06
1.0e-06
Summary
Name: SCAN_1
Description: Scan 1
Started: 2017-Apr-06 17:17:04
Ended: 2017-Apr-06 17:17:23
Metrics
Open area: 3374
Open UI %: 52.31
Settings
Link settings: N/A
Horizontal increment: 1
Horizontal range: -0.500 UI to 0.500 UI
Vertical increment: 1
Vertical range: 100%

LAB 19: HARDWARE DEBUG

The figures in these slides are taken from:

- Digital Design: Principles and Practices, Fourth Edition, John F. Wakerly, ISBN 0-13- 186389-4. ©2006, Pearson Education, Inc, Upper Saddle River, NJ. All rights reserved
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