Introduction to FPGA Programming

Report of Contributions

Contribution ID: **1** Type: **not specified**

Lesson 1: Digital Systems, FPGAs and HDL

Monday, 2 September 2024 09:00 (45 minutes)

Presenter: CIERI, Davide (Max-Planck-Institut für Physik)

Contribution ID: **2** Type: **not specified**

Lab 1: First Look at Vivado

Monday, 2 September 2024 09:45 (20 minutes)

Contribution ID: **3** Type: **not specified**

Lab 2: Simulating an HDL design with Vivado and GHDL

Monday, 2 September 2024 10:05 (55 minutes)

Contribution ID: **4** Type: **not specified**

Lesson 2: VHDL Fundamentals

Monday, 2 September 2024 11:30 (30 minutes)

Presenter: CIERI, Davide (Max-Planck-Institut für Physik)

Contribution ID: **5** Type: **not specified**

Lab 3: Wiring Switches to LEDs

Monday, 2 September 2024 12:00 (30 minutes)

Contribution ID: **6** Type: **not specified**

Lesson 3: Boolean Algebra, Look-up Tables and IOs

Tuesday, 3 September 2024 09:00 (30 minutes)

Presenter: CIERI, Davide (Max-Planck-Institut für Physik)

Contribution ID: **7** Type: **not specified**

Lab 4: Wiring Switches to LED (part II)

Tuesday, 3 September 2024 09:30 (30 minutes)

Contribution ID: **8** Type: **not specified**

Lab 5: Implement a Full Adder

Tuesday, 3 September 2024 10:00 (20 minutes)

Contribution ID: **9** Type: **not specified**

Lab 6: Hierarchical Design

Tuesday, 3 September 2024 10:20 (40 minutes)

Contribution ID: **10** Type: **not specified**

Lesson 4: Sequential Logic and Flip-Flops

Tuesday, 3 September 2024 11:30 (30 minutes)

Contribution ID: **11** Type: **not specified**

Lab 7: Counters and Debouncing

Tuesday, 3 September 2024 12:00 (30 minutes)

Contribution ID: **12** Type: **not specified**

Lab 8: An LED Blinker

Tuesday, 3 September 2024 12:30 (30 minutes)

Contribution ID: **13** Type: **not specified**

Lesson 5: Types, Arrays and Arithmetic Functions

Wednesday, 4 September 2024 09:00 (30 minutes)

Presenter: CIERI, Davide (Max-Planck-Institut für Physik)

Contribution ID: **14** Type: **not specified**

Lab 9: Design an Arithmetic Logic Unit

Wednesday, 4 September 2024 09:30 (1 hour)

Contribution ID: **15** Type: **not specified**

Lesson 6: VHDL Simulation

Wednesday, 4 September 2024 11:00 (40 minutes)

Contribution ID: **16** Type: **not specified**

Lab 10: Testbench Coding

Wednesday, 4 September 2024 11:40 (1 hour)

Contribution ID: **17** Type: **not specified**

Lesson 7: Storing Data on FPGAs

Thursday, 5 September 2024 09:00 (30 minutes)

Contribution ID: **18** Type: **not specified**

Lab 11: Trigonometric Functions on FPGA

Thursday, 5 September 2024 09:30 (1 hour)

Contribution ID: **19** Type: **not specified**

Lesson 8: Packages, Libraries and Parametrisation

Thursday, 5 September 2024 11:00 (30 minutes)

Contribution ID: **20** Type: **not specified**

Lab 12: Packages and libraries

Thursday, 5 September 2024 11:30 (30 minutes)

Contribution ID: **21** Type: **not specified**

Lab 13: Parameters and Parametised Generation

Thursday, 5 September 2024 12:00 (30 minutes)

Contribution ID: **22** Type: **not specified**

Lesson 9: Finite State Machines

Friday, 6 September 2024 09:00 (30 minutes)

Presenter: CIERI, Davide (Max-Planck-Institut für Physik)

Contribution ID: **23** Type: **not specified**

Lab 14: Improve the Traffic Light

Friday, 6 September 2024 09:30 (30 minutes)

Contribution ID: **24** Type: **not specified**

Lesson 10: IP Blocks

Monday, 9 September 2024 09:00 (30 minutes)

Contribution ID: **25** Type: **not specified**

Lab 16: Using IPs

Monday, 9 September 2024 09:30 (30 minutes)

Contribution ID: **26** Type: **not specified**

Lesson 11: Timing on FPGAs

Monday, 9 September 2024 10:00 (45 minutes)

Contribution ID: **27** Type: **not specified**

Lab 17: Timing Constraints

Monday, 9 September 2024 11:15 (30 minutes)

Contribution ID: **28** Type: **not specified**

Lab 18: Generating Clocks

Monday, 9 September 2024 11:45 (45 minutes)

Contribution ID: **29** Type: **not specified**

Lesson 13: External Interfaces

Wednesday, 11 September 2024 09:00 (30 minutes)

Contribution ID: **30** Type: **not specified**

Lab 20: UART Transmitter

Wednesday, 11 September 2024 09:30 (1 hour)

Contribution ID: **31** Type: **not specified**

Lesson 9a: The 7-segment Display

Friday, 6 September 2024 10:00 (20 minutes)

Contribution ID: **32** Type: **not specified**

Lab 15: Design a Stopwatch

Friday, 6 September 2024 10:50 (2 hours)

Contribution ID: **33** Type: **not specified**

Lesson 12: Hardware Debugging

Tuesday, 10 September 2024 09:00 (30 minutes)

Contribution ID: **34** Type: **not specified**

Lab 19: Hardware Debugging

Tuesday, 10 September 2024 09:30 (1 hour)

Contribution ID: **35** Type: **not specified**

Lab 21. Connect to the VGA Display

Wednesday, 11 September 2024 11:30 (1 hour)

Contribution ID: **36** Type: **not specified**

Lesson 14: Advanced Vivado Flow

Tuesday, 10 September 2024 11:00 (30 minutes)

Contribution ID: **37** Type: **not specified**

Lab 22: Advanced Vivado Flow

Tuesday, 10 September 2024 11:30 (1 hour)

Contribution ID: **38** Type: **not specified**

Lesson 15: Design Management with Vivado

Contribution ID: **39** Type: **not specified**

Lab 23: Design Management

Contribution ID: **40** Type: **not specified**

Lesson 15: Processors on FPGA

Thursday, 12 September 2024 09:00 (30 minutes)

Contribution ID: **41** Type: **not specified**

Lab 23: Implementing a Microblaze soft processor

Thursday, 12 September 2024 09:30 (1 hour)

Contribution ID: **42** Type: **not specified**

Lesson 16: Advanced FPGA topics

Thursday, 12 September 2024 11:00 (1 hour)

Contribution ID: **43** Type: **not specified**

Lesson 13a: VGA Screens

Wednesday, 11 September 2024 11:00 (30 minutes)

Contribution ID: **44** Type: **not specified**

Course Examination

Friday, 13 September 2024 09:00 (2 hours)