Goal:

Design and build a fully functional Belle II half-ladder ("module") without DEPFETs

Why:

- check whether there is space enough for the full circuit, including passives
- foresee test pads for direct probing of the signals and voltages on the module
    - signal integrity, voltage drops, parasitic caps and res …
- test technological feasibility of the 3-metal system
- practice on-module (Flip chip) and off-module interconnect (kapton cable)
- do we need Cu in the sensitive region????
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Main features:

- Metal system like in final module: 3 metal layers → alu1, alu2, cu
- circuitry at the periphery for 4 DHPs, 4 DCDs, 6 Switchers, default geometry like on wiki
  http://twiki.hll.mpg.de/twiki/bin/view/DepfetInternal/ModuleLayout
- power supply, slow control and I/O over kapton cable
- sensitive region free for test structures

I Design rules and basic technology parameters for the 3-metal system

-: *SUB*: ~400 Ohm.cm silicon, on cutting edge potential

-: *ILD0*: isolation to first metal layer, thermal SiO2, 180nm (**LTO,nitride??**)

-: *M1*: Al, 1 micron, 30mOhm/sq**, design dimensions gap/line???**

-: *ILD1*: 1000nm LTO**, contacts to M1??**

-: *M2*: Al, 1 micron **design dimensions gap/line???**

-: *ILD2* : 5 micron BCB, contact holes 15 micron, stacked via to M1 over M2 possible

-: *M3*: 5 micron ep-Cu, expect 5mOhm/sq

-: *PA*: passivation, solder mask BCB, 5 micron

- landing pads for bumps, solder pads for passives, Al wire bond pads open

- **is soldering/bump bonding after BCB passivation possible???**

- if there is no Cu in sens. Region, no extra passivation in thin area necessary

BCB properties: http://www.dow.com/cyclotene

BCB Properties	**Value**	**Additional Information**
Dielectric Constant	**2.65 – 2.5 (1MHz – 10 GHz)**	**Dielectric Constant vs. Frequency and Temperature**
Dissipation Factor	**0.0008 – 0.002 (1MHz – 10 GHz)**	
High Frequency (400 – 1500 GHz)		**CYCLOTENE* 3022 Resin Dielectric Constant and Loss vs. Frequency**
Breakdown Voltage	**5.3 ± 0.2 x 10^{6} V/cm**	
Leakage Current (dry-etch)	**4.4 ± 0.5 x 10^{-10} A/cm^{2} (0.5 MV/cm)** **6.8 ± 0.8 x 10^{-10} A/cm^{2} (1.0 MV/cm)**	
Leakage Current (photosensitive)	**2.9 ± 1.4 x 10^{-10} A/cm^{2} (0.5 MV/cm)** **4.7 ± 1.6 x 10^{-10} A/cm^{2} (1.0 MV/cm)**	
Volume Resistivity	**1 x 10^{19}Ω-cm**	

II Module geometry and schematic of periphery

-: Use standard wafers, Modules will not be thinned

-: take 106-011110.idw, (inner layer module, slit design at EOS) as starting point

- need to be updated for wide kapton layout and large screw/washer opening

-: *ASICs:* DHP 0.2, DCDB, SwitcherB

- DHP: final DHP will not be available for the E-module, use DHP 0.2 but foresee space on EOS as for final version (same chip size as DCDB)

- SwitcherB: default is latest SwitcherB design

  - segmentation of the analog Switcher voltages along z is difficult to realize due to space constraints on the balcony
  - a possible solution could be local regulators on each switcher but this needs to be confirmed by chip designers, issues are space constraints on the chip (need HV transistors) and power consumption
  - bumping: check whether mechanical bump bonds at the corners of the Switchers are possible to improve stability of the chips on the module. The idea is to avoid adhesive between switchers and substrate.

-: *I/O*: layout and schematic for wide kapton

  - position of the slit/hole needs to be confirmed by the mechanics group
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-: *passives:* foresee solderable pads for decoupling caps and termination resistors at EOS and balcony

-: *testability*: foresee wire-bond jumpers (Alu pads) for bypassing of chips not present on the Module

Test pads (probe station probing) for switcher outputs, clock distribution and power lines etc …

III Testability and the “sensor” region

-: use sensitive region to provide test pads and bypass bond pads for missing ASICs

-: provide integrated resistive and capacitive integrated load for DCD inputs and switcher output

-: test noise and functionality of DCD/DHP pair using test inputs of DCD

-: Hans: provide test inputs for DCD by using switcher outputs and voltage dividers. In this way synchronicity between switchers and DCDs could be tested.

-: Jelena: use small PXD6 matrix, glue place it in a corner of the E-Module,
interconnection between matrix and e-Module by wire bonds
supply of matrix over kapton