

2ND WORKSHOP ON SILICON SENSORS FOR
RADIATION DETECTION AND QUANTUM APPLICATIONS

PXD9 BELLE-TYPE MINIMATRIX CHARACTERIZATION

Paula Scholz on behalf of Erik Büchau

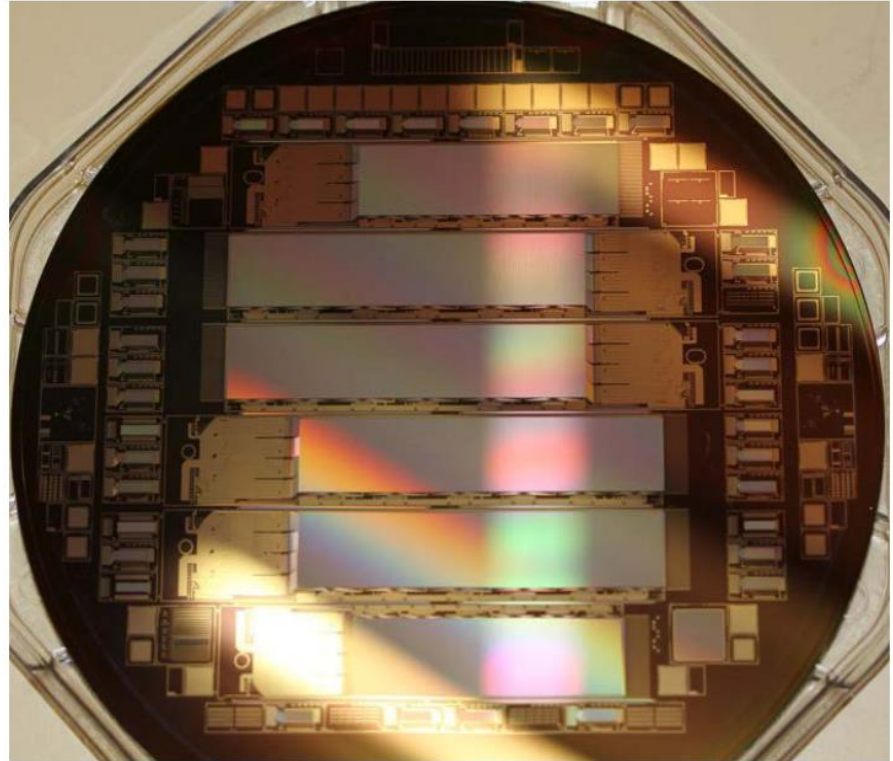


1. Base level testing

- Punch through depletion
- DEPFET IV-curves
- Transconductance

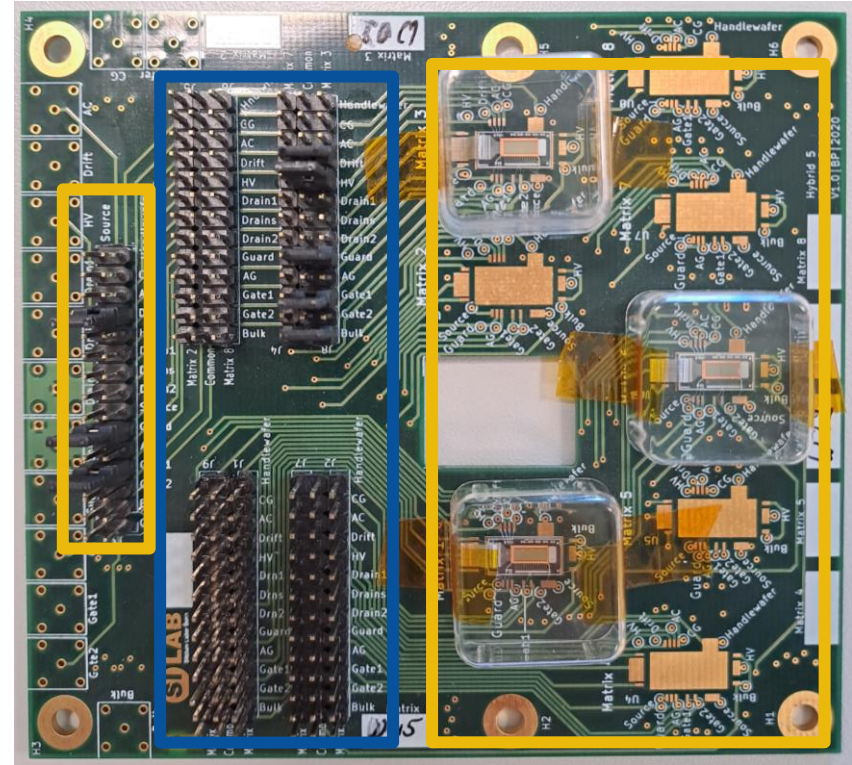
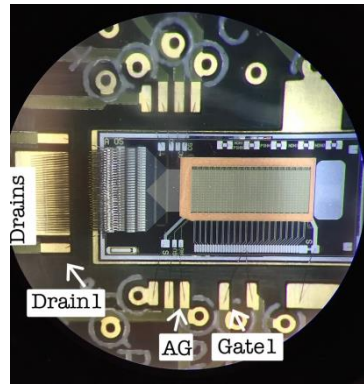
2. Full module testing

- Transconductance
- Charge gain
- Energy calibration



MINI MATRIX PCB

- Test board for low-level tests by supplying voltages directly to the matrix
- Different rows and columns of pixels can be activated and steered
- Working point: single active pixel has a current of about $100\mu\text{A}$



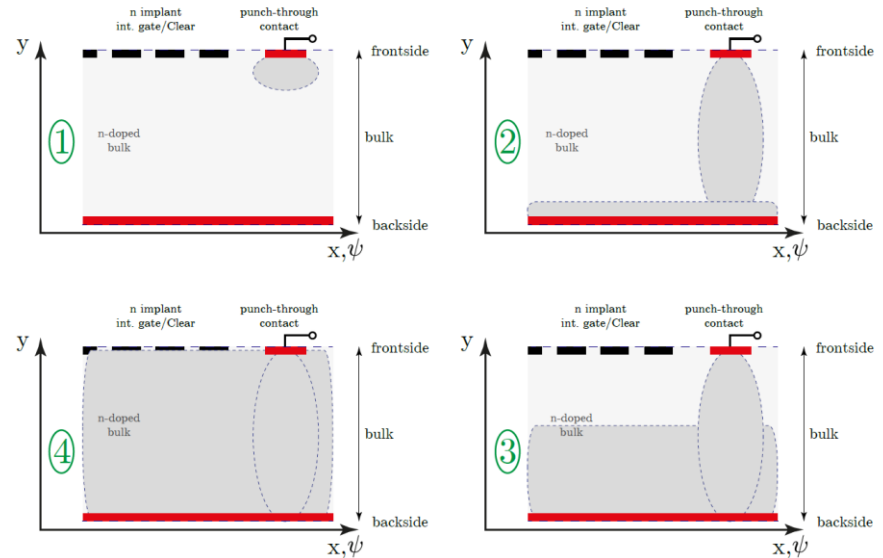
Voltages

Matrix selection

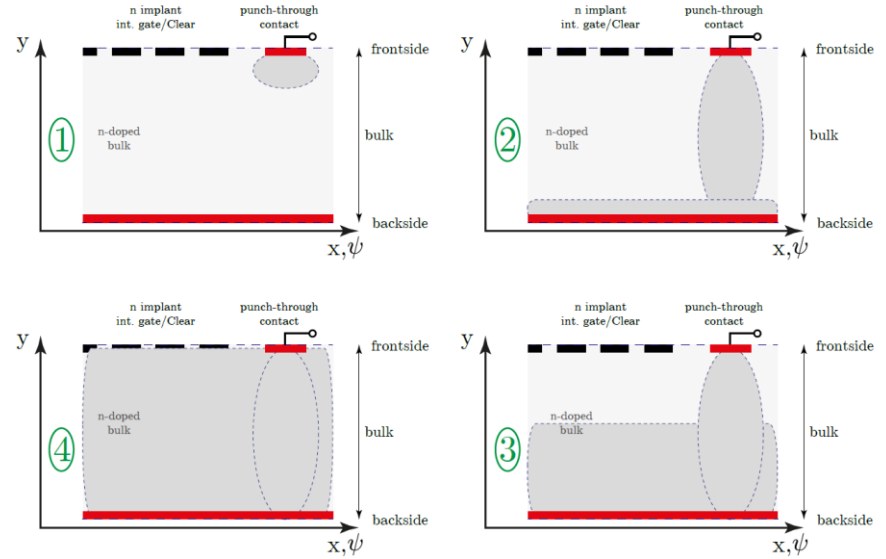
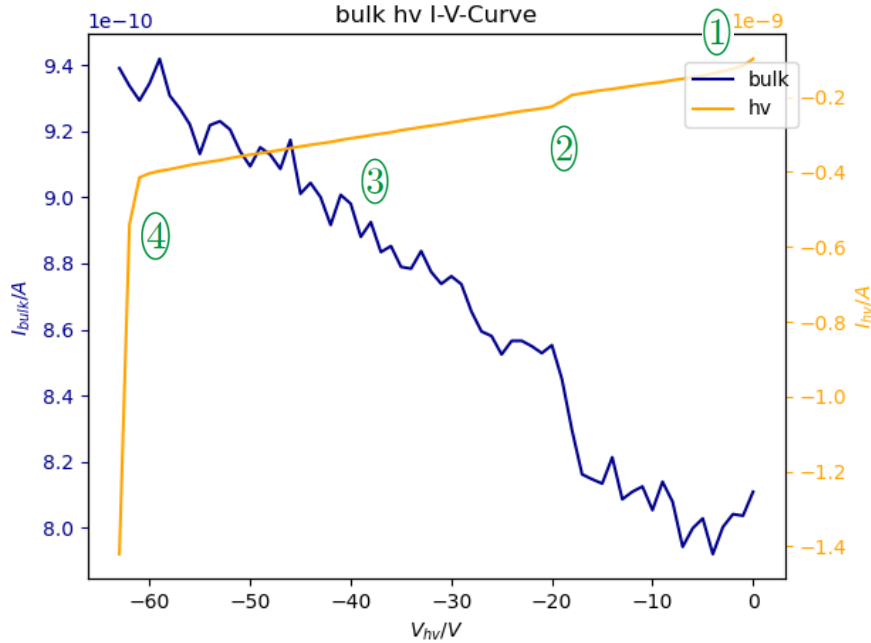
Matrices

BACKWARDS BIASING

- Depletion of bulk via **punch through**
- **HV-contact on top**, p+ back side
- Depletion builds up as follows:
 - Applying negative voltage at HV contact (1)
 - Depletion reaches the back side (2)
 - Depletion region grows towards front side (3)
 - Depletion region reaches front side
 - Punch-through reaches front side (4)

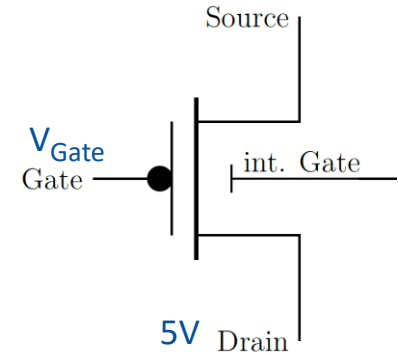


HV-IV CURVE OF PXD9 MINI MATRIX



MINI MATRIX PCB – UNBIASED

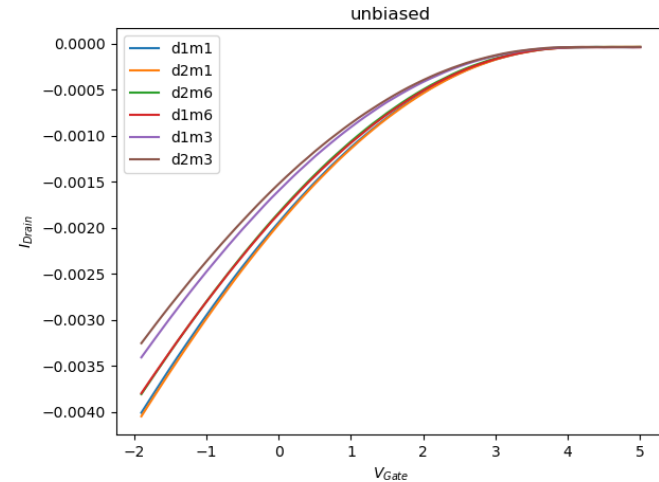
- Activate the FET by applying a gate voltage
- Drain implant set to 5V in reference to source



- Measure drain current

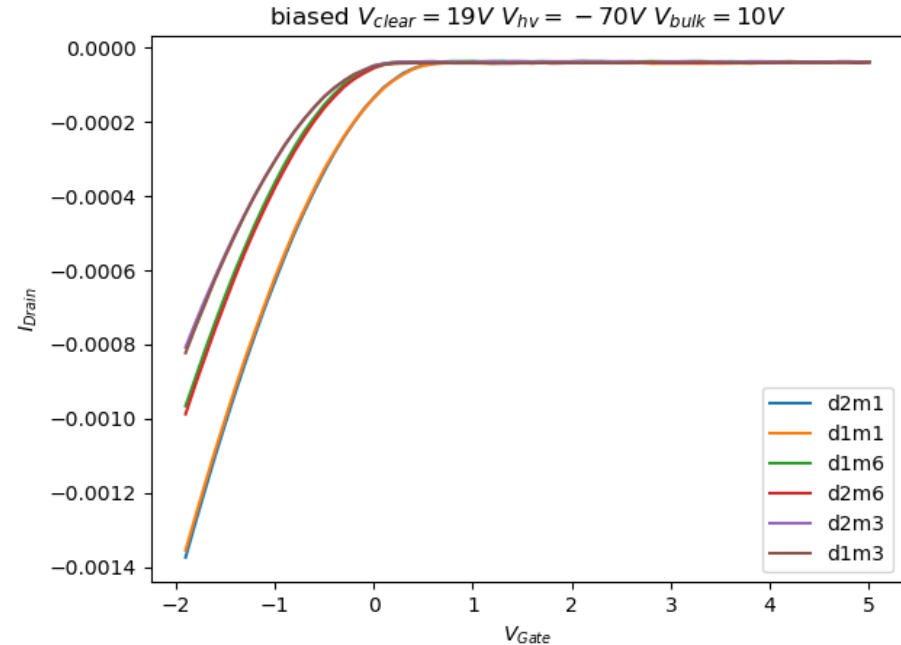
$$I_D \approx \frac{1}{2} \mu C_{ox} \frac{W}{L} (U_{Gate} - U_{th})^2$$

- No clear voltage applied
 - Current higher than nominal value since the internal gate is full



MINI MATRIX PCB – BIASED TESTS

- Clear voltage applied to empty the internal gate
 - Lower current
- High voltage applied to deplete the sensitive volume
 - Lower threshold voltage
- Bulk voltage stops electrons entering from outside the sensitive volume
 - Reduced signal distortion



MINI MATRIX PCB – TRANSISTOR PROPERTIES

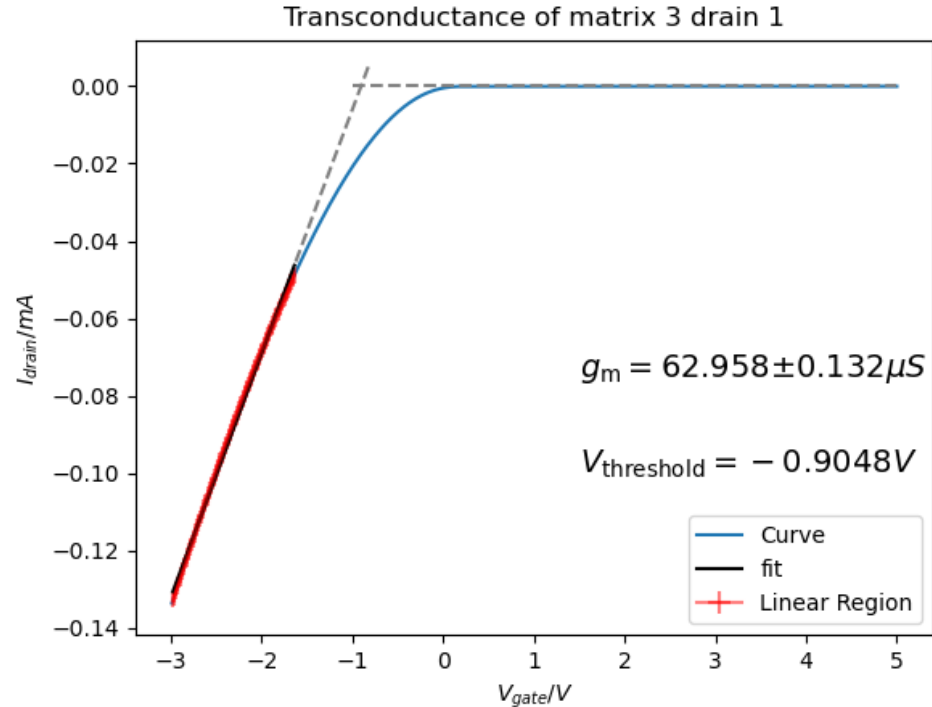
IV-curve used to determine

1. transconductance

$$g_m = \frac{\partial I_D}{\partial V_{Gate}} = 62.958 \mu S$$

2. threshold voltage

- Indicates FET in on-state
- $V_{threshold} = -0.9048V$



HYBRID5 – A FULL SYSTEM DEMONSTRATOR

SWITCHERS

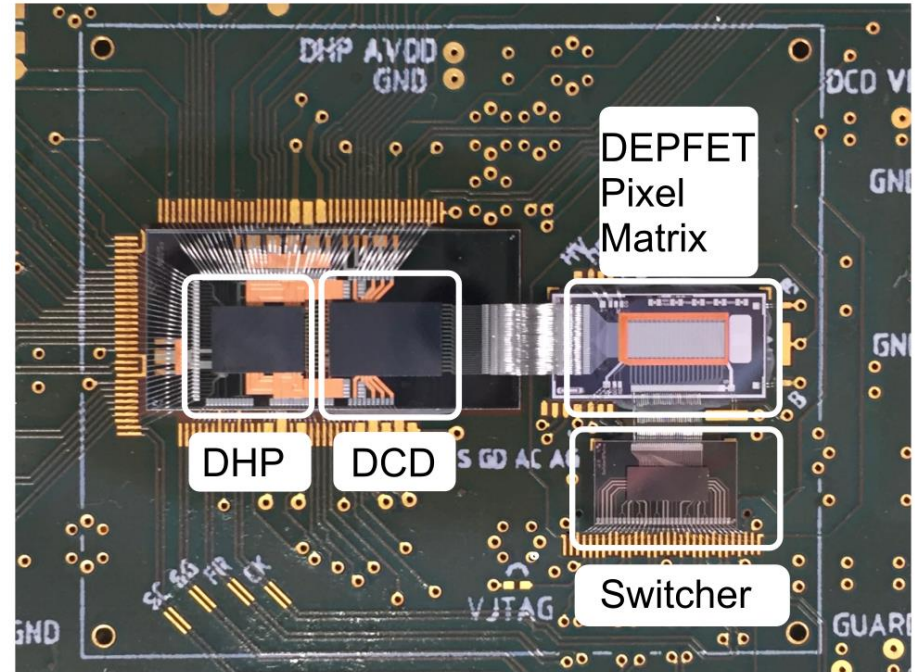
- Activate pixel with gate voltage
- Clear pixels with clear voltage

DCD

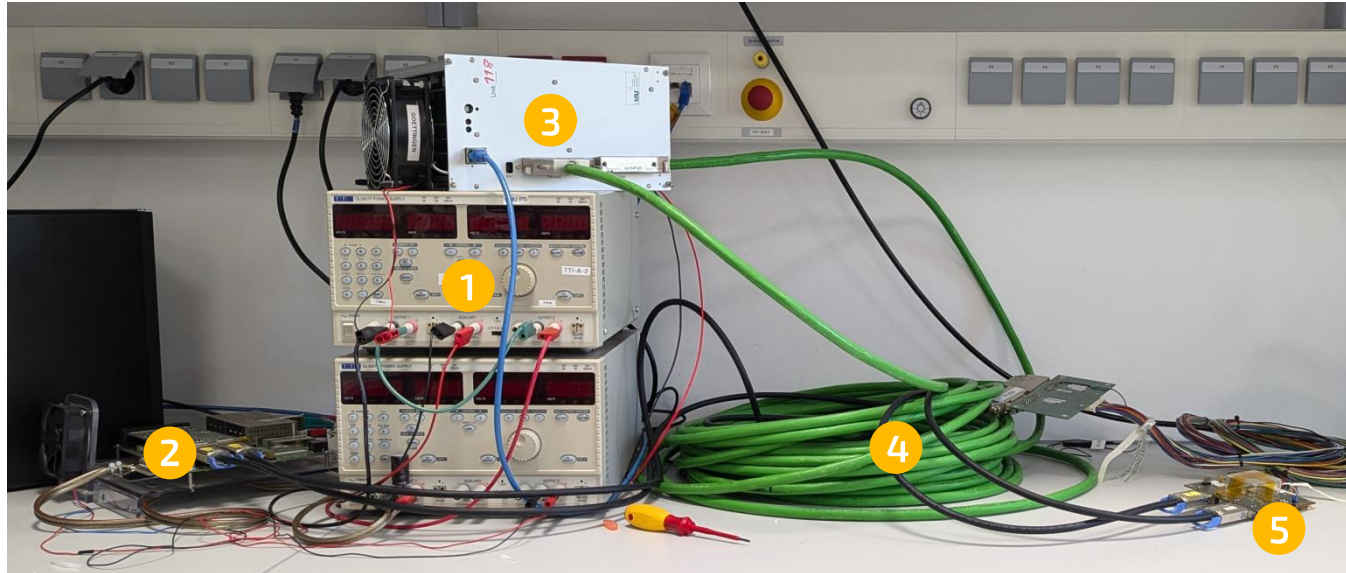
- Digitize drain currents
- amplifies signal (DCD gain)

DHP

- Data handling and ASIC control
- Important for mapping and clustering



HYBRID5 TEST SETUP IN BONN



1 Primary Power Supplies

3 PXD Power Supply

5 Hybrid5 Board

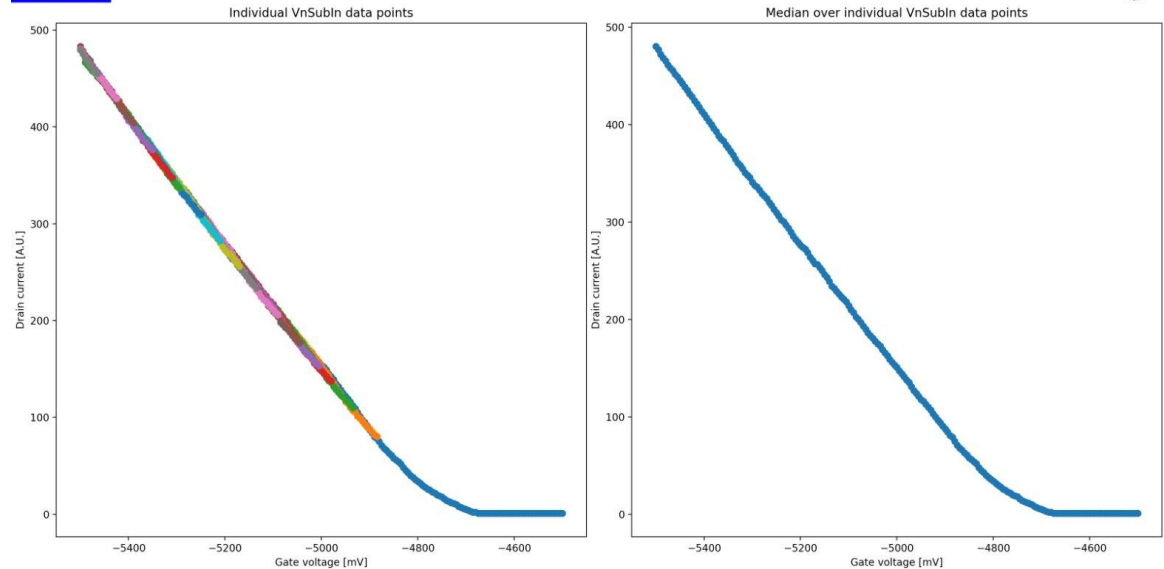
2 DHE (Data Handling Engine)

4 14m Power Cable

- As before: variation of gate voltage and determination of drain current
- This time: drain current from DCD in ADU
- Possibility to vary additional voltage to stay in dynamic range of DCD (different colors) and combine the results

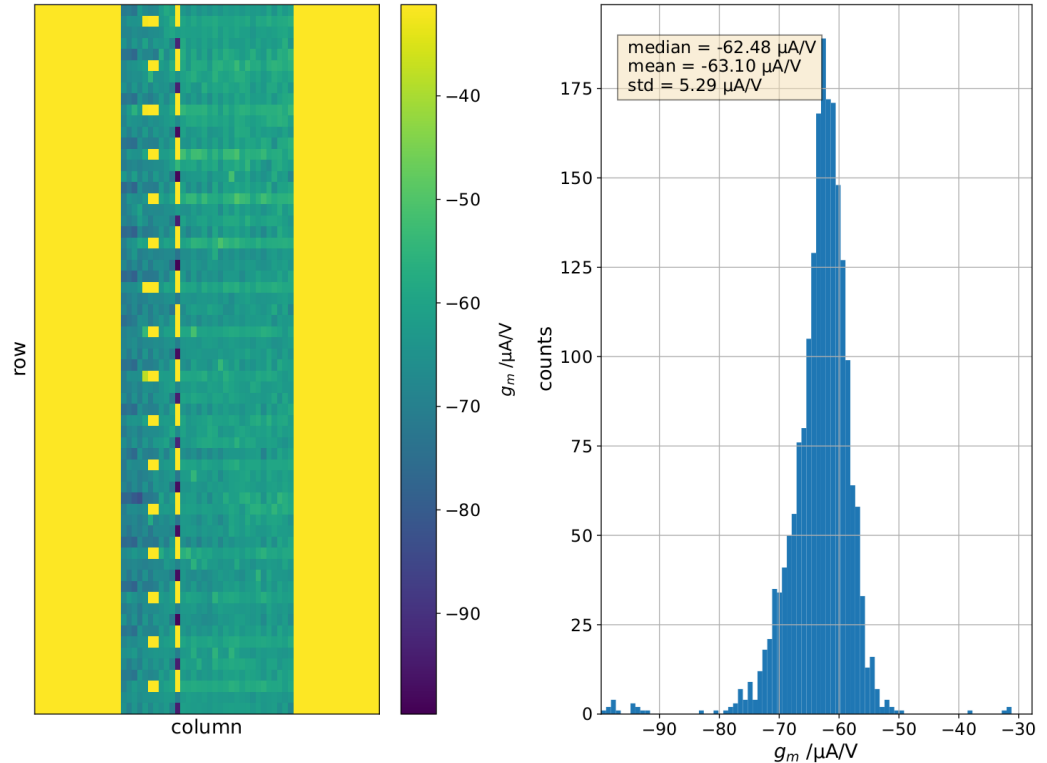


IV-Curve for Pixel at row 5 and column 4 (unmapped)



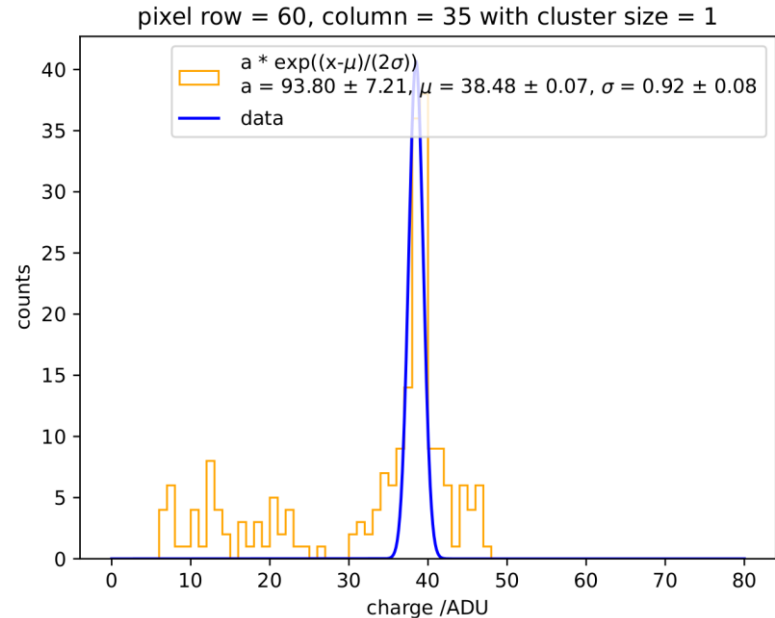
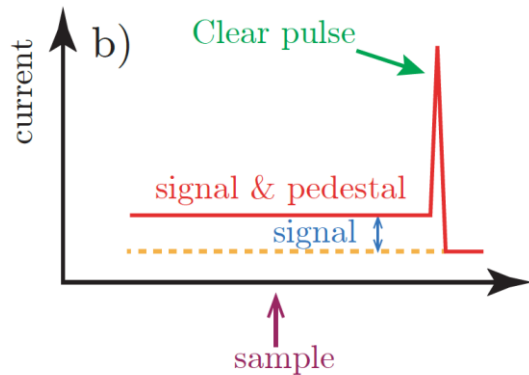
HYBRID5 MEASUREMENTS - TRANSCONDUCTANCE

- Conversion of ADU to A by performing DCD calibration
- Applied to every pixel yields a Gaussian distribution
 - Mean value: $g_m = -63.10 \mu\text{S}$
- Matches expectations from the previous test results
 - $g_m = -62.958 \mu\text{S}$
- Also visible: dead drain line



HYBRID5 SOURCE MEASUREMENTS

- measure base current of the pixel
- Install source and measure current of the pixel
 - Amplitude of the current is equivalent to charge deposited in internal gate



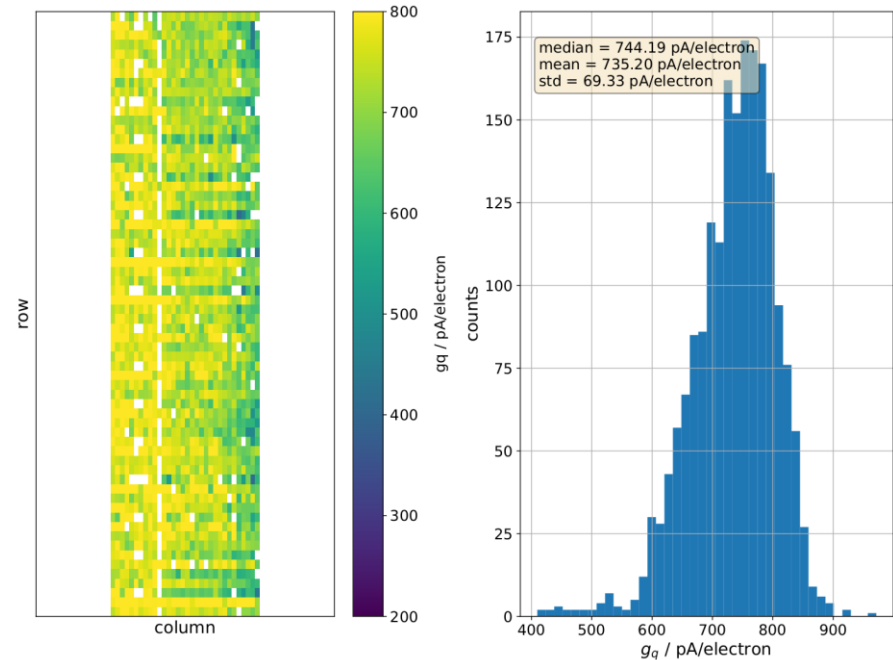
HYBRID5 SOURCE MEASUREMENTS

- Charge gain g_q from known parameters

$$g_q = \frac{\mu_{\text{fit}}}{E_{K\alpha}^{\text{Cd109}}} \cdot \frac{1}{\text{DCD gain}} \cdot \langle E_{eh} \rangle$$

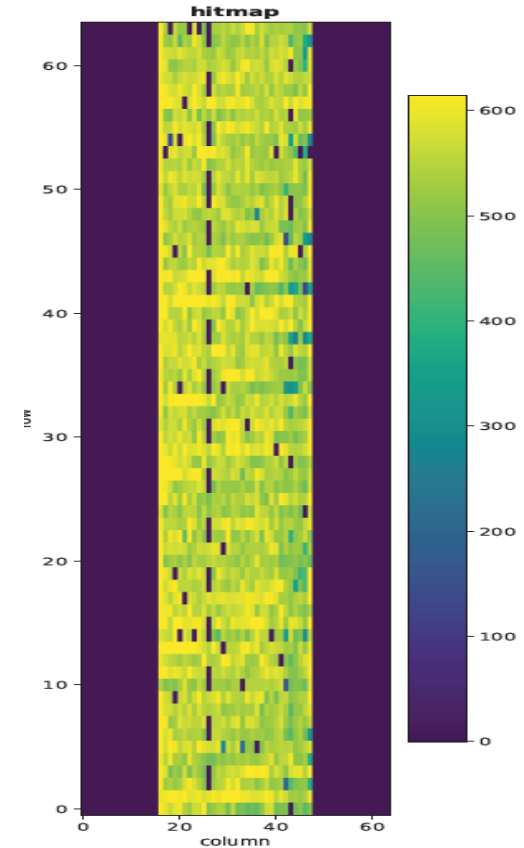
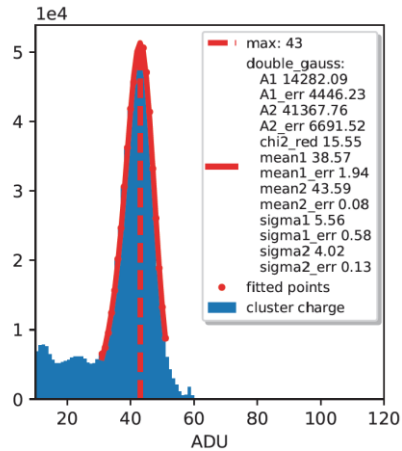
$$[g_q] = \frac{\text{ADU}}{\text{eV}} \cdot \frac{\text{nA}}{\text{ADU}} \cdot \frac{\text{eV}}{e} = \frac{\text{nA}}{e}$$

- Calculated for every pixel yields Gaussian distribution
 - Mean value: $g_q = 735.20 \text{ pA/e-}$
- Value higher than expected ($\sim 500 \text{ pA/e-}$)



ENERGY CALIBRATION OF HYBRID5

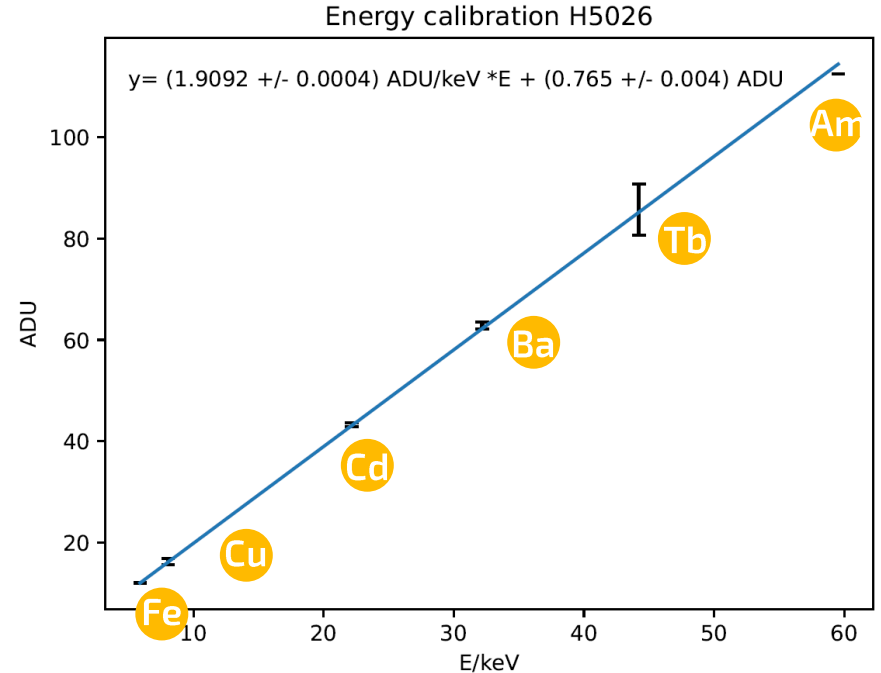
- Perform source measurements with different radiative sources
- Fit (double-) Gauss peak to histogram
- ADU values per frame



ENERGY CALIBRATION OF HYBRYID5

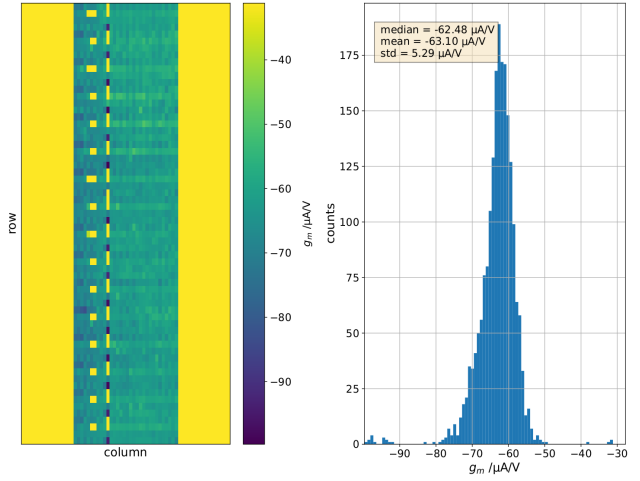
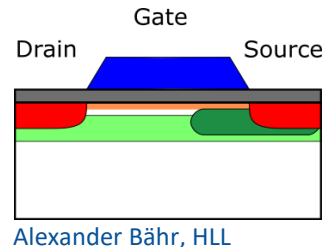
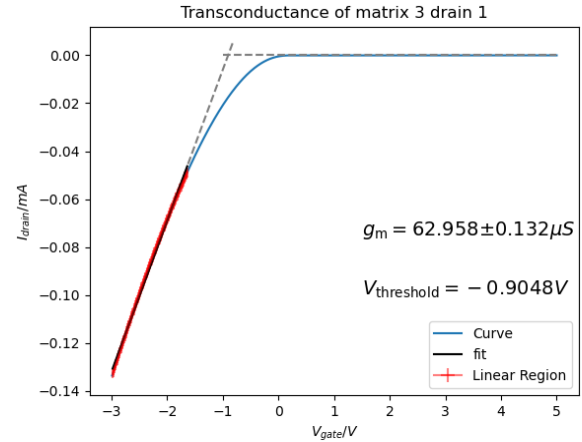
- Assign measured ADU values to energy values
- Gate voltage adjusted for $I_{Source}=100 \mu\text{A/Pixel}$
 - Hybrid5 and gate voltage specific energy calibration

$$X_{ADU} = (1.9092 \pm 0.0004) \frac{\text{ADU}}{\text{keV}} \times E + (0.765 \pm 0.004) \text{ADU}$$



SUMMARY

- Validated measurement of transconductance with the full module with a single pixel measurement
 - $g_m = 62.958 \mu\text{S}$ compared to $g_m = 63.10 \mu\text{S}$
- Measurement of $g_q = 735.20 \text{ pA/e-}$
- Next step: Characterize mini matrices of new DEPFET PXD13 technology
- Test of the charge gain and matching with the expectations

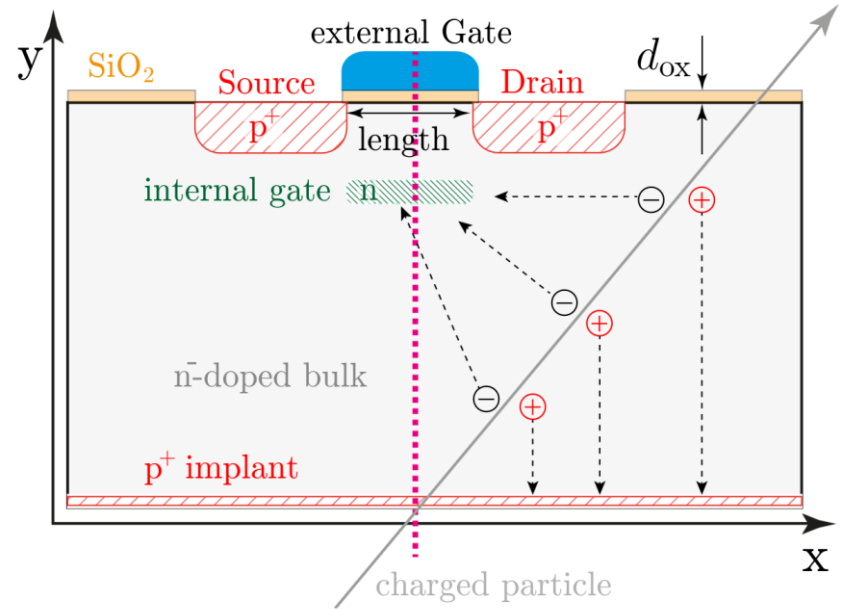


THANK YOU!

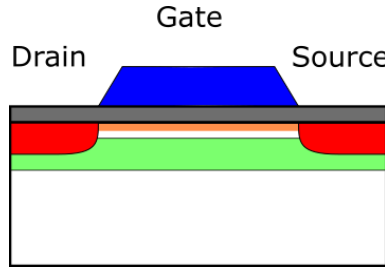
BACKUP

DEPFET WORKING PRINCIPLE

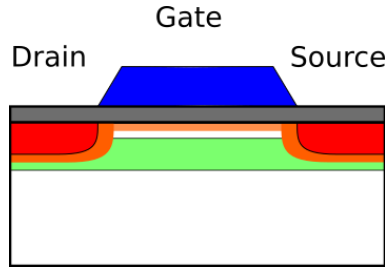
- **D**epleted n-doped silicon bulk with **P**-channel **FET**
- Small highly doped n-implant below the p-channel (internal gate)
- Created electrons drift to the internal gate
- Changes in potential in p-channel
 - Transistor channel current depends on charge deposited in the internal gate
 - Excellent signal-to-noise ratio of about 40



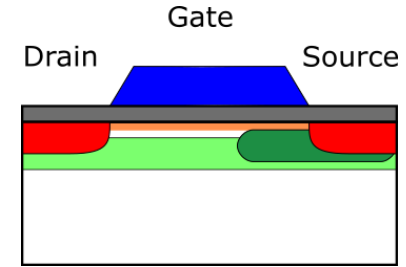
PXD13 TECHNOLOGY



- Standard
- About 500pA/e- expected



- HALO implant
- Lightly doped area around implants
- Smoother field configuration
- Higher charge gain (10%)

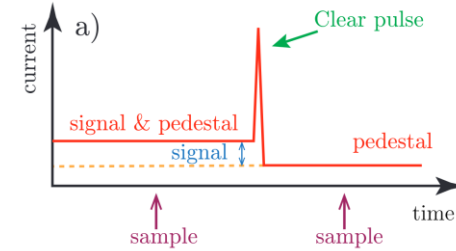
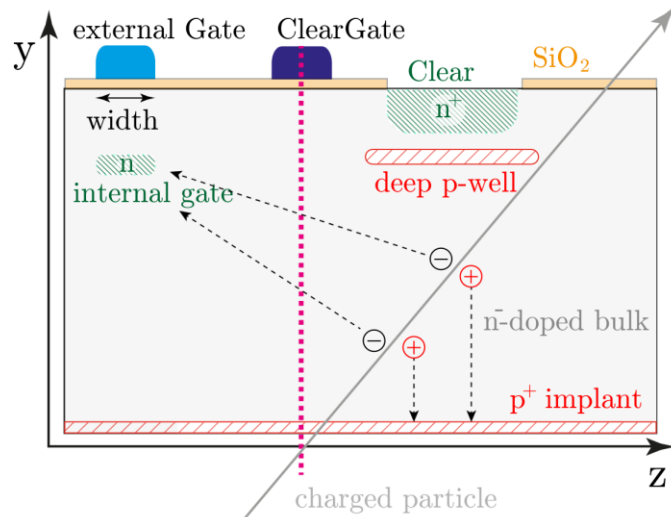


- Deep-n implant on source side
- Localized internal gate to part of the channel
- Expected charge gain of about 1.3nA/e-

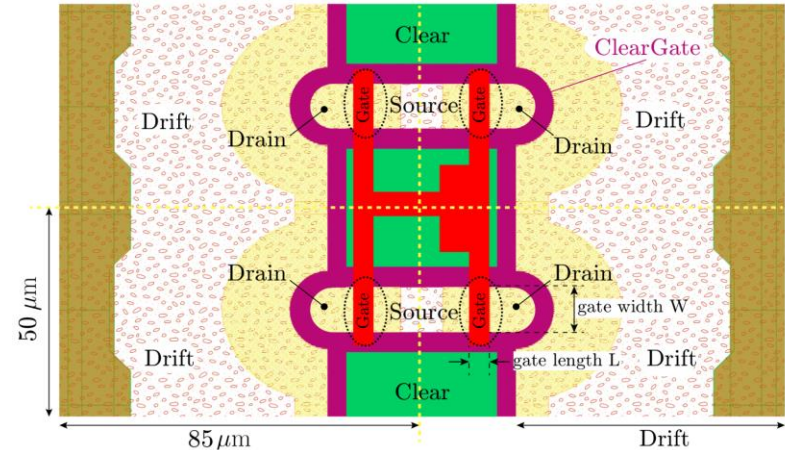
Illustrations: Alexander Bähr, HLL

DEPFET WORKING PRINCIPLE

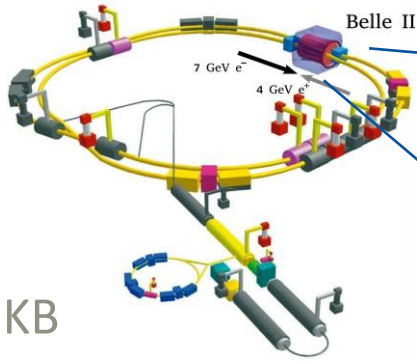
- Clear implant allows for emptying of the internal gate
- Switchers turn the clear process on and off, a p-well shields the clear implant
- Drift field guides the electrons to the internal gate



- Four pixels share the implants



SUPERKEKB AND BELLE II

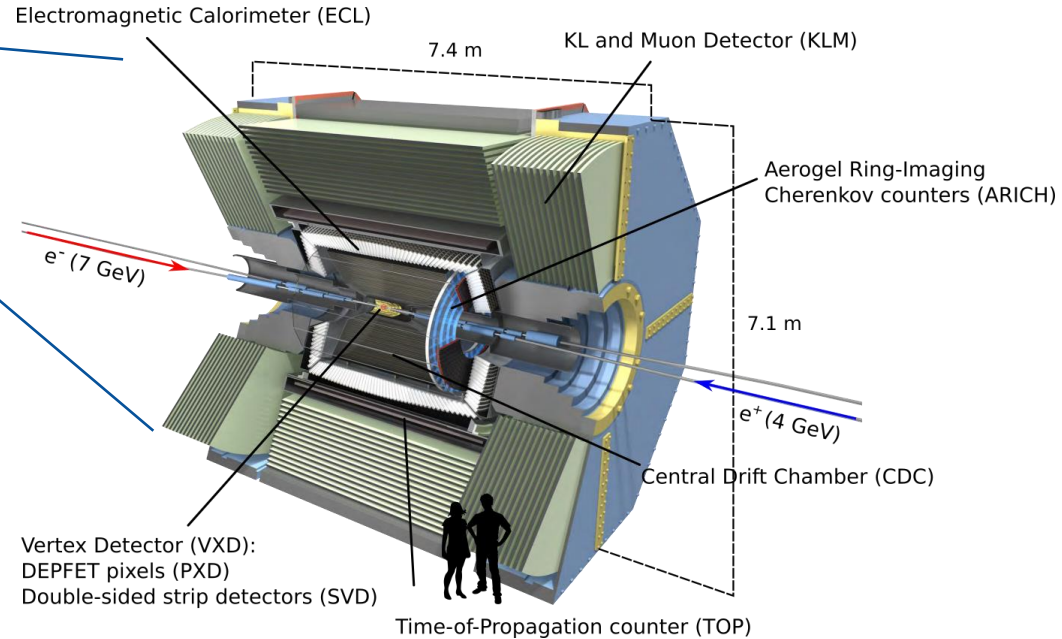


SUPERKEKB

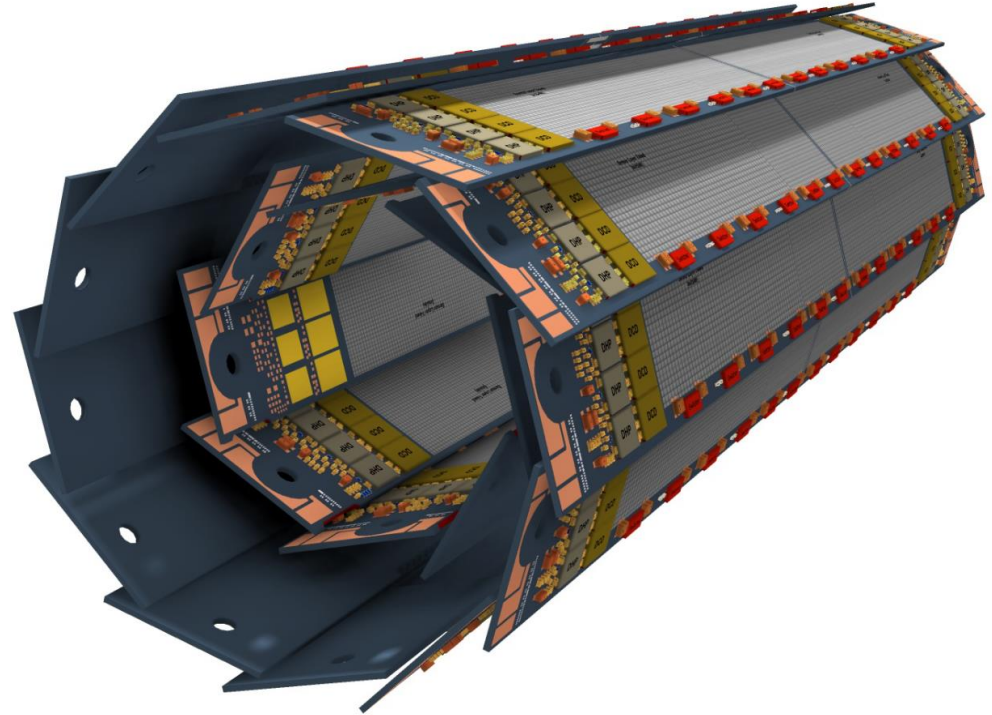
- Asymmetric e^+e^- collider
- Peak luminosity $L = 4.7 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$
- $E_{\text{CM}} = 10.58 \text{ GeV}$

BELLE II

- Reconstruction of B-Meson decays



- Most inner detector (14mm and 22mm to interaction point)
- Angular acceptance 17° to 150°
- Consists of 8 inner and 12 outer ladders
 - Each module combines a forward and a backward module
- Ring structure with overlap allows 3D-track-reconstruction for vertexing
- Material budget about $0.2\%X_0$ per ladder
 - Silicon only $0.05\%X_0$ per ladder



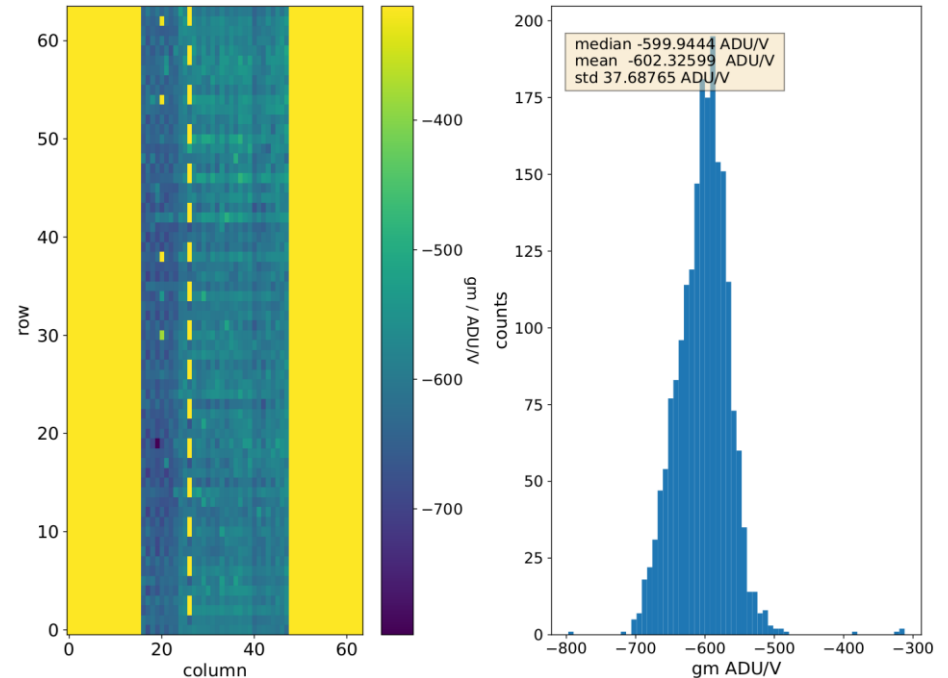
IV-CURVE DEPFET

- Full formula with influence of internal gate:

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} \left(U_{Gate} + \frac{Q}{C_{gate}} - U_{th} \right)^2 (1 + \lambda U_D)$$

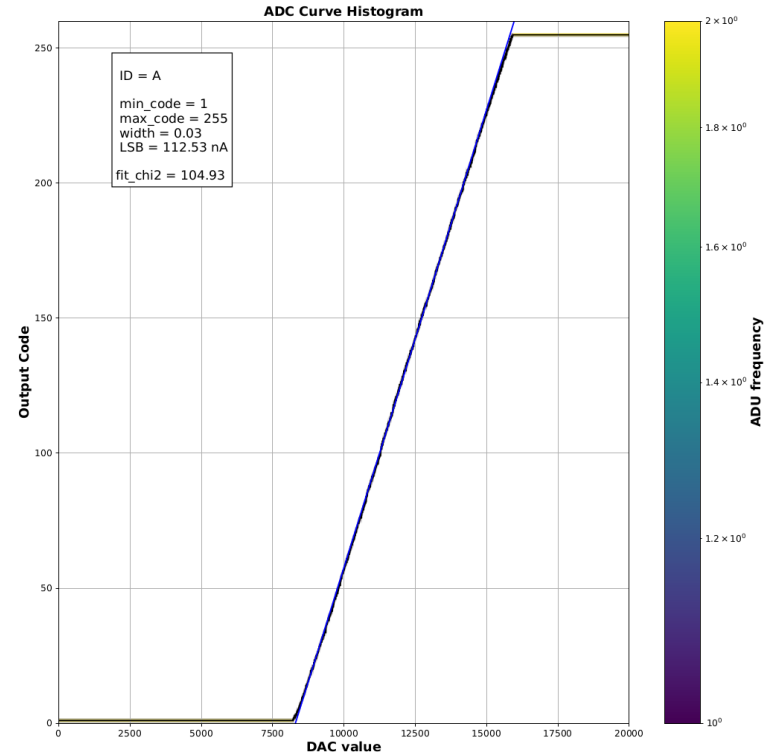
DETERMINATION OF TRANSCONDUCTANCE

- Transconductance in ADU/V directly from the IV-curve
- Calibration of DCD to get ADU to A



DETERMINATION OF TRANSCONDUCTANCE

- Calibration of DCD to get ADU to A



DETERMINATION OF INTERNAL AMPLIFICATION

- Average energy for the creation of an electron hole pair
- Known source energy
- Calibrated DCD to convert ADU into A
- ADU value from spectrum fit

$$g_q = \frac{\mu_{\text{fit}}}{E_{K_\alpha}^{\text{Cd109}}} \cdot \frac{1}{\text{DCD gain}} \cdot \langle E_{eh} \rangle$$

$$[g_q] = \frac{\text{ADU}}{\text{eV}} \cdot \frac{\text{nA}}{\text{ADU}} \cdot \frac{\text{eV}}{e^-} = \frac{\text{nA}}{e^-}$$

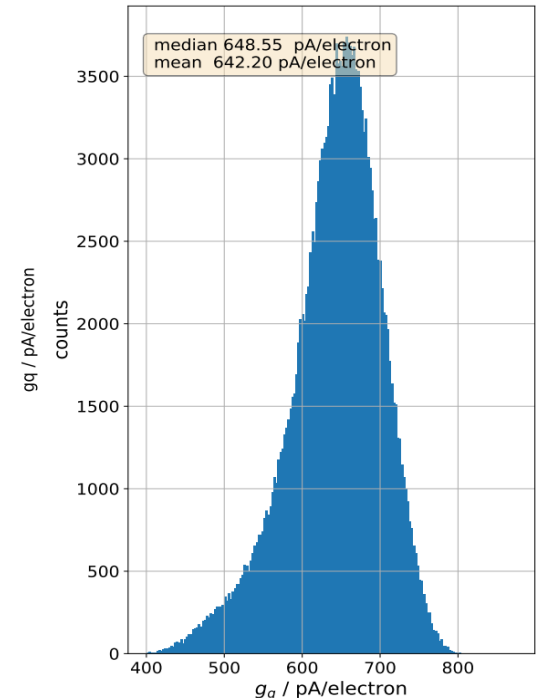
G_Q MEASURED FOR DIFFERENT MODULES

- Different results for different modules
- All measurements performed with $V_{gate} = 2.1$ V
 - No adjustment of Source current per pixel (working point)
 - Results should be taken with caution

Larissa v. Jasienicki

	W67_IB	W57_IB	W60_OF1
median g_q / $\mu\text{A}/\text{electron}$	517.40	648.55	743.91
std(g_q)/ $\mu\text{A}/\text{electron}$	49.96	59.52	62.35

Table 8.5: Median internal amplification g_q for different modules.



- Potential distribution

