New Semiconductor Laboratory of the Max-Planck-Society at Garching | Germany





Super-g_q DePFET Put to the Test

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 - Clear, Clear Gate, Backside/BIGR
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EXPERIMENTAL SETUP

Device under test



Top view of Hybrid-PCB

Left view

Device Layout:

- ✤ 64x64 matrix
- ✤ 130 µm pixel size
- ✤ 3.5 µm gate length
- ✤ 20 µm gate width
- ✤ 450 µm thickness



Device Operation:

- Rolling shutter mode
- Integration time $1 \ \mu s$
- ✤ Shaping time 6.3 µs
- ✤ Frame rate 13 ms
- ✤ Exposure time 12.5 ms



Zoom on DePFET Matrix



EXPERIMENTAL SETUP Instrumentation



Opened cooling plates and detached Hybrid-PCB

Zoom on entrance window (center) of the installed Hybrid-PCB

Open vacuum chamber with installed DUT ready for Fe55 energy resolution measurement



EXPERIMENTAL SETUP Instrumentation



Power supplies beneath the table, Vacuum pump top right, Cryo-Cooler top left.



Center: PCB-Stack of XU1, MSM, MSMA and flex cable.



EXPERIMENTAL SETUP Calibration





Super-g_q technology (Backside sweep)





Super-g_q technology (Clear sweep)

GainMap_Mean vs Clear Voltage

at 233K, Fe55 | for two Source Voltages

CalibNoiseMap_Mean vs Clear Volta

at 233K, Fe55 | for two Source Voltages





Super-g_q technology (Clear Gate sweep)





Super-g_q technology (Interim Summary)

=> Clear = 400 mV greater than Source => Clear Gate = 600 mV less than Source => Back/BIGR = -120 V



Super-gq technology (Gate & Source sweep)





Super-g_q technology (Gate & Source sweep)





GAIN AND NOISE PERFORMANCE

Super-g_q technology (GA=5.8V, SC=5V => \sim 100µA/pix)



• Gain

- ✤ 1.887 [ADU/eV]
- ✤ 0.483 [nA/eV]
- * 1.77 [nA/e^{-}] (charge gain g_q)

• Noise

- ♦ Mean: 10.72 (1σ: 0.86) [e⁻ ENC]
- Mean: 75.71 (1σ: 6.14) [ADU]



GAIN AND NOISE PERFORMANCE

Super- g_q technology ((GA=4V, SC=4.5V => ~ 281µA/pix || good Noise)



• Gain

- ✤ 1.851 [ADU/eV]
- ✤ 0.474 [nA/eV]
- ♦ 1.74 $[nA/e^-]$ (charge gain g_q)

• Noise

Mean: 4.60 (1σ: 0.48) [e⁻ ENC]
Mean: 31.51 (1σ: 3.33) [ADU]



GAIN AND NOISE PERFORMANCE

Super- g_q technology ((GA=7.6V, SC=7.8V => ~ 281µA/pix || good Gain)



• Gain

- ✤ 2.273 [ADU/eV]
- ✤ 0.581 [nA/eV]
- * 2.129 [nA/e⁻] (charge gain g_q)

Noise

Mean: 6.30 (1σ: 6.54) [e⁻ ENC]
Mean: 53.77 (1σ: 44.08) [ADU]



GAIN AND NOISE PERFORMANCE Standard technology (GA=5.8V, SC=5V => ~100µA/pix)



• Gain

- ✤ 0.857 [ADU/eV]
- ✤ 0.210 [nA/eV]
- ♦ 0.769 [nA/e^{-}] charge gain (g_q)

• Noise

- ✤ Mean: 3.50 [e⁻ ENC]
- ✤ Mean: 22.40 [ADU]



COMPARISON TO STANDARD TECHNOLOGY

	Standard @ 100µA/pix	Super-g _q @ 100µA/pix	Super-g _q good Noise	Super-g _q good Gain
Charge Gain [nA/e ⁻]	0.769	1.77 (x 2.3)	1.74 (x 2.26)	2.13 (x 2.77)
Noise Mean [e ⁻ ENC]	3.5	10.72	4.6	6.3
Energy Res. (all events) [eV]	134.36	188.53	139.53	166.31



SUMMARY

- ✓ Overall successful super-g_q production
- ✓ Principal functionality could be confirmed
- ✓ Charge gain increase by a factor of 2.77
 - \checkmark In good agreement with simulation

NEXT STEPS

- > Thorough investigation of noise performance
 - Thermal, shot and 1/f noise
- Rectification of simulation deviations
- \succ Higher gain @ 5.9 keV, Noise density



MANY THANKS FOR YOUR INTEREST

Reference:

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 A. Bähr *et al.*, "Advanced DePFET concepts: super gq DePFET,". doi: <u>10.1117/12.2562484</u>.
 M. Porro *et al.*, "VERITAS 2.0 a multi-channel readout ASIC suitable for the DEPFET arrays of the WFI for Athena,". doi: <u>10.1117/12.2056097</u>.

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BACKUP



INTRODUCTION

The DePFET standard technology







INTRODUCTION

The DePFET working principle





THE SUPER-G_Q TECHNOLOGY^[2]

Doping concentration p-channel cut

Super-g_q DePFET:

- Deep n-implant + strip implant
- Greater design freedom
- Localized steering effect
- Mitigating impact ionization noise



Standard-DePFET:

- Deep n-implant
- > Internal gate defined by gate oxide size
- Steering effect over hole p-channel









TCAD SIMULATIONS

Device simulation results





Super-g_q technology (Backside sweep)

AllResolution_Fwhm vs BACK_Voltage

at 233K, Fe55





Super-g_q technology (Clear Gate sweep)

AllResolution_Fwhm vs CG_Voltage

at 233K, Fe55





Super-g_q technology (Clear Gate sweep)

GainMap_Mean vs Clear Voltage

at 233K, Fe55 | for two Source Voltages

CalibNoiseMap_Mean vs Clear Volta

at 233K, Fe55 | for two Source Voltages





Super-g_q technology (Clear Gate sweep)





Super-g_q technology (Clear Gate sweep)

Gate Bias = 5770 mV, Source Bias = 5V





CHARACTERIZATION Super-g_q technology (Gate & Source sweep)





Super-g_q technology (Gate & Source sweep)





ENERGY RESOLUTION FINDINGS Standard technology





NOISE, GAIN AND SPECTRUM Standard technology



• Gain

- ♦ 0.857 in [ADU/eV]
- ✤ 0.210 in [nA/eV]
- ♦ 0.769 in $[nA/e^-]$ charge gain (g_q)

• Noise

- ✤ Mean: 3.50 [e⁻ ENC]
- ✤ Mean: 22.40 [ADU]

preliminary

^{@ -30°}C



ENERGY RESOLUTION FINDINGS Super- g_q technology





NOISE, GAIN AND SPECTRUM Super-g_q technology



• Gain

- ✤ 2.219 in [ADU/eV]
- ◆ 0.567 in [nA/eV]
- ◆ 2.075 in [nA/e⁻] charge gain (g_q)
- > 2.7 times more than standard

• Noise

- ✤ Mean: 4.75 [e⁻ ENC]
- ✤ Mean: 39.10 [ADU]
- 2 times more than standard

@ -30°C

preliminary