



Studies on radiation hardness of DEPFET-like test structures

DPG Frühjahrstagung 2011

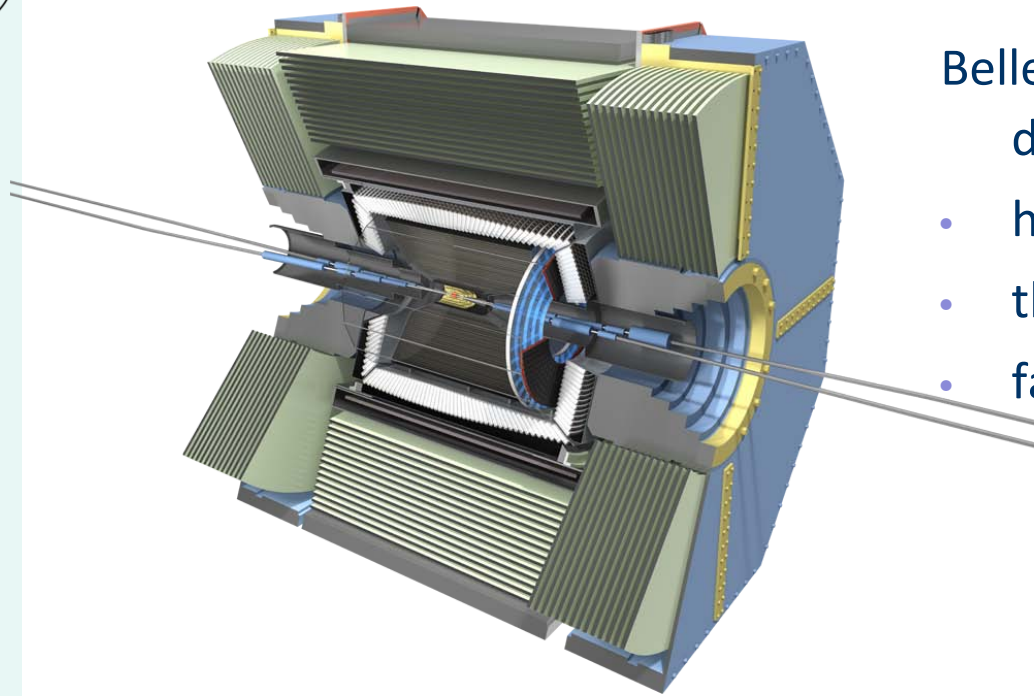
Karlsruhe

Andreas Ritter, Ladislav Andricek, Christian Koffmane, Hans-Günther Moser, Jelena Ninkovic,
Rainer Richter, Andreas Wassatsch - on behalf of the DEPFET-Collaboration





Motivation – Pixel Detector at Belle II

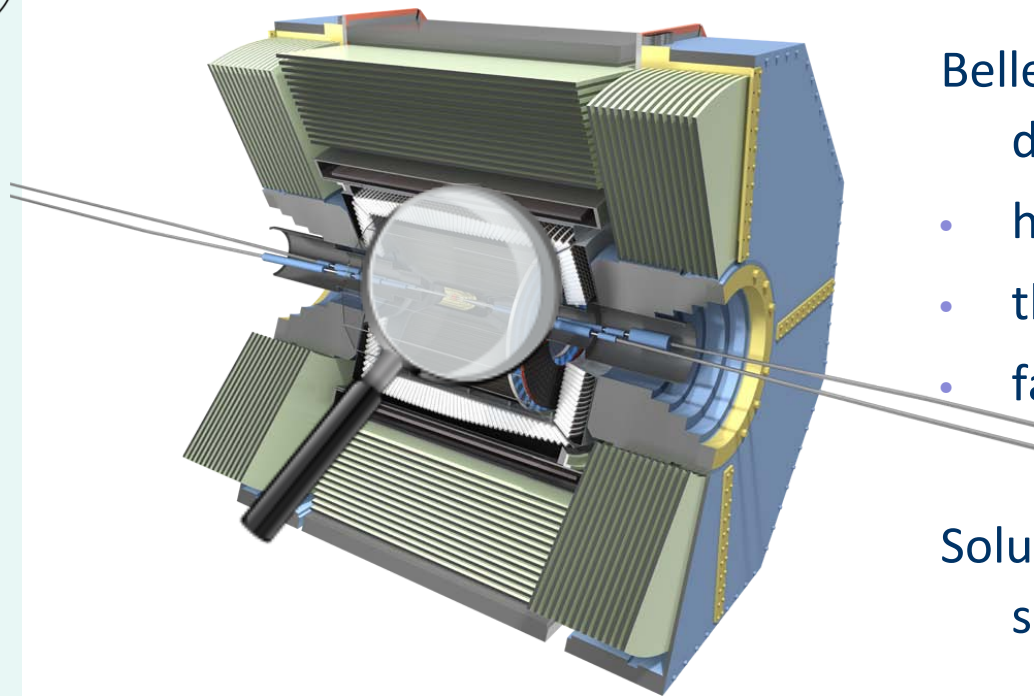


Belle II requirements for Vertex detector:

- high vertex resolution
- thin detector material
- fast readout and DAQ



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Solution: DEPFET pixels on thin silicon ($75\ \mu\text{m}$)

One Issue: Radiation Hardness in SiO_2

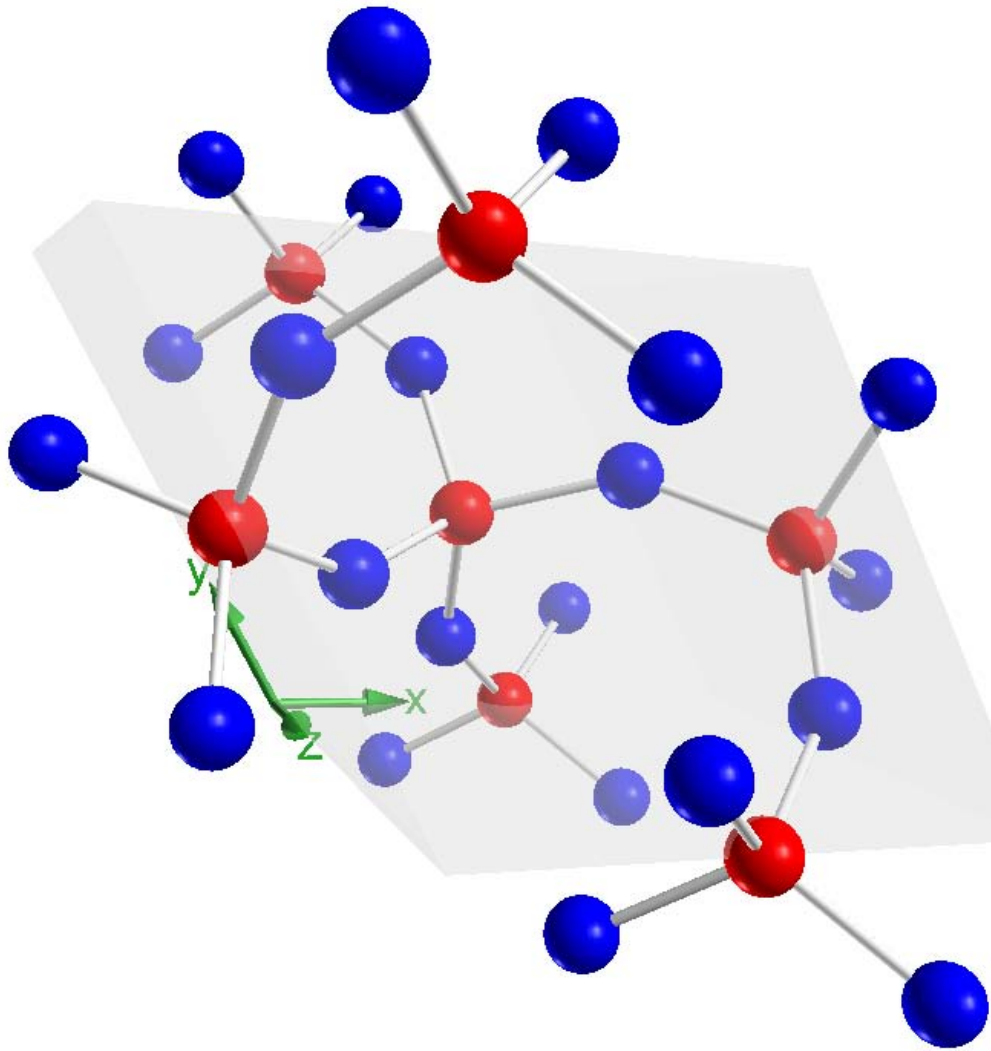
Sources:

- Touschek effect
- synchrotron radiation
- beam gas interaction





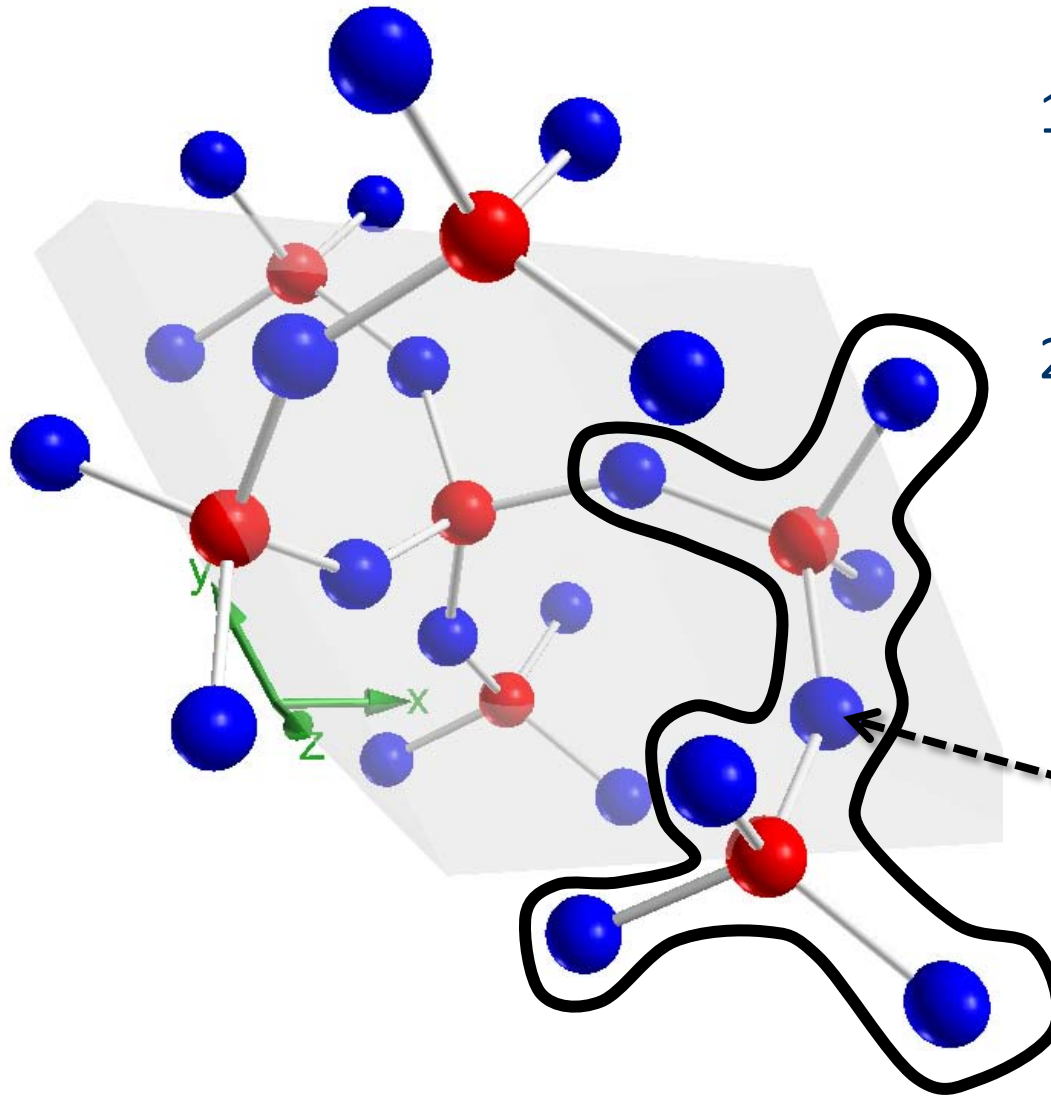
Silicon dioxide - Formation of radiation induced E' defect



1. SiO_2 crystal lattice near Si-SiO_2 suffers from lattice mismatch.



Silicon dioxide - Formation of radiation induced E' defect

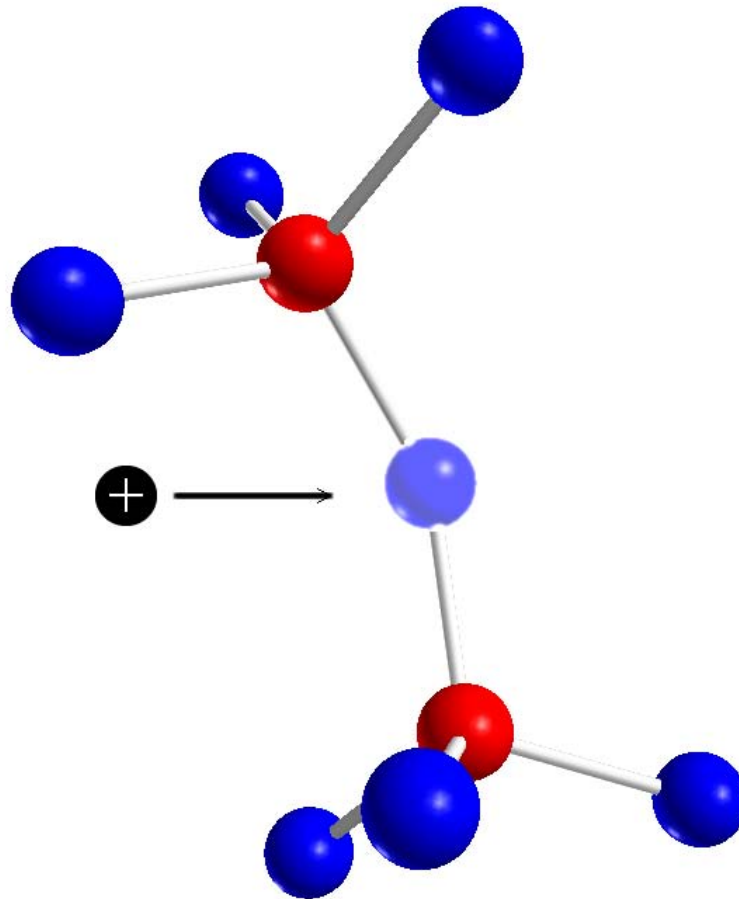


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2. Binding between two Si atoms is stretched and weak.

Oxygen vacancy
(precursor)



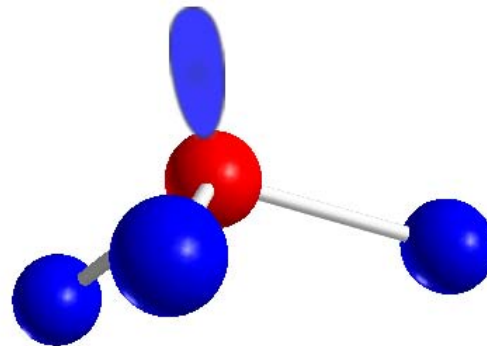
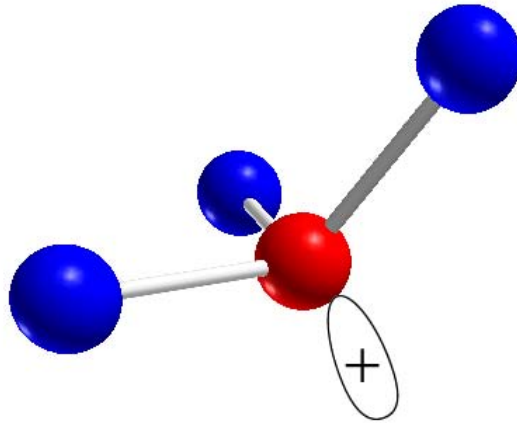
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3. Holes from e/h pairs (generated by ionizing radiation) travel to the interface...



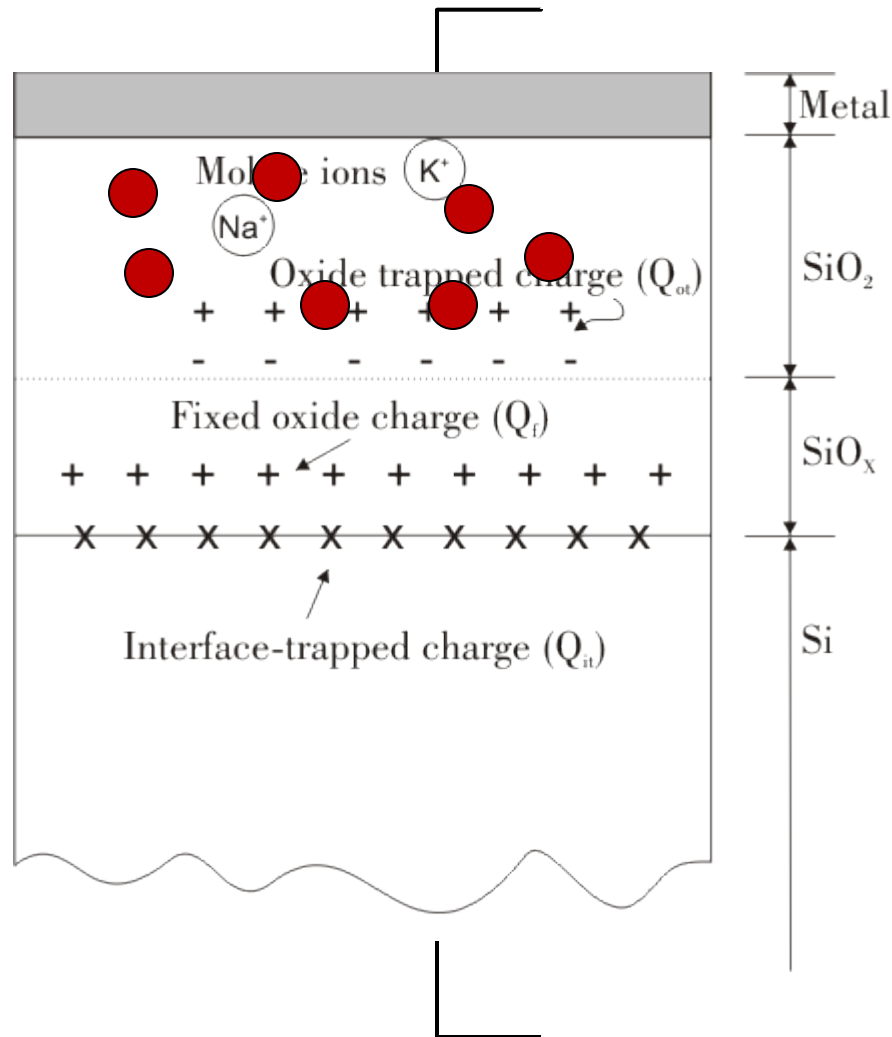
Silicon dioxide - Formation of radiation induced E' defect



1. SiO_2 crystal lattice near Si-SiO_2 suffers from lattice mismatch.
2. Binding between two Si atoms is stretched and weak.
3. Holes from e/h pairs (generated by ionizing radiation) travel to the interface...
4. ...and destroy the binding. One Si atoms remains in a positive charge state \rightarrow E' defect



Dependency of threshold shift



Amount of traps depend on:

- amount of precursors
- dose
- charge yield
- trapping probability

Important parameter:

$$V_{thshift} = \frac{Q_{ot}}{C_{ox}}$$

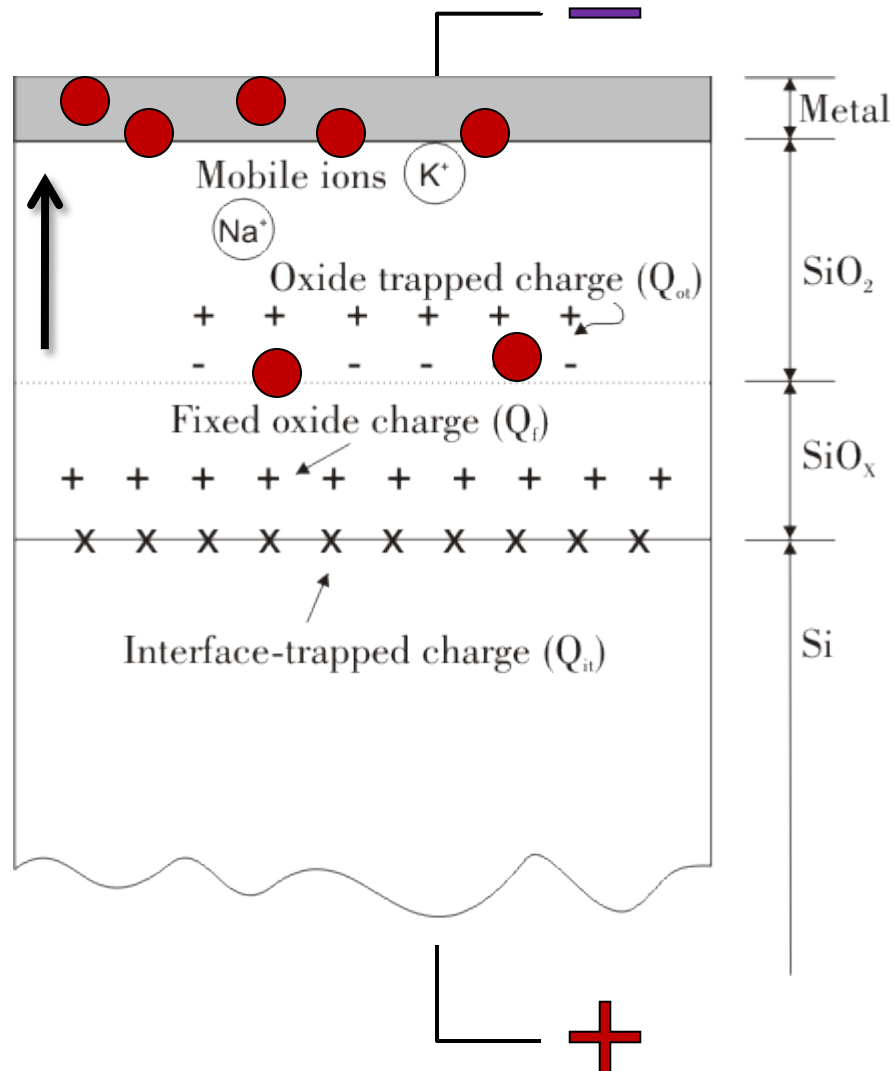
Improvement via:

1. C_{ox} bigger \rightarrow use **thinner** gate dielectrics

2. Avoid trapping of charge:
Voltage on gate influences charge yield and trapping



Dependency on gate voltage (negative)



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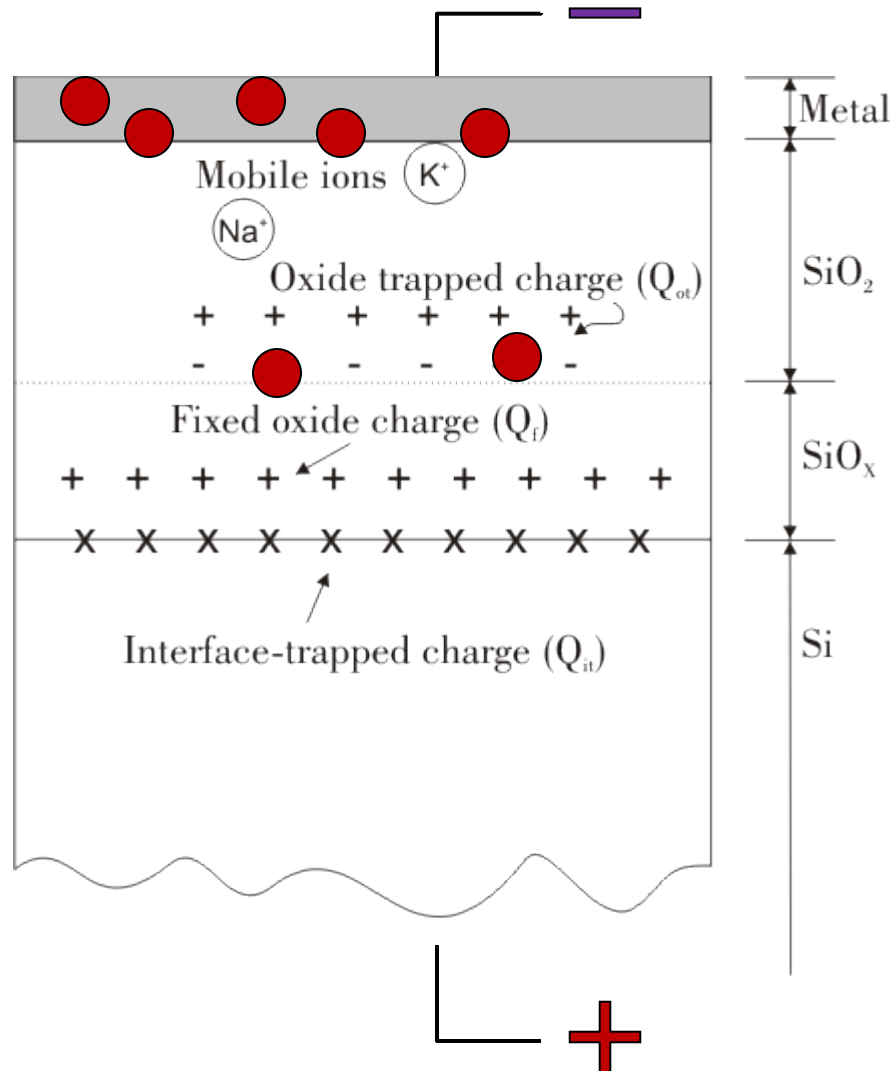
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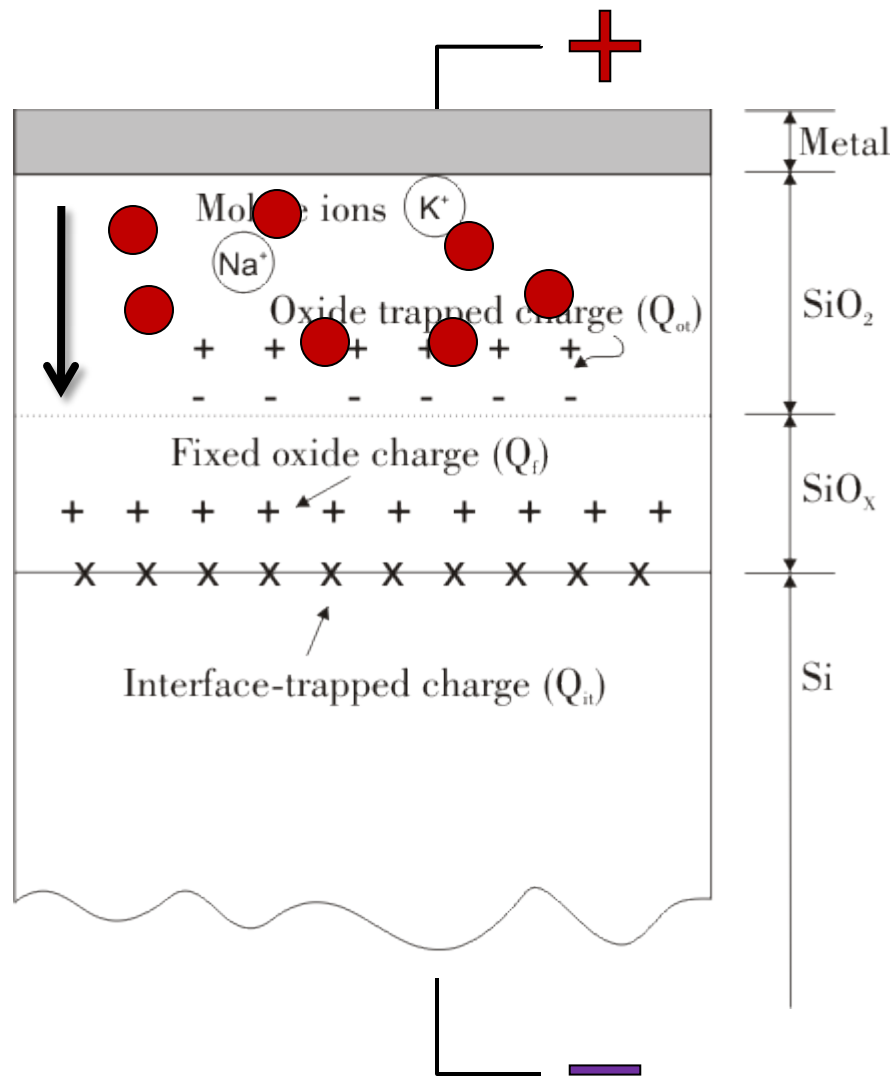
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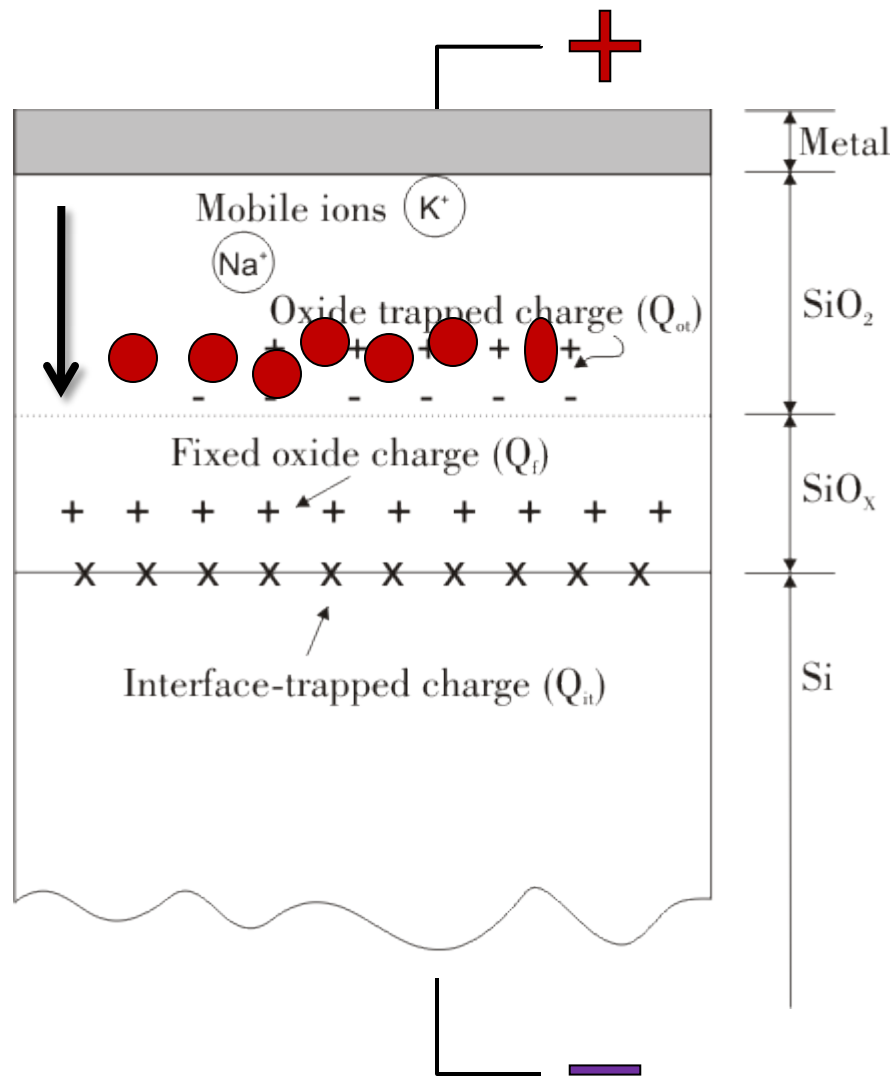
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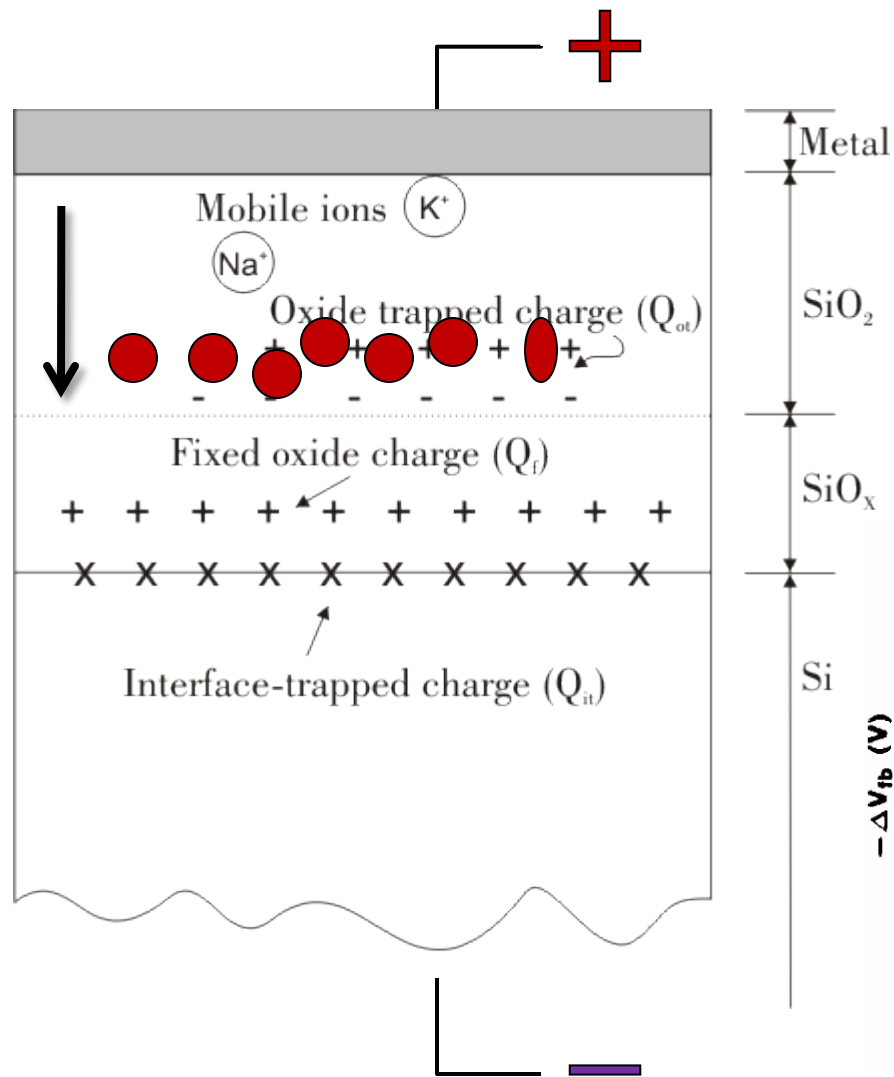
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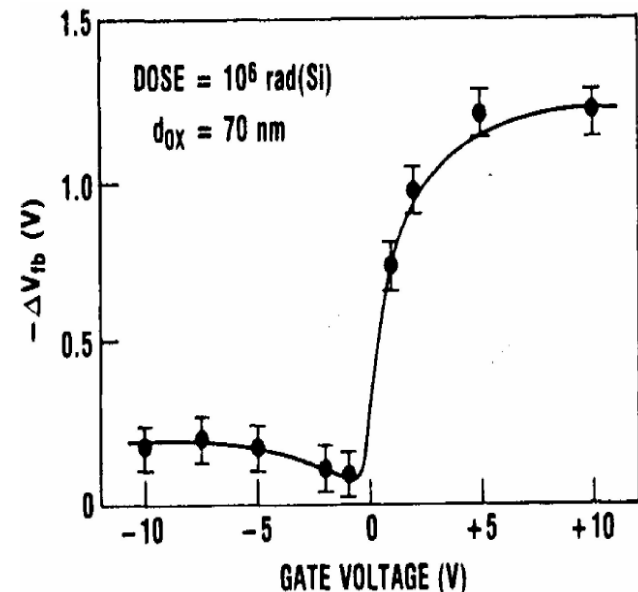


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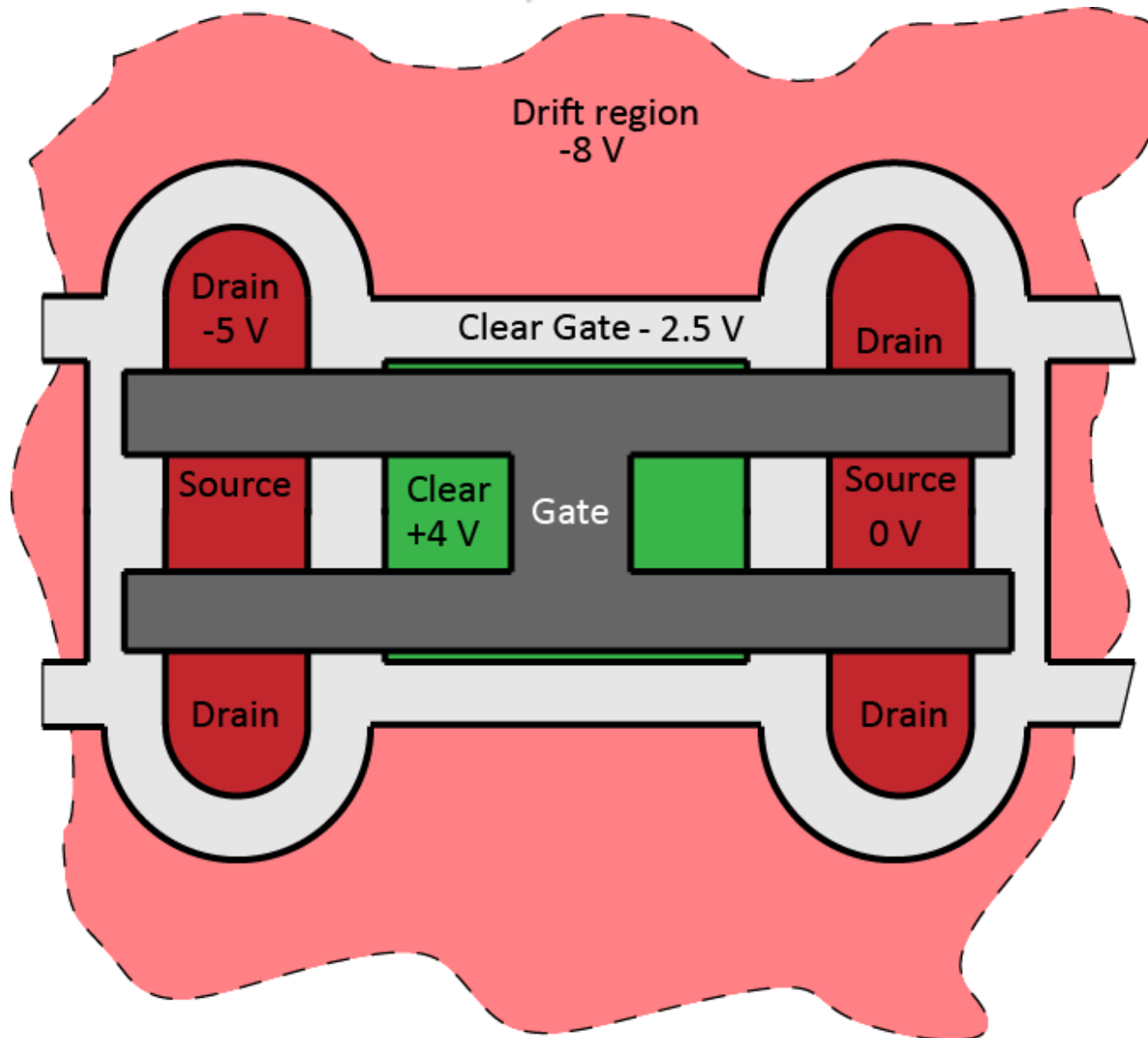
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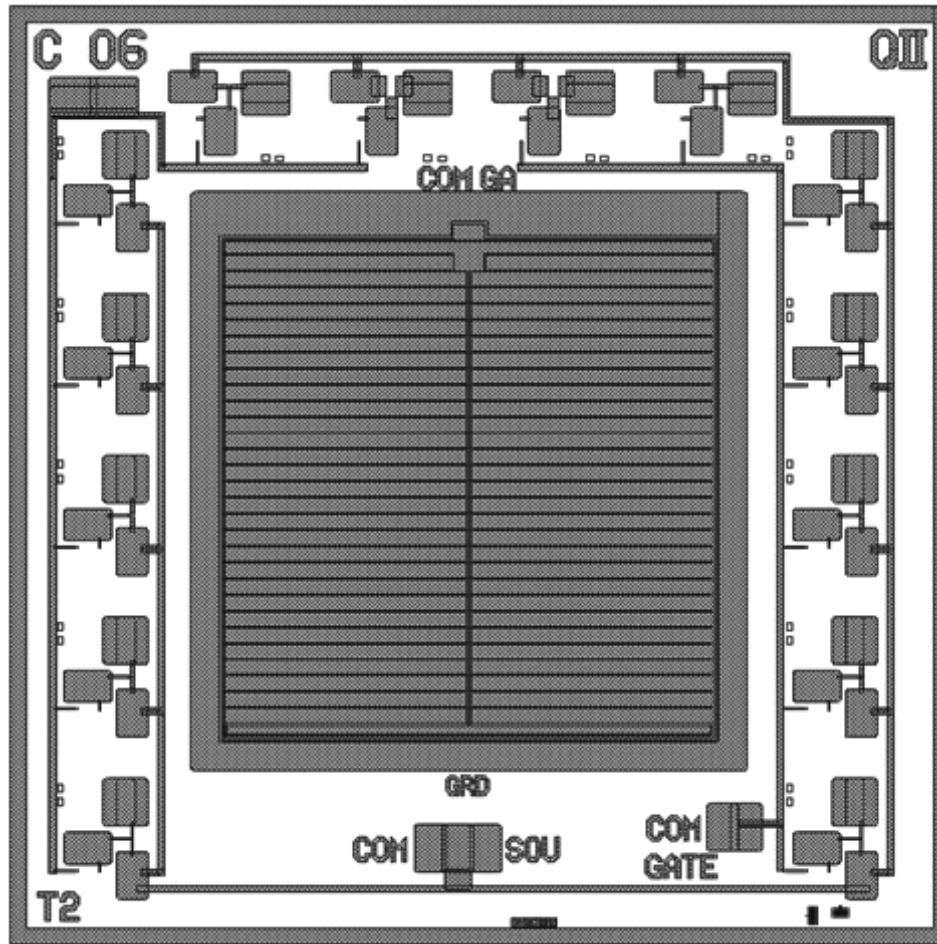
Ma/Dressendorfer

Why voltages on gates are important – Possible Layout of Belle II pixel matrix





Layout of thin oxide test devices

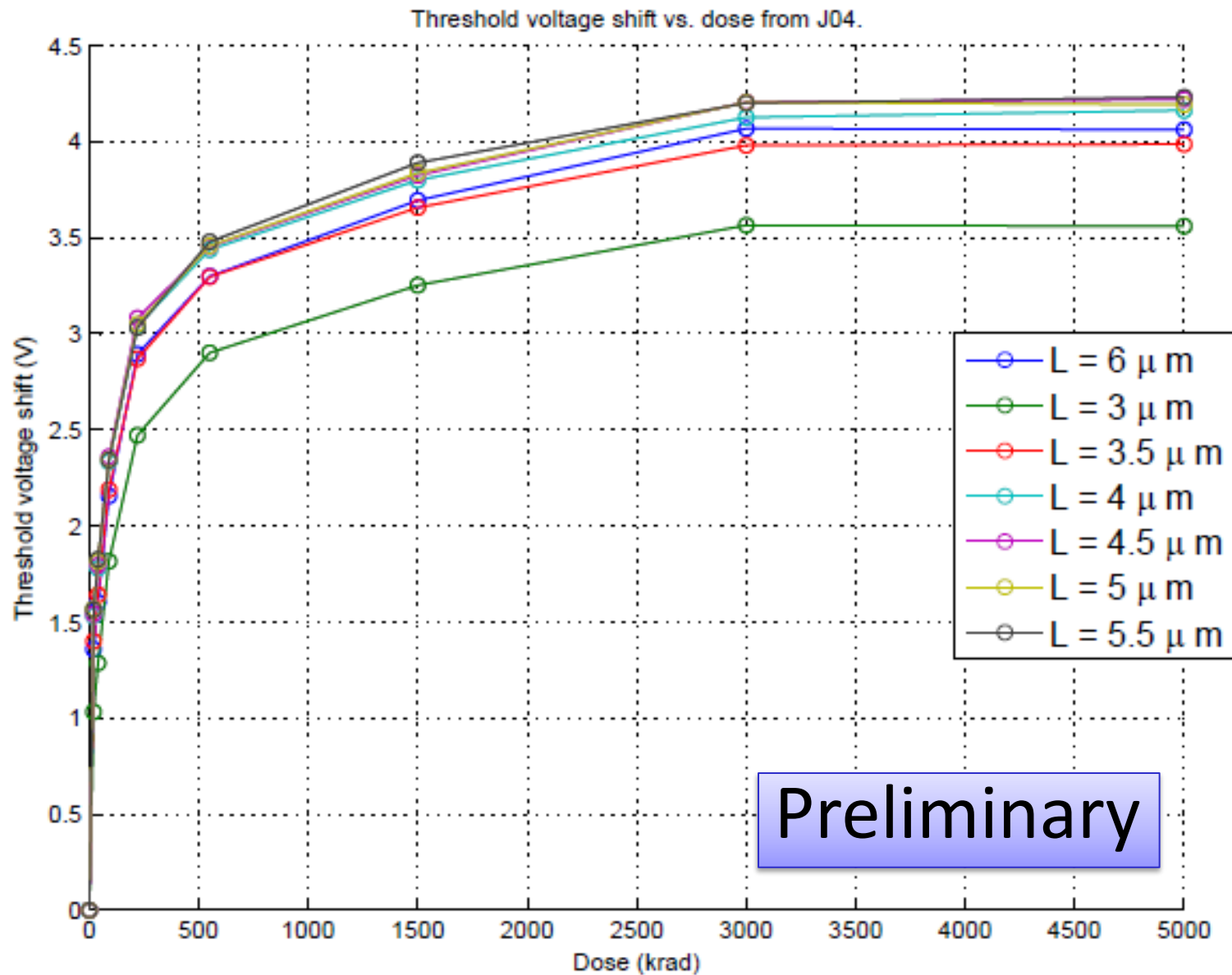


Characteristics of thin oxide structures:

- Central device: capacitor or gate controlled diode
- 14 transistors (=2x7), with diff. gate length and width
- Different doping profiles available

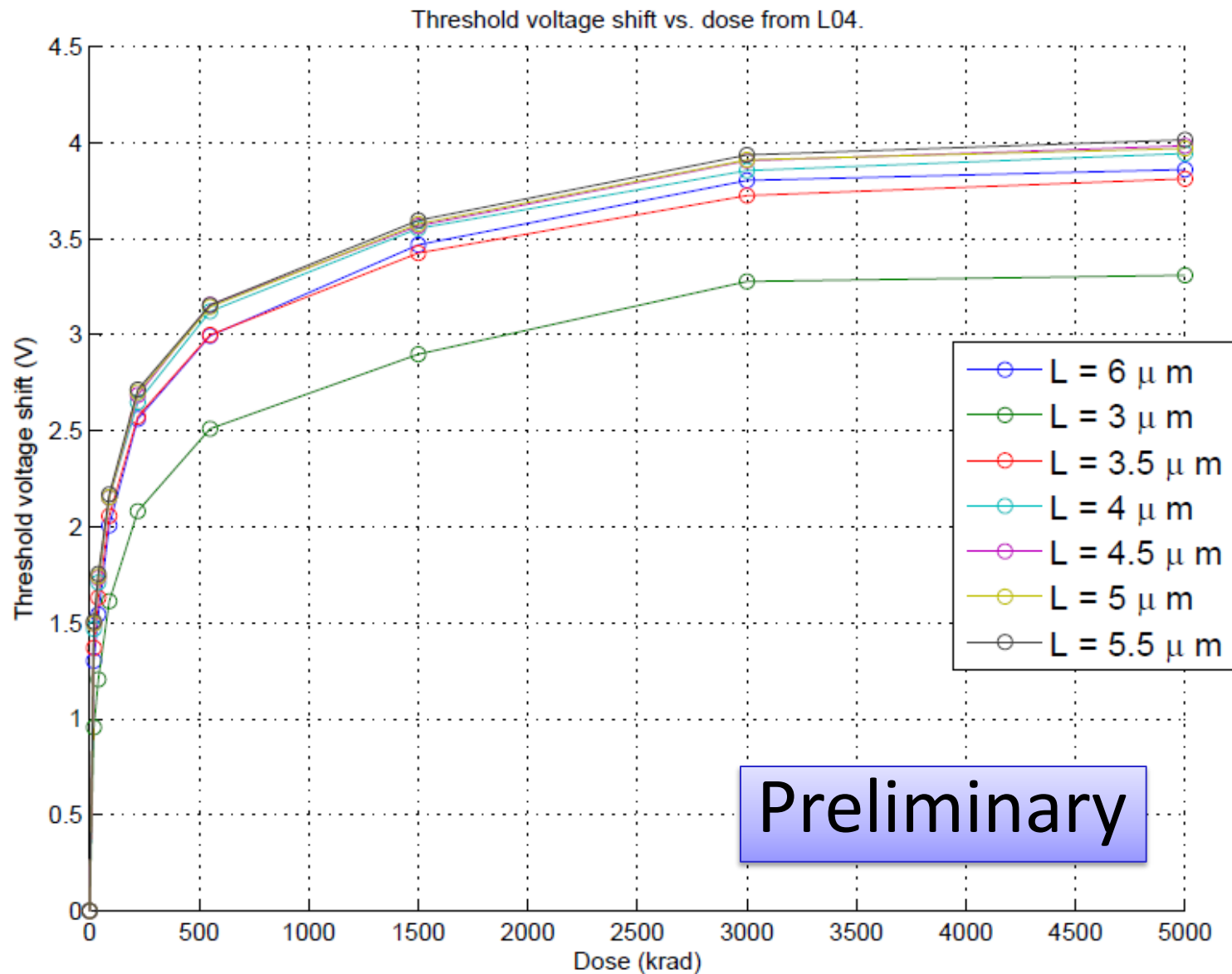


Clear Gate Results, -5 V during Irradiation



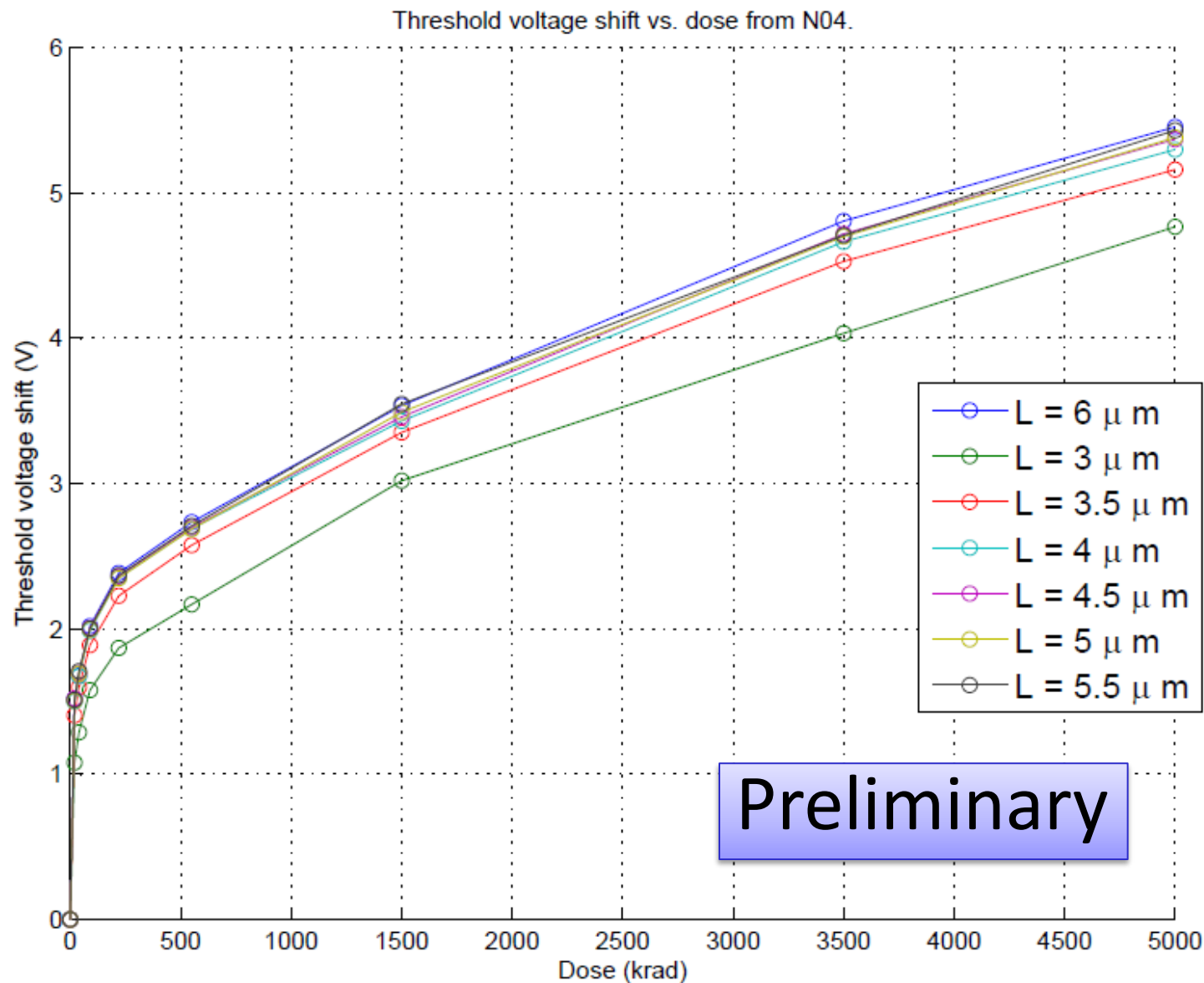


Clear Gate Results, -2.5 V during Irradiation



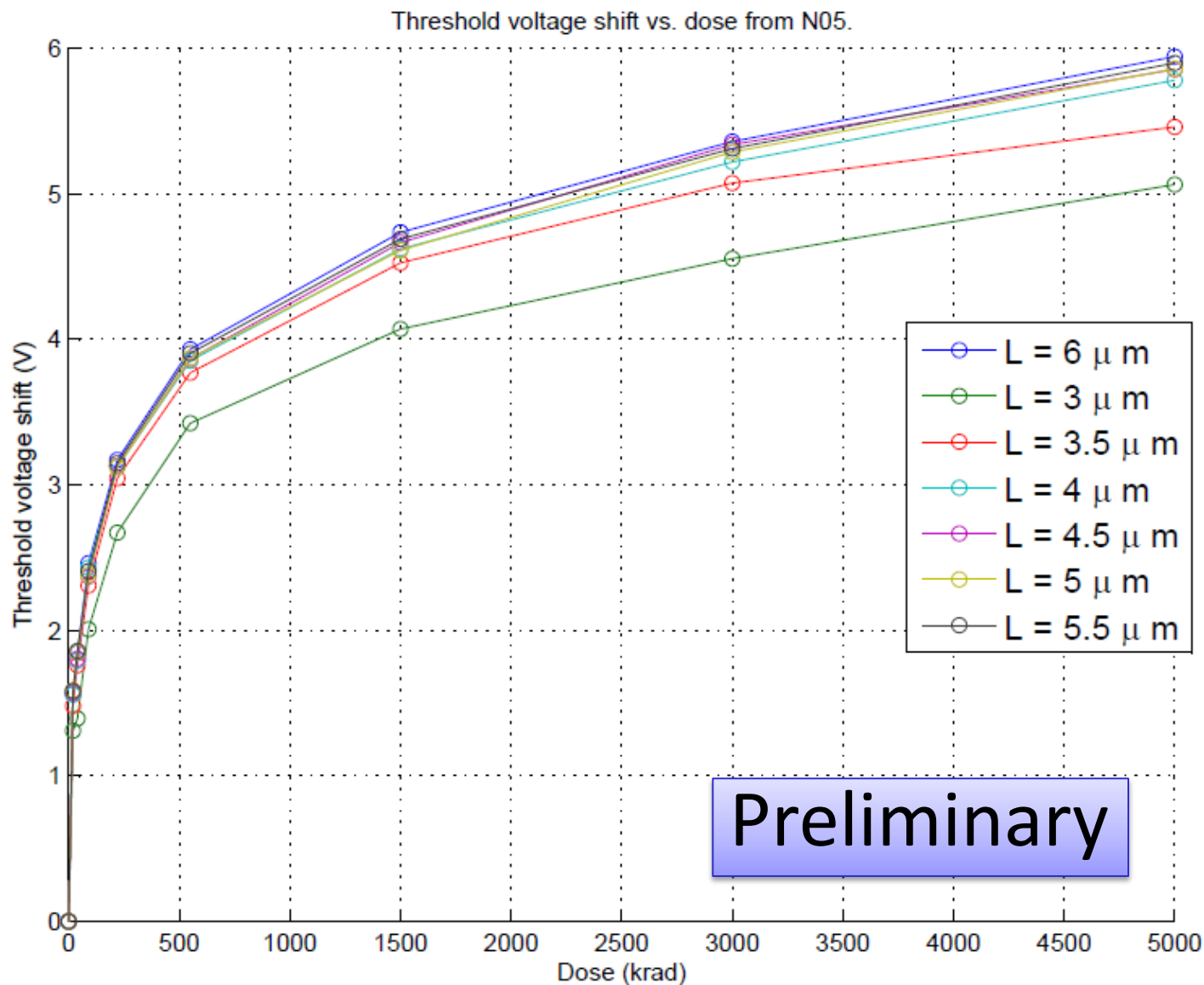


Clear Gate Results, 0 V during Irradiation



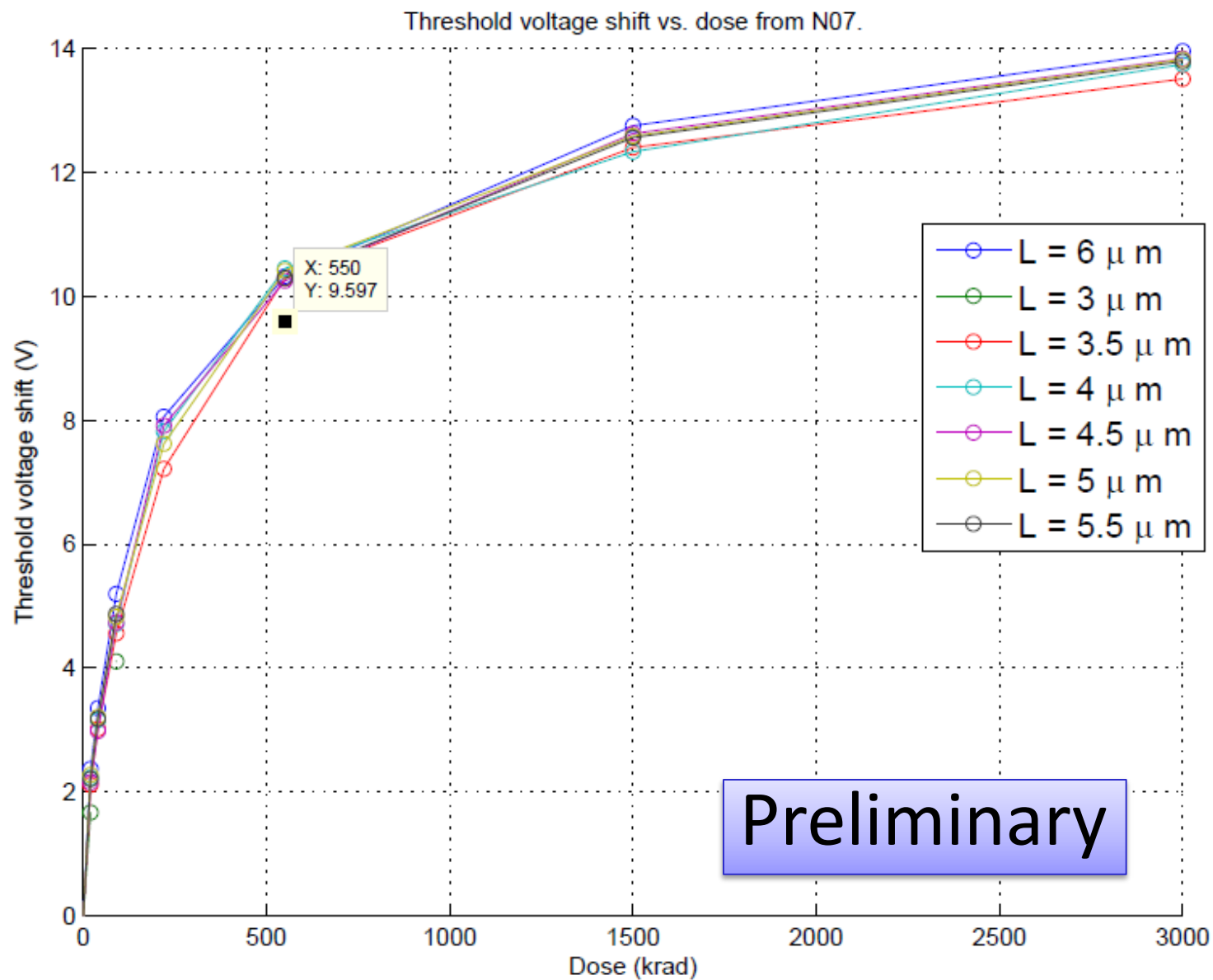


Clear Gate Results, +2.5 V during Irradiation



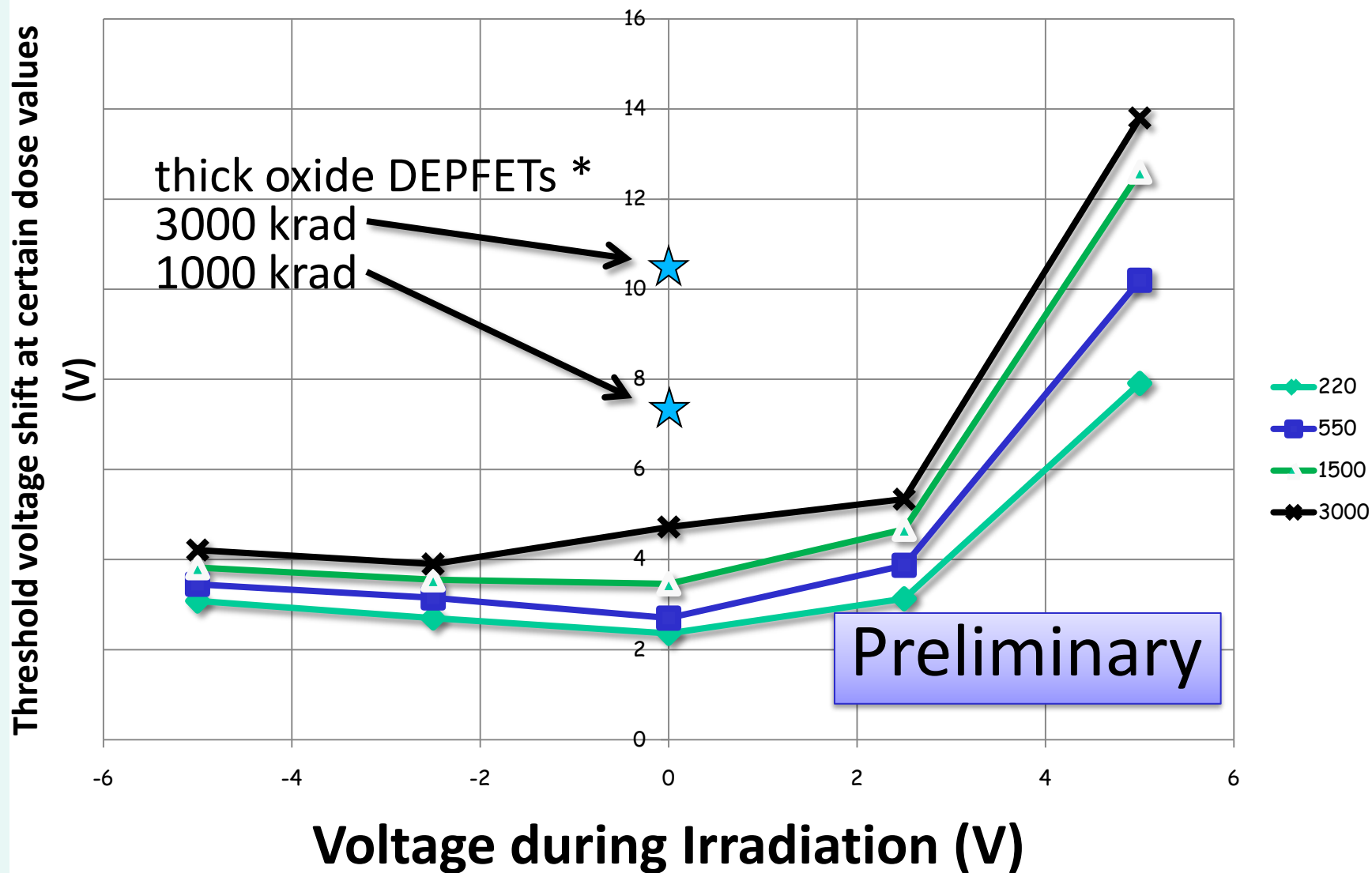


Clear Gate Results, +5 V during Irradiation





Change in threshold voltage shift due to certain Gate voltages



* measurements by Peter Müller



Comparison and summary

Thin oxides have proven to be a good candidate to reduce threshold shift (5 V shift with thinned oxide vs. 10.5 V at 3000 krad)

Only one gate voltage available, but different electric potential along pixels → Improve technology / adapt layout



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Thank you

Special thanks to Inst. f. Experimentelle Kernphysik from KIT for their x-ray tube



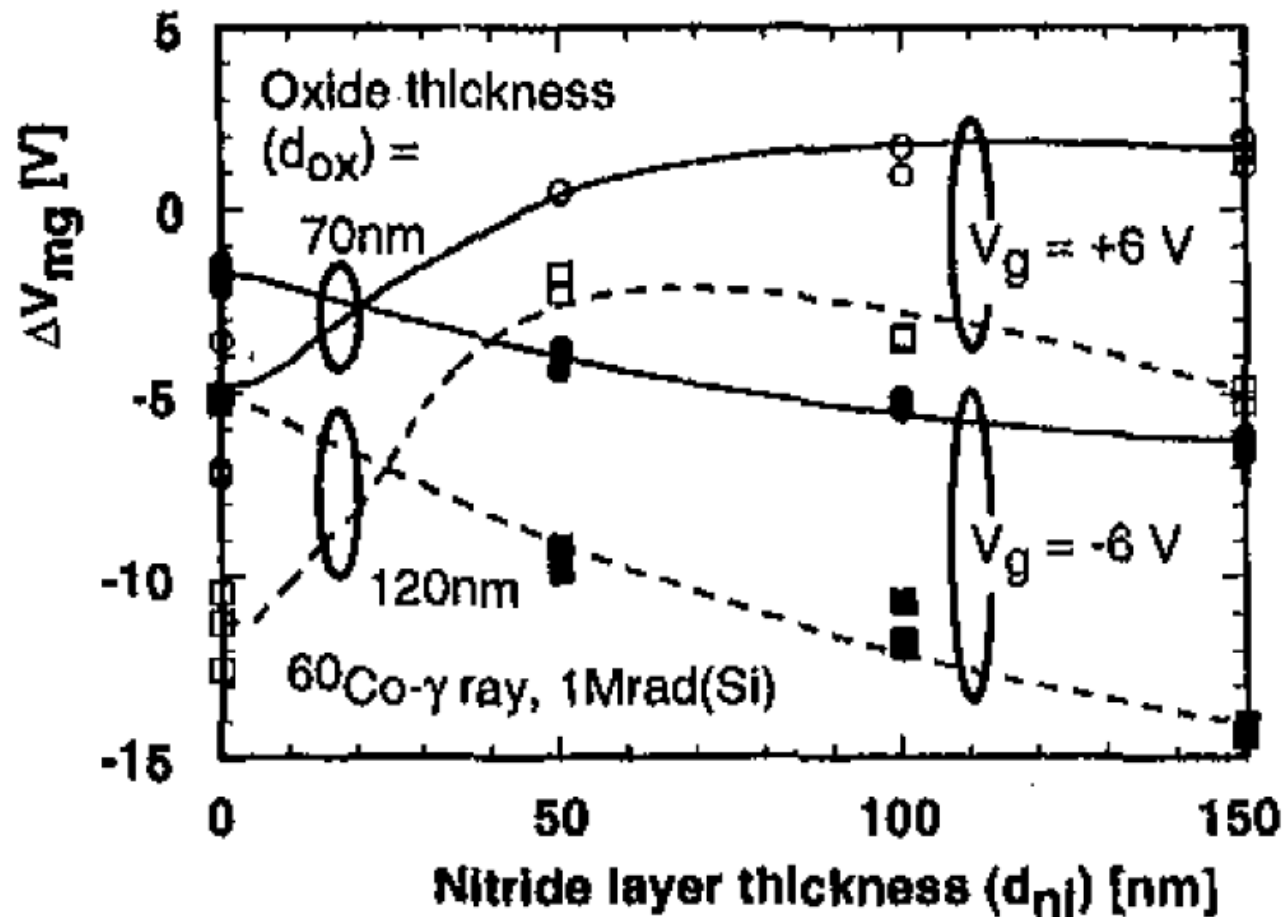
Backup



Thick nitride and Gate voltages

Thicker nitride could be a solution to the problem at hand.

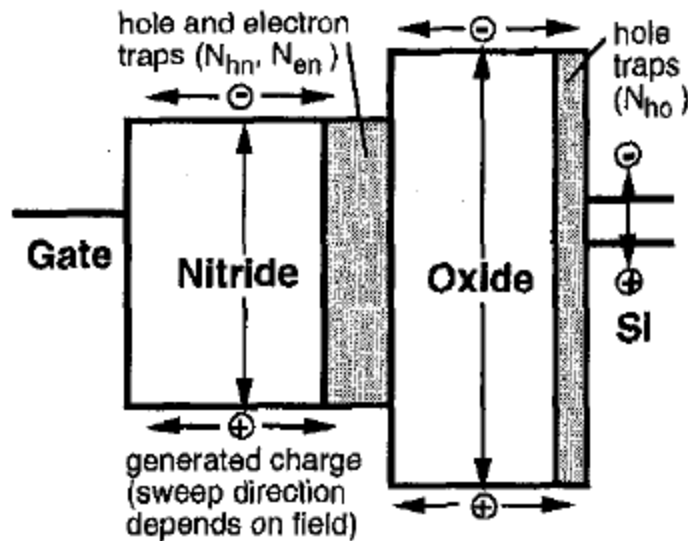
Up to now, only irradiations on diff. nitride thicknesses (TO chips) were conducted with zero gate voltages during irradiation.



Radiation-Induced Trapped Charge in Metal-Nitride-Oxide-Semiconductor Structure; Takahashi et. al.
IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOX 46, NO 6, DECEMBER 1999



Trapping in insulator layer



$+V_G$

1. Holes in oxide to Si-SiO₂ interface
2. Holes in Si₃N₄ and electrons from SiO₂ to N-O interface
3. Recombination rate in Si₃N₄ higher than in SiO₂ → more e⁻ trapped at N-O
4. Build-up of e⁻ reduces field in oxide → saturation

$-V_G$

Field always present

Thick Si₃N₄

→ Reduces field in ox → saturation