DPG Frühjahrstagung 2011 – T61.2
Electrical Simulation of a DEPFET Pixel Matrix

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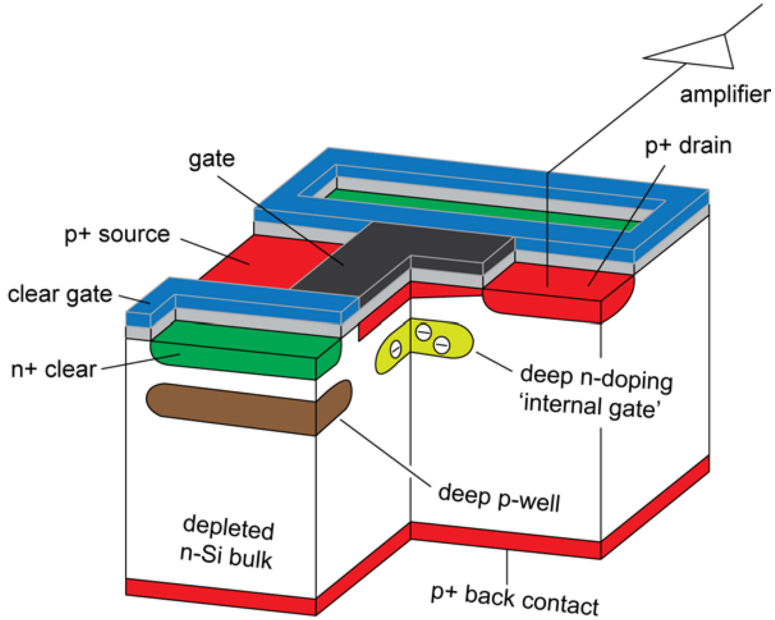
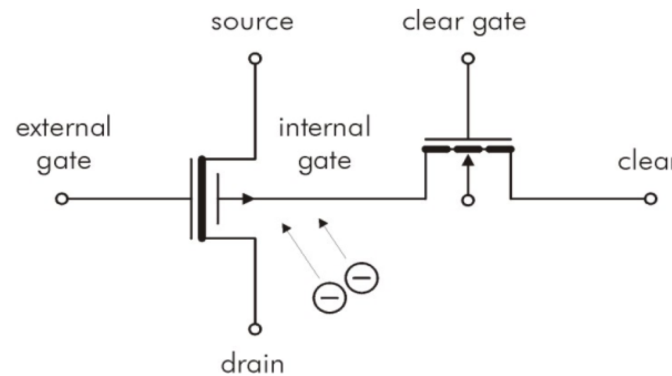
What’s a DEPFET Pixel?

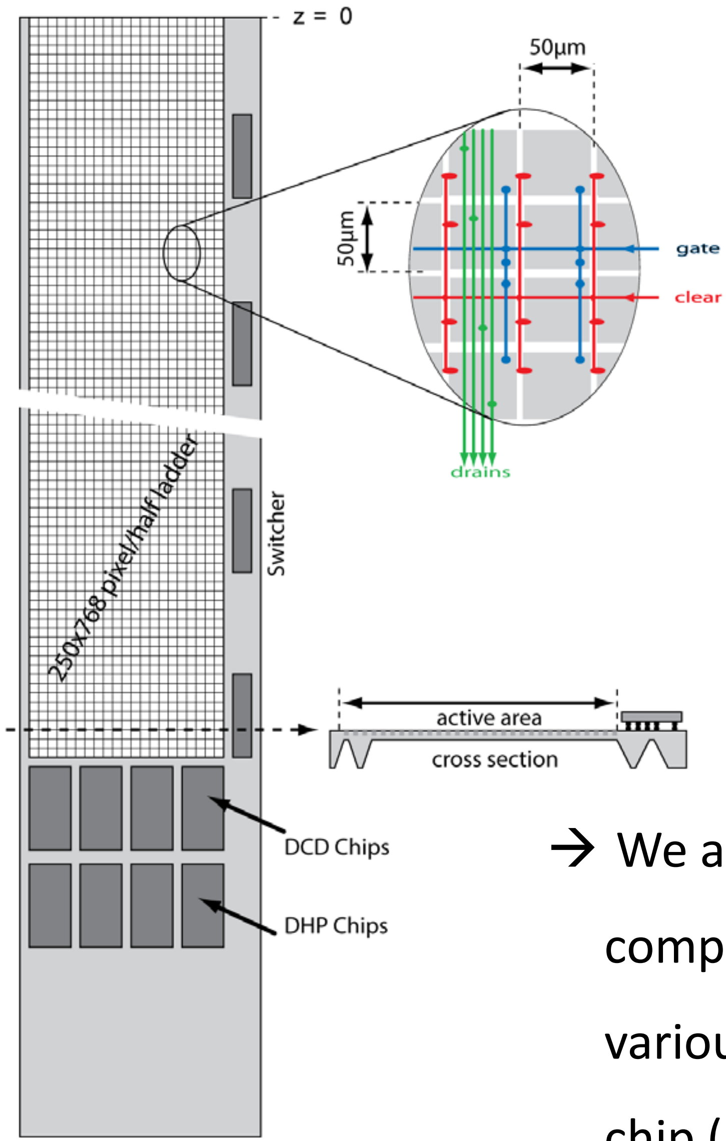


J. Kemmer & G. Lutz, 1987



- DEPFET is an acronym for depleted p-channel field effect transistor
- Collection of signal electrons within the internal gate
- Modulation of the FET current by the charge in the internal gate
- Fully depleted sensitive volume
- Charge collection in the transistor "off" state, read out on demand
- Clear contact to empty the internal gate

DEPFET Pixel Array

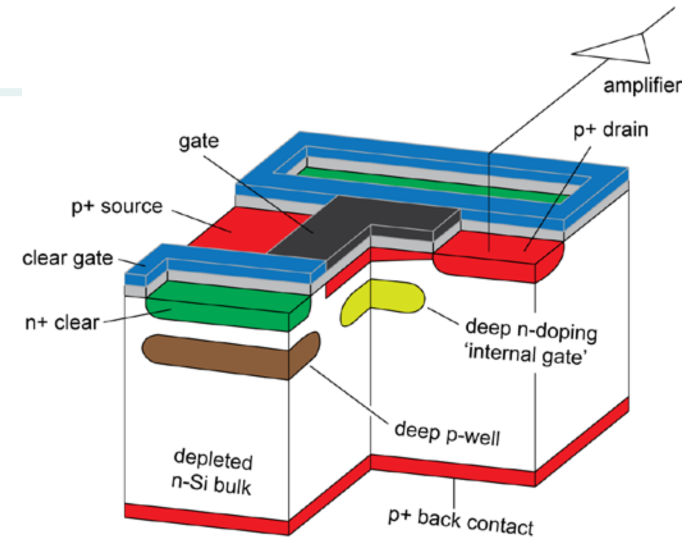


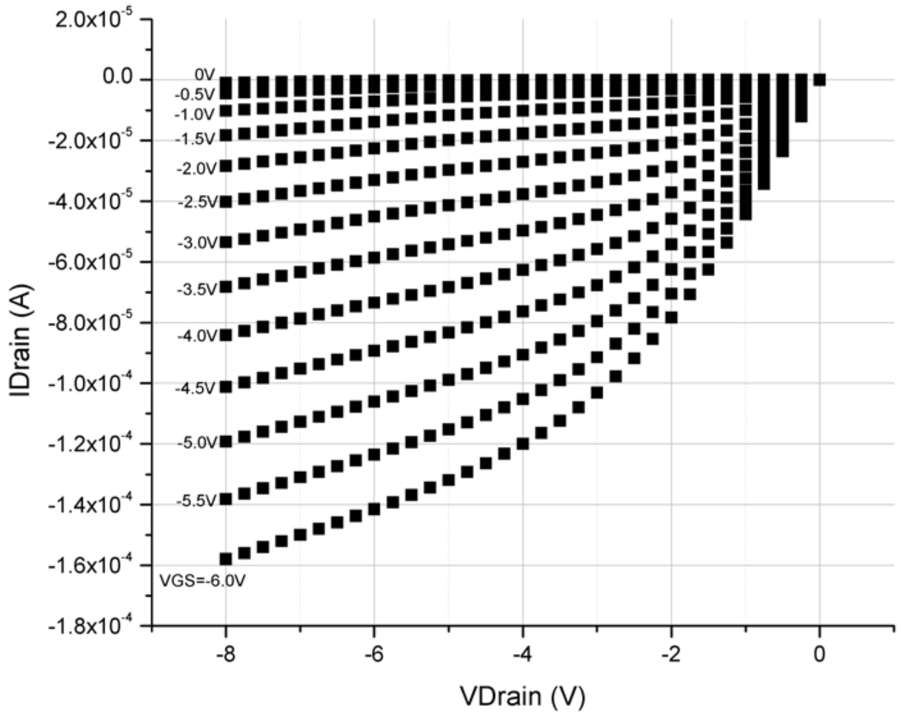
- Belle-II Pixel Detector will consist of 40 half-ladders → roughly 8M Pixel
- Read out will be done in rolling-shutter mode with a speed of 100 ns per row
- 4 rows will be read out in parallel so that the read-out time per half-ladder is about 20 µs

→ We aim for a simulation environment of the complete Si-Module: Switcher, DEPFET pixels at various positions within the array, Read-Out chip (DCD)

DEPFET Tabular Model

- Model uses look-up table with I_{DS} measurements for different bias voltages (V_{GS} and V_{DS})
- Only quasi stable condition if the internal gate is empty → I_{DS} measured @ $V_{cl\ high}$ = 10V
- For DEPFET read mode ($V_{cl\ low}$) correction of I_{DS} is needed
- Spline interpolation for the values which are not in the table

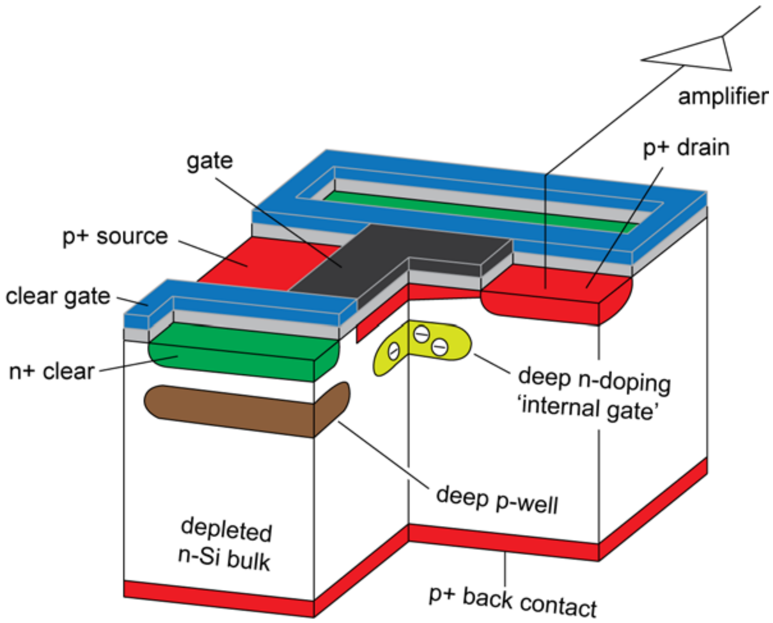




DEPFET Specific Properties

DEPFET specific properties can be described by following equations:

- Filling the internal gate



$$I_{"1"}^{CLLo} = I_{"0"}^{CLLo} - \sqrt{\frac{I_{"0"}^{CLHi}}{I_{"0"Ref}^{CLHi}}}\, g_q \, N_{SIG}$$

internal amplification (g_q)

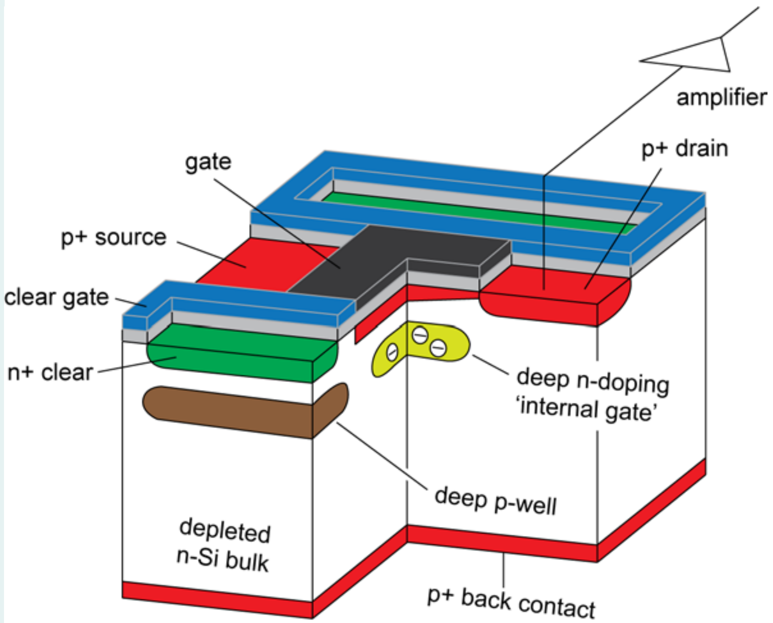
number of signal electrons (N_{SIG})

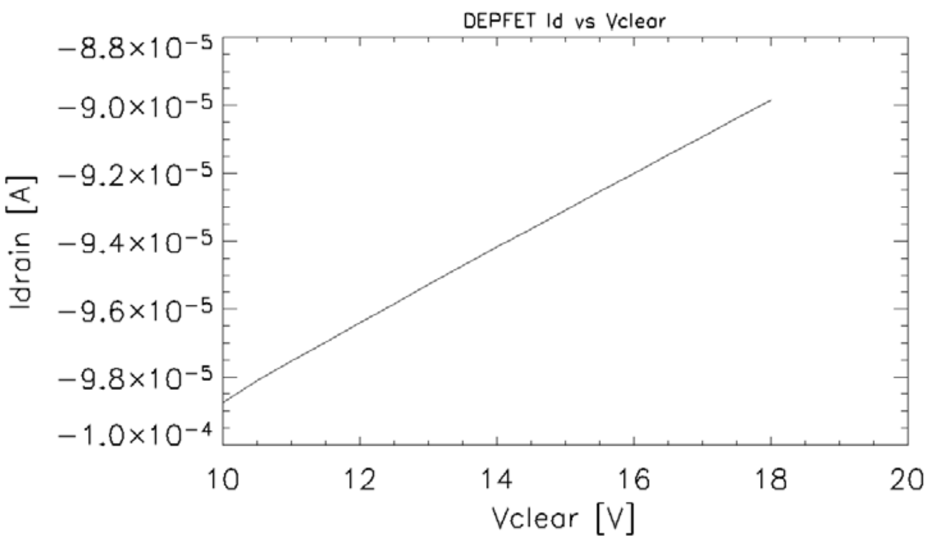
g_q - internal amplification @V_G=V_D=-5V

400pA/electron

DEPFET Specific Properties

- Transconductance of the clear electrode on the drain current



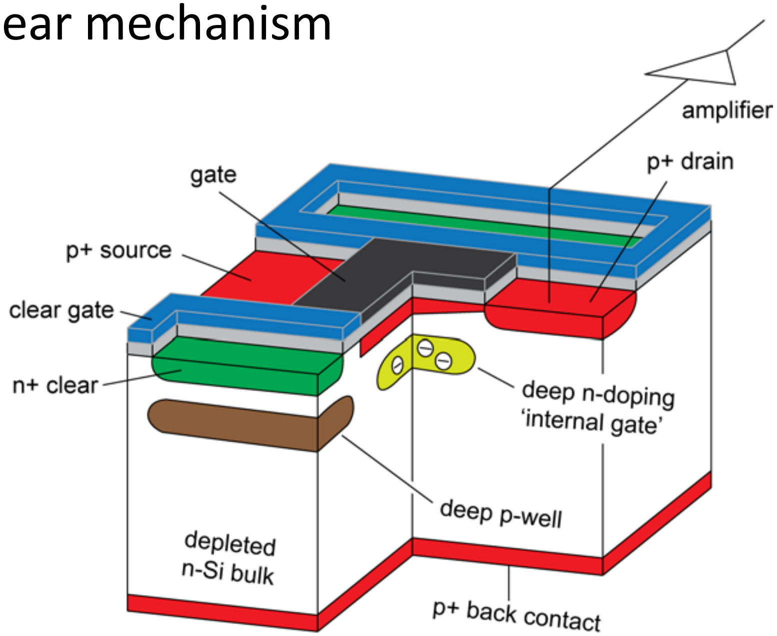


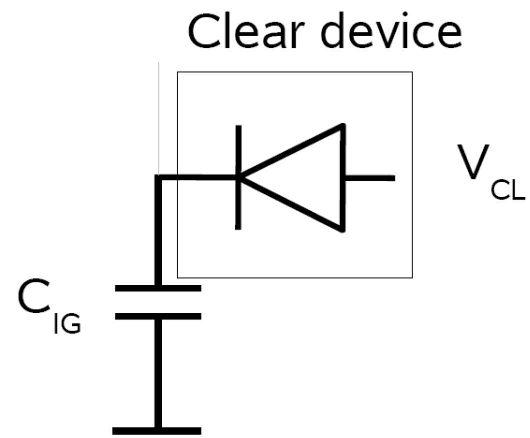
$g_m^{Cl} = 1.1\ \mu S$

→New look-up table for the drain current is calculated taking the reduced voltage at the Clear terminal into account

DEPFET Specific Properties

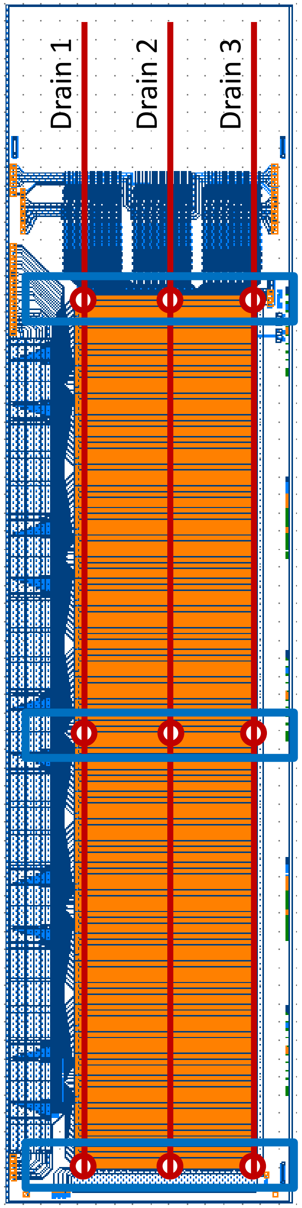
- Clear mechanism



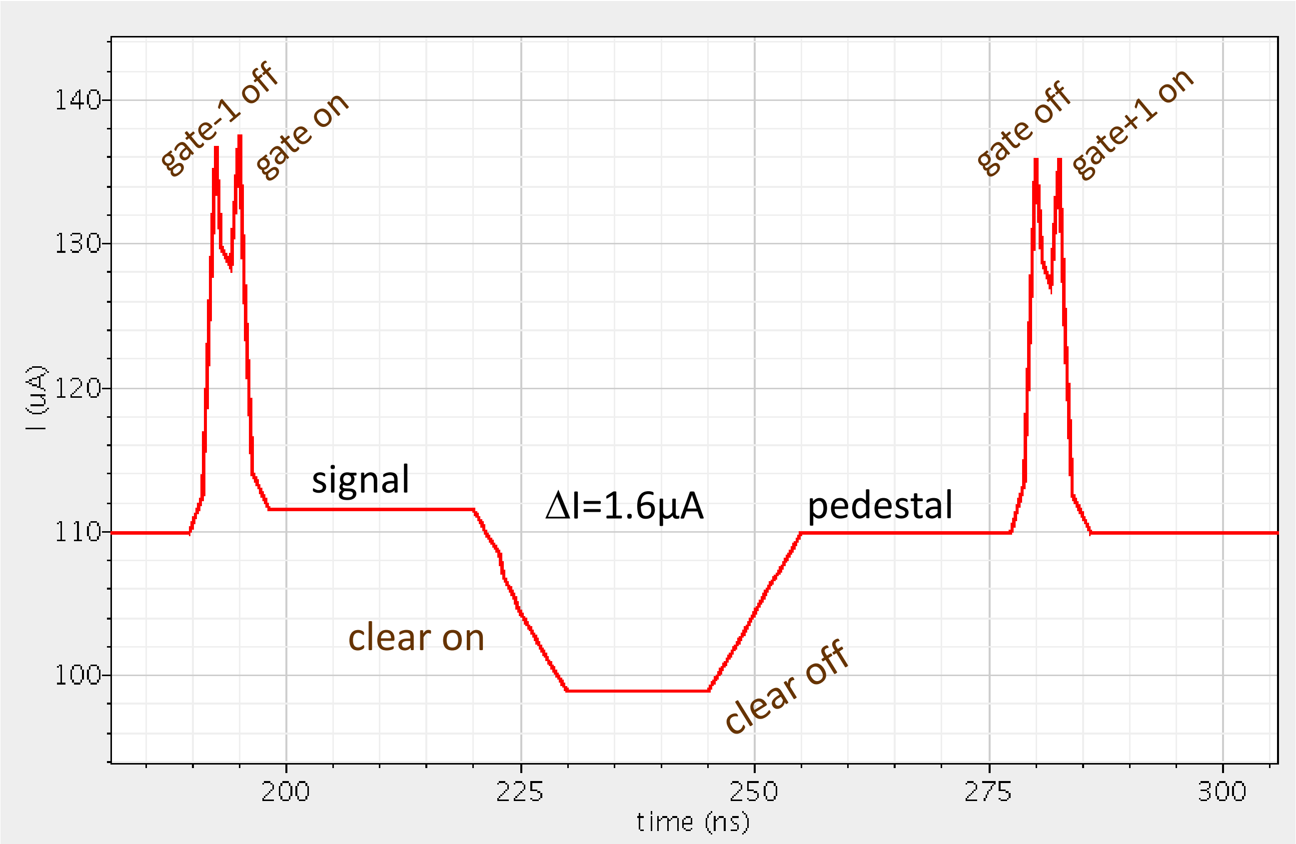


- Simulation programm provides a time step Δt
- The corresponding ΔQ at the applied Clear voltage
- The new signal charge changes the drain current

DEPFET Model without parasitic RCs



Simulation of the drain current of a DEPFET Pixel matrix without parasitic RCs.



Simulation tool: Cadence SpectreCMI, T Gate on = 90ns

Specific Parameters of a DEPFET Model

- Influence of the internal gate on the drain current
- Transconductance of the clear and clear-gate electrode on the drain current
- Clear mechanism

} using Cadence Spectre Compiled Model Interface

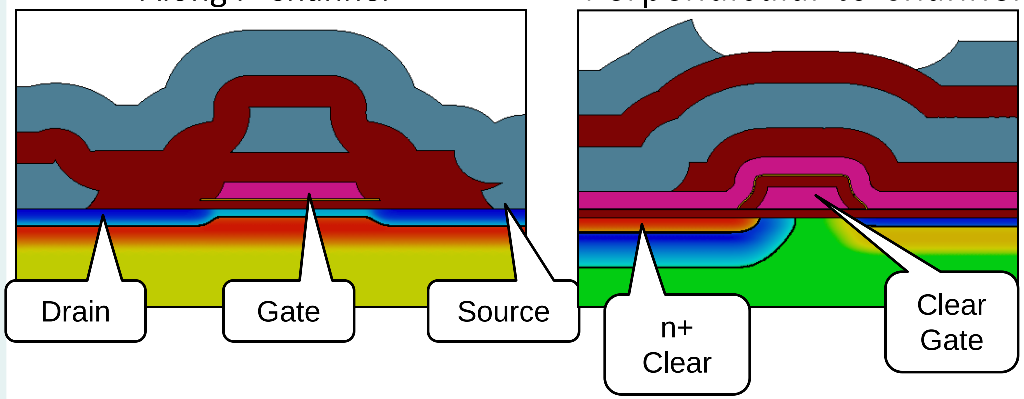
- Capacitive coupling and line resistivity is missing ➡ RC extraction based on layout and technology necessary

Synopsys Raphael RCV + Sentaurus Structure Editor

Non-planar technology

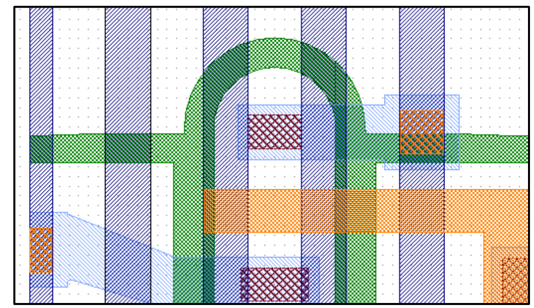
Along P-Channel

Perpendicular to Channel




```
DEPOSITION THICKNESS=0.2 MATERIAL=Oxide TYPE=iso
ETCH THICKNESS=0.2 MATERIAL=Oxide TYPE=iso MASK=via1
        POLARITY=NEGATIVE
DEPOSITION THICKNESS=0.4 MATERIAL=Metal TYPE=patterned
        MASK=poly1 POLARITY=POSITIVE
```

GDS II

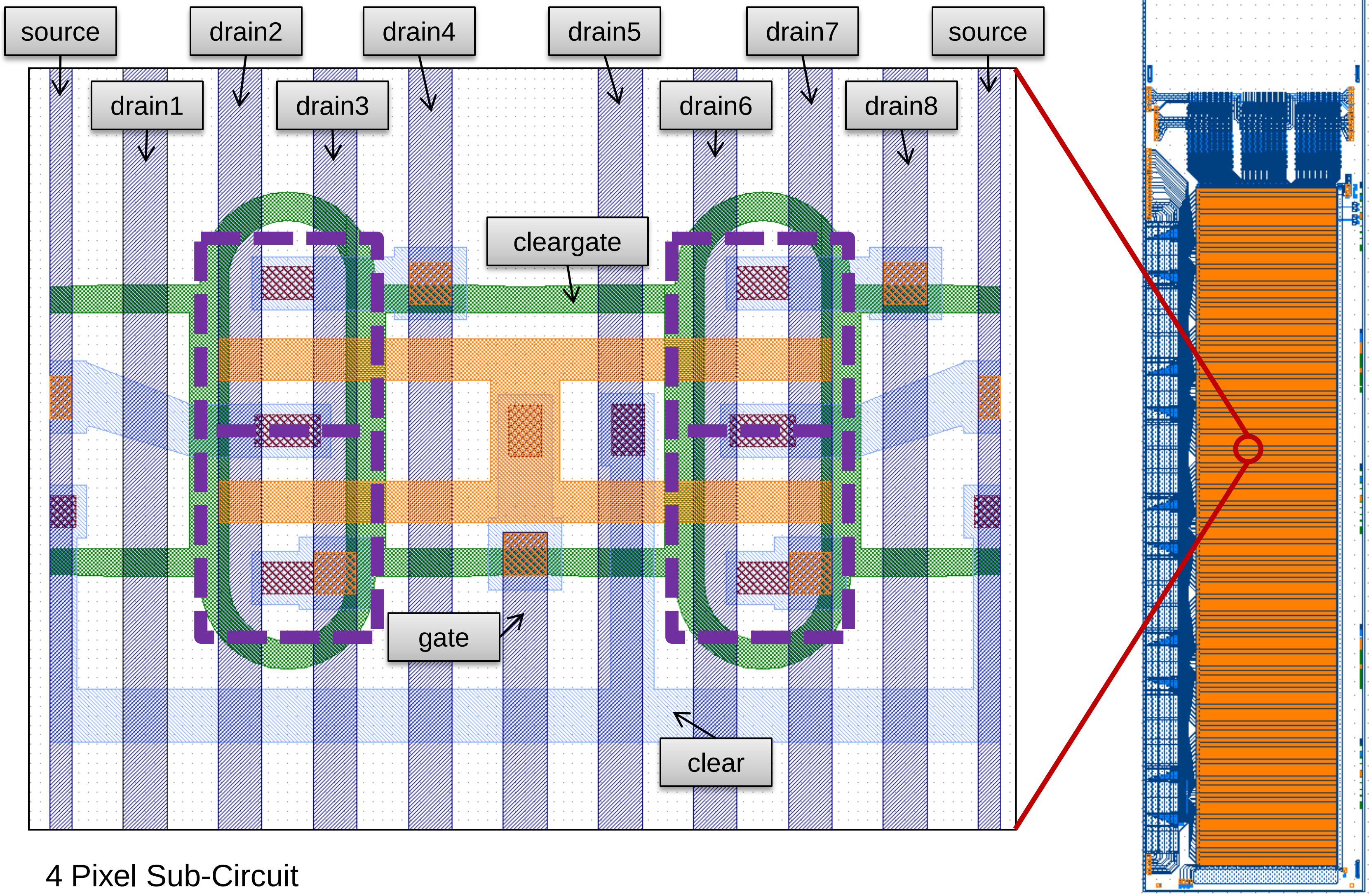


Synopsys Tools

- 3D Model
- MESH Generator
- Charge Calculation

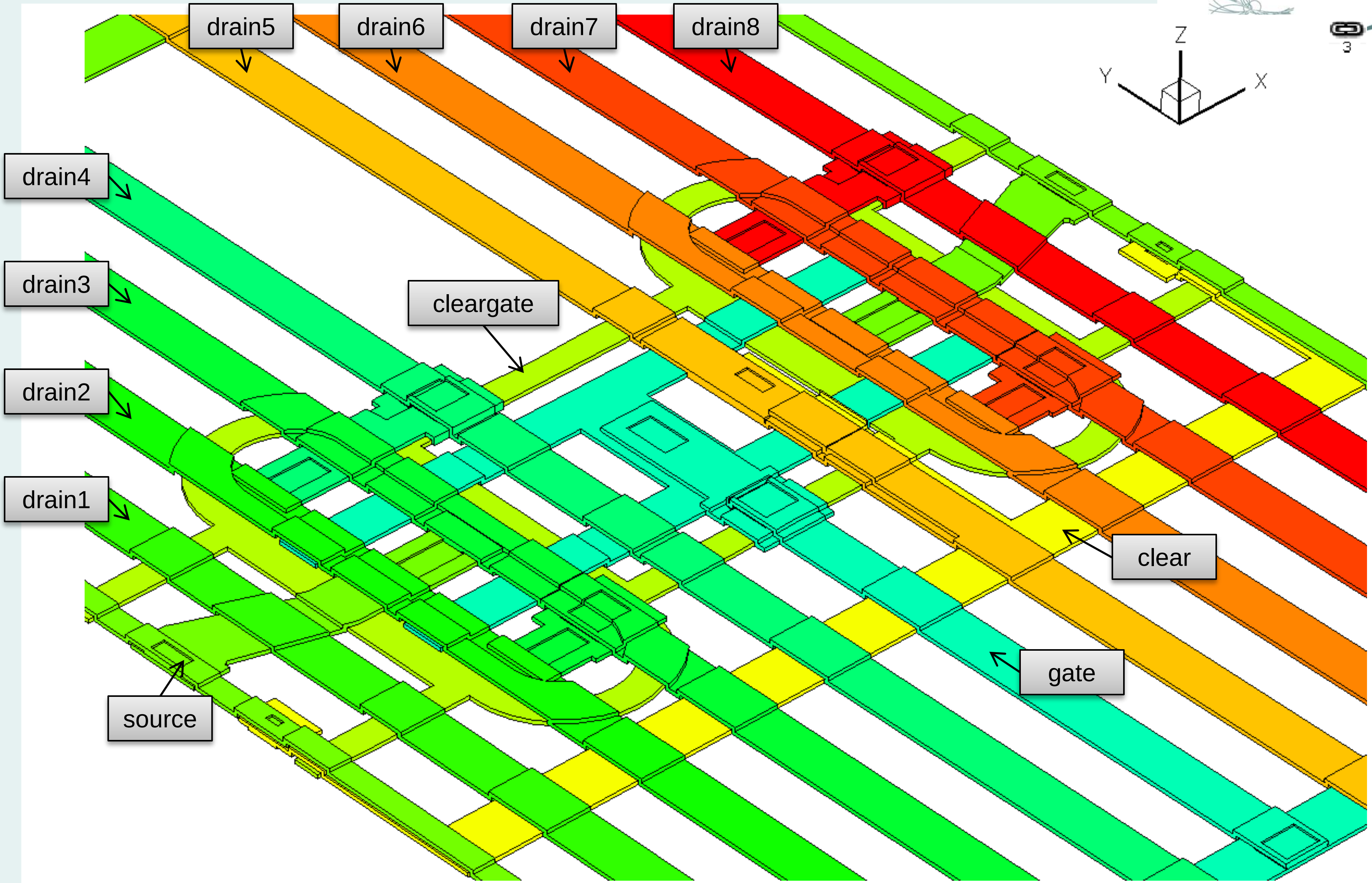
Capacitance Report
SPICE net list

Detail of a DEPFET Layout

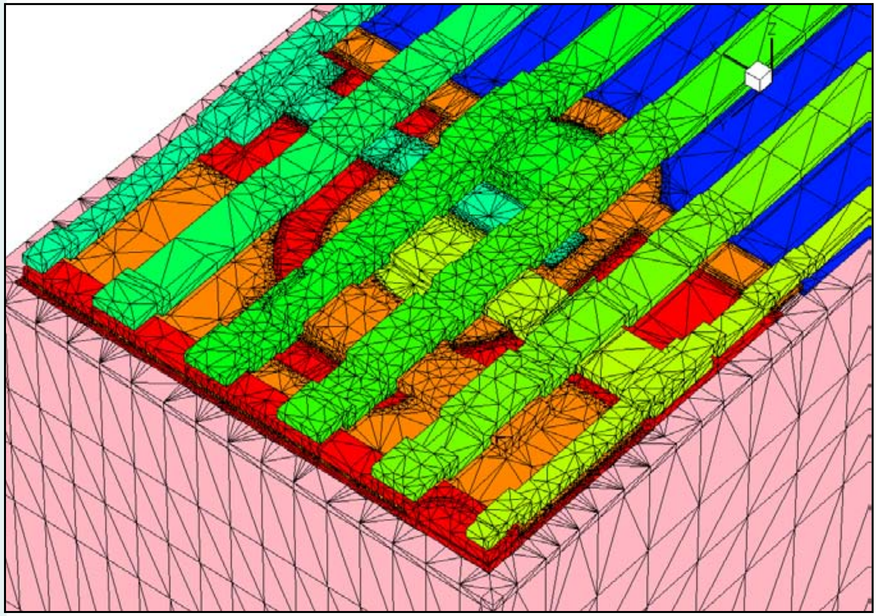


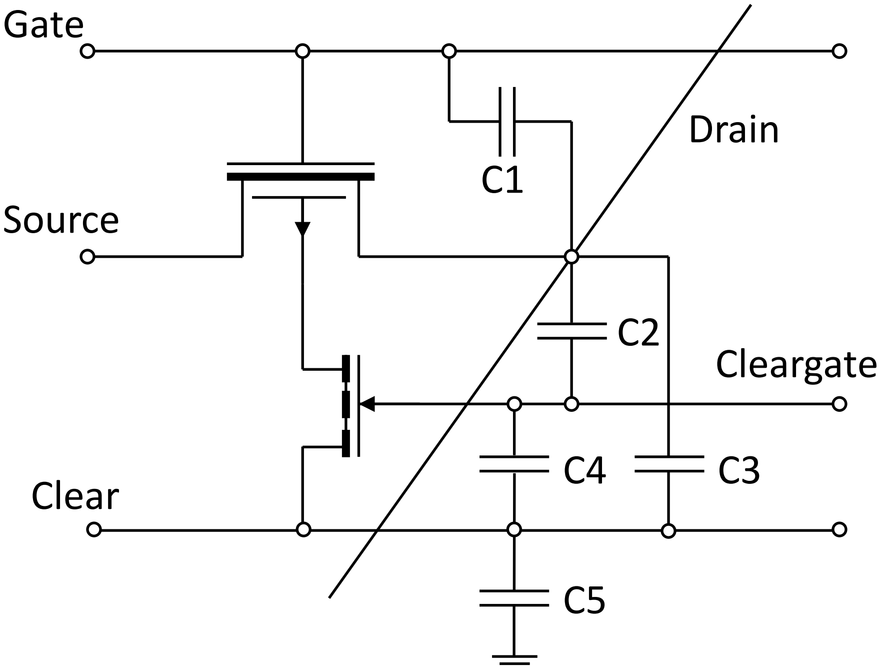
4 Pixel Sub-Circuit

3D Geometrical Model



Results for a Capacitive Coupled Clear Gate Pixel





cap label	net1	net2	cap [fF]
C1	Gate	Drain	8.7
C2	Cleargate	Drain	17
C3	Clear	Drain	4.5
C4	Clear	Cleargate	167
C5	Clear	All except cleargate	56

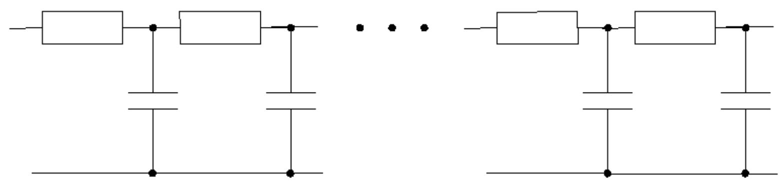
For a pixel array 768x160:

Cclear_array = 100 * 227fF = 22pF

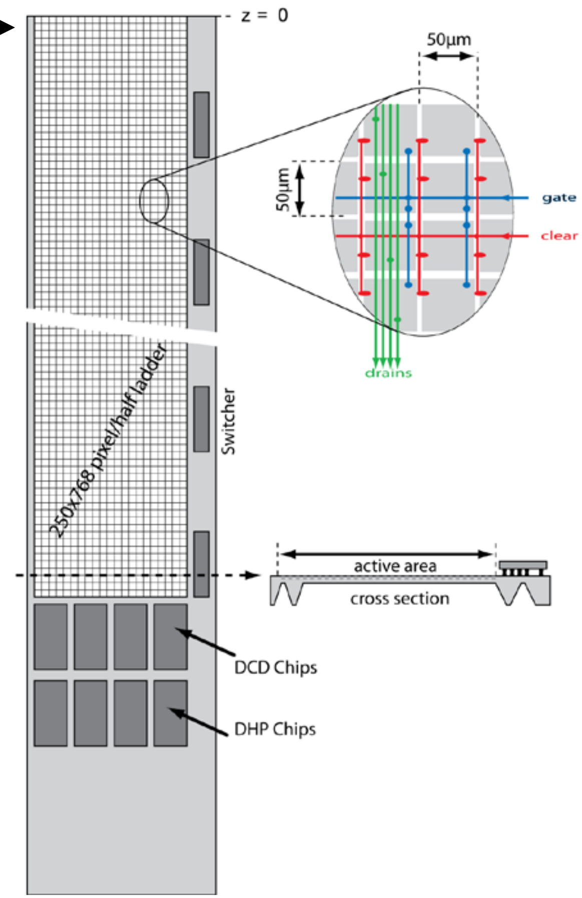
Number of layout sub-circuits per row.

Simulation DEPFET- Pixel Array

Each line is a distributed RC line
of 50 segments



worst case pixel



Control lines

Switcher: Rdown 30 Ohm, Rup 52.5 Ohm

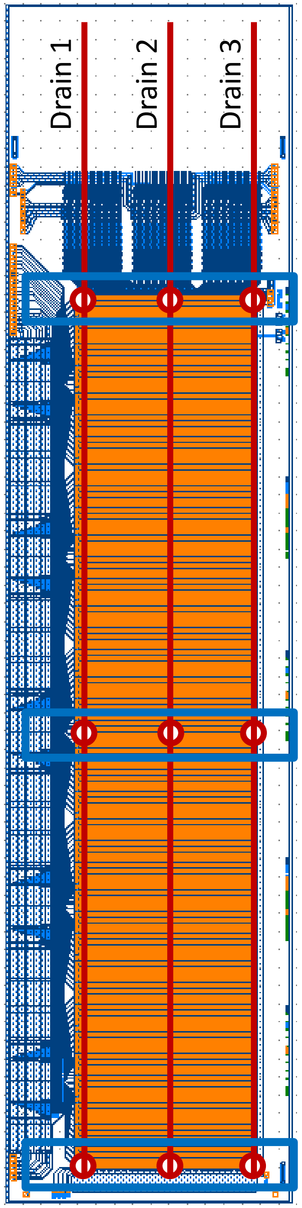
Gate line: Rtotal = 40 Ohm, Ctotal = 50pF

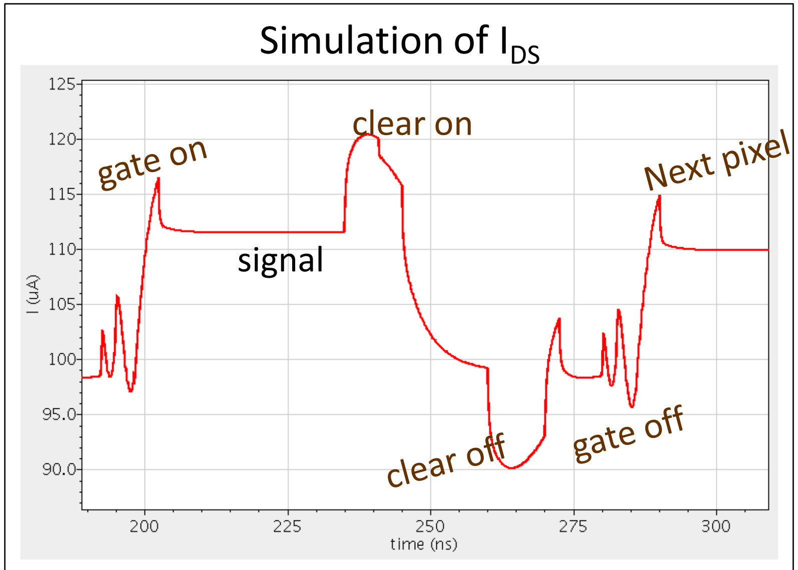
Clear line: Rtotal = 40 Ohm, Ctotal = 50pF

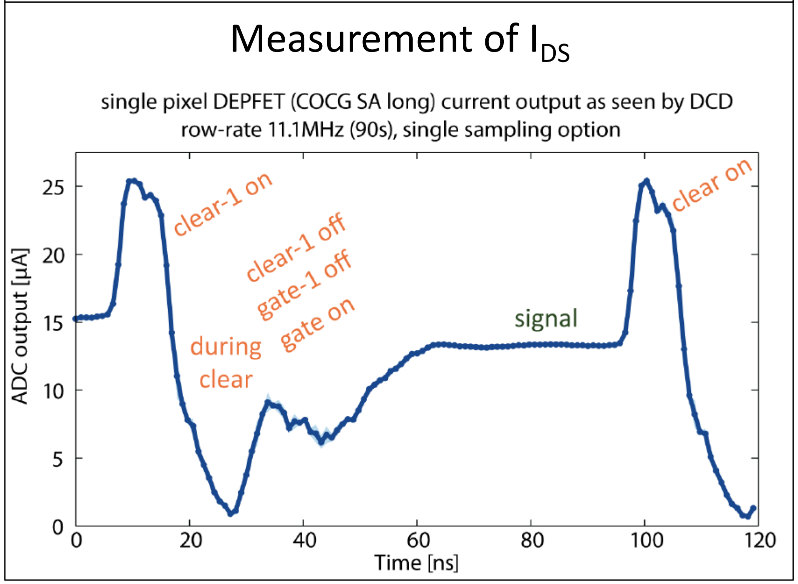
Readout (drain) line

Rtotal = 215 Ohm, Ctotal = 50pF

Simulation DEPFET- Single Sampling







Measurement done by Manuel Koch, Uni Bonn

Summary and Outlook

- DEPFET Parameter Model describes the unique DEPFET specific properties and includes parasitic RC values (based on layout and technology)
- Enables the investigation of fundamental speed limits and optimization by changes in design or technology
- Simulation environment including the full-chip models of the Switcher-B and DCD-B is available at the University of Heidelberg (Prof. Fischer‘s group)
- Next steps are the simulations of the current PXD6 designs and the setup of the full-chip models of Switcher-B and DCD-B at MPI Munich

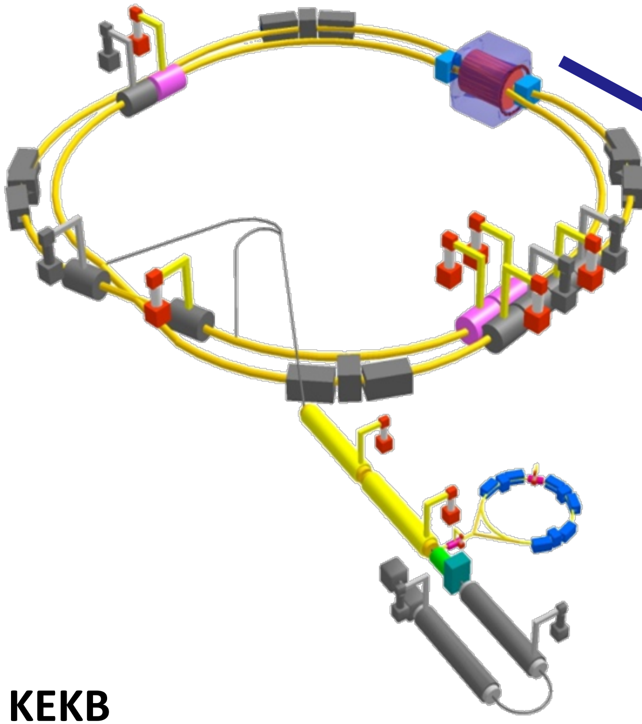
Thank you!

Questions?

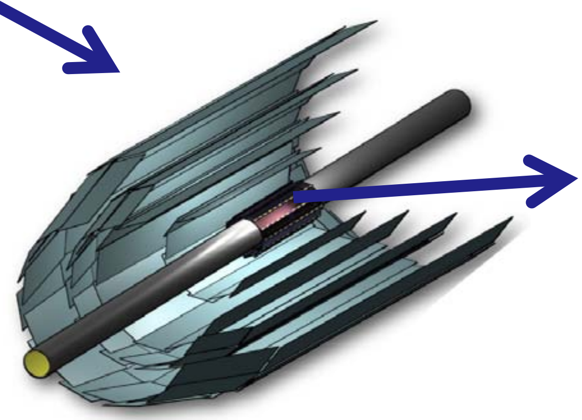
Supplementary Slides

DEPFET PXD for Belle II Detector @ SuperKEKB

KEKB e+/e- collider



Sub-System of Belle II Detector (SVD and PXD)



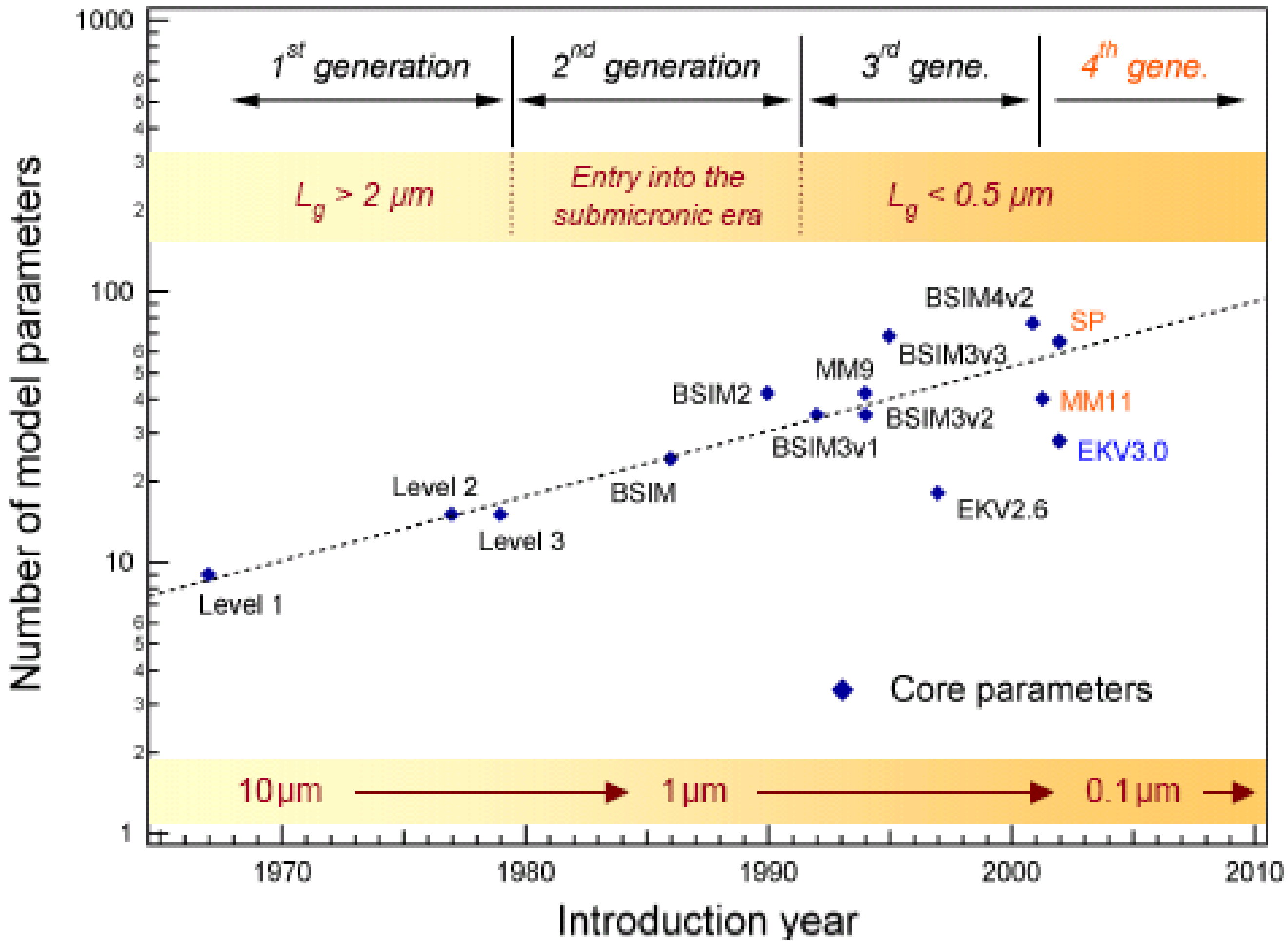
PXD Si-Modules

KEKB

- Aims to prove CP-violations in the B meson/anti-B meson decay (CP = charge-parity)
- Upgrade of KEKB to increase the luminosity by 40

Belle Detector

- Detection of particles which result from the e+/e- collision
- SVD: 4 layers of double sided silicon strip sensors
- PIX: 2 layers of DEPFET pixel detectors



Source : http://legwww.epfl.ch/ekv/mos-ak/stuttgart/Pregaldiny-mos-ak-STR04.pdf

Clear Mechanism

$$\frac{\Delta Q}{\Delta t} = I_{C0}\left(e^{y} - 1\right)$$

Ebers-Moll like diode eq.

$$y = k\left(V_{CL} - V_{ON} - V_{IG}\right)/V_T * \frac{V_{IG}^{"0"} - V_{IG}}{V_{IG}^{"0"}}$$

$$V_{IG} = \frac{Q + \Delta Q}{C_{IG}}$$

$V_{IG}^{"0"}$

I_{C0}

k

V_{ON}

V_T

$$\frac{\Delta Q}{\Delta t} = I_{C0}\left(e^{y} - 1\right)$$

$$f = I_{C0}\left(e^{y} - 1\right) - \frac{\Delta Q}{\Delta t}$$

Search for the root (null) gives ΔQ

Clear Mechanism

Newton-Raphson iteration

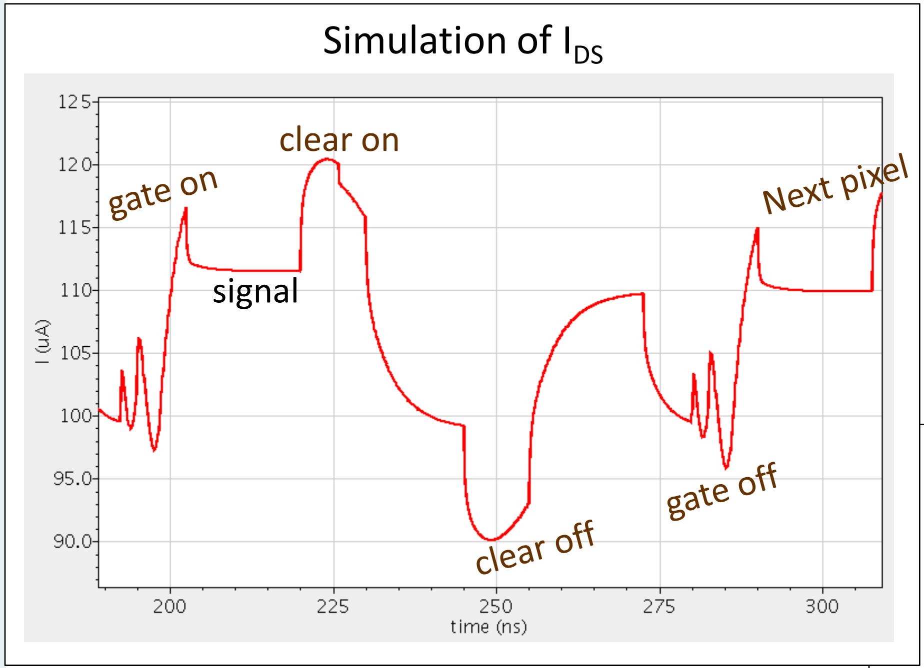
$$\Delta Q_{new} = \Delta Q_{old} - \frac{f}{f\,'}$$

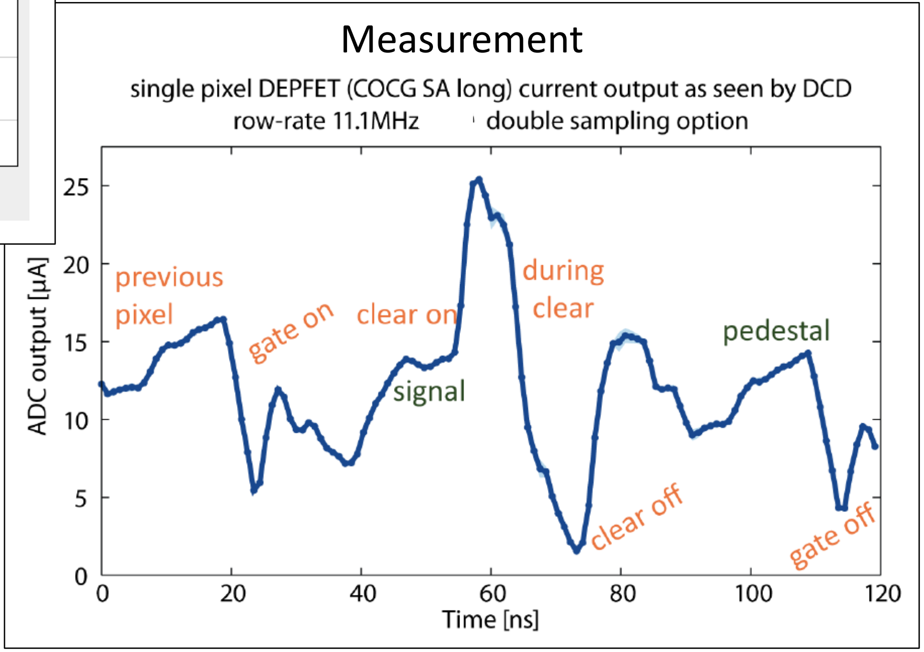
Very efficient!

Usually 4 iterations to reach a precision of 10^{-20}As

It‘s easy to implement more refined Clear models
requirements for f : derivative, monotony

Simulation PXD5 COCG - Double Sampling





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