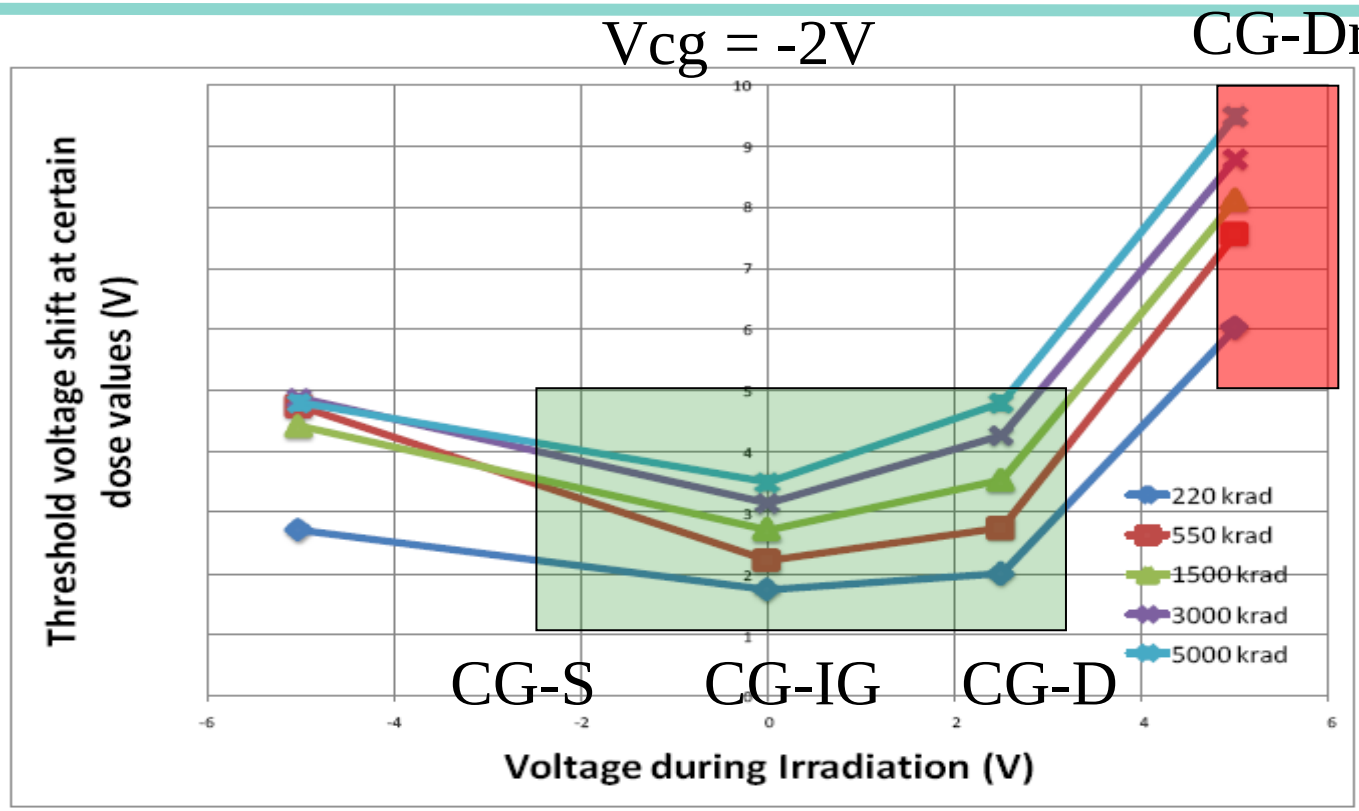
PXD6 Production Status, final pixel design ?

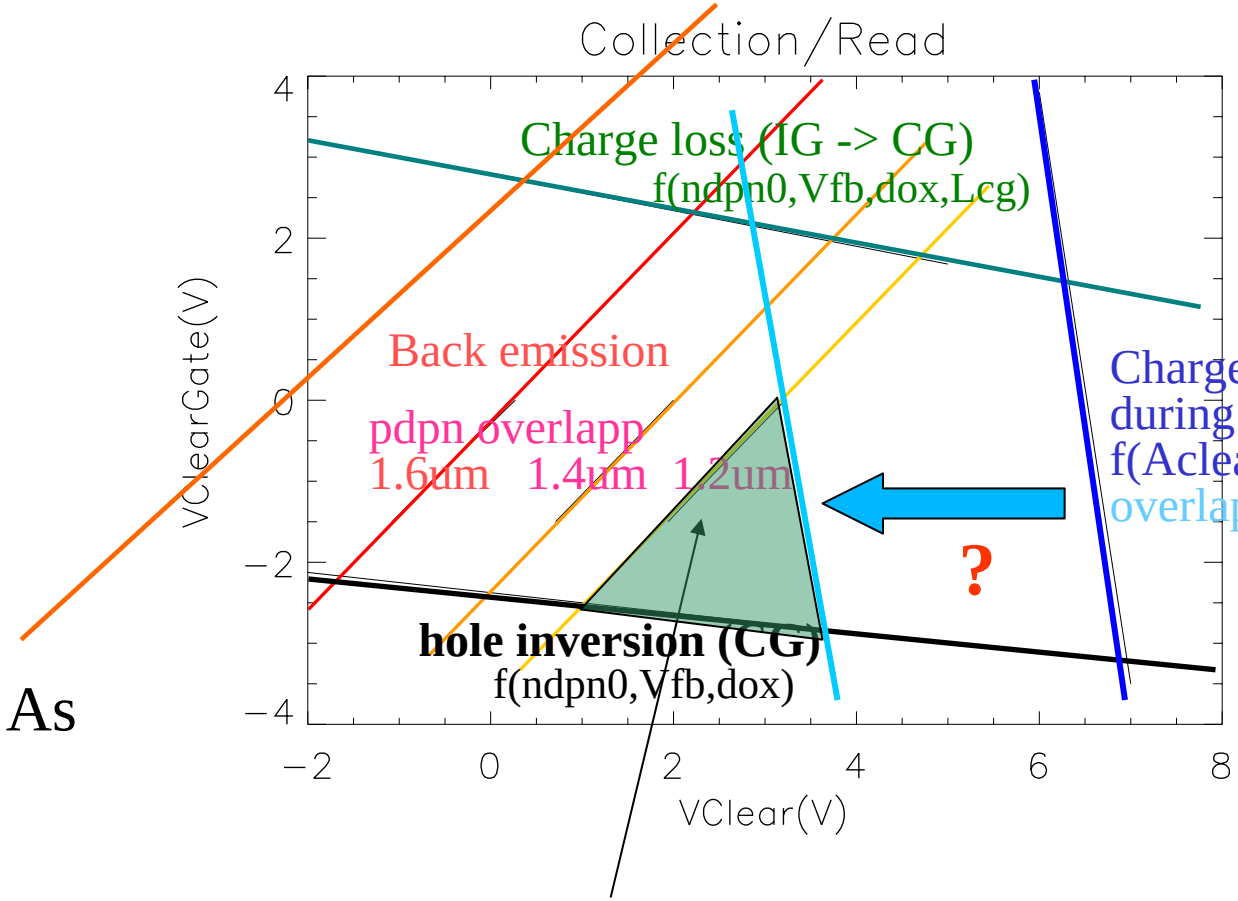
Proposal for a more radiation tolerant design

PXD6 Production Status

The Clear Gate Problem



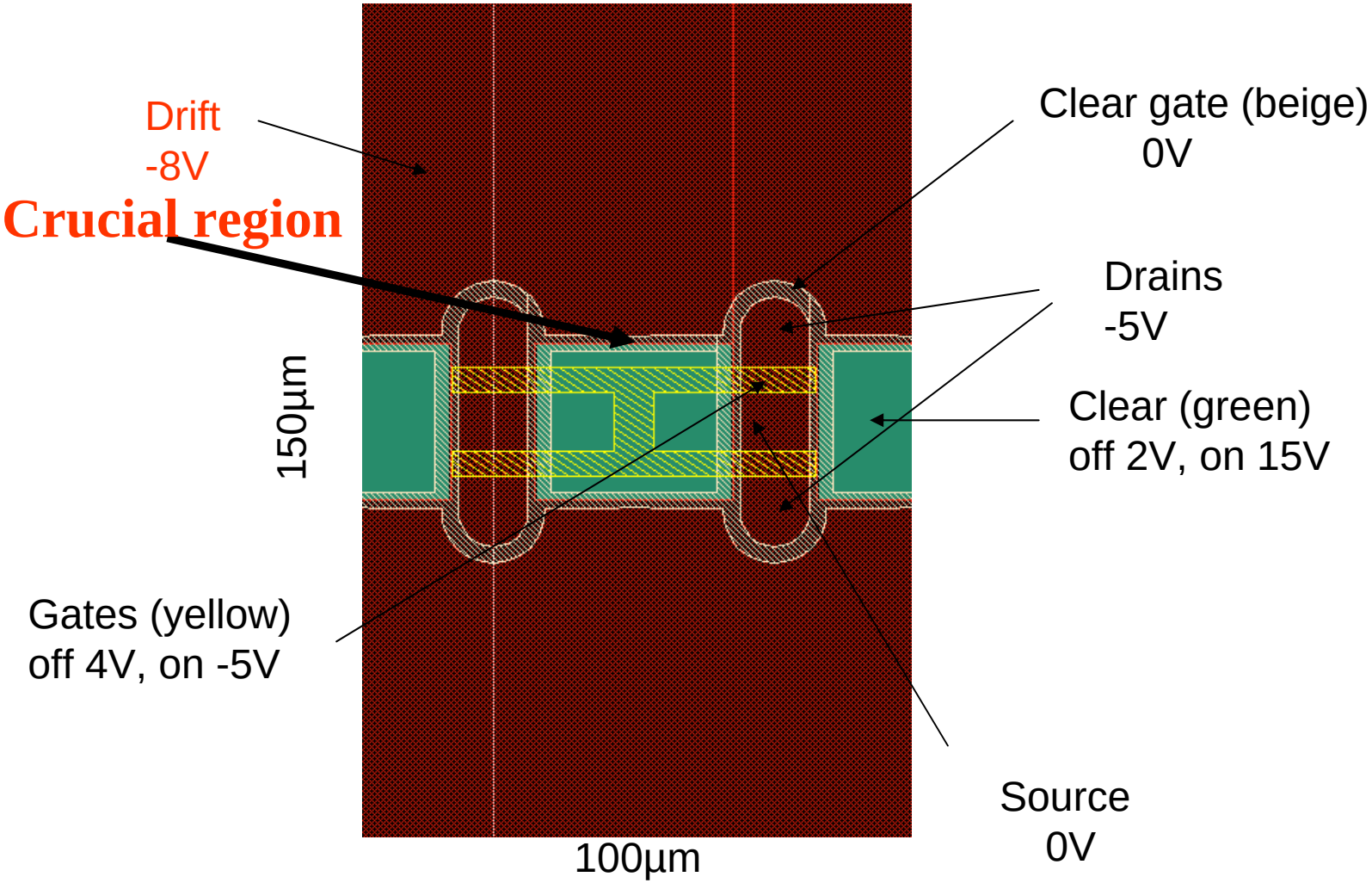
Which Clear and ClearGate voltages ensure a safe operation?



As

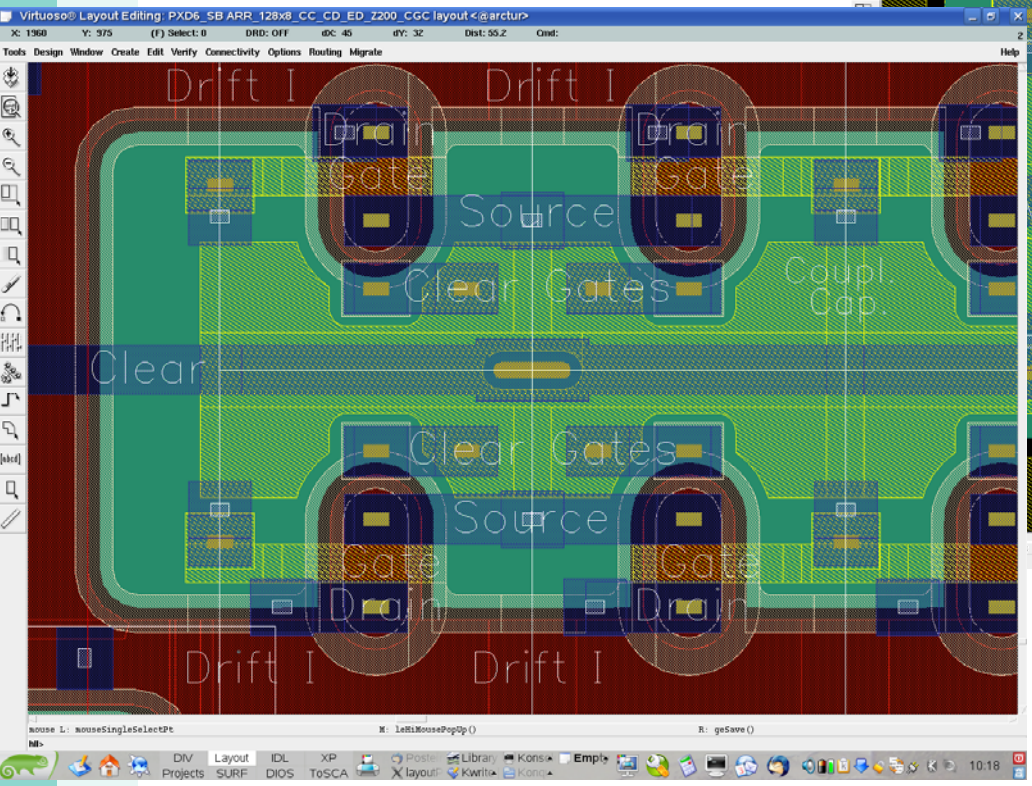
Operation triangle

DEPFET - matrix section 2x2 pixel
(metal and contact layers are omitted)

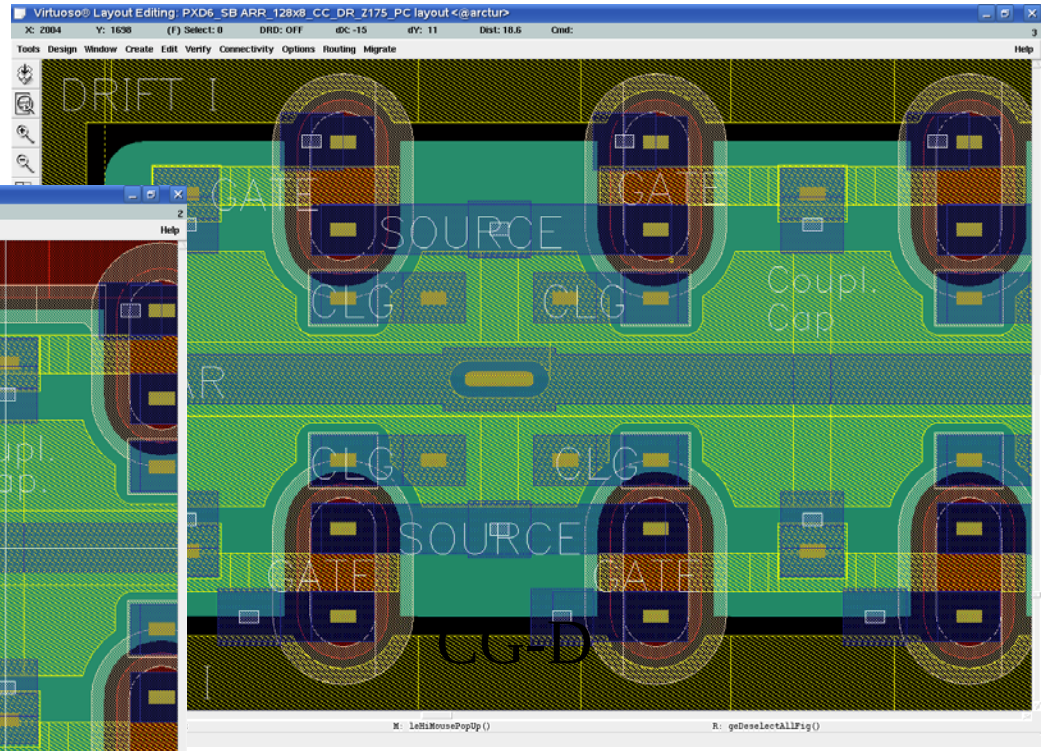


PXD 6 Design options

SCG Design
(Surrounded Clear Gate

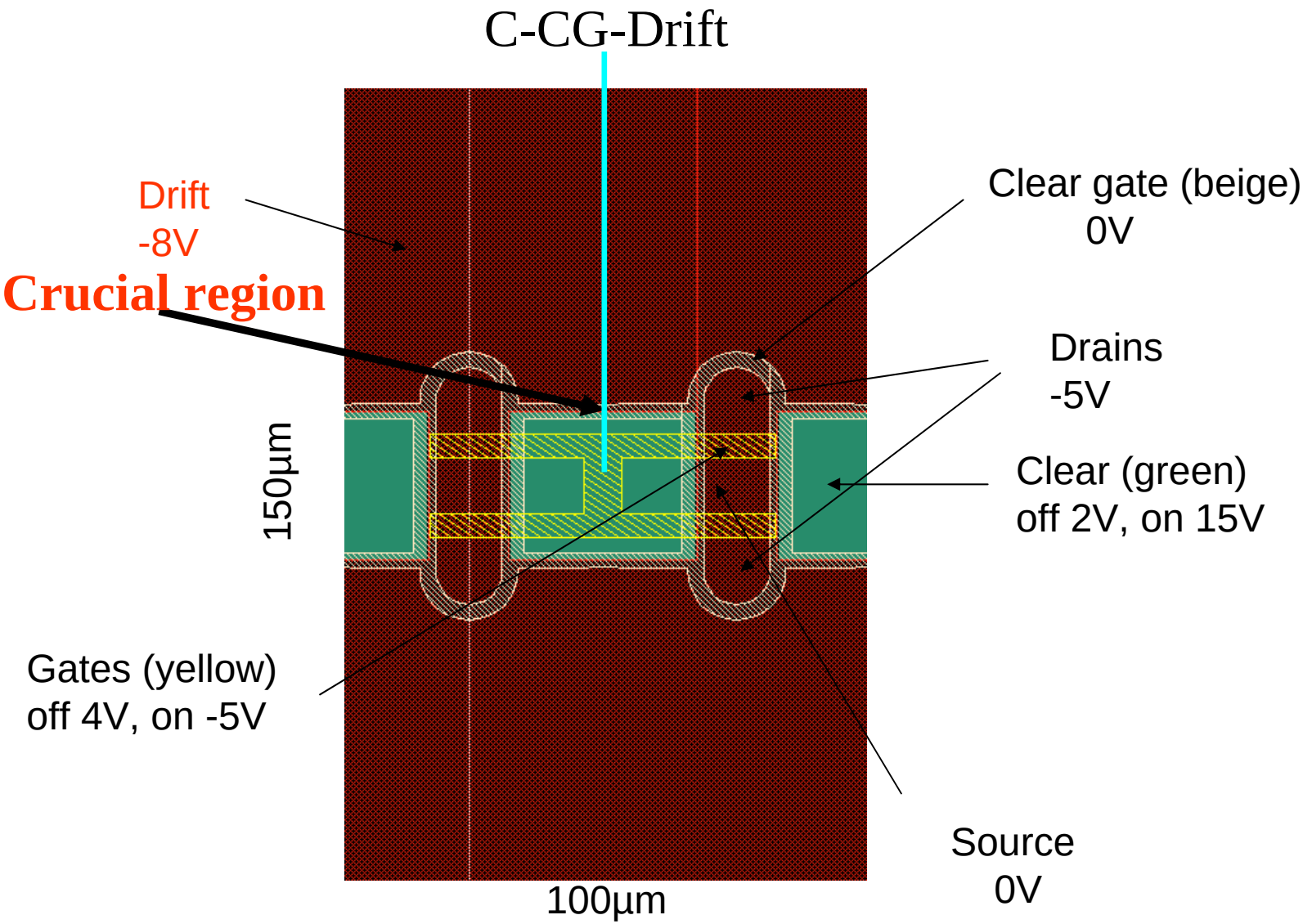


PC Design (Poly Cover)
would solve this problem



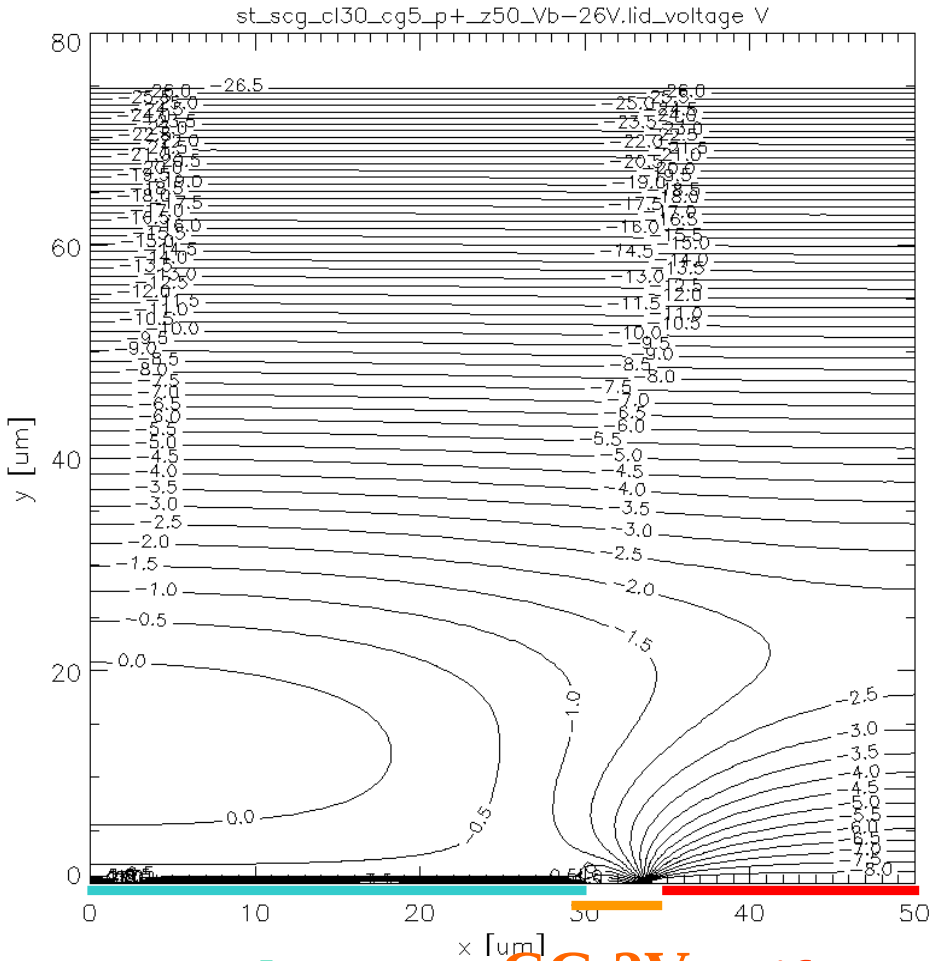
higher leakage current
more control lines
more poly1/poly2 overlapps
☹

Simulation


C-CG-Drift
Drift
-8V
Crucial region
Clear gate (beige)
0V
Drains
-5V
Clear (green)
off 2V, on 15V
150µm
Gates (yellow)
off 4V, on -5V
Source
0V
100µm

Clear-ClearGate-Drift

unirradiated

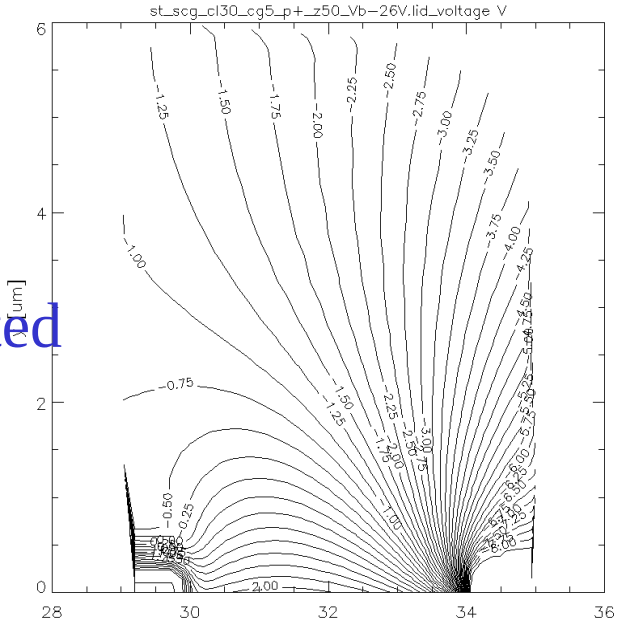


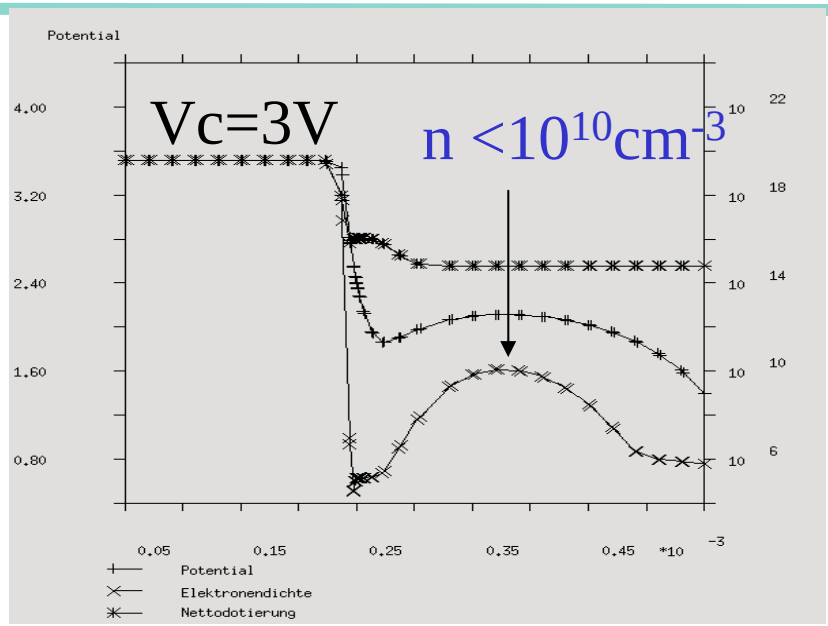
Backside
75µm at -26V

Gap region (CG)

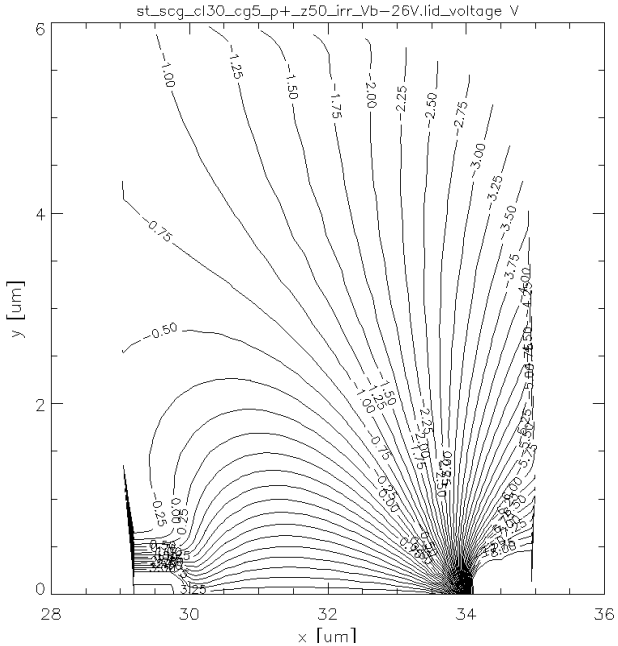
u

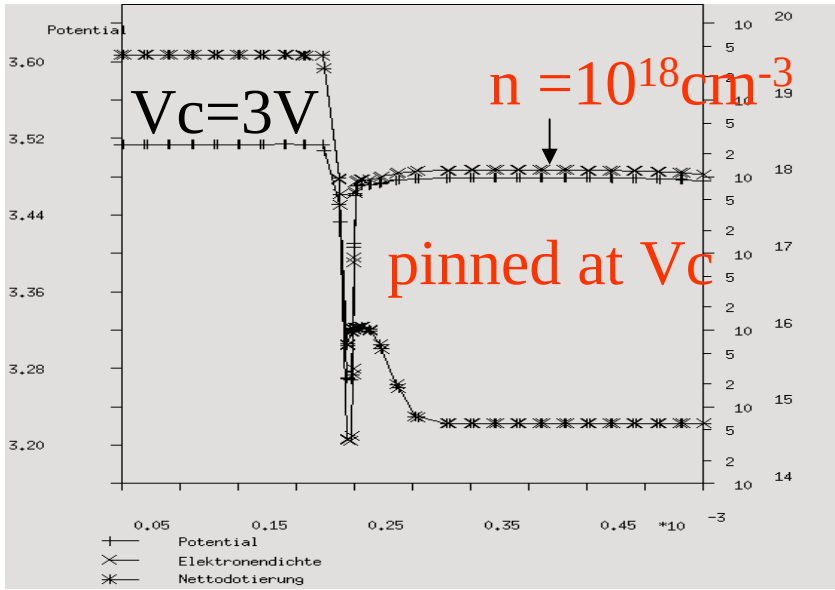
unirradiated





irradiated
Vcg = 8V

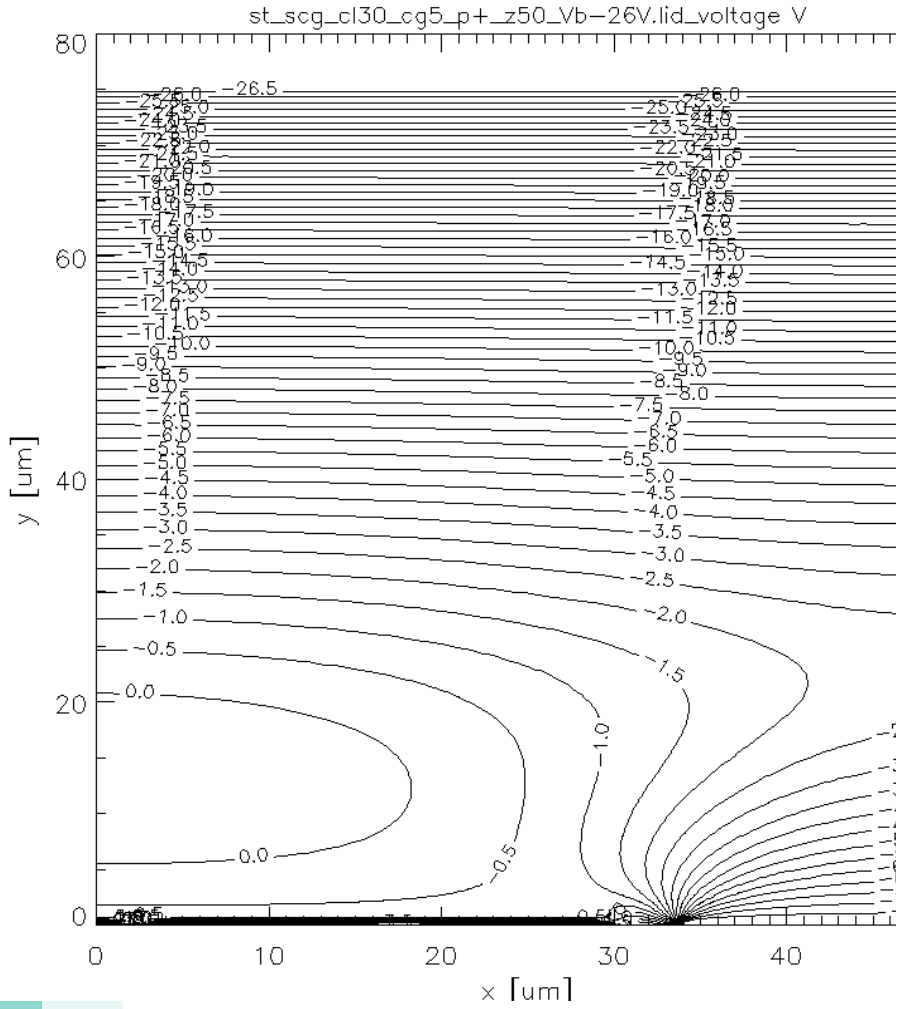




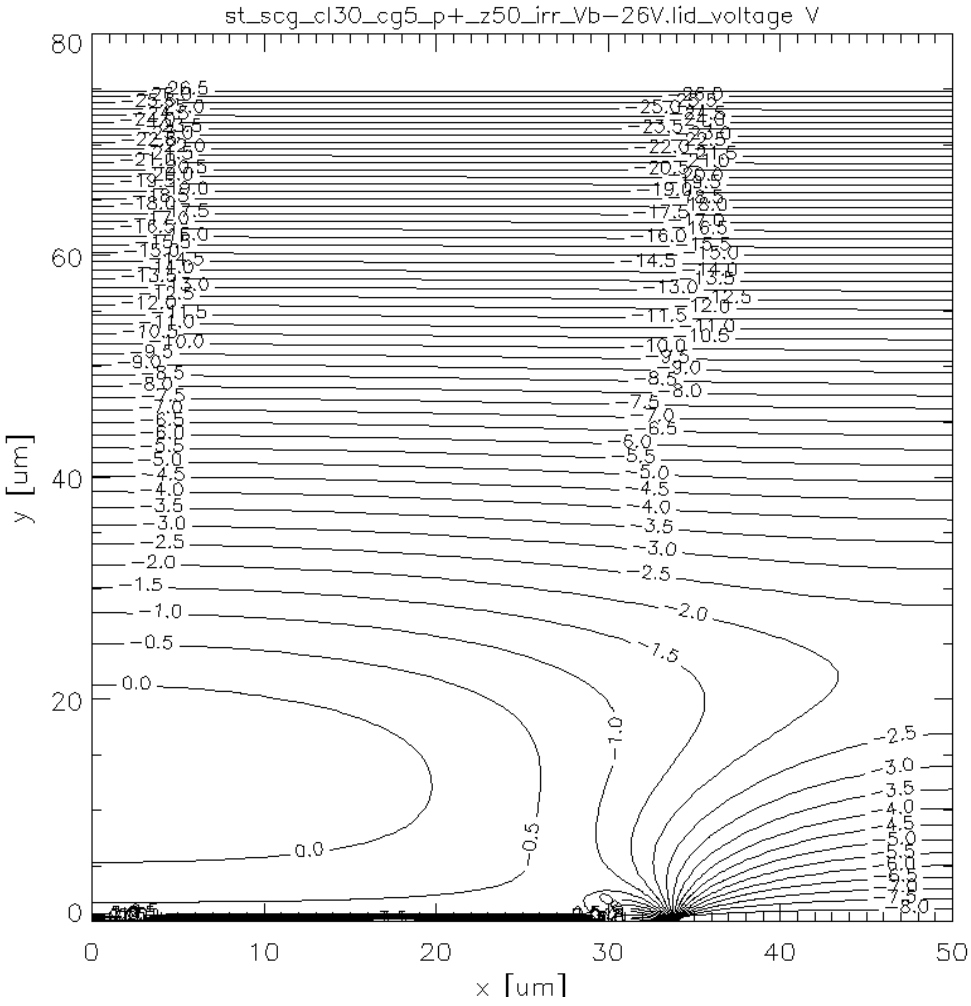
Charge collection (C-CG-Drift)

Does not change !

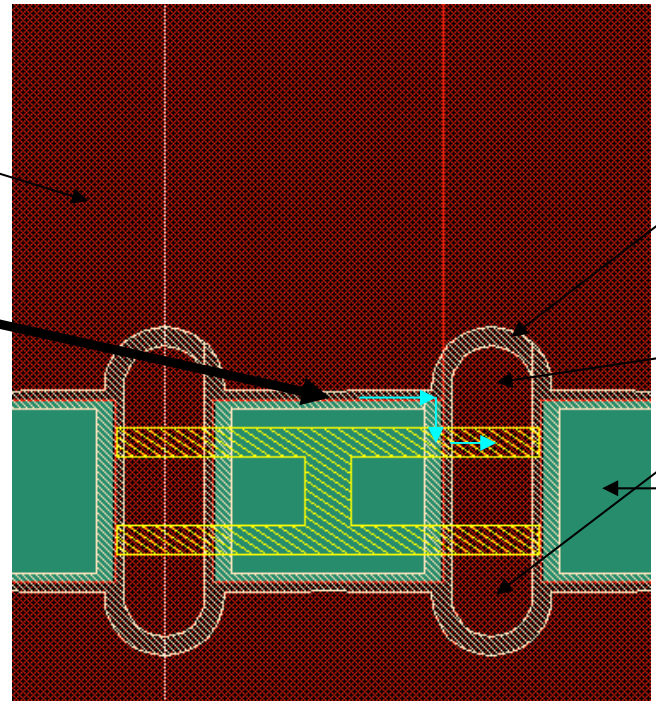
unirradiated



irradiated



What happens with the electrons in CG region?

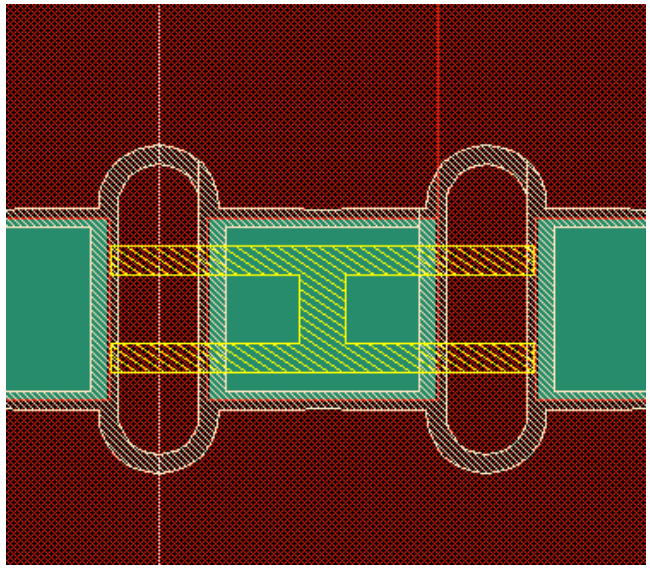


PXD6 pixel are designed in a way that these electrons are treated as signal electrons -> they drift into the internal gate ☹
after they are pushed by a global n doping into the depth

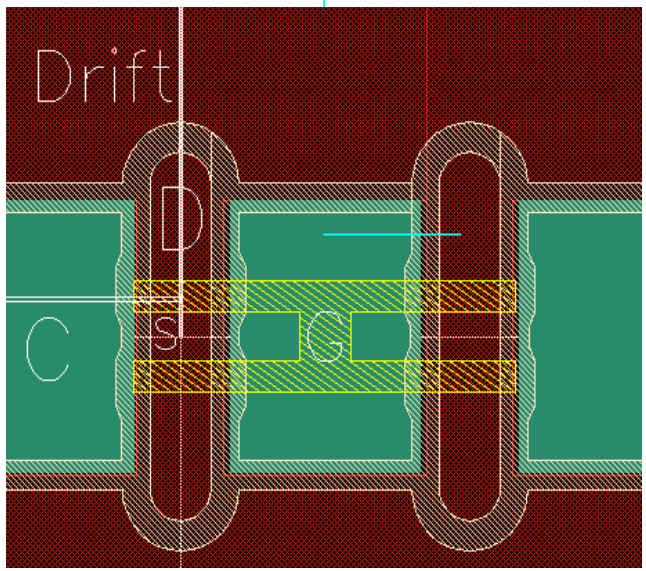
New Approach

Forming a barrier for electrons

PXD 6
ST_SCG …

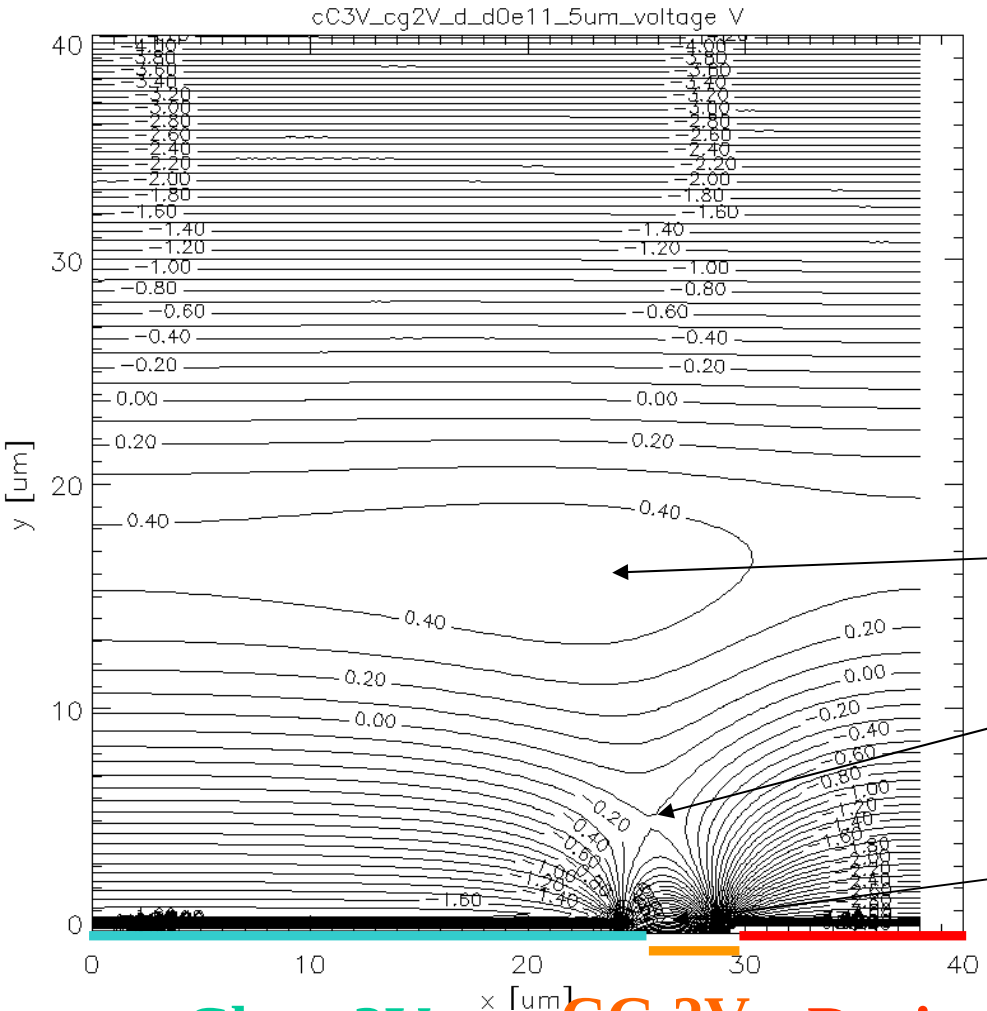


Modified design



- Keeping electrons at the surface (by omitting the global n doping in the crucial regions)
- Longer Drain (barrier) regions

Clear-CG-Drain Vc=3V,Vd=-5V Vcg=2V



Separation of electrons paths

Signal electrons

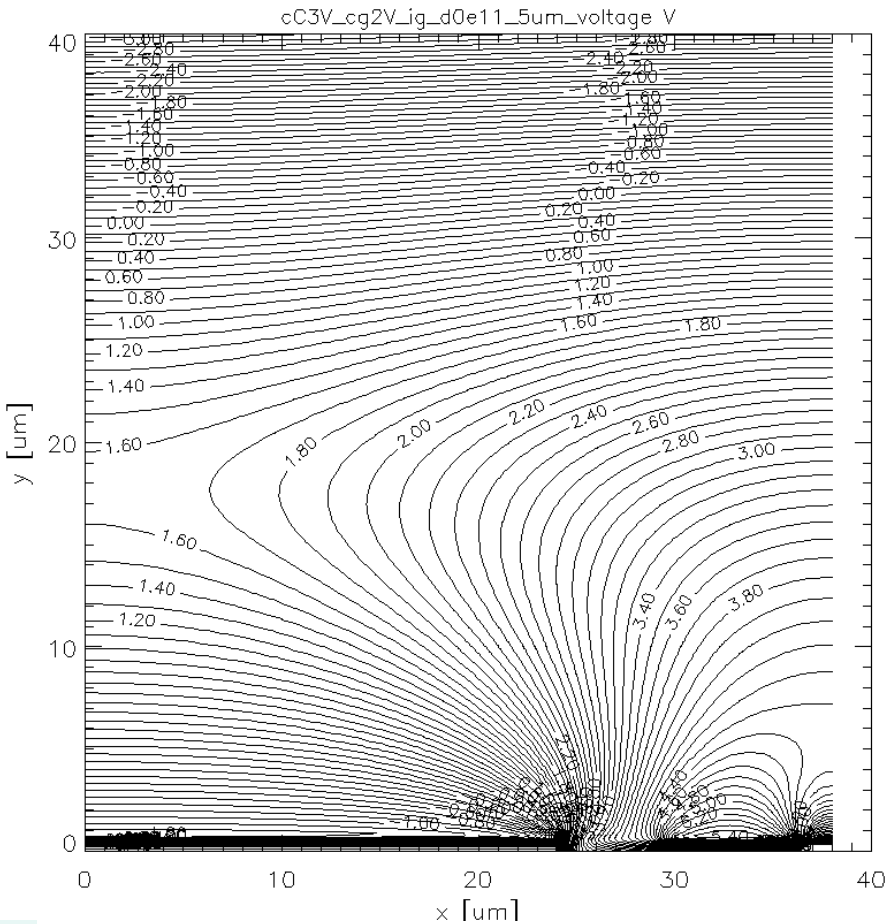
Saddle point formation
Due to neg. Drain potential
and omited n-doping

Surface electrons
(to be blocked)

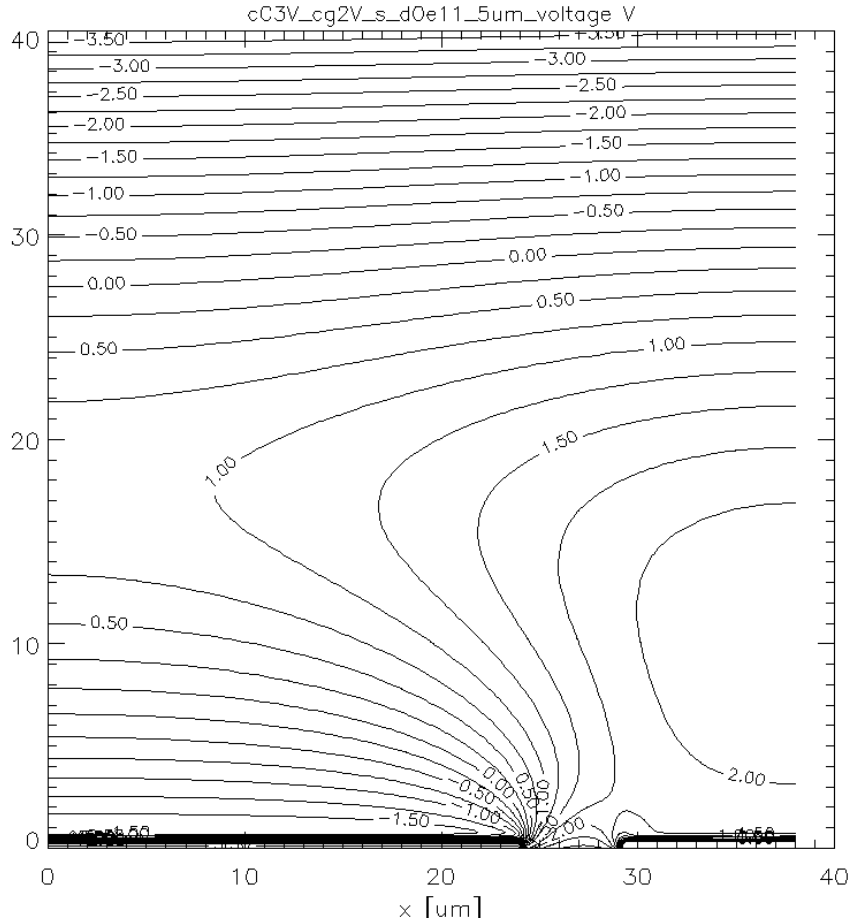
Clear 3V **CG 2V MOS** **Drain -5V**

For completeness …

C-CG-Internal Gate



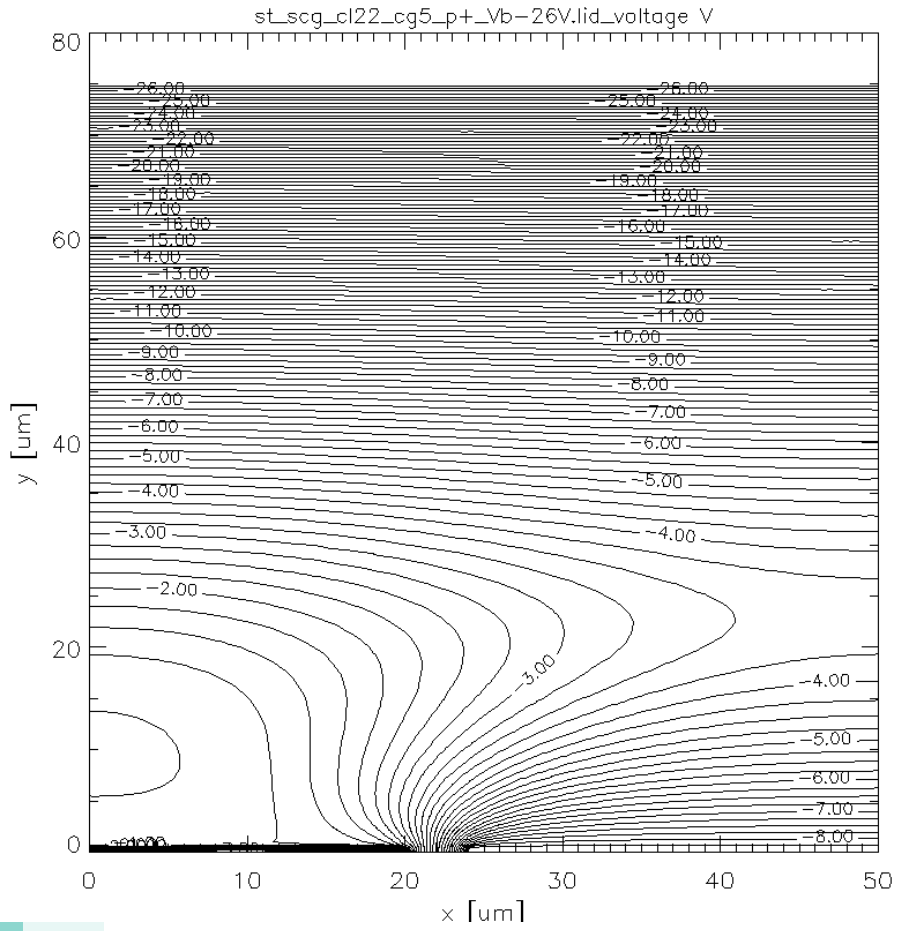
C-CG-Source



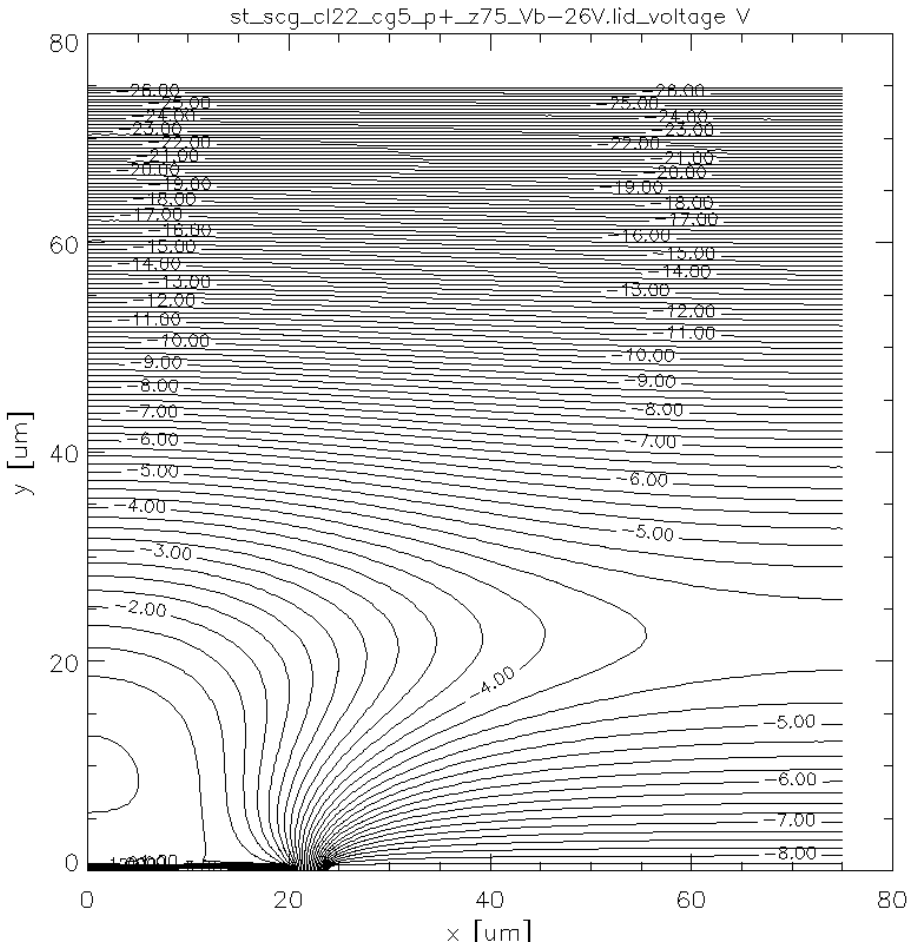
‘global‘ n-doping is necessary here to prevent early hole inversion and to punch the clear path in the depth

C-CG-Drift (Vb=-26V)

Z =50um

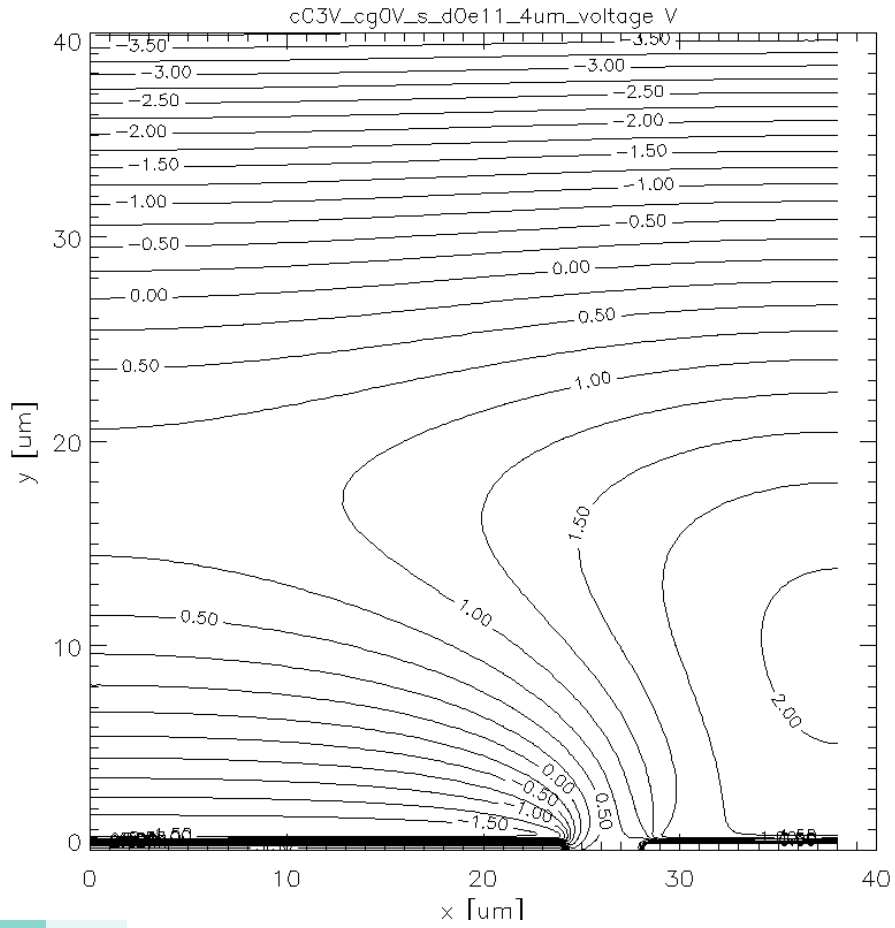


Z =75um

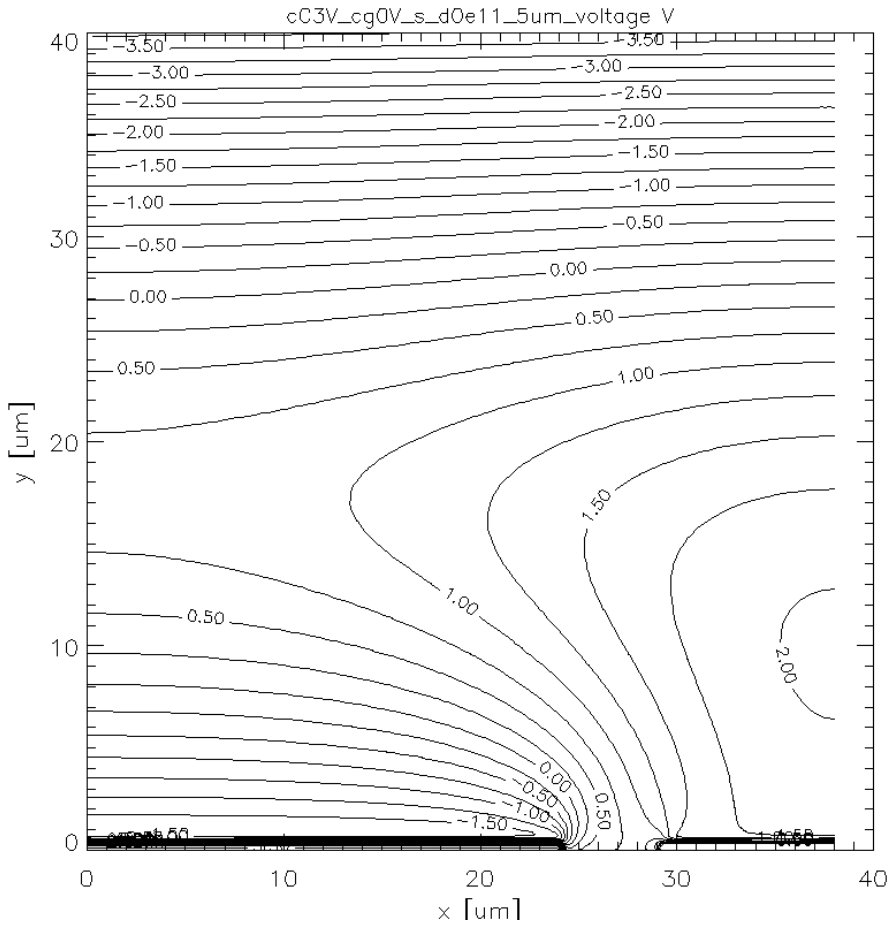


C-CG-S Vc=3V, Vcg=0V

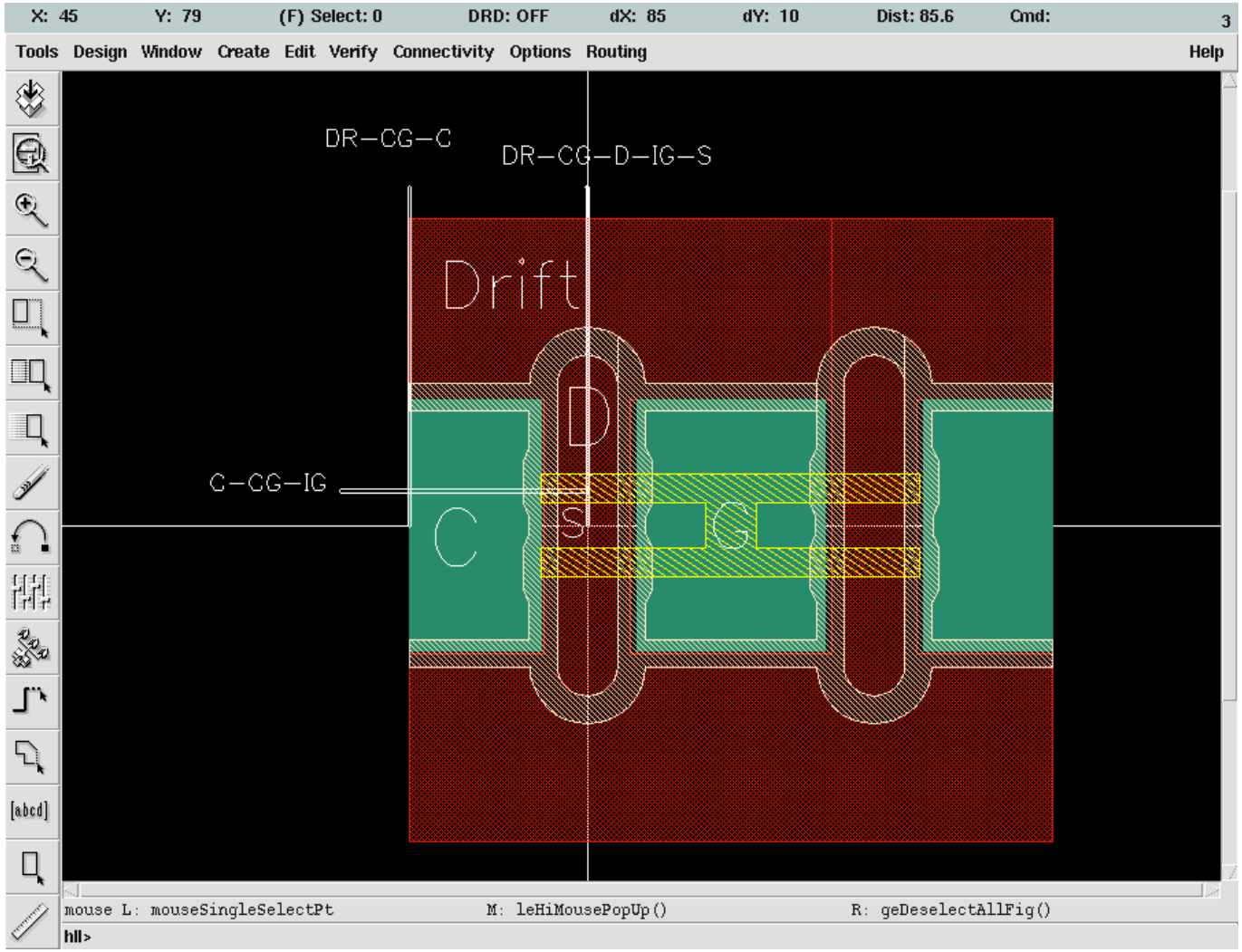
Lcg = 4um



Lcg = 5um

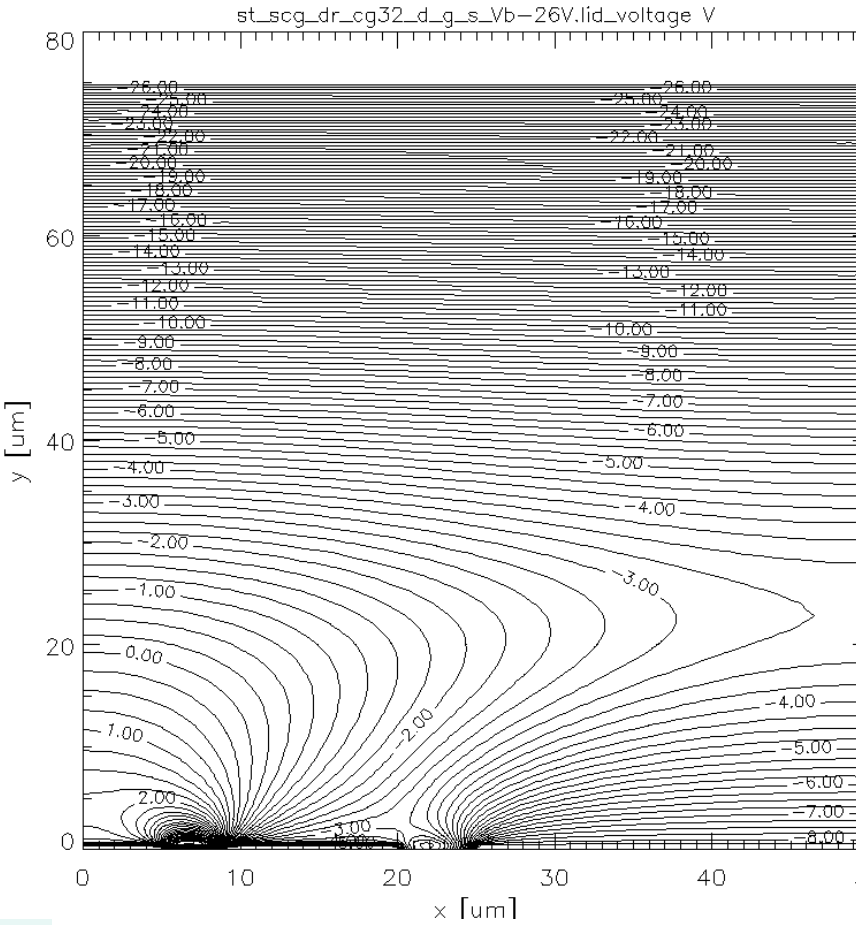


Cut through the transistor

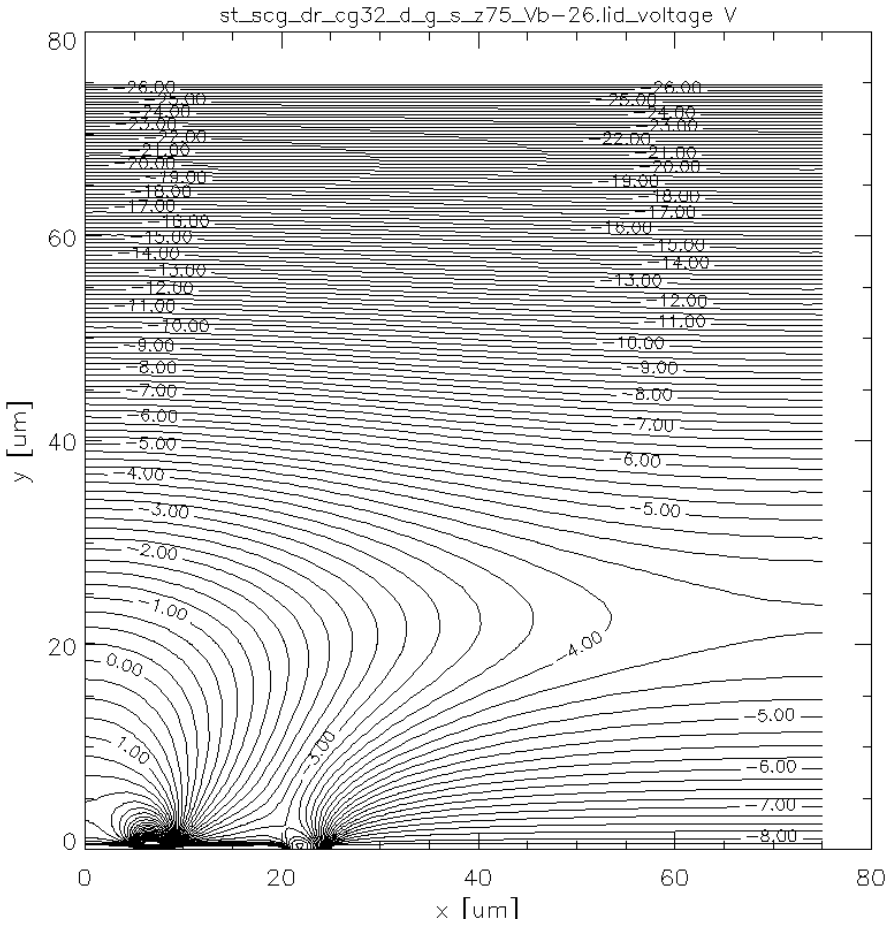


Source-Int. Gate-Drain-CG-Drift

Z =50um

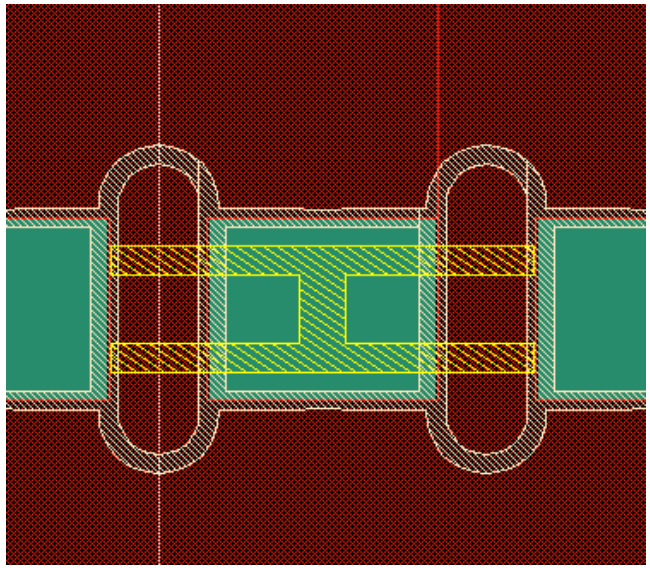


Z =75um

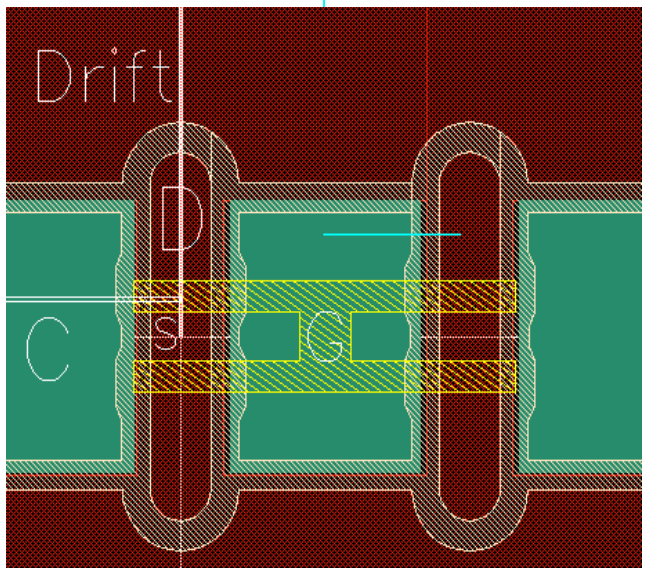


Other pros and cons

PXD 6
ST_SCG …



Modified design



Simpler design to arrange clear line
charge collection should be betterl

larger parasitic drain capacitance

PXD6 technology status

2nd Batch got back side aluminum (3 SOI wafer)

After metal etching, ready for measuring and dicing

in two weeks

2 wafers reserved for DHP and copper

DHP footprint implemented

Next processing step: contact openings between metal 1 and metal2

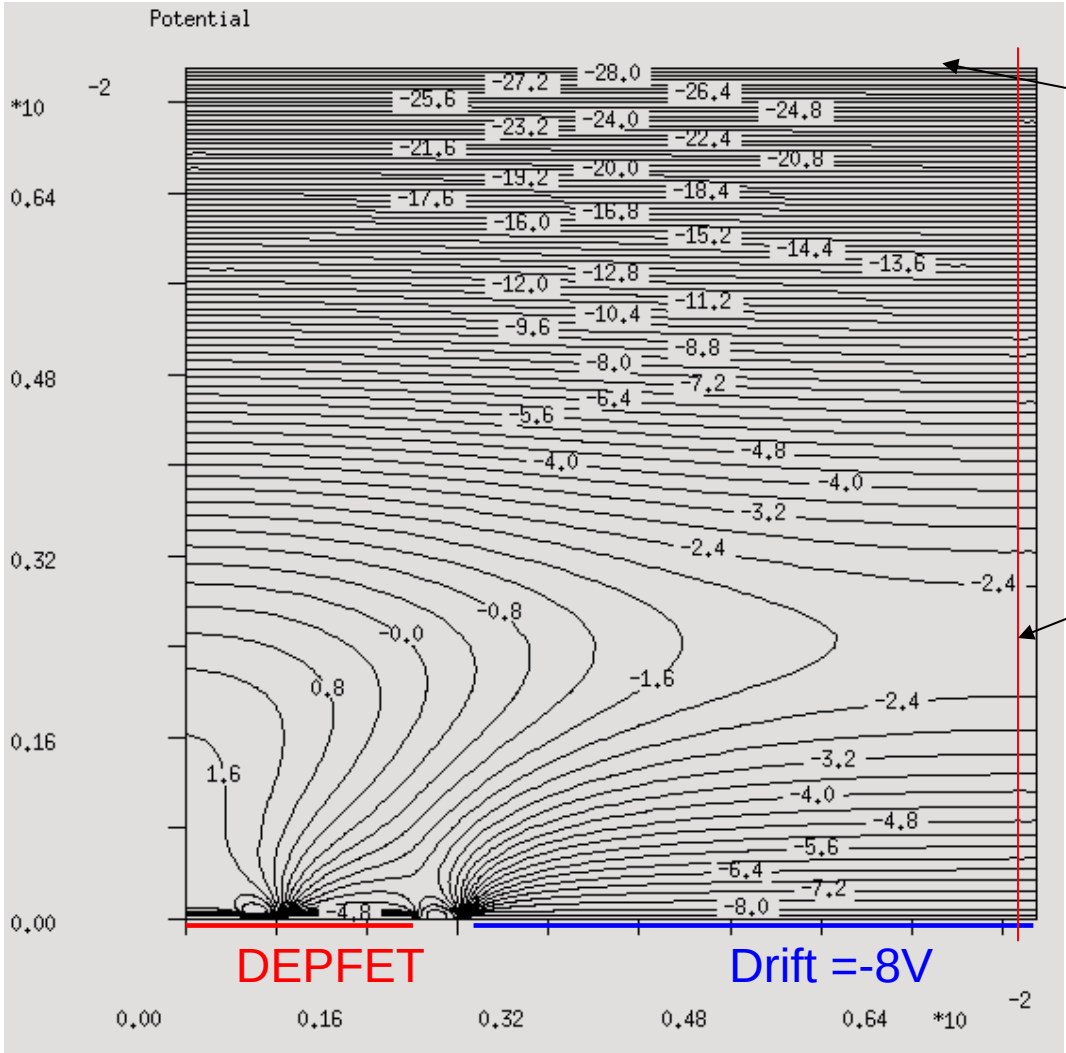
ready in about 8 weeks

Test project to improve the metal 1 / metal 2 isolation has been started

Summary

- - A more radiation tolerant DEPFET pixel design is proposed based on a modest modification of a PXD6 prototype device
- - According to simulations it solves the 'inhomogeneous threshold shift problem' of the Clear Gate
- - further studies necessary, especially 3 D simulation
- - the remaining PXD6 batches are expected soon

Potential distribution along the DEPFET transistor and drift region

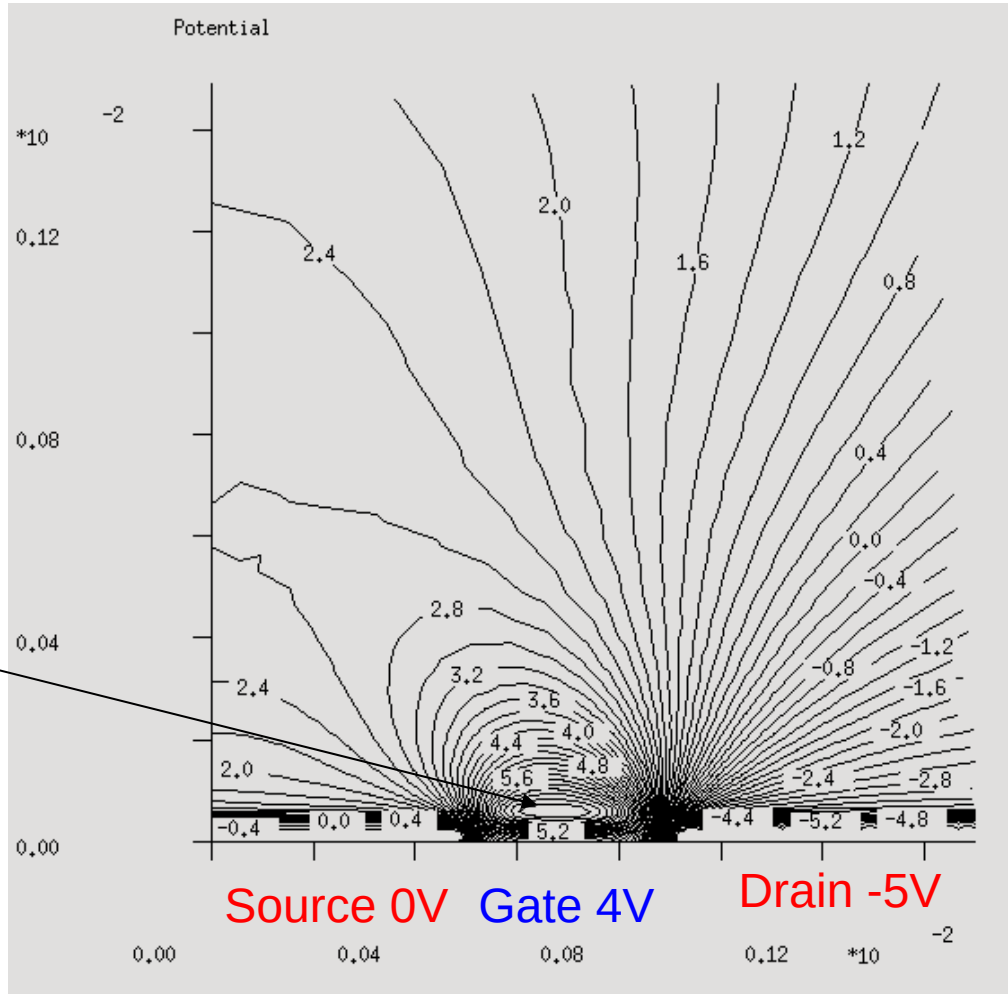


Back contact -28V at 75µm

Generation of 10000 electron/hole pairs simulating a hit at the edge of the drift structure (74µm)

See page 5

Zoom into DEPFET

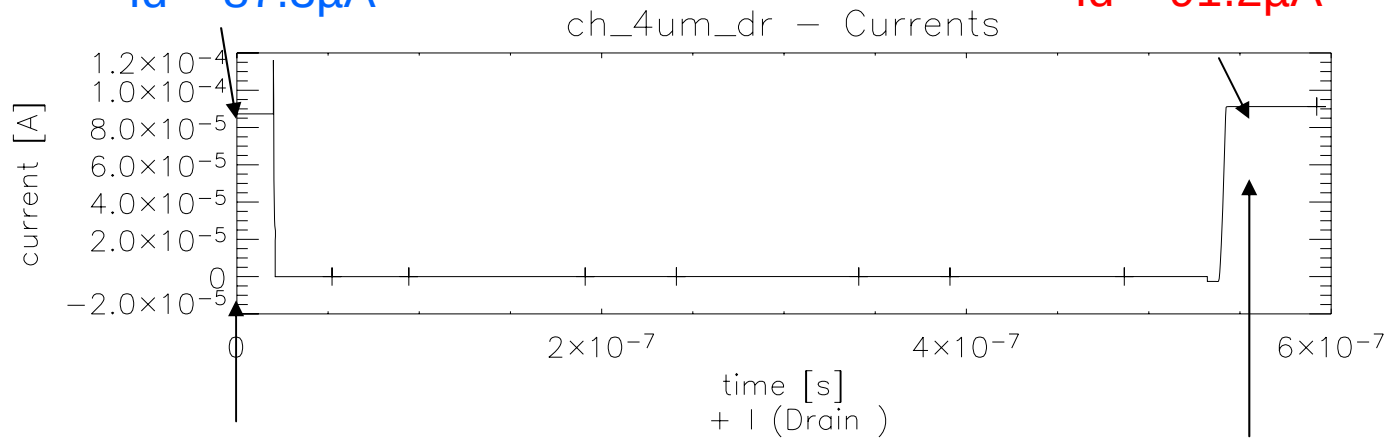


Internal Gate

DEPPFET response

empty internal gate
Id = 87.3µA

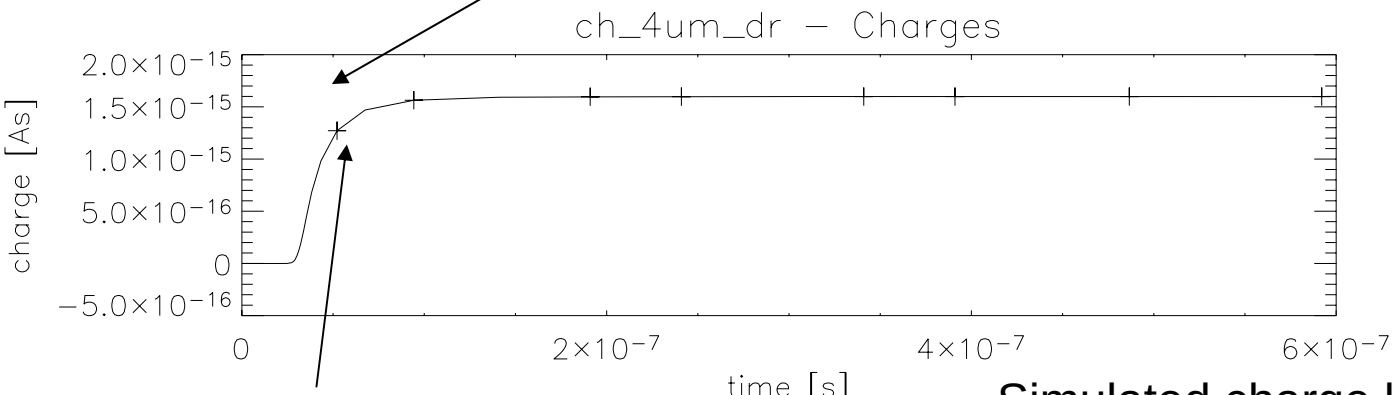
internal gate filled with 10k e-
Id = 91.2µA



Read “0“

Hit

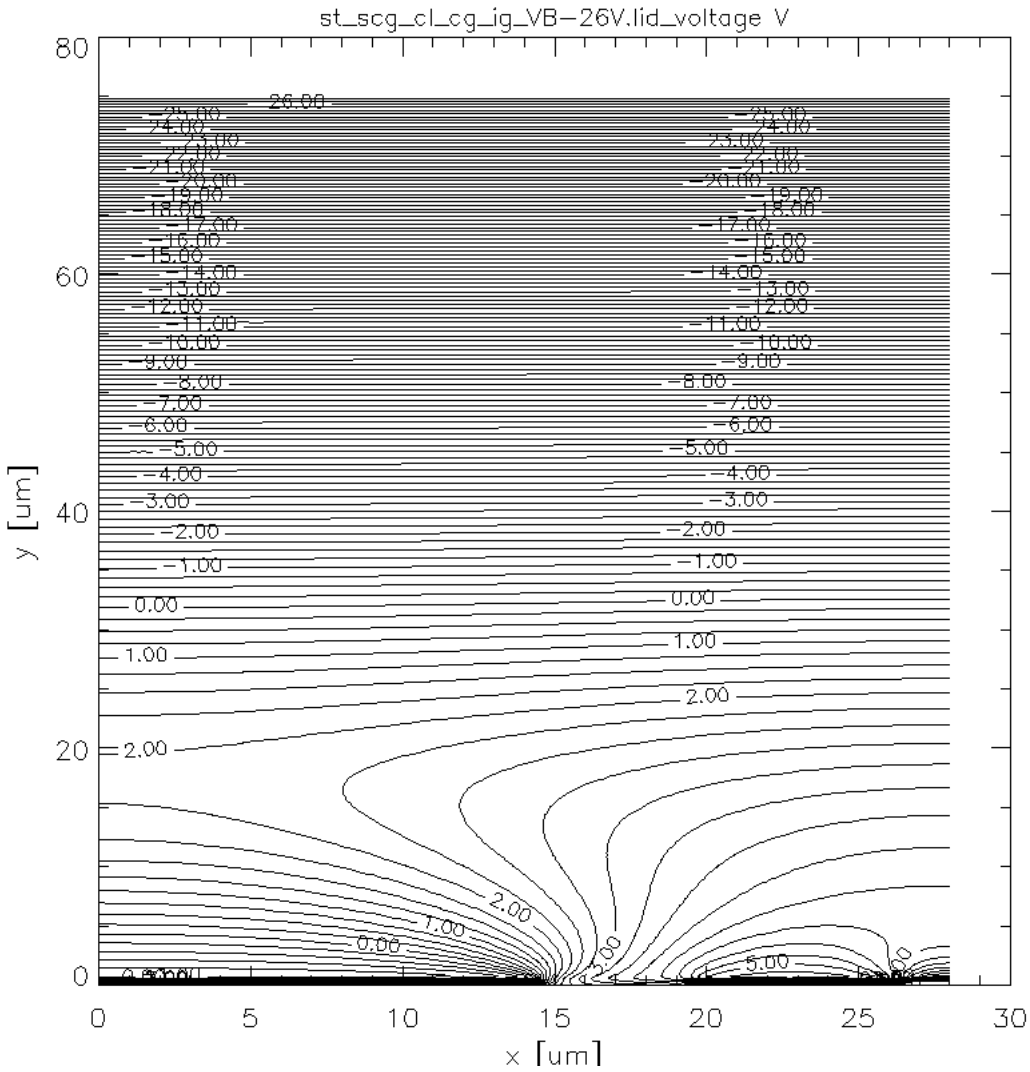
Read “1“



collection time < 100ns (worst case)

Simulated charge loss
< 1e-6

C-CG-IG (Vb=-26V)


st_scg_cl_cg_ig_VB=26V.lid_voltage V
y [um]
x [um]
0
20
40
60
80
0
5
10
15
20
25
30
26.00
2.00
1.00
0.00
5.00