The SOI issue

Raw wafer supply → pre-processing → SOI → DEPFET process → thinning, dicing, mounting..

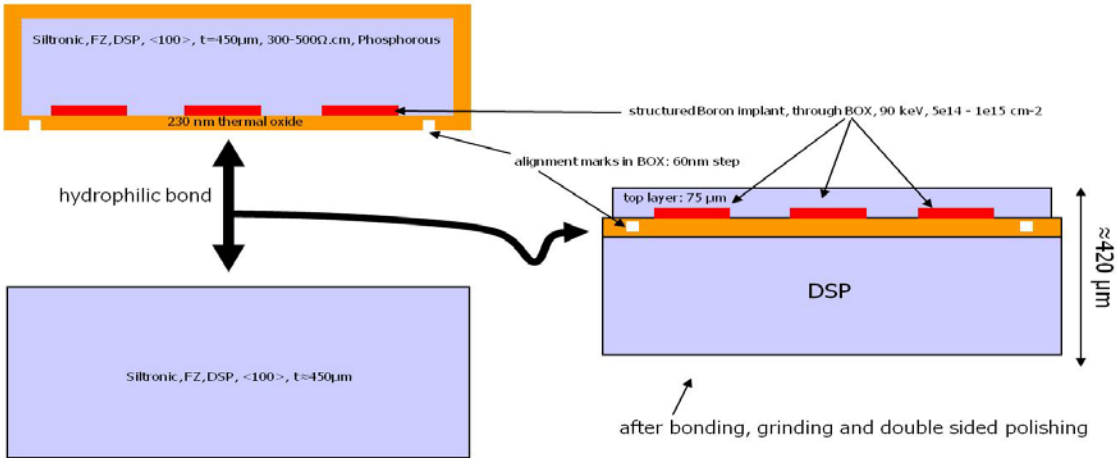
Key Process Modules for (thick) SOI production:

1/ Wafer bonding → *Somewhat special due to our implanted back side*

2/ Edge treatment of the top wafer

3/ grinding and polishing

} *Standard for SOI Wafer production*



→ Original SOI supplier (Soitec) stopped this kind of SOI production
→ Need to find and qualify new supplier or supply chain

Overview of the actions since Bonn

0. Preparation of 12 (top) wafers at HLL: oxidation, alignment mark litho, implantation

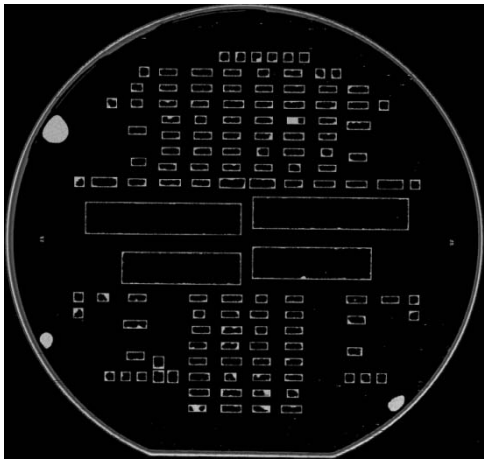
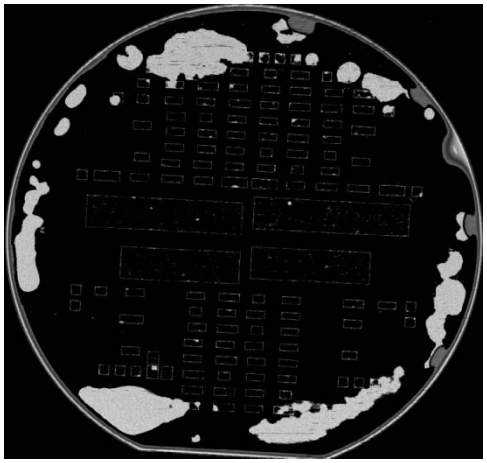
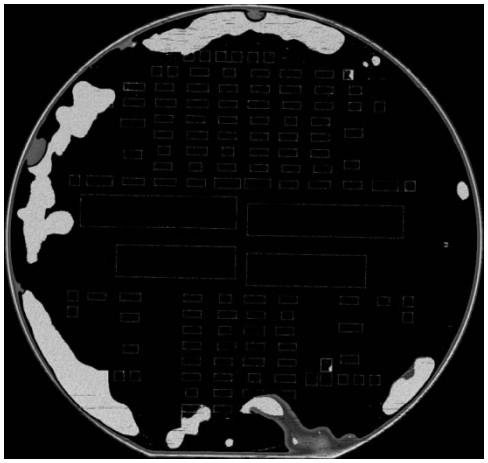
1. Order at VTT:
   - -: VTT to prepare their own top wafers and bond them to their base wafers → done
   - -: test the polishing quality at VTT → done
   - -: Complete SOI process with 6 wafers from HLL → wafers sent , wait for process plan

2. Order at Icemos:
   - -: Icemos to prepare their own top wafers and bond them to their base wafers → done
   - -: check the new edge trim of Icemos → wait for samples
   - -: Complete SOI process with 6 wafers from HLL → wafers will be sent to Icemos end of this week

3. Qualify sub-steps like edge trim and polishing separately:
   - -: grind and edge trim at Disco → done
   - -: test the polishing quality at Rockwood → done

Status VTT – Bonding pre-test

3 wafer pairs (un-thinned) with 3 different temperature treatments before bonding (SAM)

→ many and partly huge voids

-: larger ones along the edge of the wafers

-: but also at the edges of the implants!

Possible reasons:

-: bad resist removal → large voids at the wafer edge

-: oxide seems to be thinner in the implant region → voiding at that step
step was measured at the VTT wafers (~10nm-15nm)
and HLL wafers (~5nm-10nm)

Possible remedy:

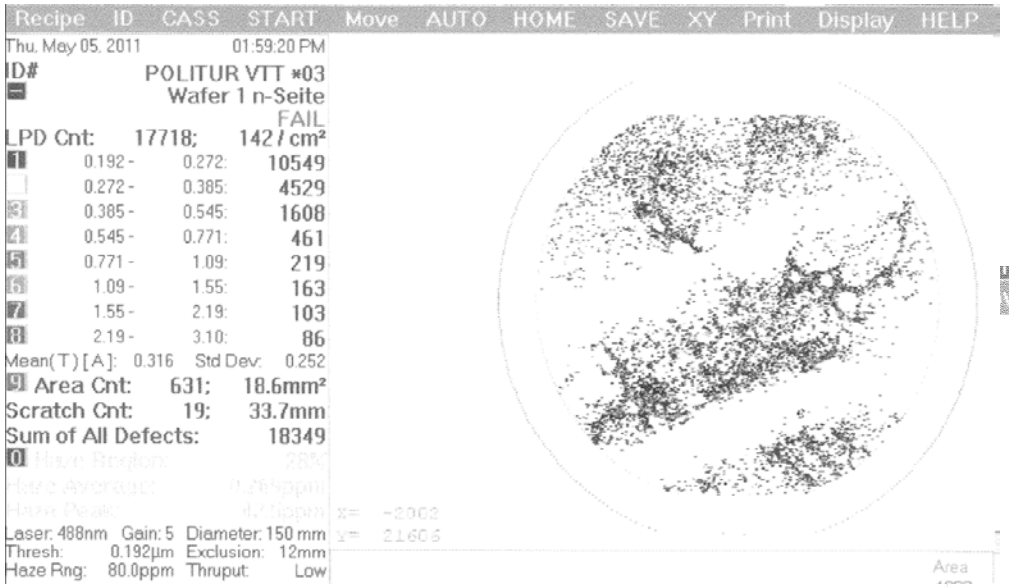
-: improve cleaning/resist stripping after implant

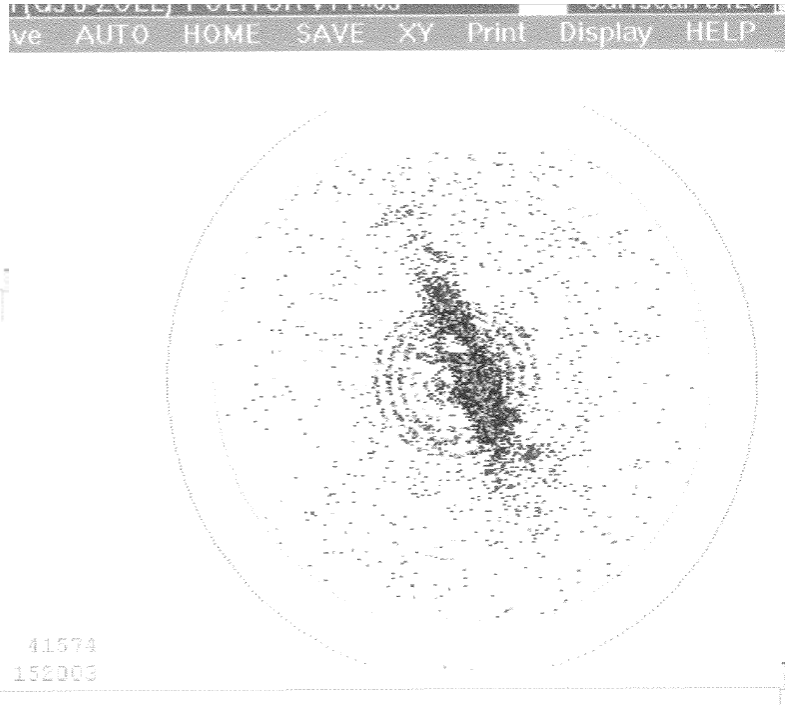
-: planarization of the surface before bonding → under investigation

Status VTT – CMP Quality

-: 2 DSP wafers were sent to VTT for polishing and cleaning on their line

-: VTT polished one side and sent the wafers back → check quality (particles, defects) at HLL

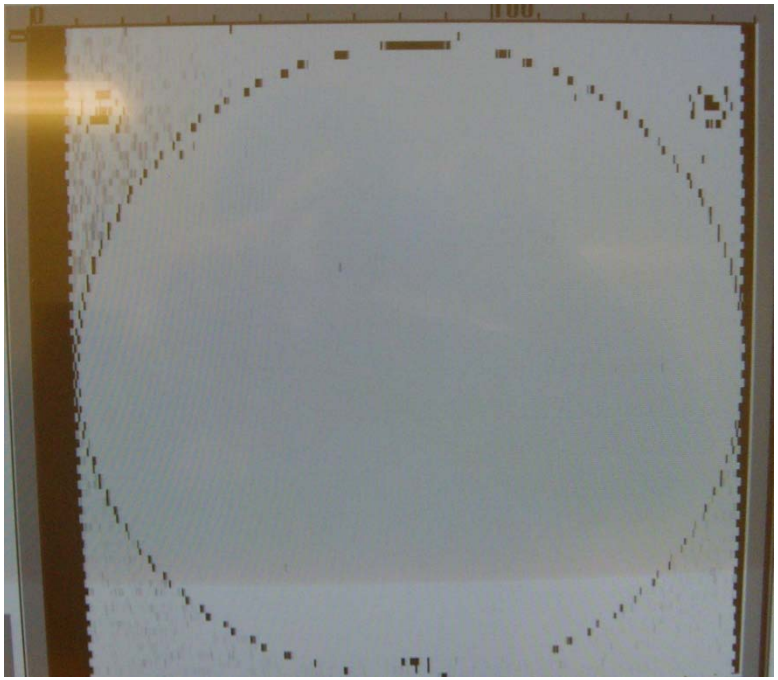




Edge trim quality of SOI still unknown !!

Status Icemos

-: 5 wafer pairs were bonded after implantation through BOX
-: Icemos claims that there were no steps in BOX due to the implant
-: void free bonding, documented by SAM pictures and back grinding of the top wafer down to a few microns



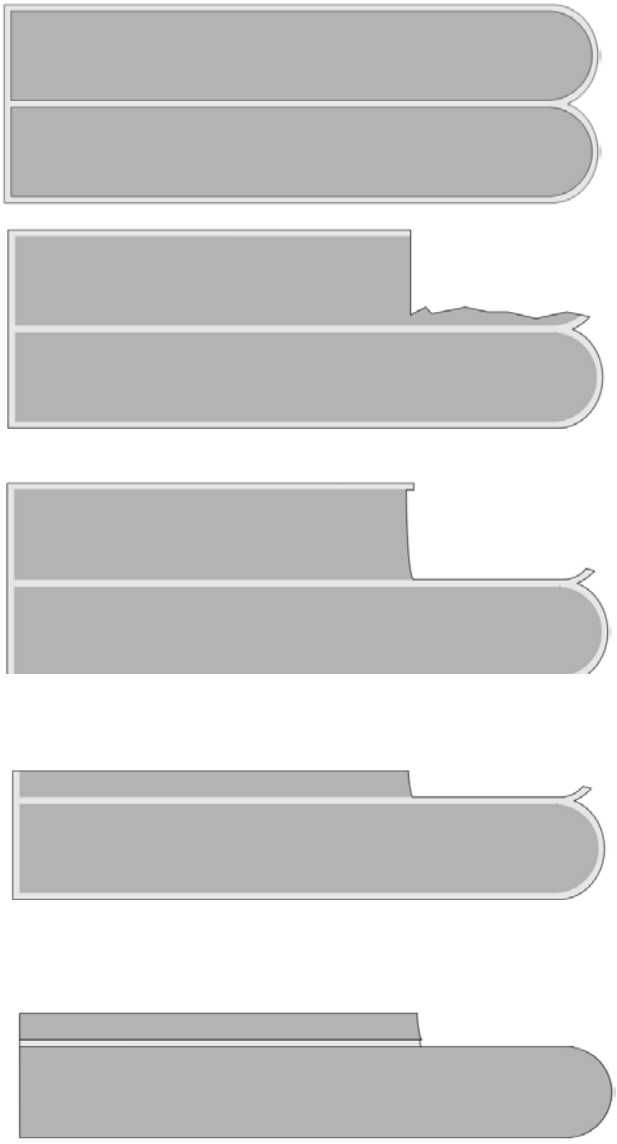
→Icemos seems to know how to bond

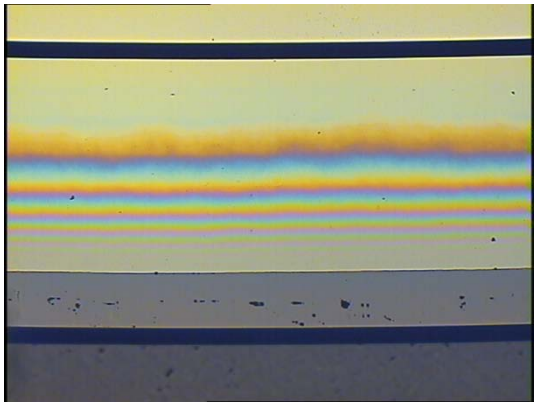
→ next step is to send them our top wafers (oxidized and implanted at HLL) let them repeat the exercise

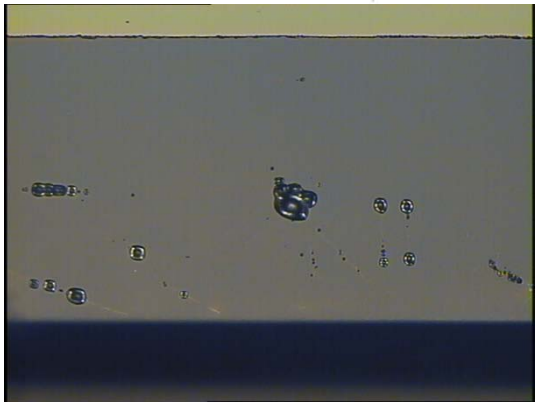
Caveat:

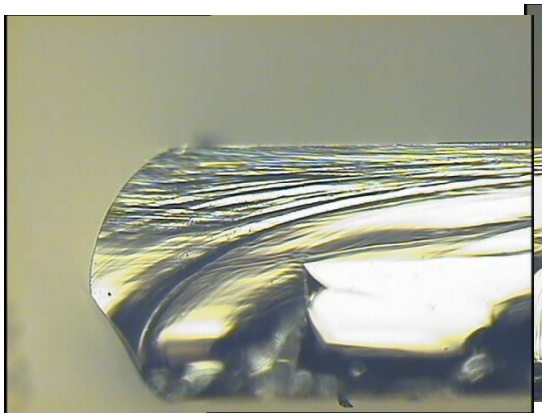
No information of polishing quality and edge trim. From previous orders, we know that these are weak points at Icemos.

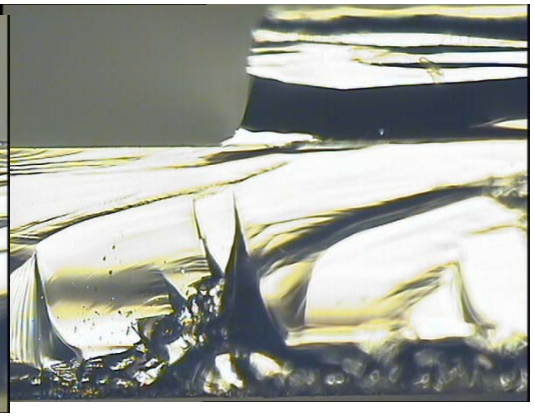
Status Edge Trim → Disco







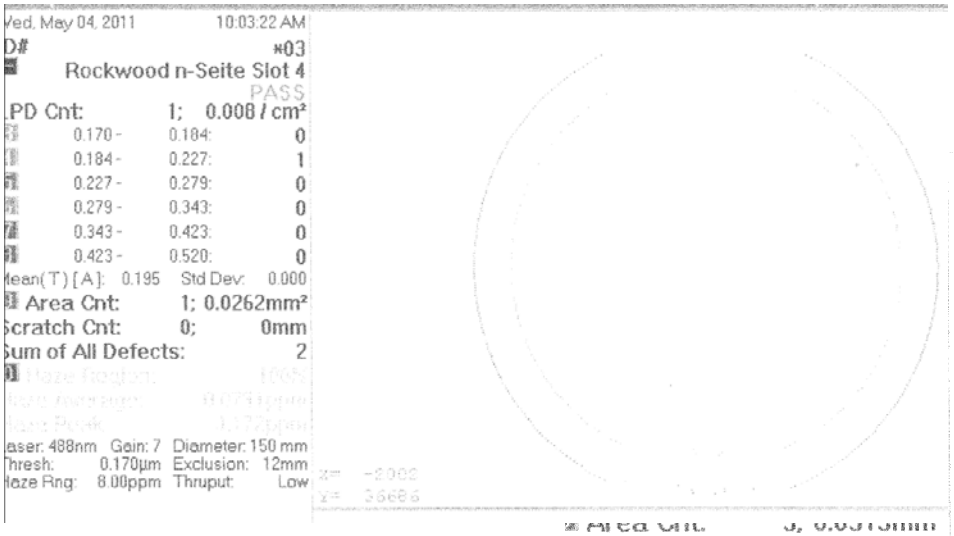


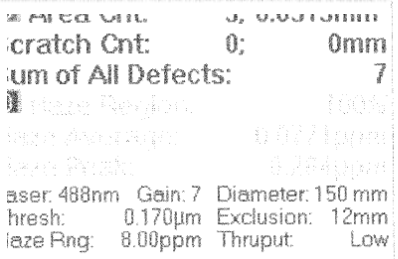


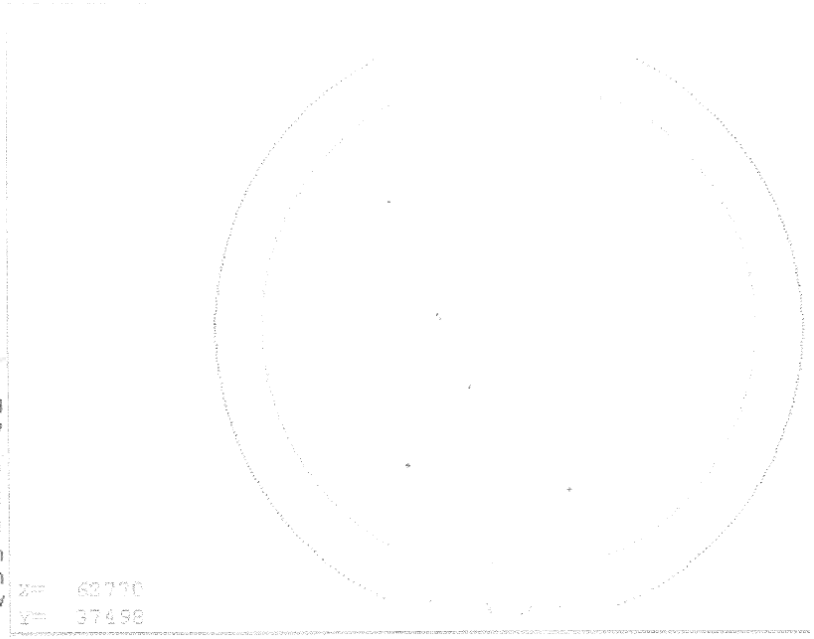
Nice edges, but some yield issues with the edge of the of the handle wafer (chipping due the grinding step). Needs still some improvement ..

Status Polish and Clean → Rockwood

-: Rockwood is a wafer reclaim company located in France close to Marseille
-: specialized in CMP, thinning and cleaning of wafers
-: after the second trial, excellent results (6 Wafers) in terms of defects and metal contamination.
The specified roughness of the of the surface (r_a=0.1 nm) needs to be verified
-: At the end of the day, test devices made on Rockwood polished wafers will count







-: planned visit at Rockwood to discuss the next steps

-: Rockwood is interested to do also the edge trim!

In Summary

-: We are making progress but we still don't have a qualified solution.

-: Icemos seems to able to bond implanted oxides, needs to be verified on our wafers.
Quality of their edge and polishing still unclear (it is bad actually, if they do not improve).

-: The cooperation with VTT is useful to get more insight in the process and to find a safe process window for the bonding.
Polishing quality of VTT not satisfactory, edge treatment still unknown

-: Progress with Disco, but procedure needs to be optimized.

-: Polishing problem seems to be solved with Rockwood. The company is interested to develop also a reliable edge trim procedure with us.

Backup slides follow