X-ray irradiations on thin oxide test structures

7th International Workshop on DEPFET Detectors and Applications

Ringberg 8-11 May 2011

Status and plans

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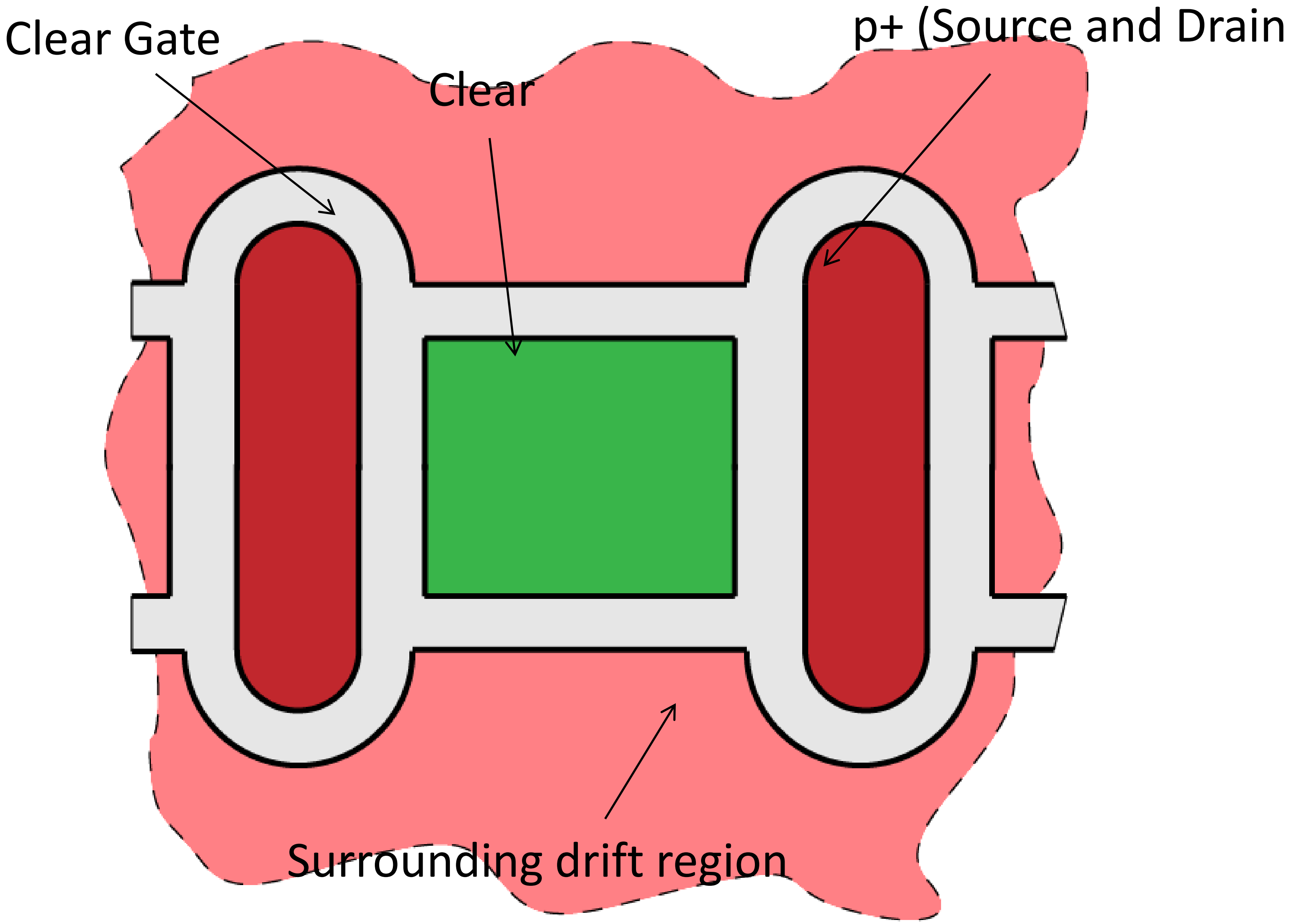
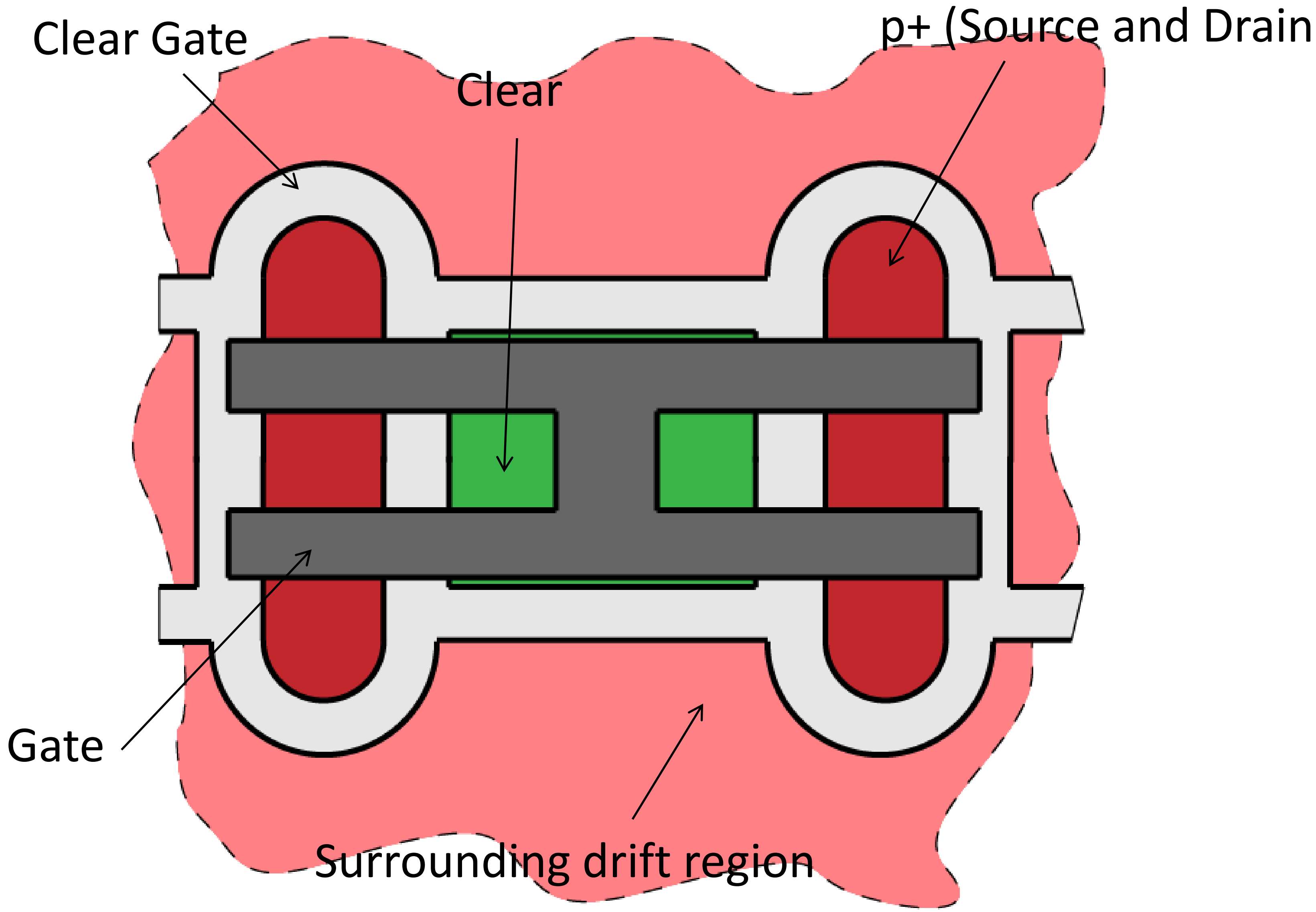
Outline

1. Motivation: Possible pixel layout
2. Aim of irradiation campaign
    1. Possible chip layout
    2. Results from former campaign december 2011 (already presented in Bonn)
3. Irradiation campaign april 2011 in Karlsruhe
    1. Clear Gate
    2. Sensitive area and cross sections
    3. Threshold voltage shift
    4. Influence of gate voltage
4. Conclusion & Outlook

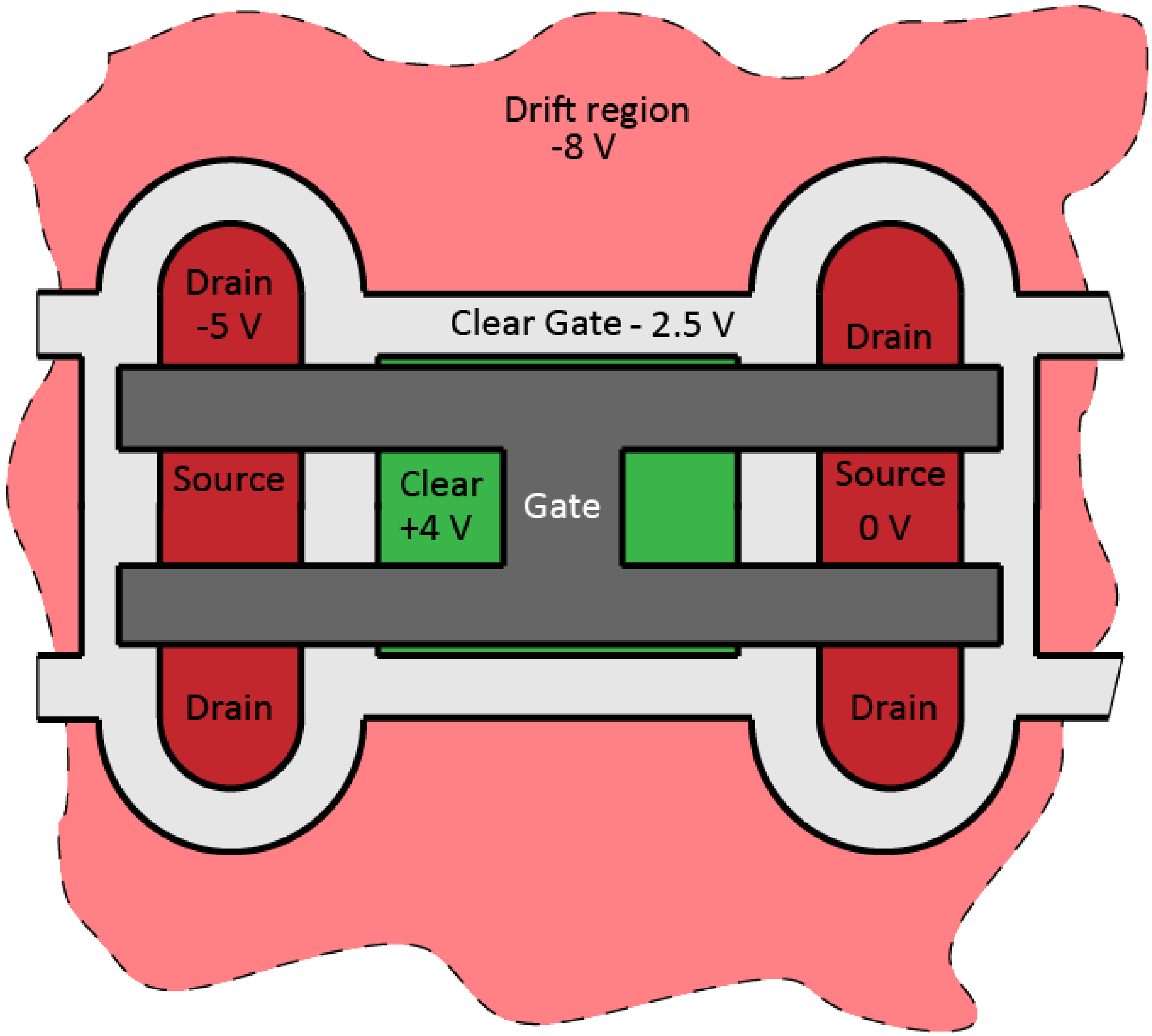
Motivation - Possible Pixel Layout



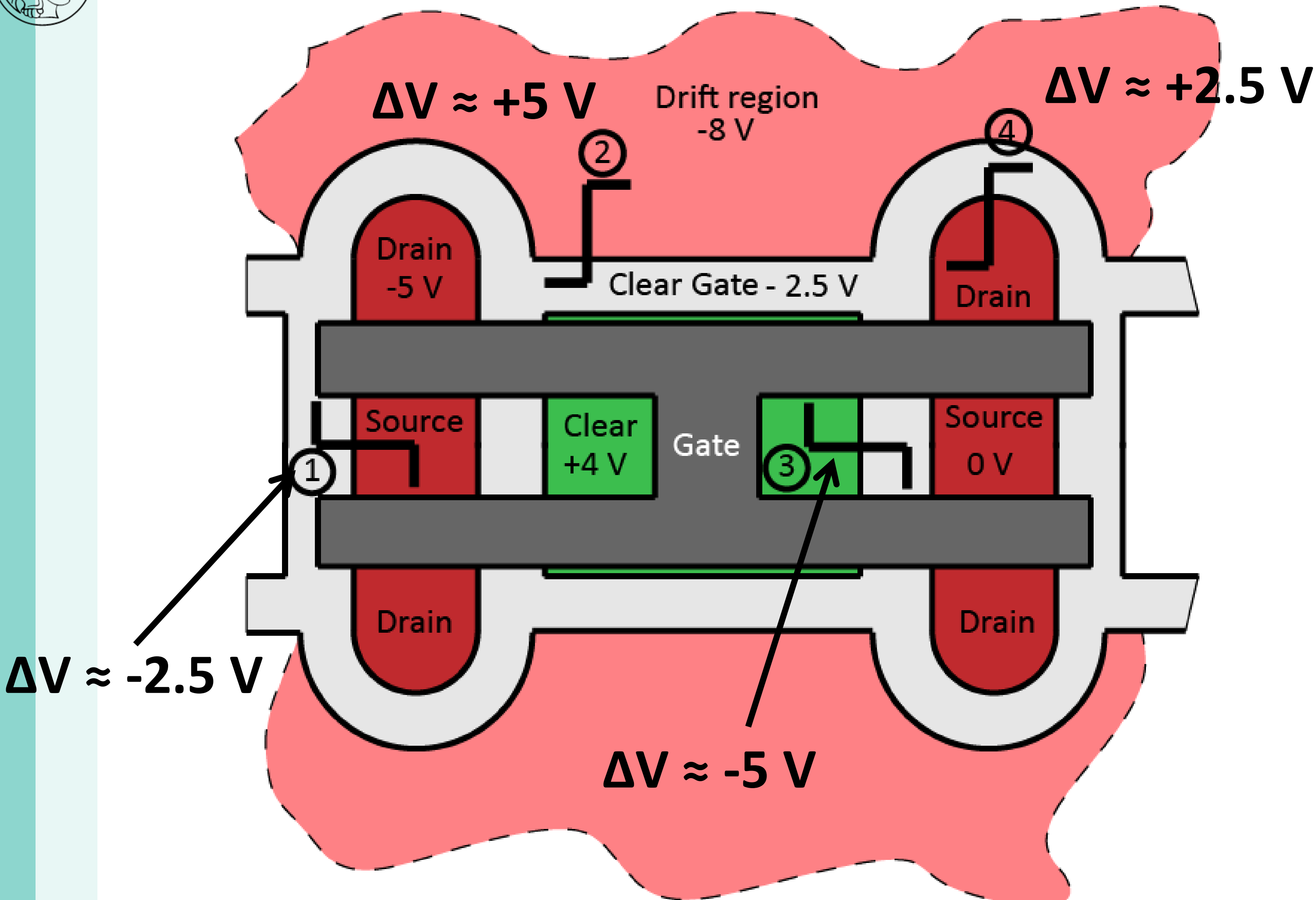
Motivation (II)- Possible Pixel Layout



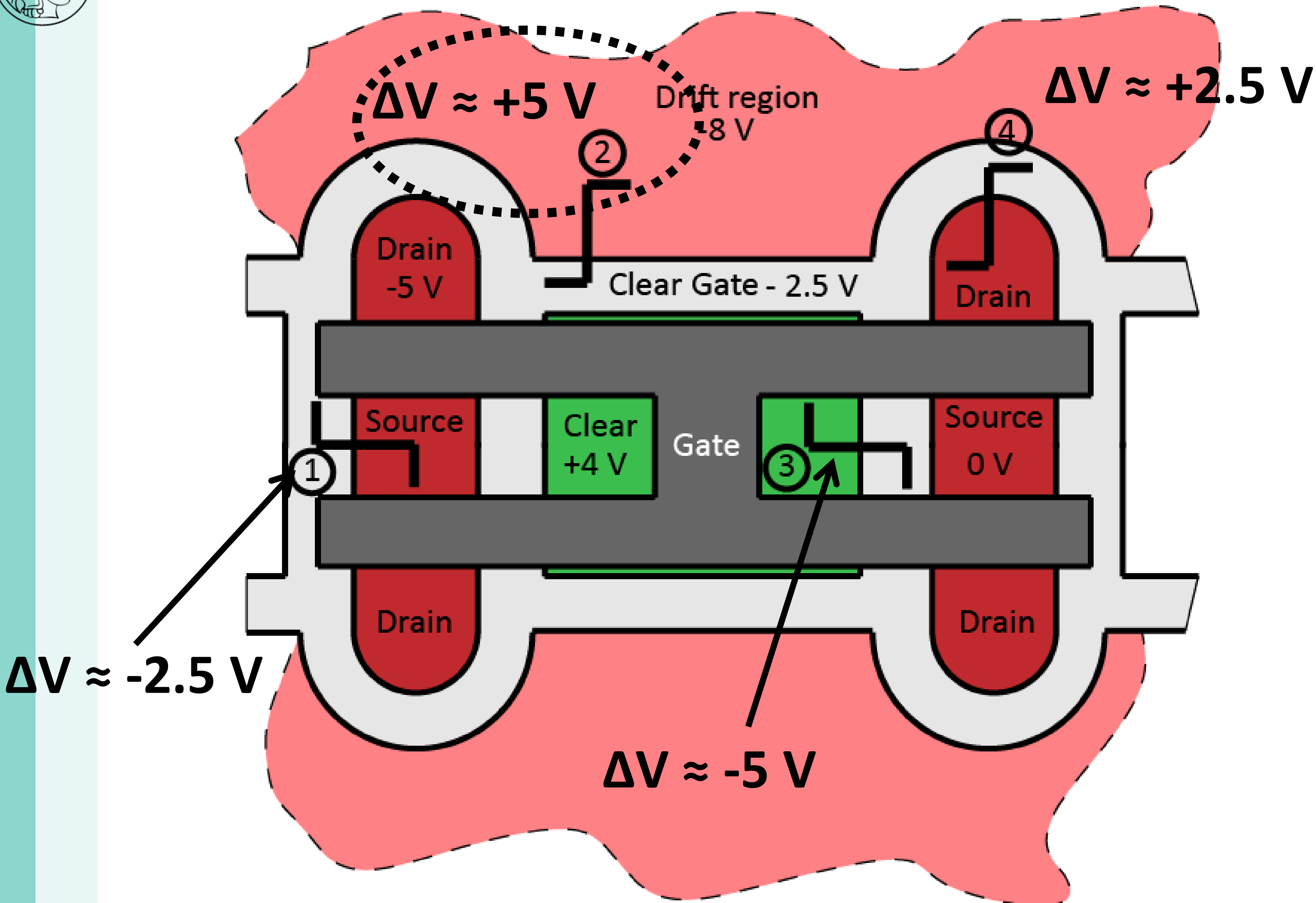
Motivation (III)- Possible Pixel Layout and Potentials



Motivation (IV)- Possible Pixel Layout and relevant cross sections



Motivation (IV)- Possible Pixel Layout and relevant cross sections



Goals and setup from last campaign

Idea

- **10 nm Si_3N_4** has proven to be a promising candidate from previous irradiations campaign

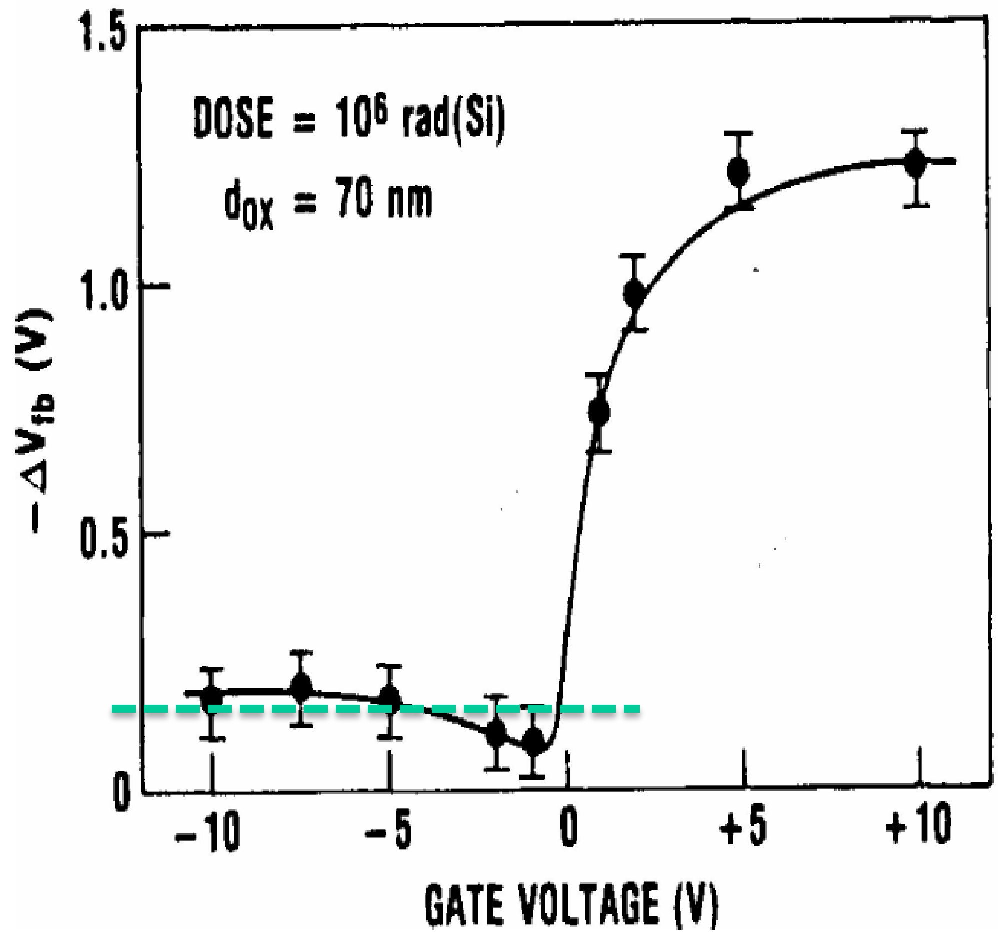
Aim

- Investigate irradiation effects at Clear Gates, especially voltage dependent behavior

Devices

- Doping of chosen transistors is similar to a DEPFET Clear Gate
- Dimensions are similar to PXD 6

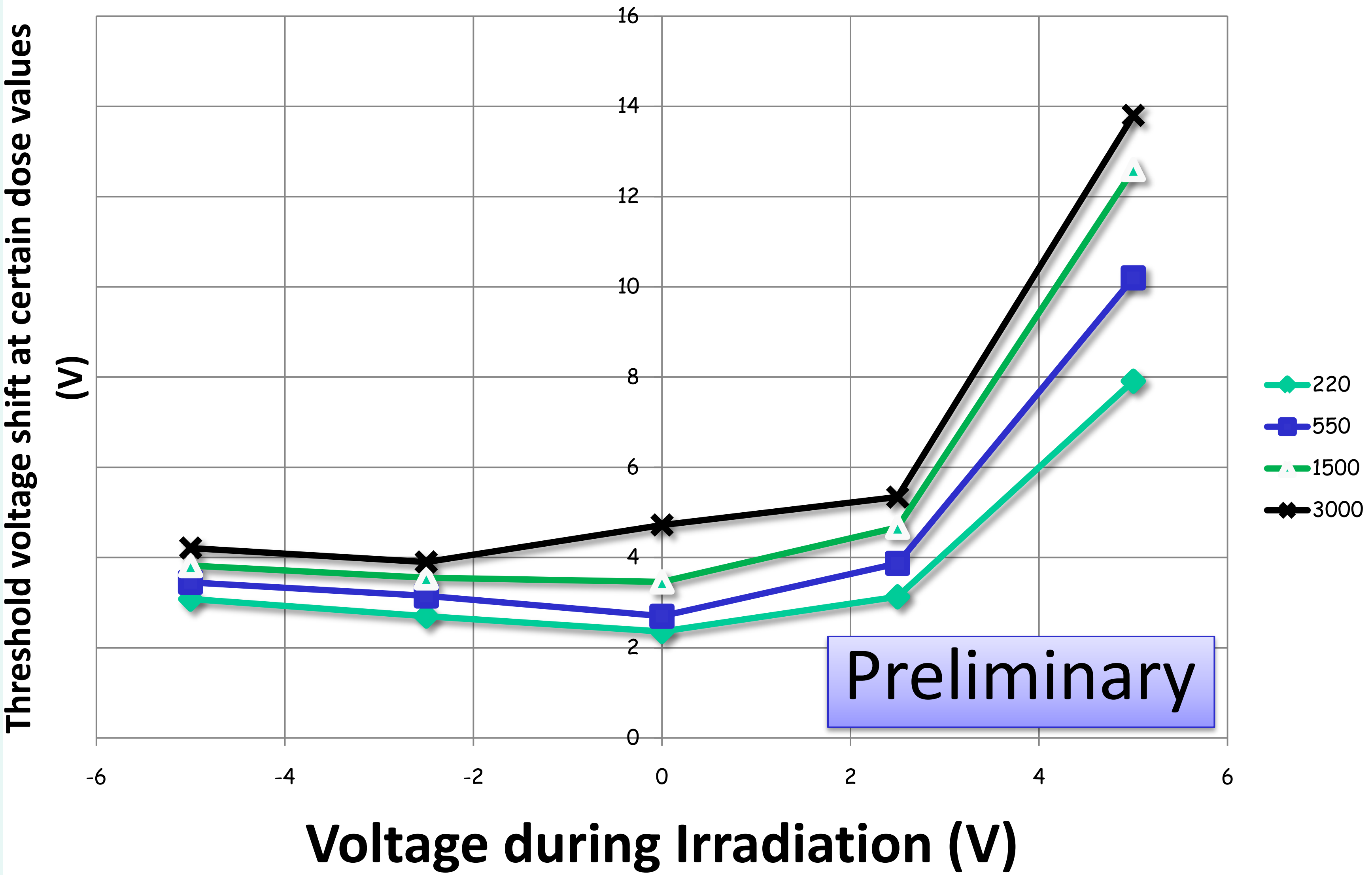
Change in threshold voltage shift due to certain Gate voltages



Ma/Dressendorfer

Only one Clear gate volatge avialable → **flat** region is favoured

Change in threshold voltage shift due to certain Gate voltages (10nm)

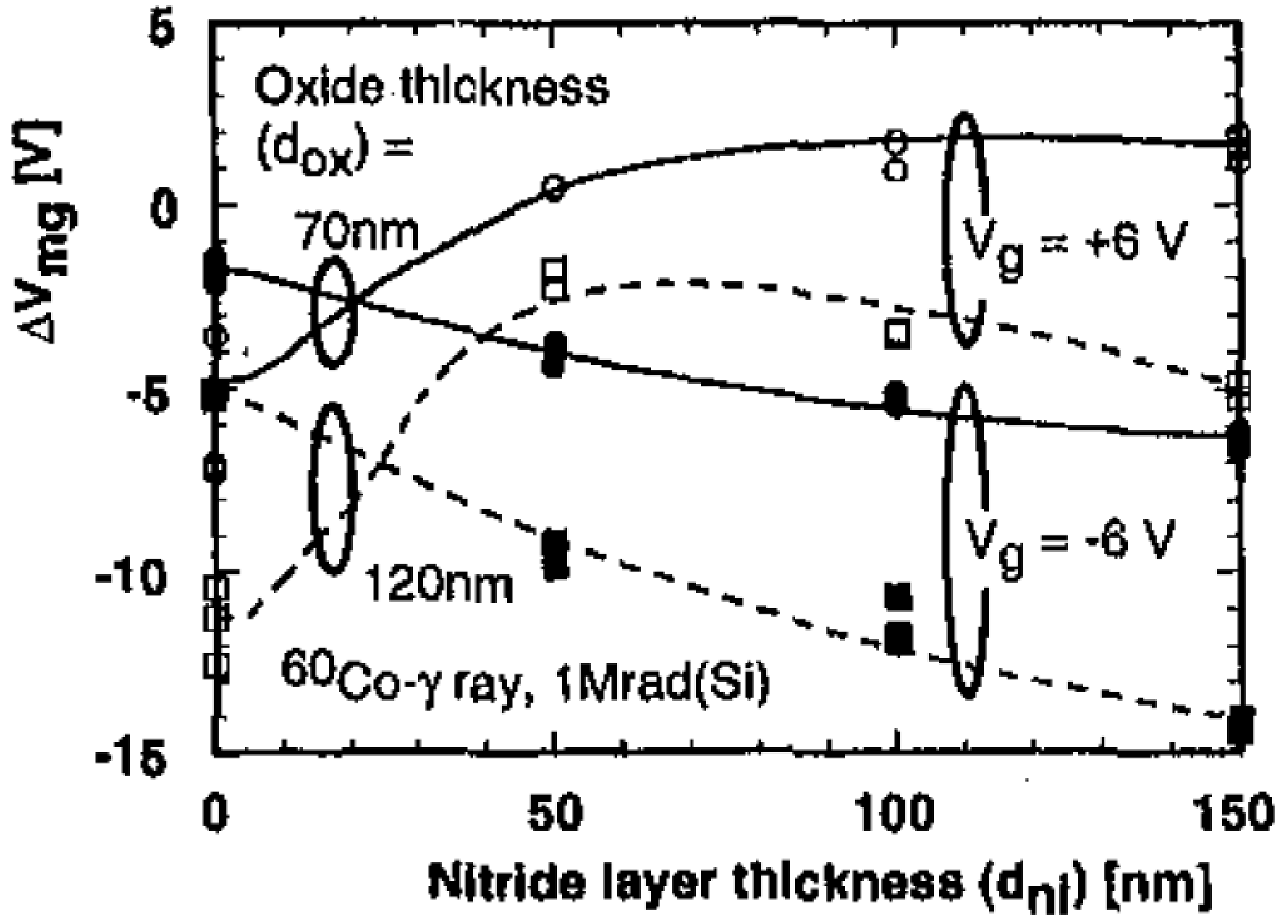


Conclusion from former (10 nm) Campaign

- Influence of Gate voltage during Irradiation was severe, especially positive voltage. This happend in the cross section from Clear Gate to drift regions
  - More irradiation campaigns needed to see, whether more nitride can help
  - New design of selected areas?

Thick nitride and Gate voltages

Thicker nitride could be a solution to the problem at hand.



Radiation-Induced Trapped Charge in
Metal-Nitride-Oxide-Semiconductor Structure; Takahashi et. al.
IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL 46, NO 6, DECEMBER 1999

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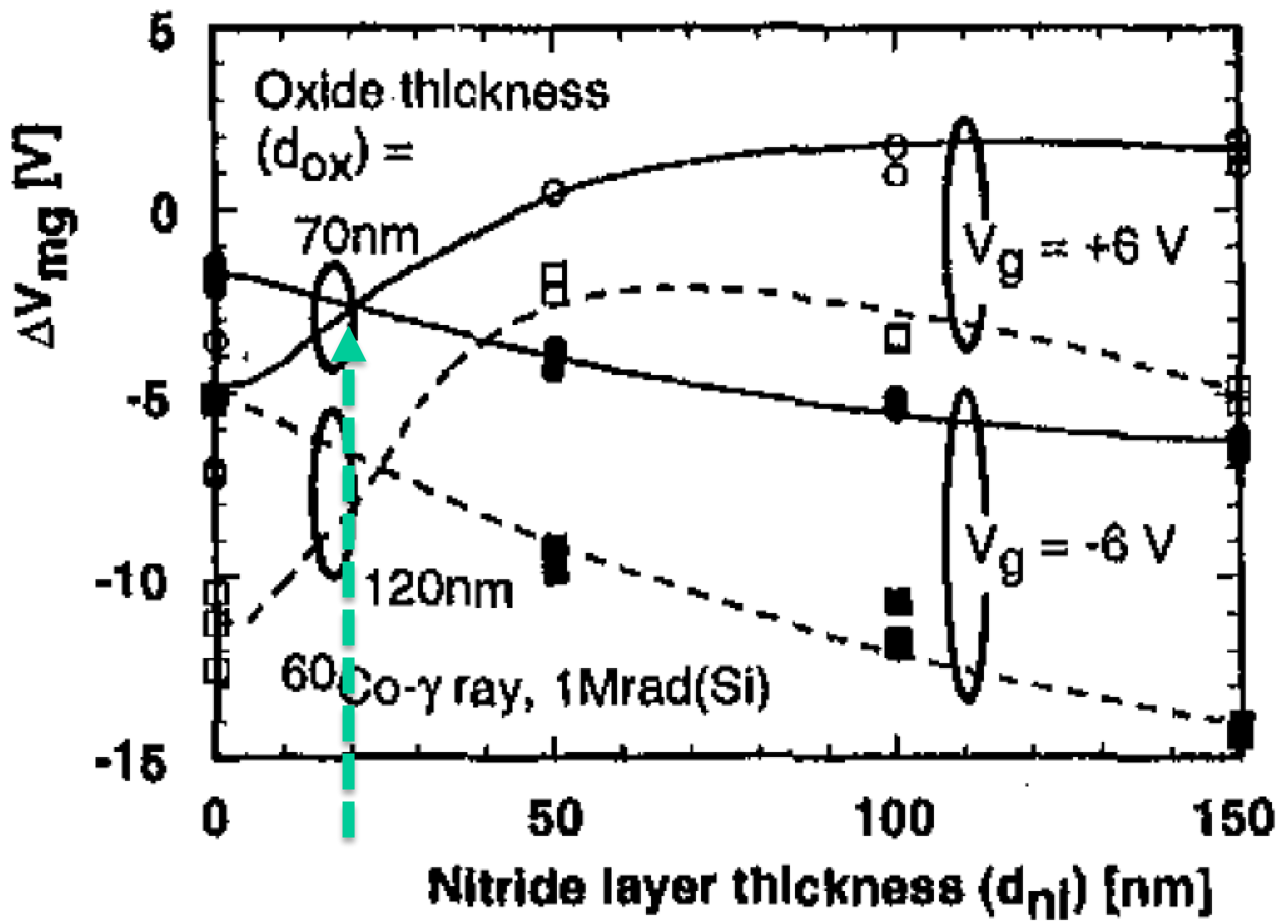

Radiation-Induced Trapped Charge in Metal-Nitride-Oxide-Semiconductor Structure; Takahashi et. al.
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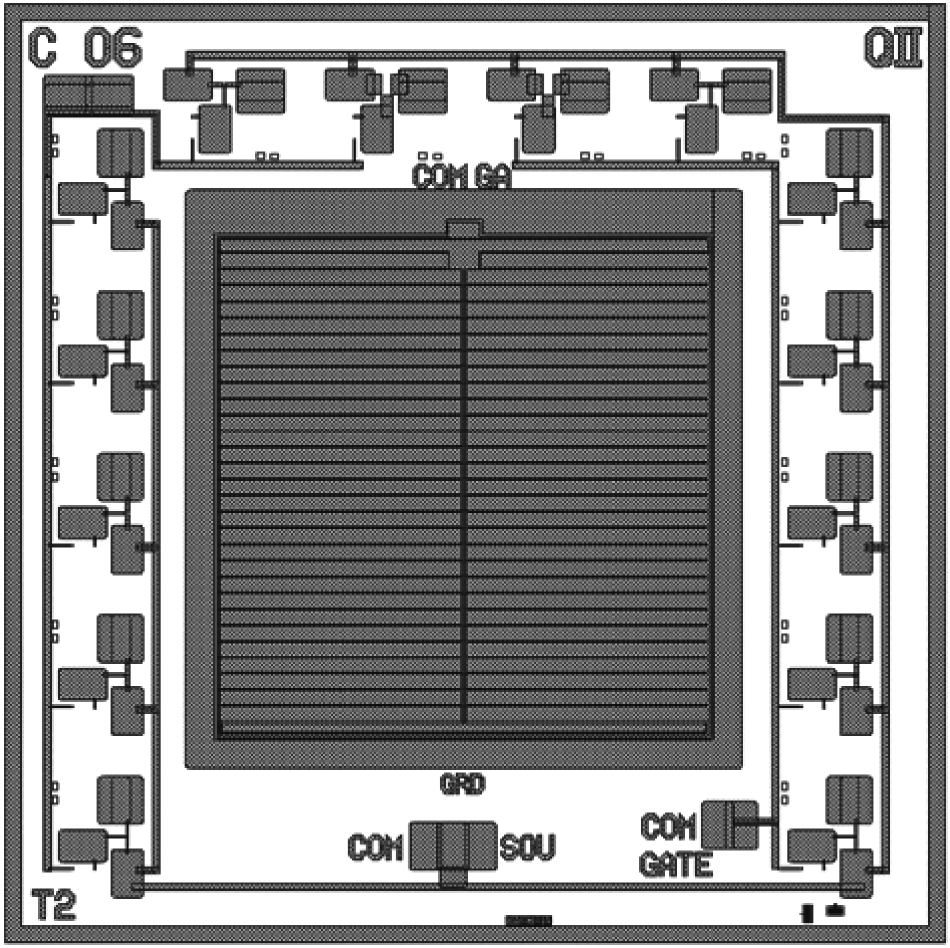
Influence of Gate Voltage during irradiation

NEW X-RAY IRRADIATION IN KARLSRUHE

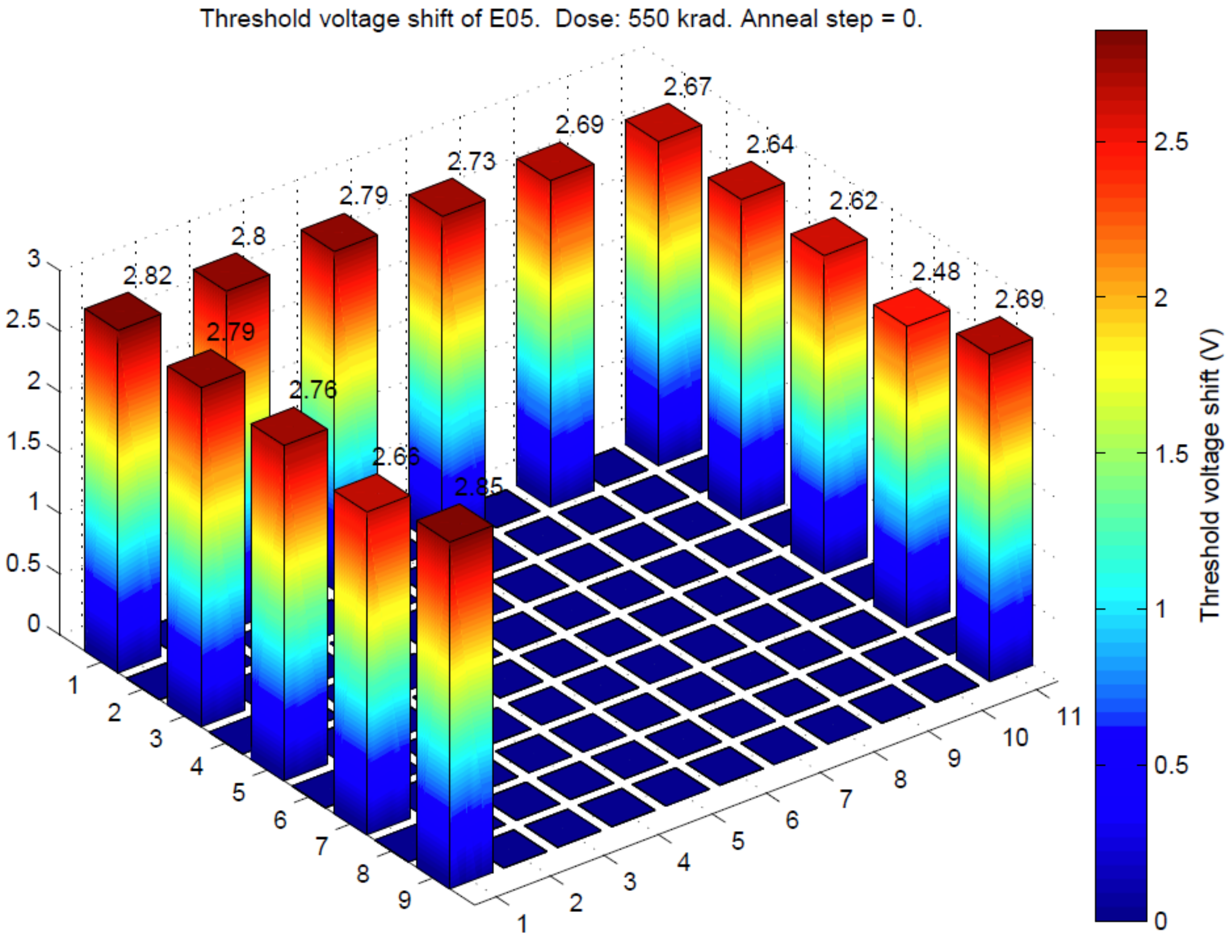
Layout of thin oxide devices



Characteristics of thin oxide structures:

- 20 nmSi_3N_4
- SiO_2 thickness is the same for all
- Central device: Gate Controlled Diode
- 14 Transistor (=2x7), with diff. Gate length and width
- Doping profiles similar to Clear gate

Homogeneity of Beam



Beam /Tube parameters:

•Distance: Exit window – DUT = 123 mm

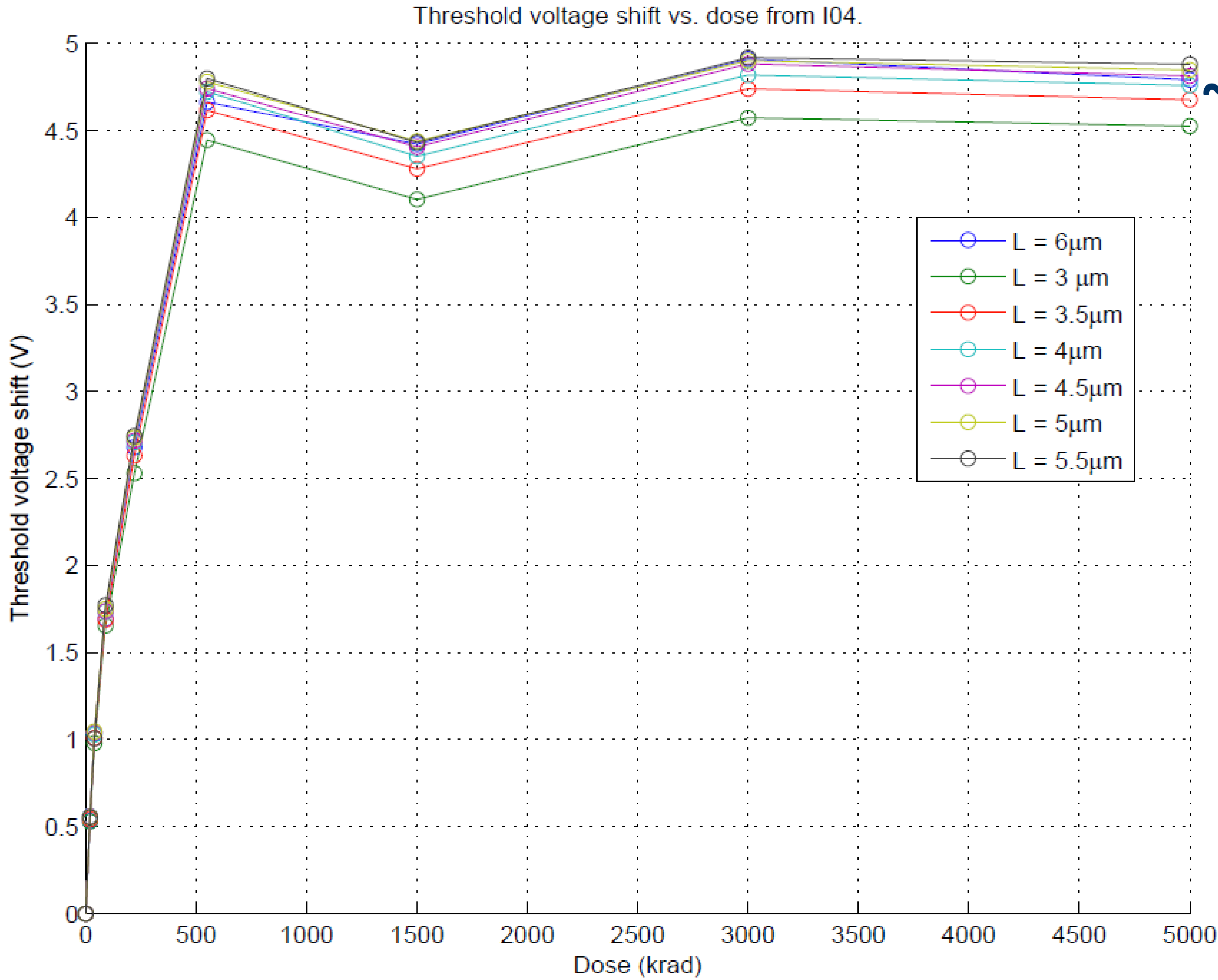
•Fe-filter

•60 kV, 33 mA

•Beam radius = 6.6 mm

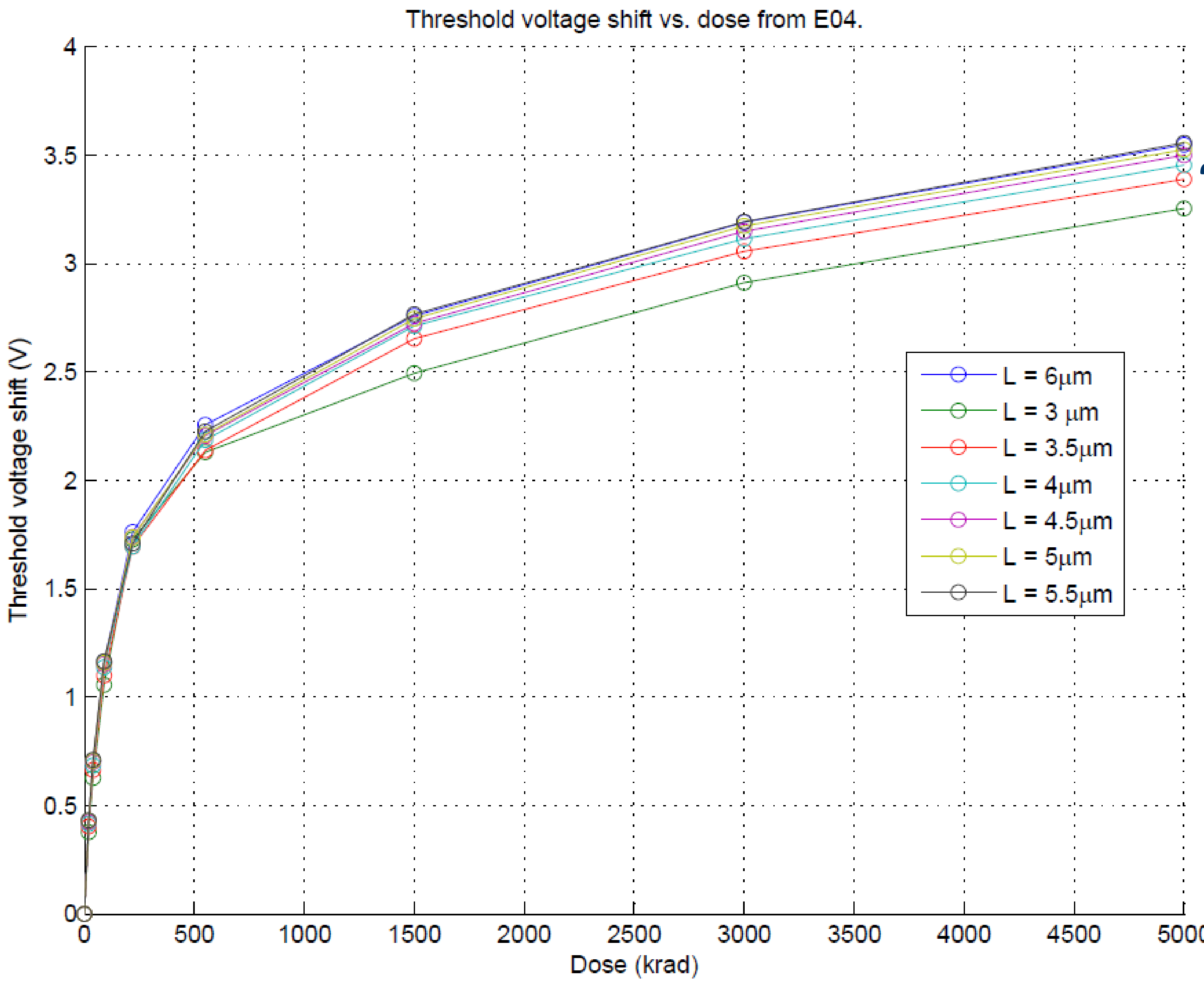
Low dose rate (~570 krad/h), but homogeneous beam

Clear Gate Results, **-5 V** during Irradiation



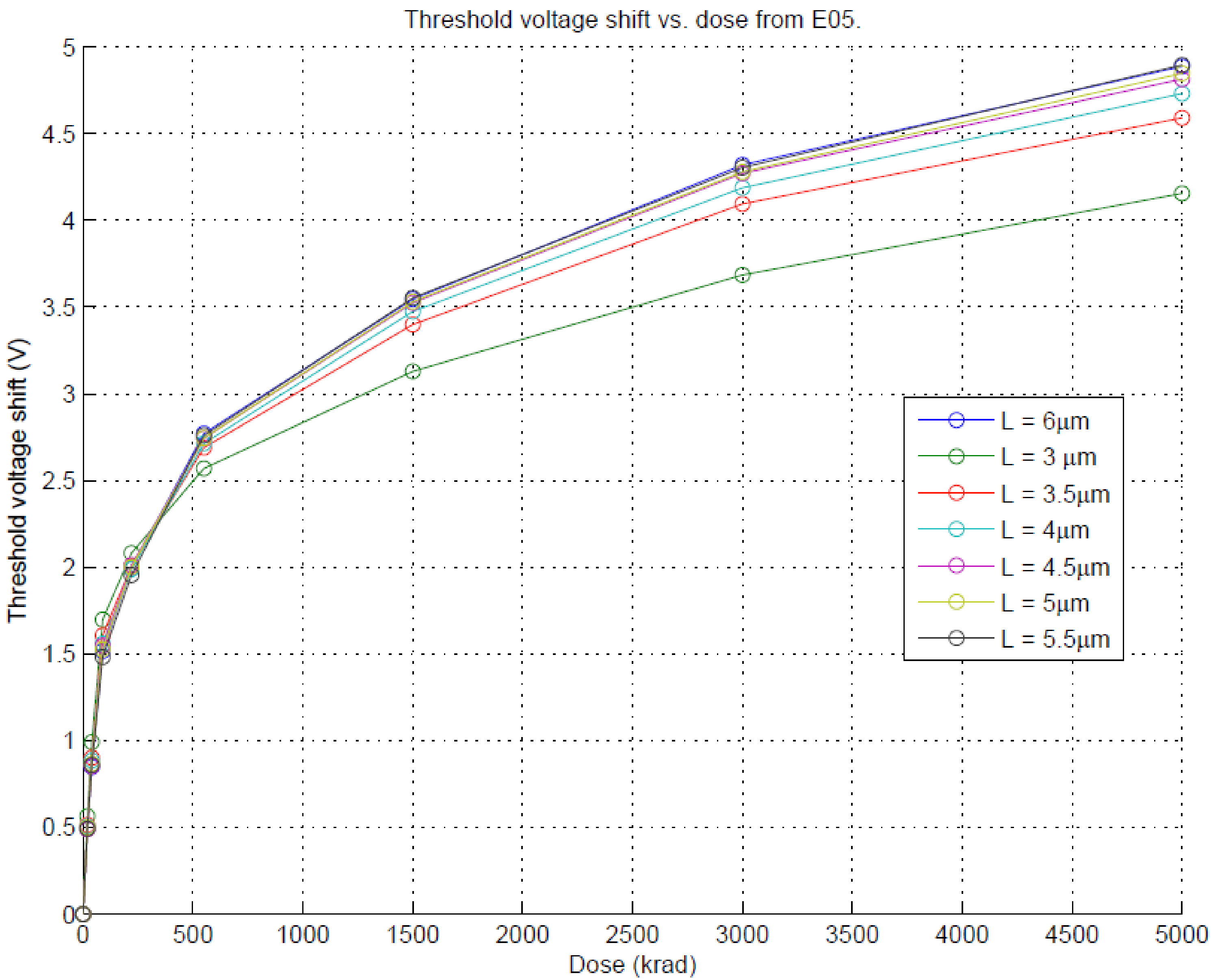
~4.7 V

Clear Gate Results, **0 V** during Irradiation



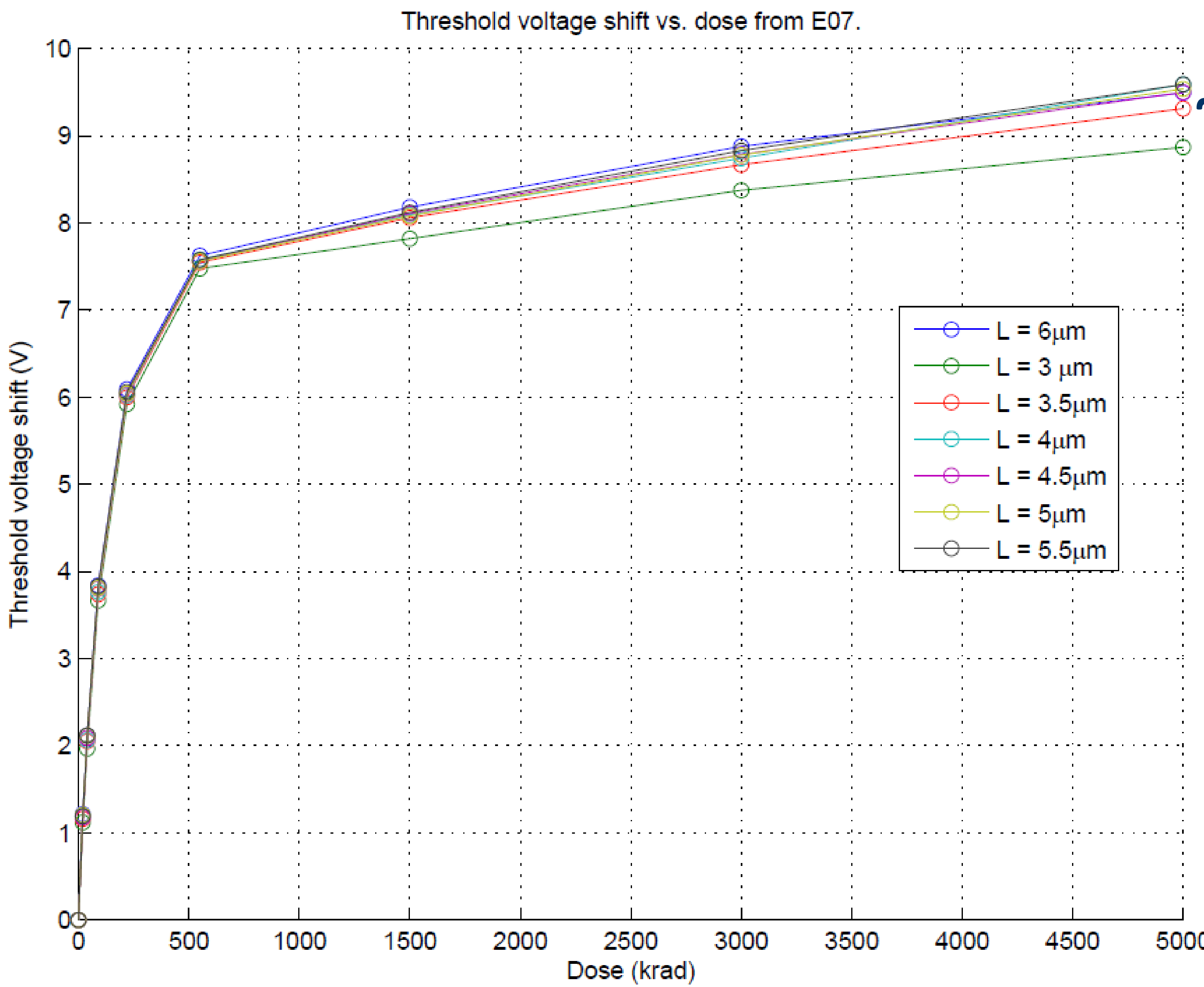
~3.4 V

Clear Gate Results, **+2.5 V** during Irradiation



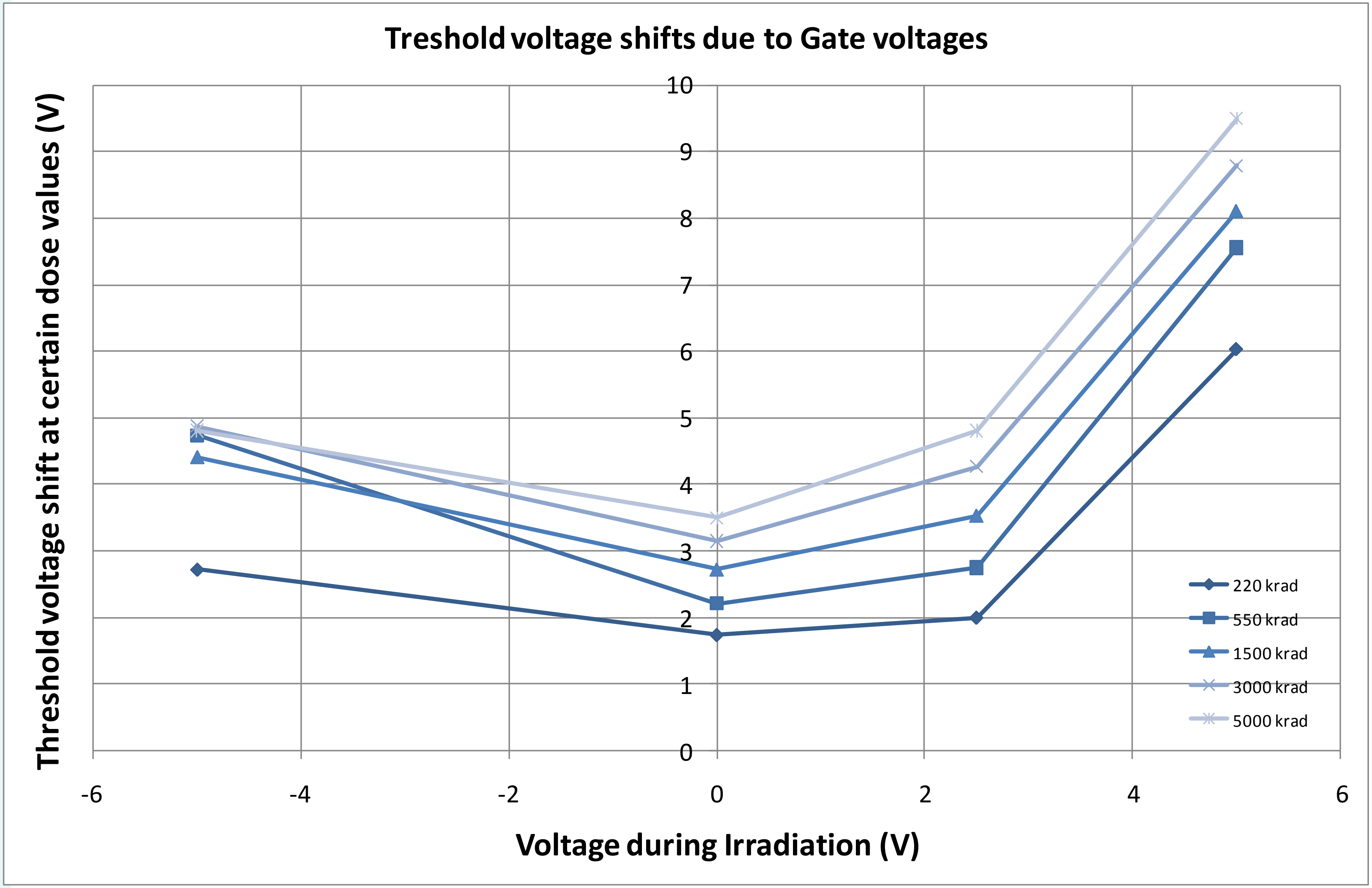
~4.7 V

Clear Gate Results, **+5 V** during Irradiation

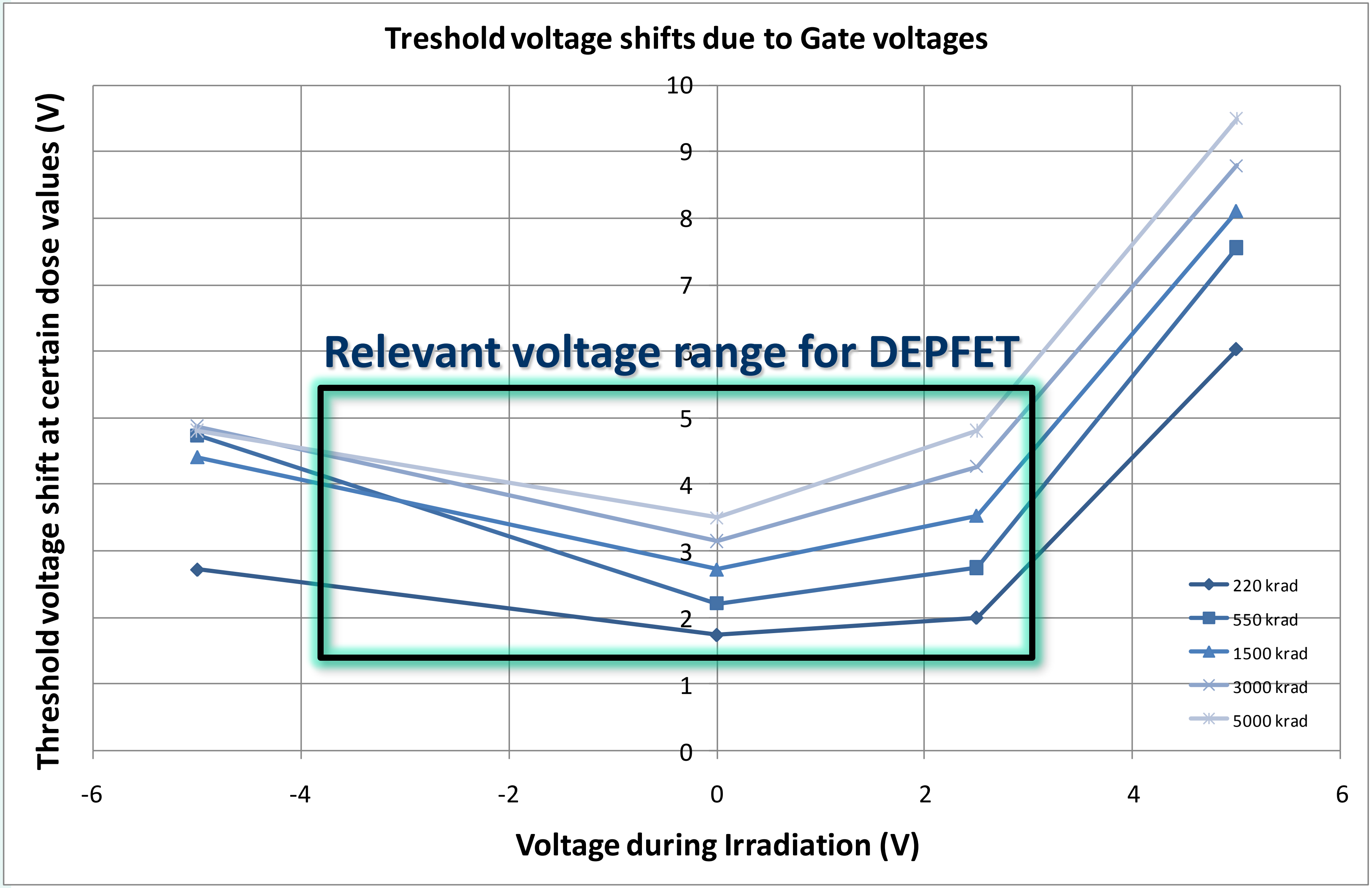


~9.4 V

Threshold voltage shifts due to Gate voltages



Threshold voltage shifts due to Gate voltages



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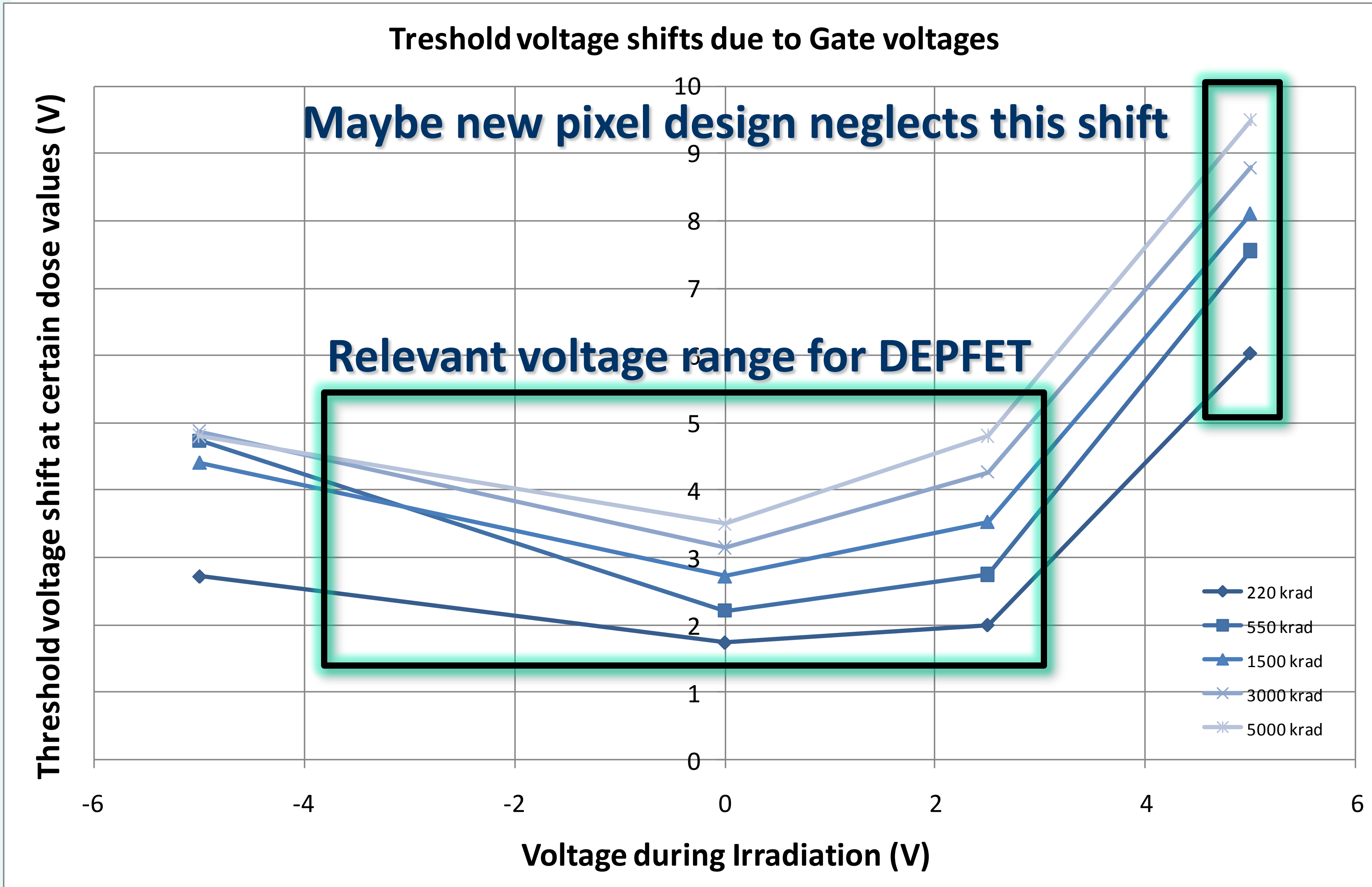


Comparison between 10 nm Si_3N_4 and 20 nm Si_3N_4

10 nm Si_3N_4

- Max. threshold voltage shift
  - 13.8 V @ 3 Mrad

20 nm Si_3N_4

- Max. threshold voltage shift
  - 9.4 V @ 5 Mrad
  - 8.6 V @ 3 Mrad

Comparison between 10 nm Si_3N_4 and 20 nm Si_3N_4

10 nm Si_3N_4

- Max. threshold voltage shift
  - 13.8 V @ 3 Mrad
- Flatness
  - Δ along Gate voltage = 1.1 V @ 3 Mrad

20 nm Si_3N_4

- Max. threshold voltage shift
  - 9.4 V @ 5 Mrad
  - 8.6 V @ 3 Mrad
- Flatness
  - Δ along Gate voltage = 1.3 V @ 5 Mrad

Comparison between 10 nm Si_3N_4 and 20 nm Si_3N_4

10 nm Si_3N_4

- Max. threshold voltage shift
  - 13.8 V @ 3 Mrad
- Flatness
  - Δ along Gate voltage = 1.1 V @ 3 Mrad
- Oxide charge density @ 3 Mrad
  - Sheet capacitance = $3.83 \cdot 10^{-8}$ F/cm²
  - Oxide charge density = $5.29 \cdot 10^{-7}$ C/cm²

20 nm Si_3N_4

- Max. threshold voltage shift
  - 9.4 V @ 5 Mrad
  - 8.6 V @ 3 Mrad
- Flatness
  - Δ along Gate voltage = 1.3 V @ 5 Mrad
- Oxide charge density @ 3 Mrad
  - Sheet capacitance = $3.62 \cdot 10^{-8}$ F/cm²
  - Oxide charge density = **$3.11 \cdot 10^{-7}$ C/cm²**

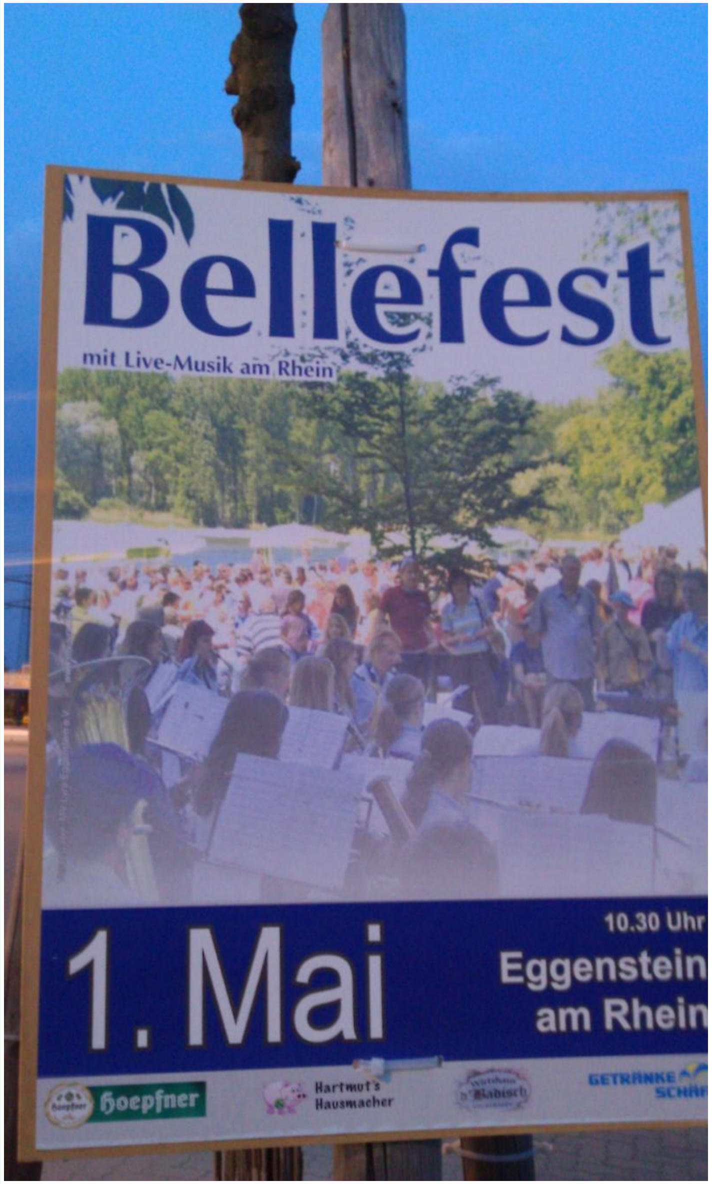
In case of breakdown stability, less oxide charges are favoured

Conclusion and Outlook

Clear Gates in Karlsruhe

- Influence of Gate voltage during Irradiation is reduced by using 20 nm Si_3N_4.
- More irradiation campaigns needed to see, whether more nitride can help. Next steps are 30 nm and 40 nm structures.
- New design of selected areas? → See Rainer’s talk.

Conclusion and Outlook



Clear Gates in Karlsruhe

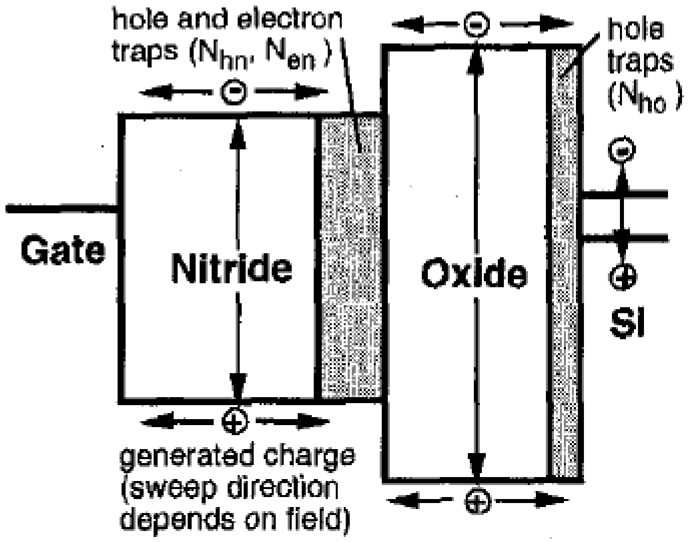
- Influence of Gate voltage during Irradiation is reduced by using 20 nm Si_3N_4.
- More irradiation campaigns needed to see, whether more nitride can help. Next steps are 30 nm and 40 nm structures.
- New design of selected areas? → See Rainer's talk.

- 20 nm nitride is a good start, the irradiation campaign went on smooth and the portents were good…

Thanks for listening

Backup

Trapping in insulator layer



$+V_G$

1. Holes in oxide to Si-SiO_2 interface
2. Holes in Si_3N_4 and electrons from SiO_2 to N-O interface
3. Recombination rate in Si_3N_4 higher than in SiO_2 → more e^- trapped at N-O
4. Build-up of e^- reduces field in oxide → saturation

$-V_G$
Field always present

Thick Si_3N_4
→ Reduces field in ox → saturation