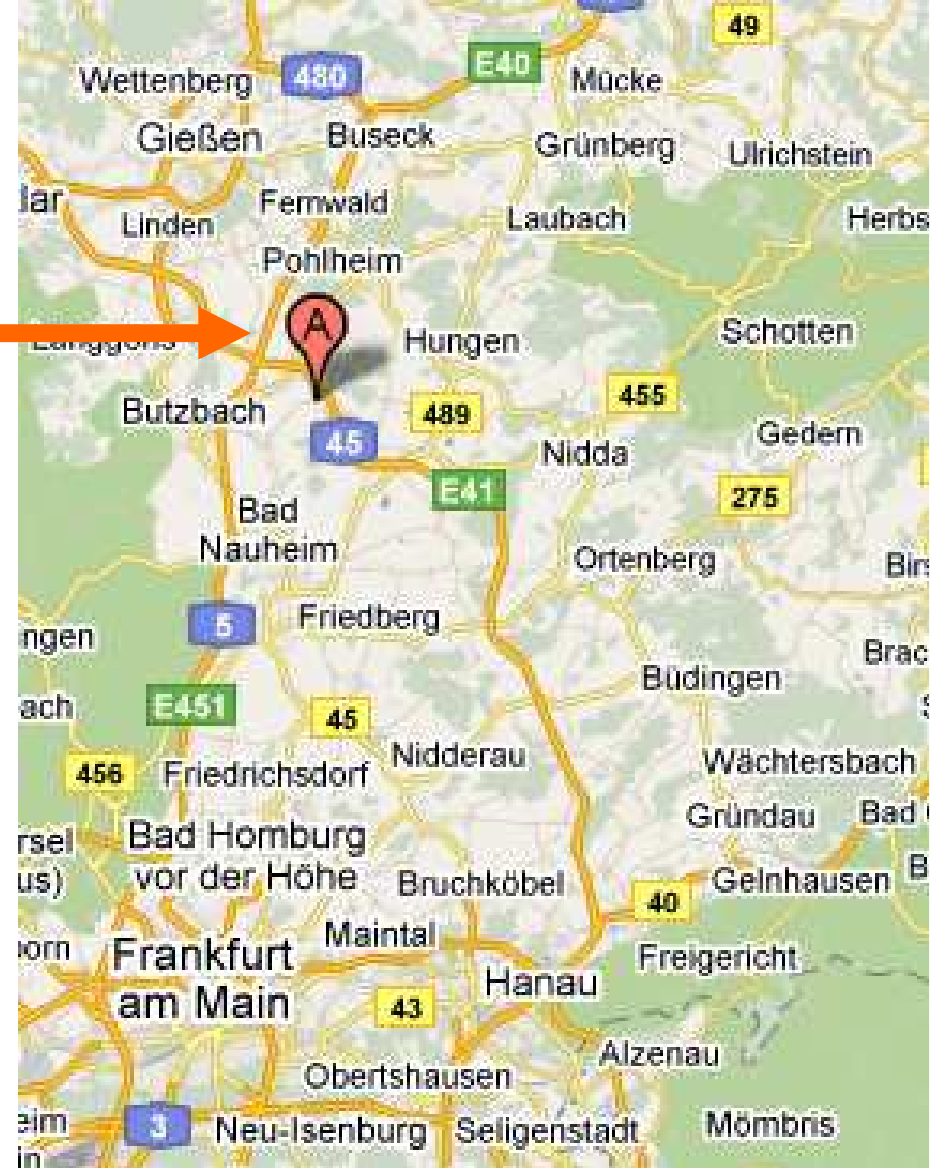


Münzenberg



# PXD DAQ Workshop June 9 and 10, 2011 Münzenberg (near Gießen)

## Goals:

1. bring DAQ people and PXD people (frontend, DHH, ATCA,...) together
2. view of the „complete“ system  
i.e. interfaces: timing distribution, trigger distribution, data formats, protocols, ...

<http://panda.physik.uni-giessen.de:8080/indico/conferenceDisplay.py?confId=44>

# Burg Münzenberg

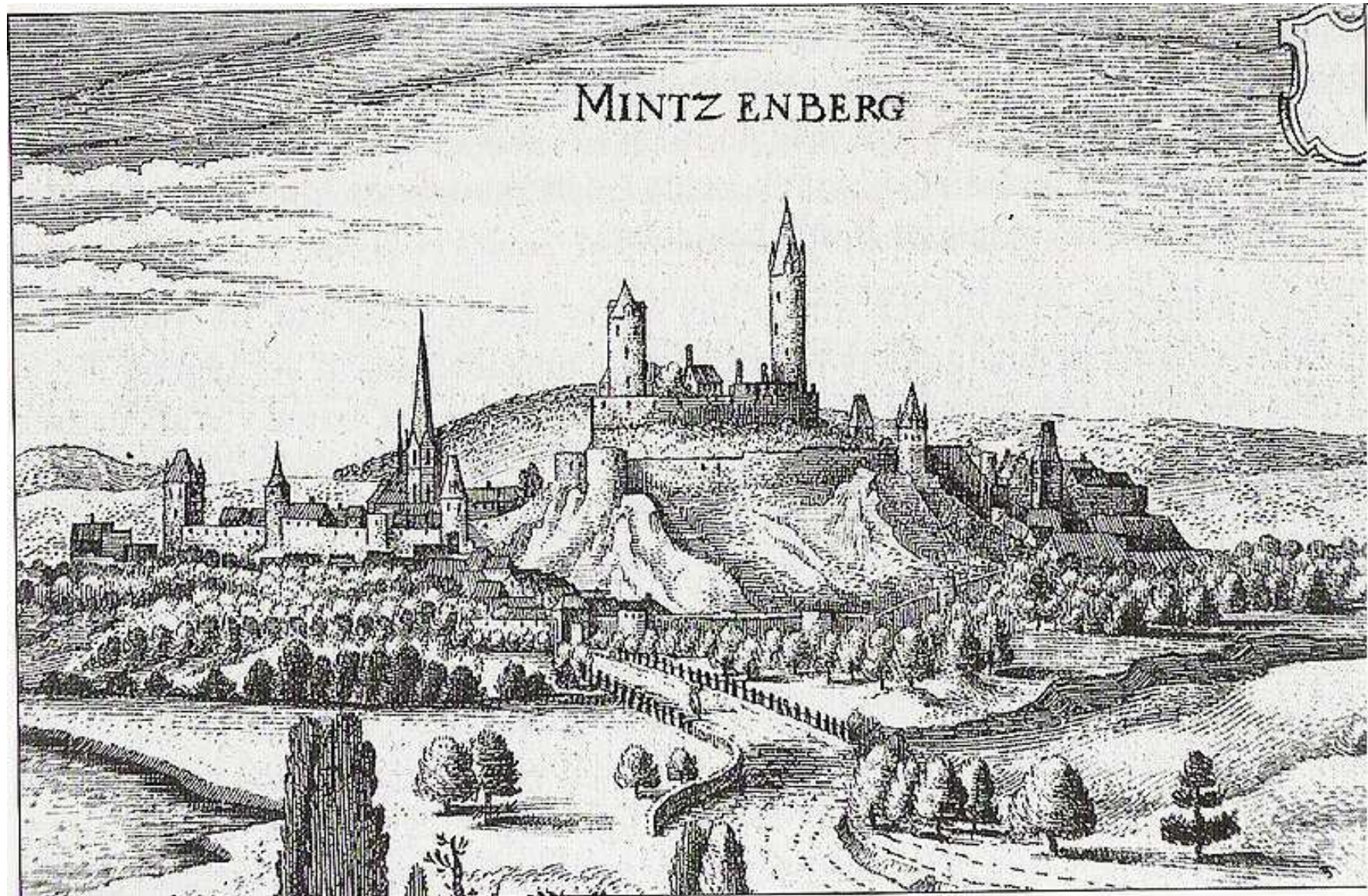
[http://de.wikipedia.org/wiki/Burg\\_Münzenberg](http://de.wikipedia.org/wiki/Burg_Münzenberg)

<http://www.burghotelmuenzenberg.de/>





Mentioned in Documents since 1162.  
This drawing by Merian dated 1620.



# Münzenberg Agenda

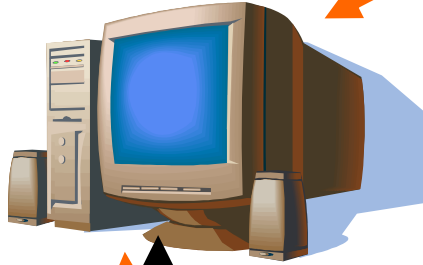
- DAQ issues
  - protocols (AURORA everywhere?)
  - clock generation and distribution ( $RF^*(3/20)$ , DHH?)
  - BUSY handshake?
  - pile-up, multiple triggers in 1 frame
  - run control (start/stop run, e.g. upload pedestals)
  - data formats (unpacking/decoding on FPGA)
- cluster finder for low pT (dedicated session)
- SVD interface
  - SVD sub-event builder, PXD sub-event builder
  - SVD tracklet finder algorithm (dedicated session)
  - SVD only or SVD+PXD
- FPGA sorting algorithms
  - hit sorting
    - partially unsorted at DHH input (because of parallel FIFOs)
    - order row-by-row required by any FPGA algorithm?
  - event sorting
    - for sending PXD data to EVB
- load balancing (Touchek hot spots)
- injection veto
  - pre-trigger
  - pedestal dump?



# A Concept for PXD Pedestals

**Idea from B2GM Nov2011  
„system as is“,  
just more channels and  
move to KEK“**

dump  
pedestal  
event  
by JTAG  
(slow)



40  
JTAG  
cables

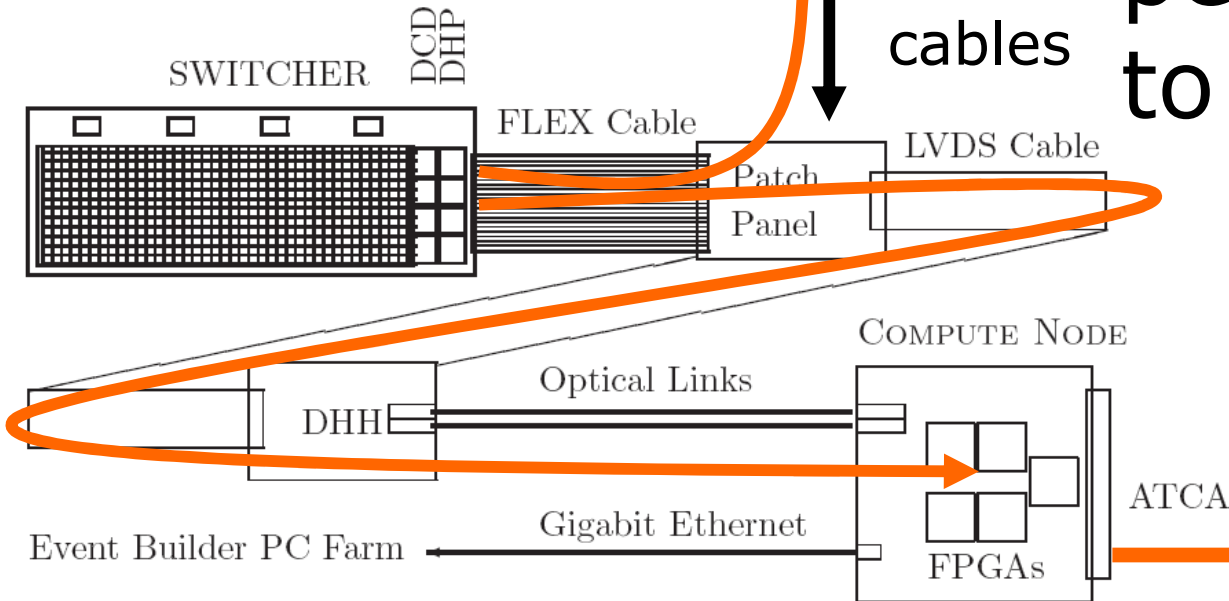
# Where to calculate pedestals and send to the PC?

## Why PC?

- 1. database (postgresql)**
- 2. Interface to slow control e.g. set DACs @ run start**

send full frames  
during injection  
4 x 1.25 Gbps  
~1/2 ms

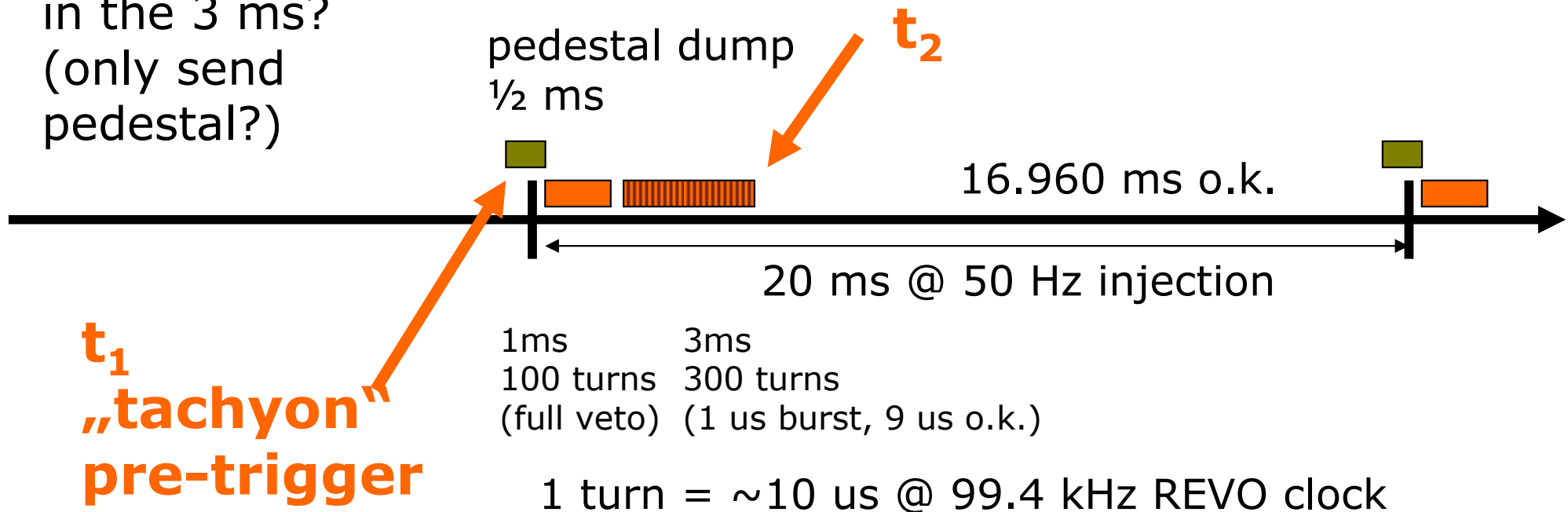
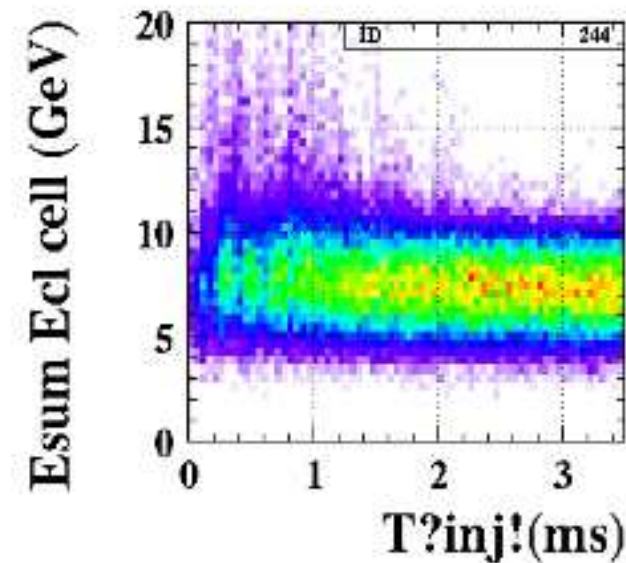
pedestals going where?



# Münzenberg Agenda

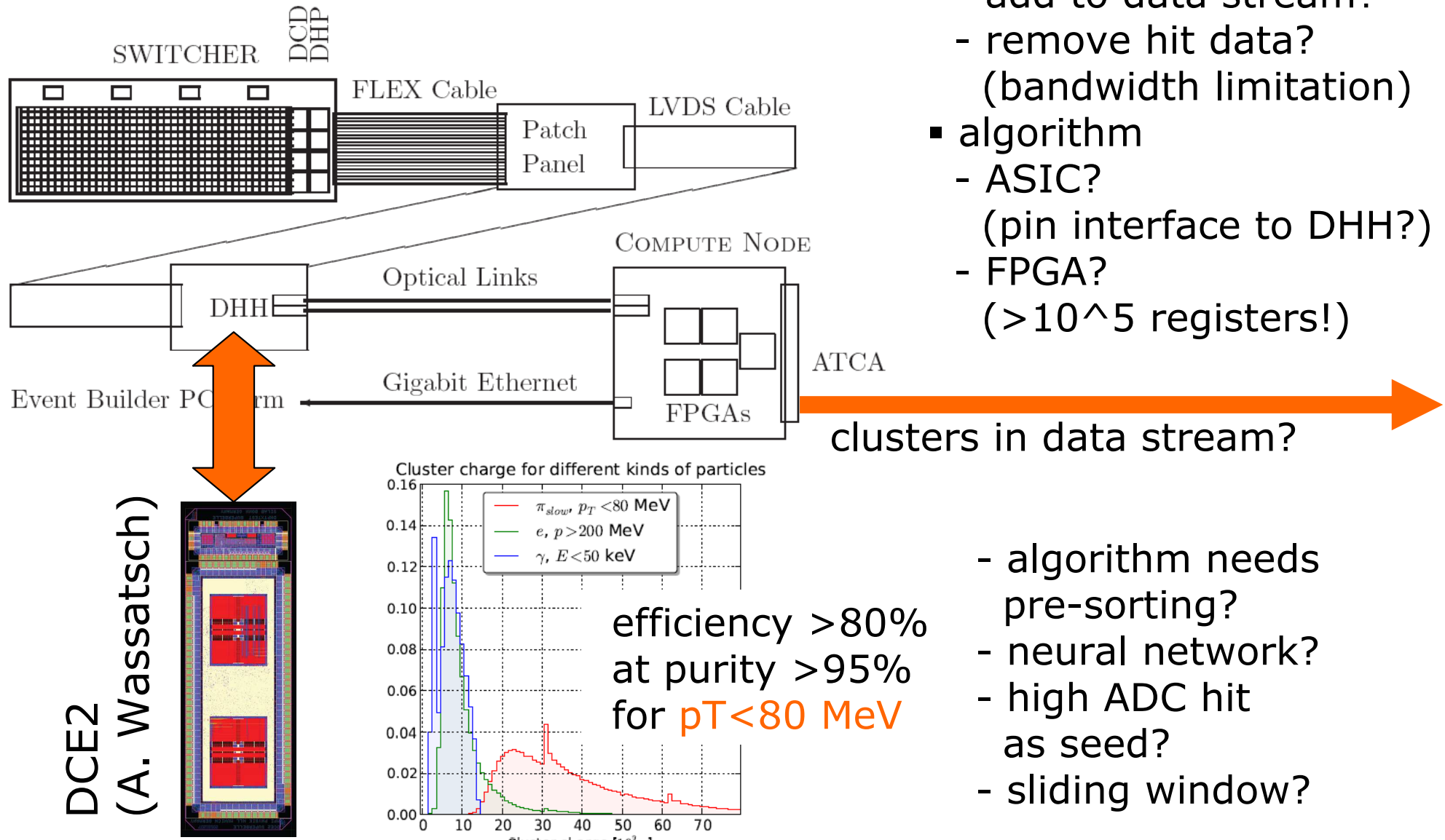
## Pedestals @ Injection Veto ?

- needs pre-trigger at  $t_1$   
[-40  $\mu$ s : -20  $\mu$ s]  
for switching DHP modes
- howto switch back at  $t_2$ ?  
needs interface to  
injection VETO signal
- What can ATCA or DHH do  
in the 3 ms?  
(only send  
pedestal?)



# Münzenberg Agenda

## A Concept for Cluster Finder



- cluster data
  - all clusters?
  - only high sum ADC?
  - add to data stream?
  - remove hit data? (bandwidth limitation)
- algorithm
  - ASIC? (pin interface to DHH?)
  - FPGA? ( $> 10^5$  registers!)

- algorithm needs pre-sorting?
- neural network?
- high ADC hit as seed?
- sliding window?

see talk by A. Ritter (Monday)

S. Lange Ringberg 2011