Data Concentrator

Ringberg

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1. Overview
   - Motivation
   - Solutions
2. Multiplexer
   - Transmission
   - Protocol
   - Multiplexing theory
   - Implementation
3. Current status
   - Test setup
   - Results
   - Task list

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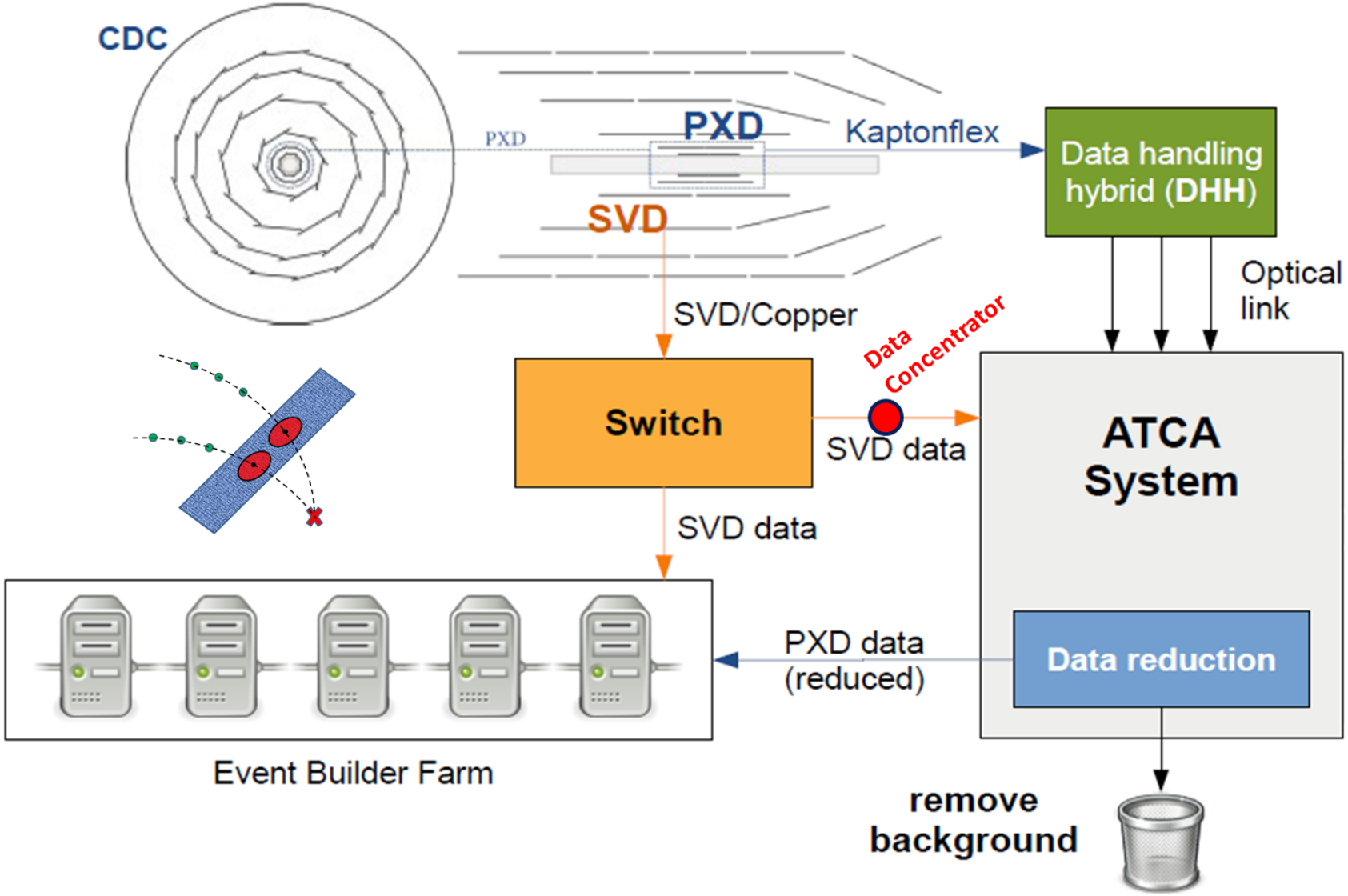
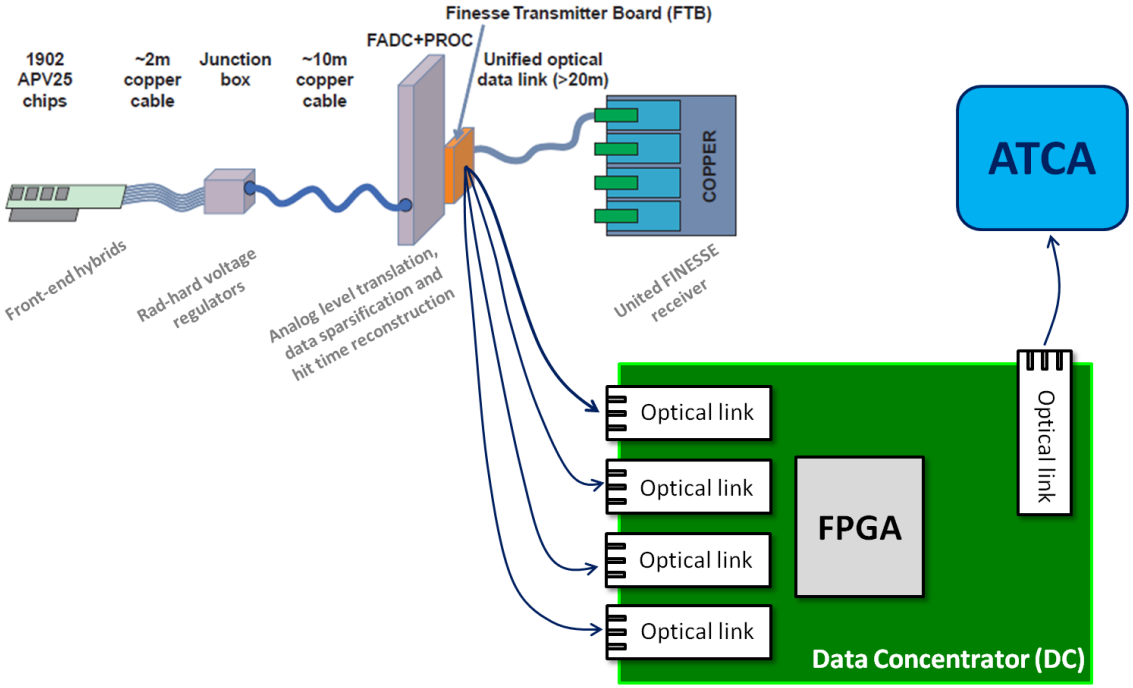
General layout



Technical specification (not final)

- Input:
  - 42 (atm) links
  - SFP Connectors
  - 1.5 Gbps max
  - Dynamic bandwidth
- Output:
  - Only a few (around 5-10)
  - 6.25 Gbps max
  - Dynamic bandwidth



Possible hardware solutions

- Commercial FPGA Boards
  - + Tested and available
  - - Connector Extension card needed
  - - Price
- ATCA Compute Nodes
  - + Close collaboration with Giessen group
  - + CN for testing (kindly provided by Giessen)
  - + Already integrated in the PXD DAQ
  - - Not final
- AMC
  - + Good scalability
  - Can the PCB layer be adapted for our purpose?
  - Enough SFP connectors?

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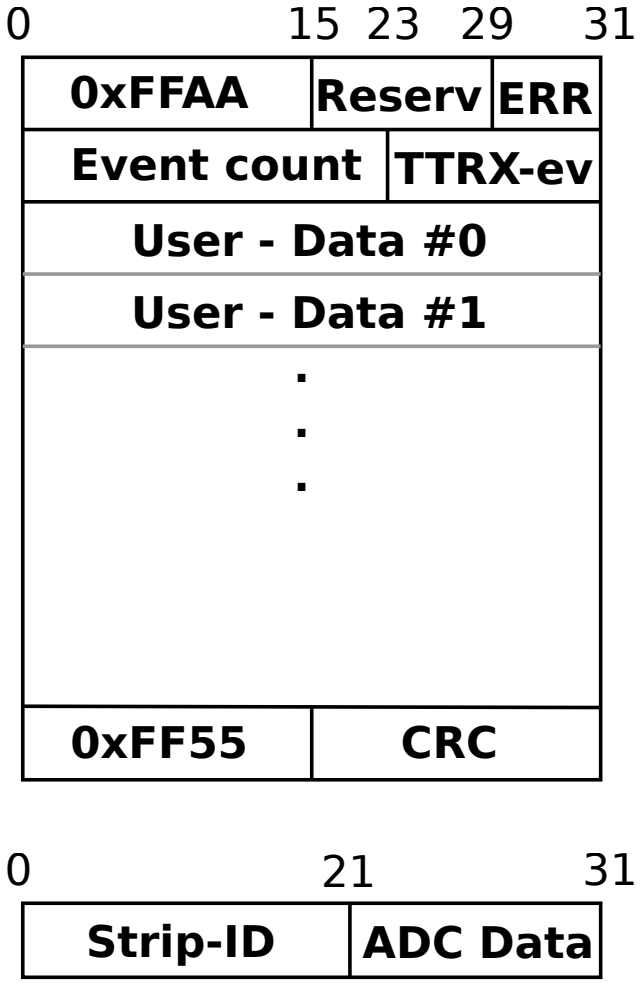
Aurora Overview

- Xilinx Aurora protocol for transmission over GTP
- Takes care of every “low level” operation like clock correction, symbol decoding and 8B/10B Encoding
- Easy data transmission/framing over locallink
- Error detection and initialization
- Status wires for channel

BELLE-II Link

- Header with event number
- Footer with CRC checksum
- 21 x 32 Bit Data
- SVD Data contains:
  Strip-ID + 10 Bit ADC Data

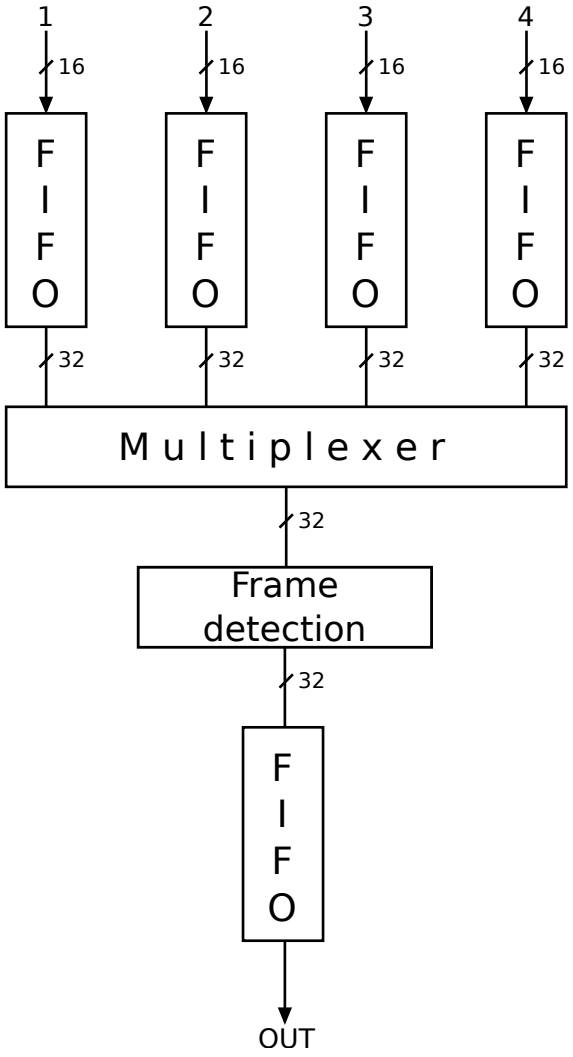


Multiplexing

- Three general types of multiplexing:
  - Frequency Division Multiplexing (FDM)
  - Time Division Multiplexing (TDM)
  - Statistical Multiplexing
- Because of dynamic bandwidth “Statistical Multiplexing” would be most suitable
- Demultiplexing is trivial, if only multiplexing of 32 Bit words is ensured

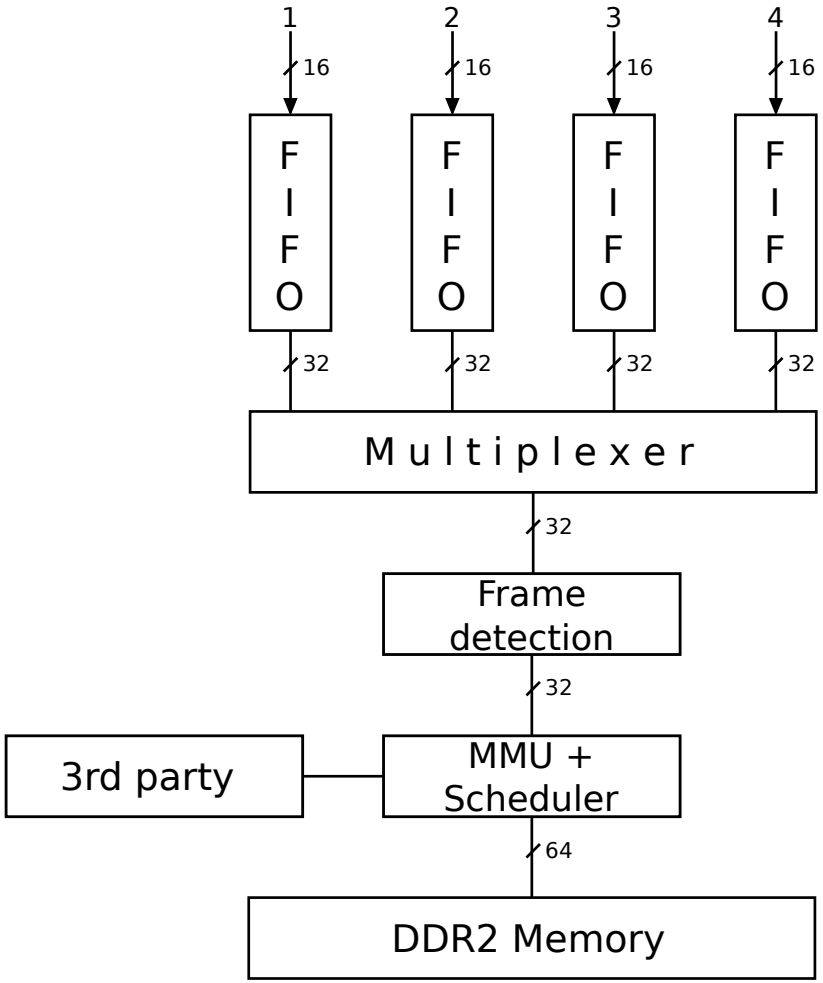
FIFOs only

- Ensure consistency of data
- Data synchronisation FIFOs for input lines
- Block RAM for FIFO
- Multiplexer to directly put data in the output FIFO



DDR2 RAM storage

- DDR2 RAM for data storage after multiplexing
- Store data in memory pages
- Easy access to data for “3rd party” application



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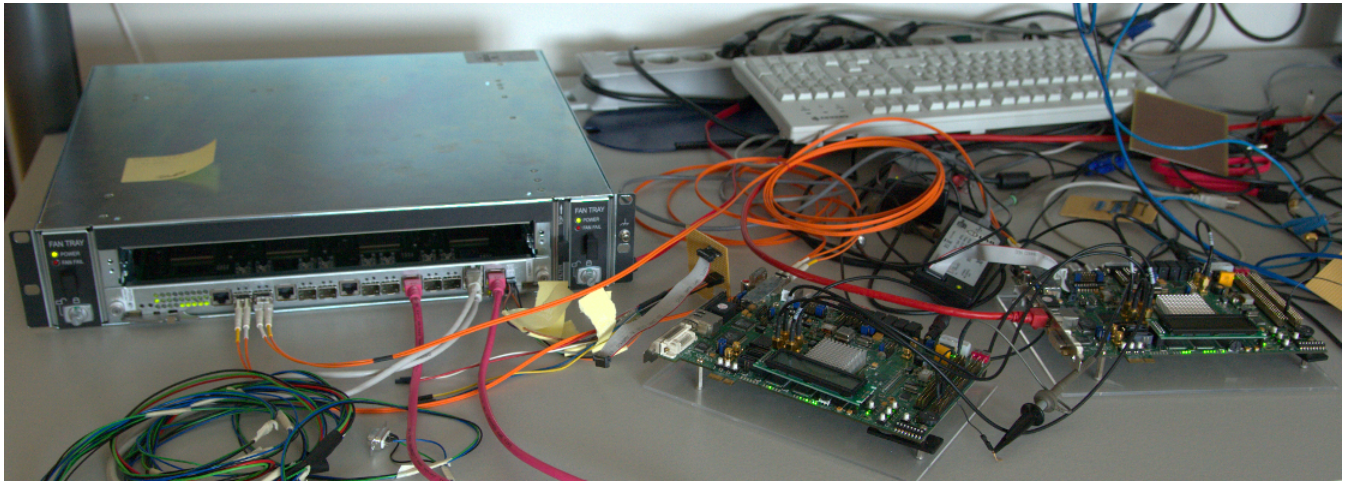
Planed test setup with Compute node

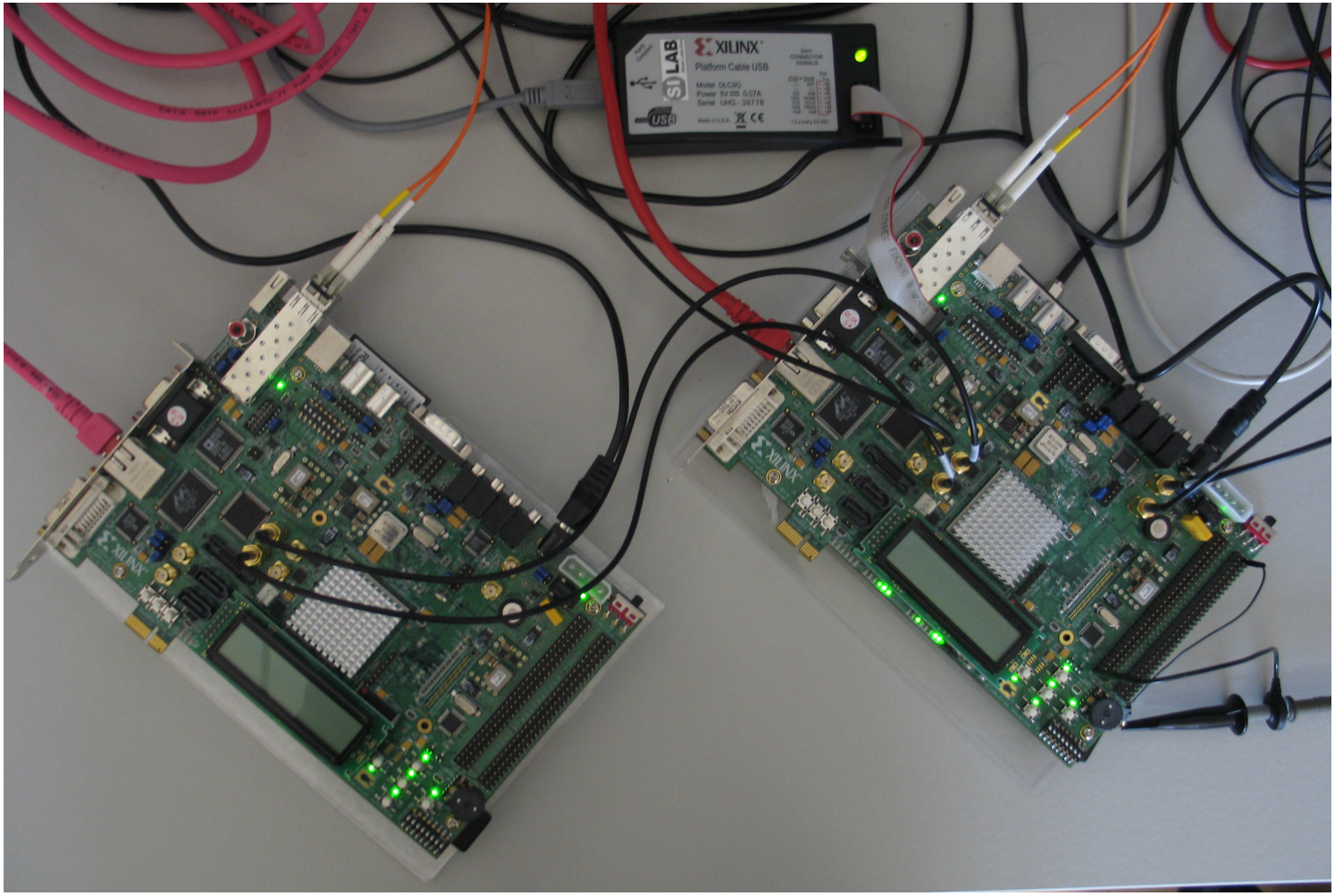
- Top: Compute node with 5 Virtex 4 (on loan from Giessen)

- Bottom: CN with transmitting boards



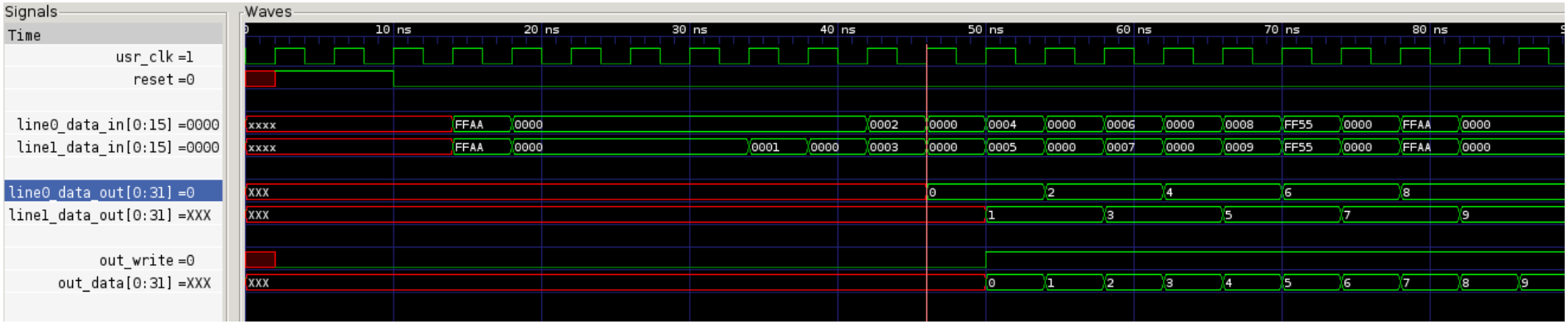
Test setup for algorithm

- Virtex 5 Evaluation Boards
- Left: Sender
- Right: Receiver

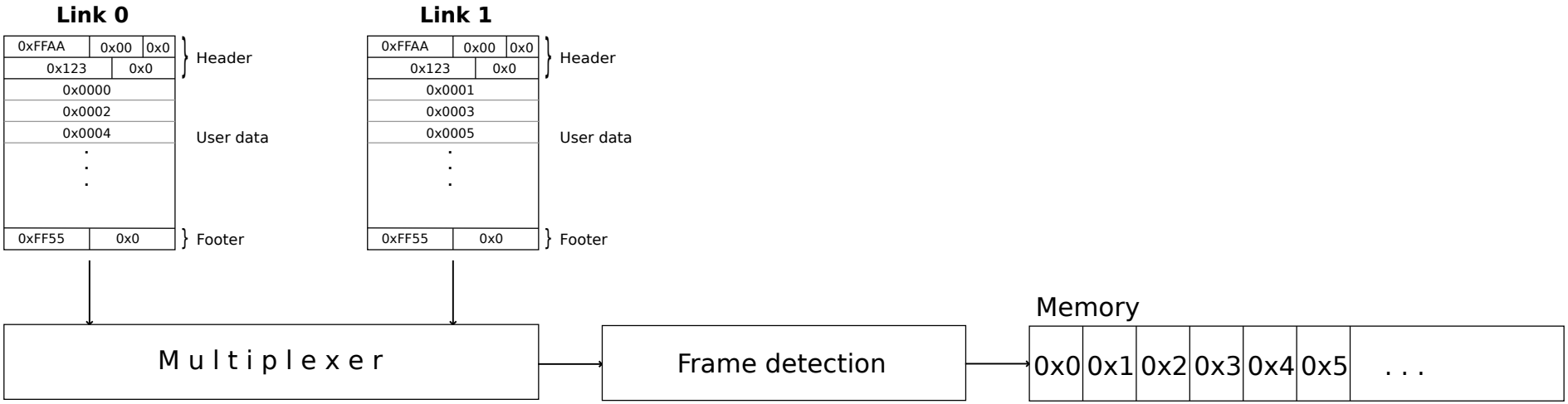


First results with “FIFOs only” (Illustration)

Waveform diagramm:

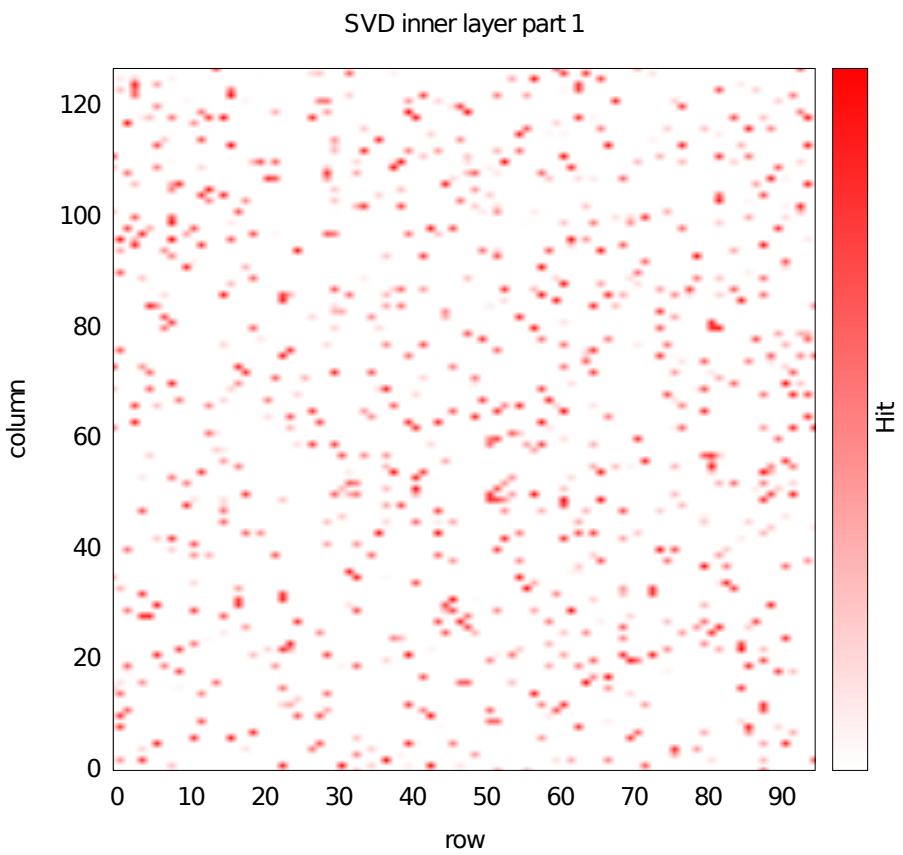


Schematic:



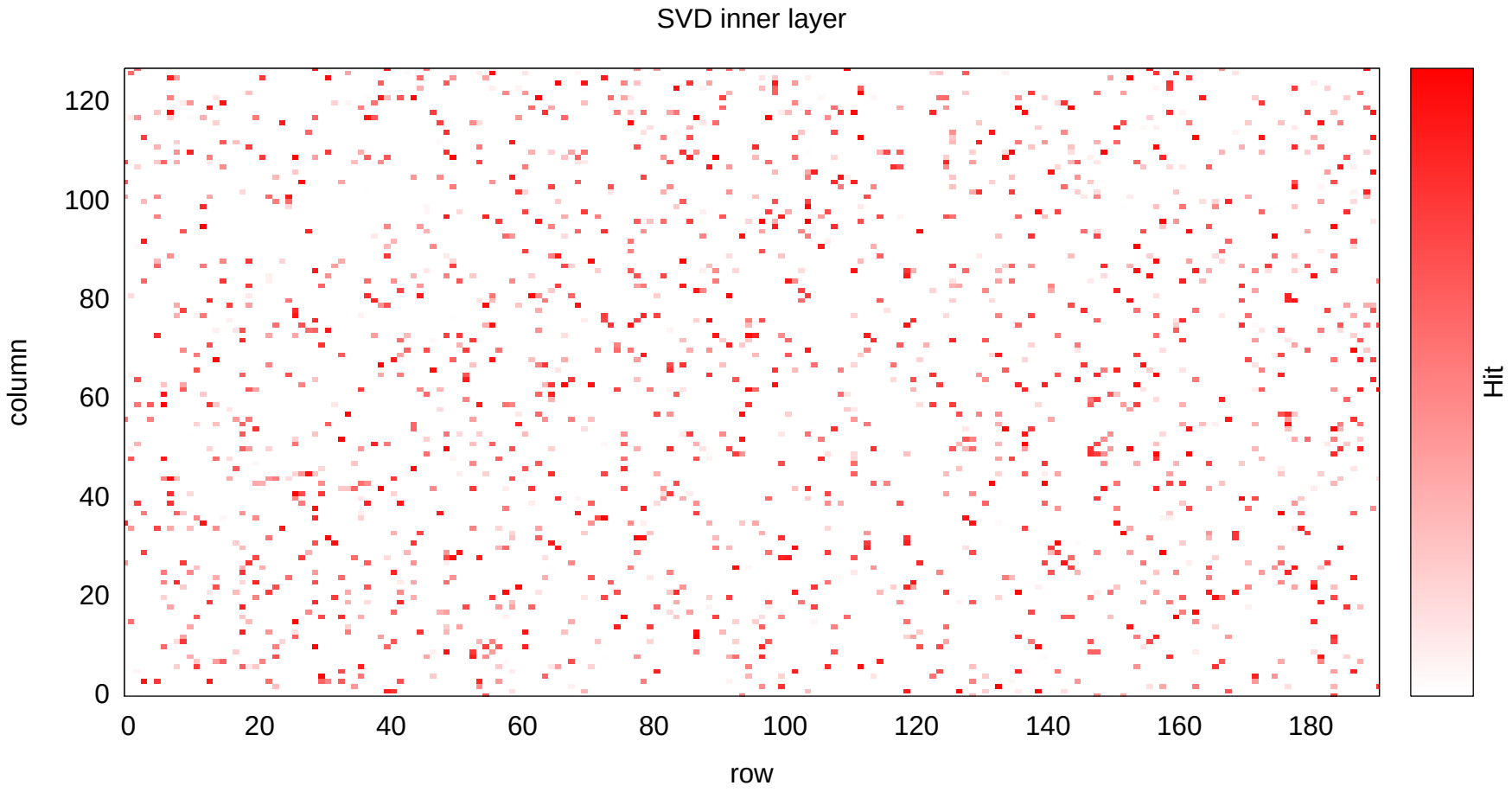
First results with SVD data

- Randomly generated SVD data, send over each link



First results with SVD data

- Apparently the multiplexed data is received correctly :-)



Task list

CPP data generator and validator...	done
Ethernet for crosschecking...	done
Data transmission...	done
Multiplexing unit...	done
DDR2 access...	in progress
Scheduler...	in progress
MMU and general management module...	in progress
Complete readout chain...	in progress
Long term bit error test	todo
Slow control error module...	todo
Final Implementation...	todo

Thank you for your attention!