Status of Compute Node Development for PXD System

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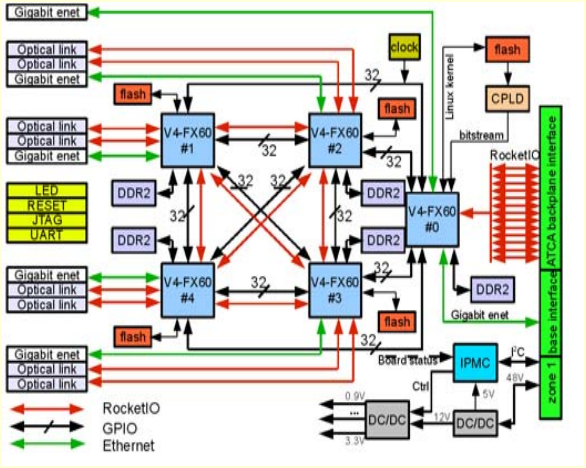
Outline

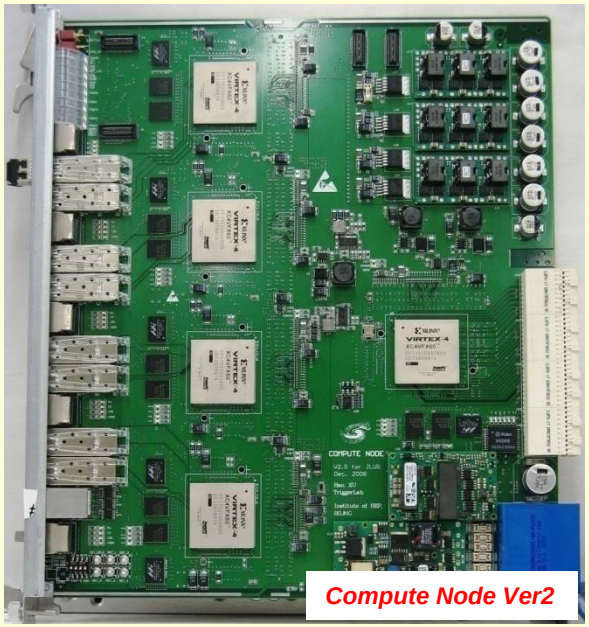
- Progress on CN
  - 10 boards production for PANDA and PXD firmware development
  - Algorithms development on CN
  - Data flow and MPMC DDR2 memory throughput test
- xTCA compliant CN development
  - xTCA carrier board
  - AMC modules
- Summary

Compute Node

An universal high performance platform prepared for multiple applications .

ATCA compliant (Full Mesh topology in backplane) and FPGA-based (now Virtex4).





High Computing power

- *5x (Virtex4 FX 60 FPGA + 2GB DDR2 + 8SFP) for PANDA*
- *5x(Virtex4 FX 60 FPGA + 2GB DDR2 + 8SFP+) for PXD*

High bandwidth

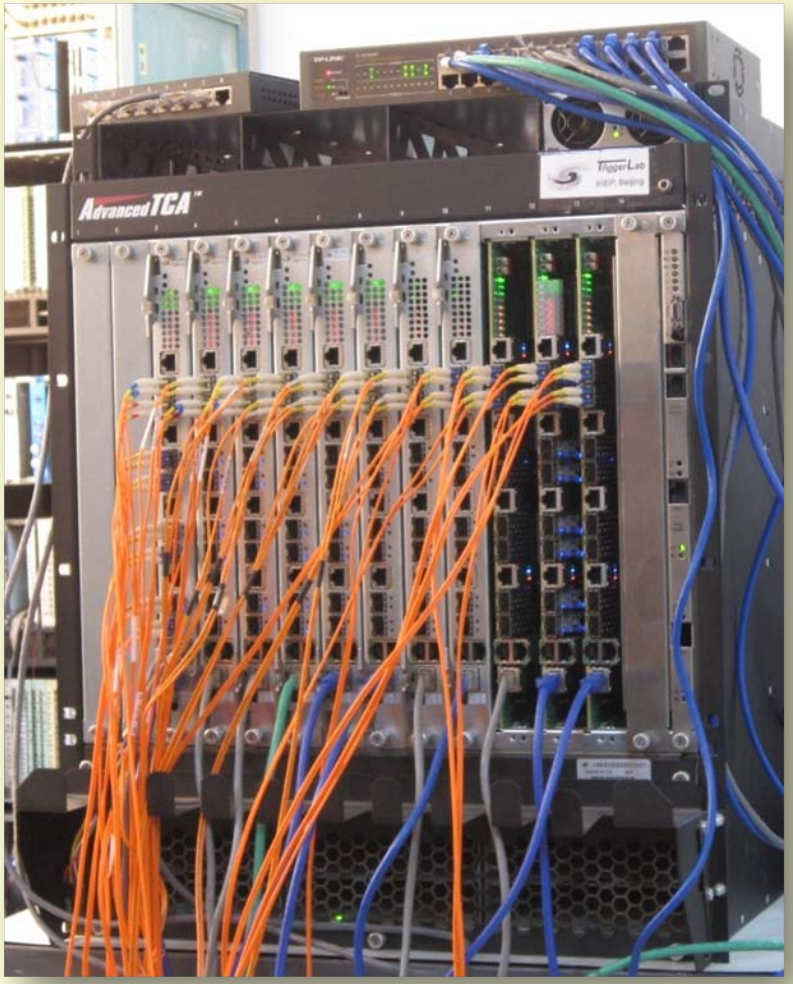
- *6 xGigabit Ethernet (one on backplane base channel)*
- *8x Optical links*
- *13x RocketIOs to backplane*

Embedded system design

- *System-on-FPGA design*
- *Open source Linux*
- *General system designs + customized processing units for different algorithms.*

Boards Production

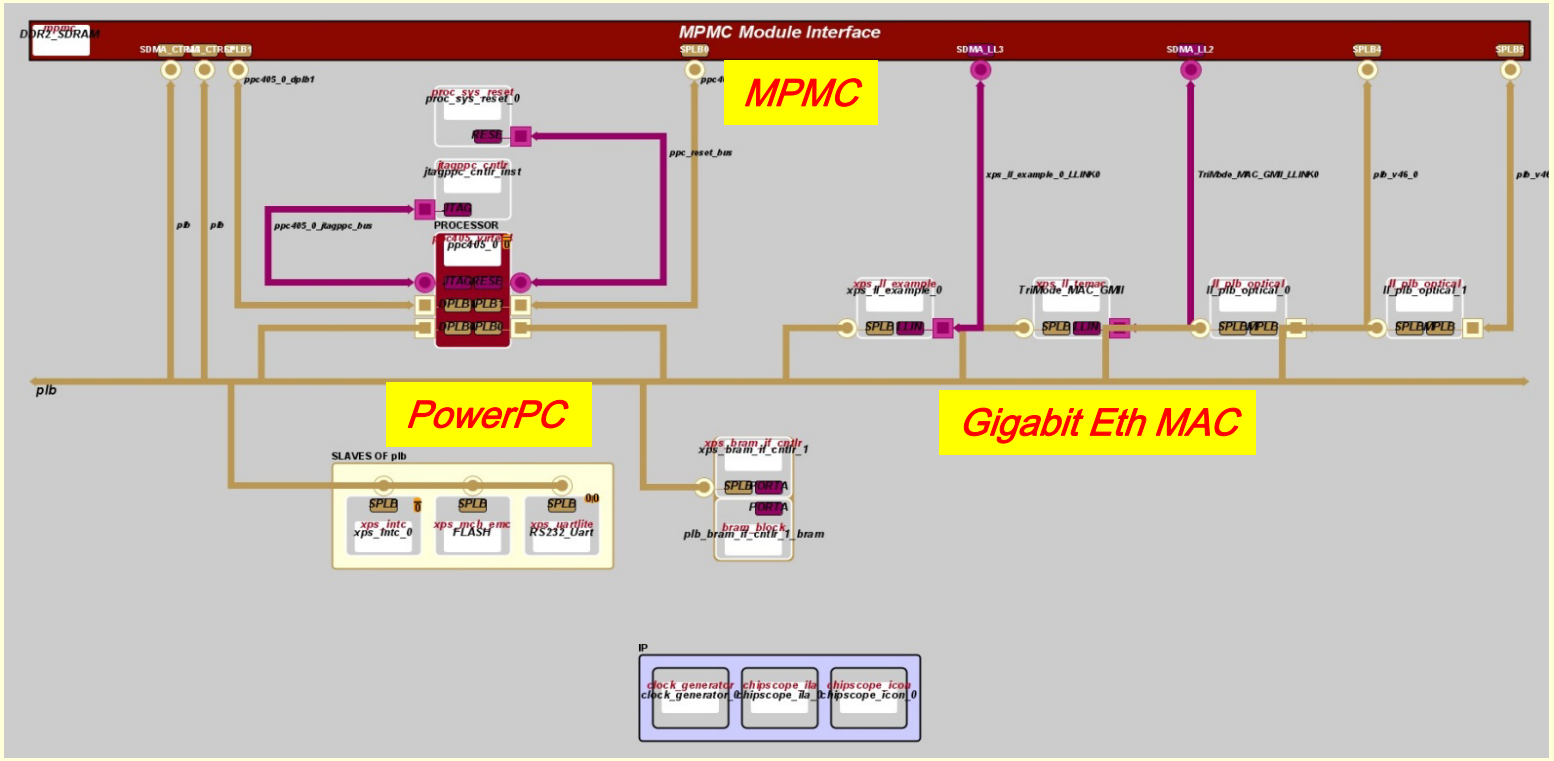
- Requirements from PXD
  - 5 FPGAs/CN
  - Gbit Ethernet link/FPGA
  - 2x6.25Gbps optical links/FPGA
  - 4 GB DDR2 memory/FPGA
- 10 boards production
  - For PANDA and PXD firmware development
  - 3 boards assembled with virtex4 fx60-11 for SFP+
    - 6.25Gbps/ch
  - 7 boards assembled with virtex4 fx60-10 for SFP
    - 3.125 Gbps/ch



Algorithms Development and Performance Test

- Data reduction algorithms
  - talk by D. Münchow
- A Prototype system on the Compute Node
  - talk by B. Spruck
- Data Flow test
  - System on programmable chip
  - Memory throughput

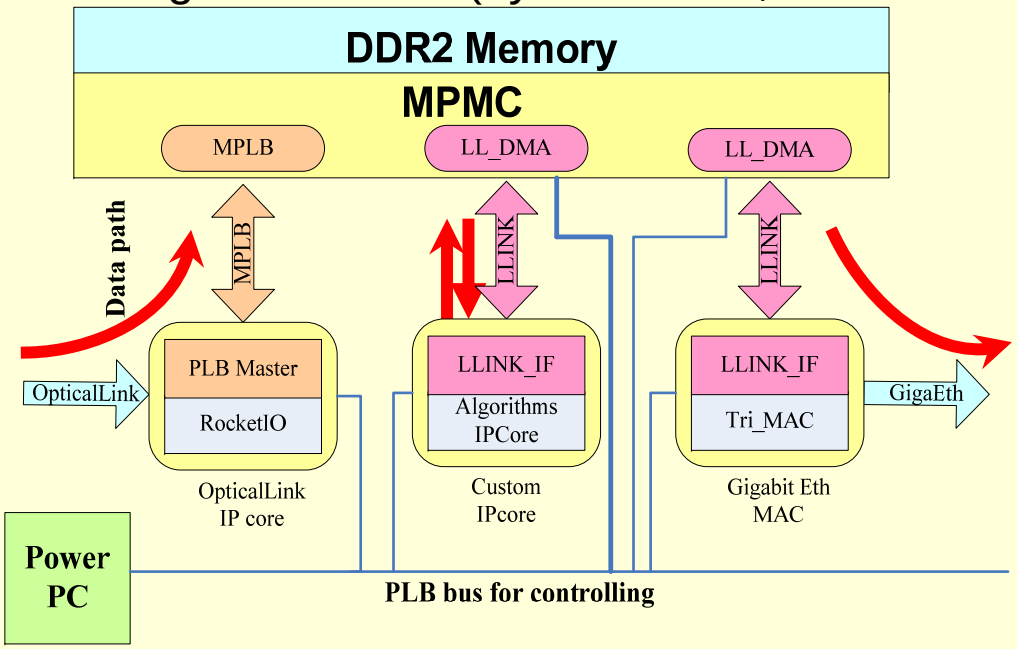
System on Programmable Chip



- Based on PowerPC hardcore inside Xilinx FPGA and other open source IP cores to build a general purpose system, Open source Linux is ported for system management and UDP/TCP stack processing
- Algorithms are designed as custom IP cores and a on-chip data switching module is build based on MPMC

Data Flow

- Raw data received from optical link and buffered in DDR2 memory
  - By Master PLB
  - Low latency(write/4, read/23 PLB clocks), high bandwidth(theoretical maximum 800MB/s)
- Data sent to algorithm IP cores and result written back to DDR2 memory(by LocalLink DMA, flexible and high bandwidth)
- Results sent out via Gigabit Ethernet(by UDP/TCP, standard design)



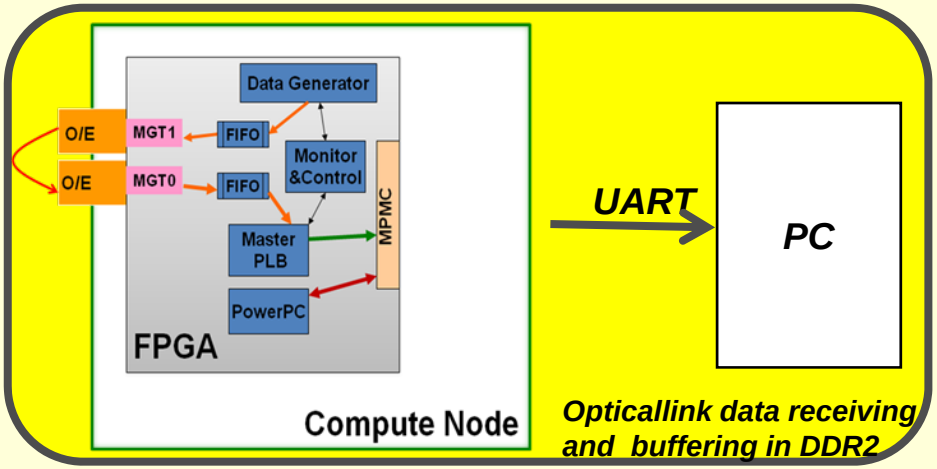
Test Results of Memory Throughput

~550MB/s per optical link: ~3% occupancy

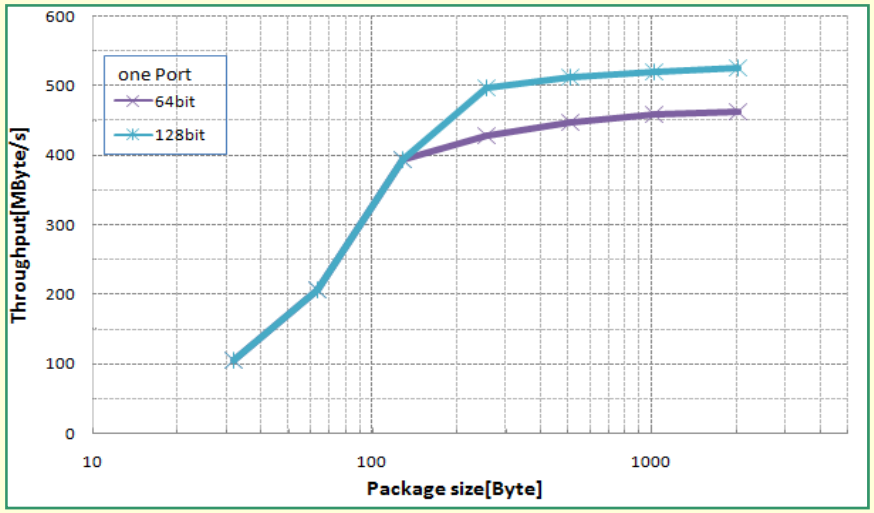
~110MB/s accepted event: ~20% reduction

~660MB/S write/read needed

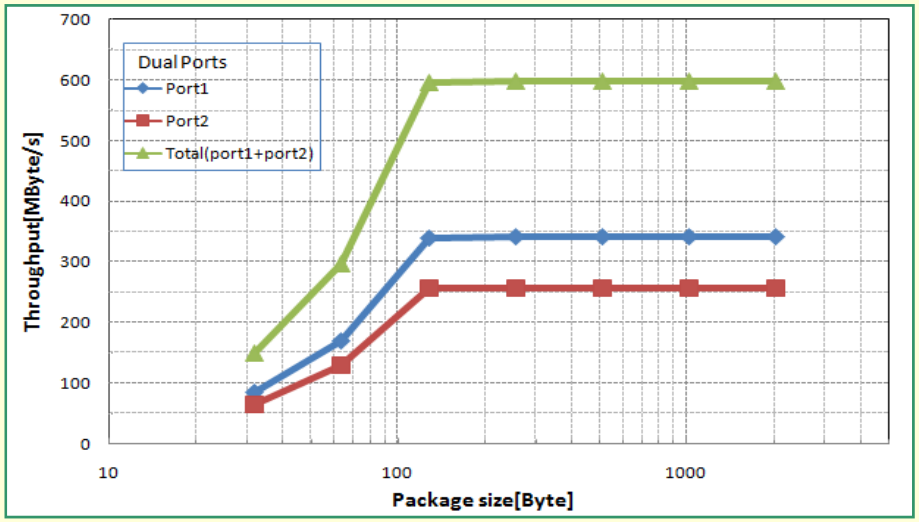
The real throughput is limited by MPMC and PLB PIM. The single port throughput is lower than expected



Opticallink data receiving and buffering in DDR2



Single PLB master IF writing speed test



Dual PLB master IF writing speed test

xTCA Compliant Design

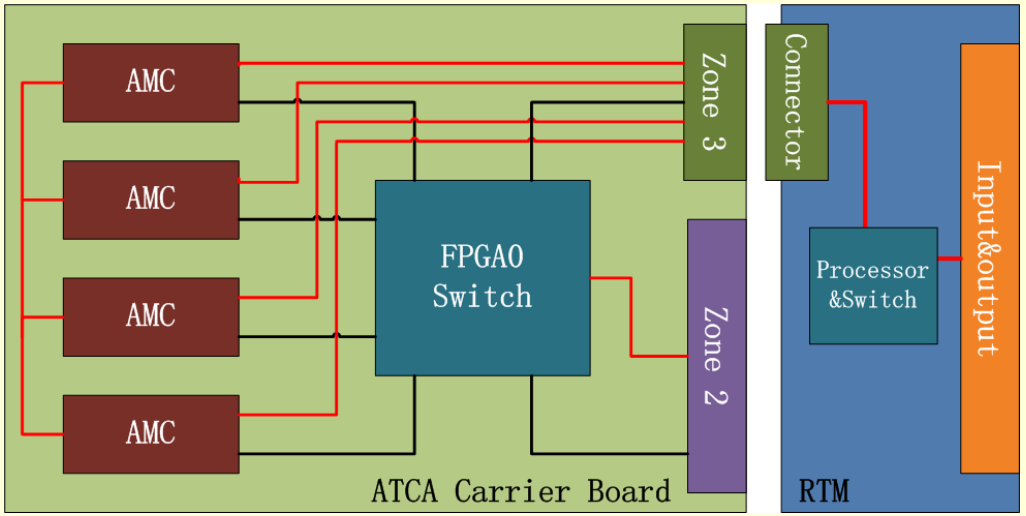
- Motivation
- xFP module and test
- Development for SVD concentrator

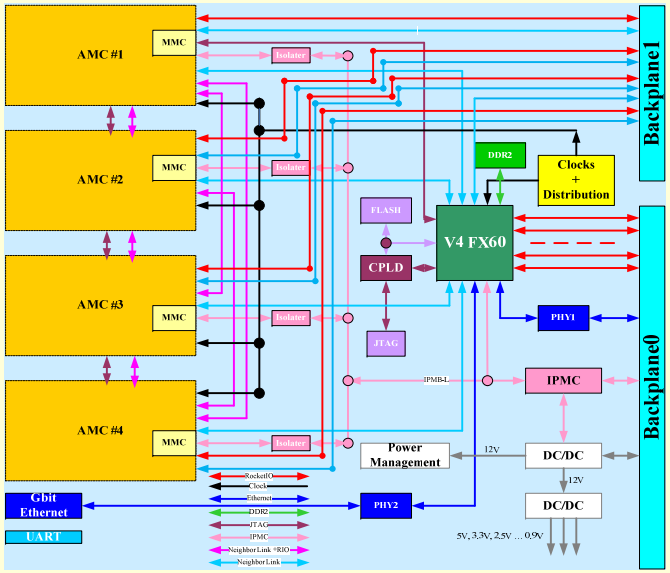
Motivation

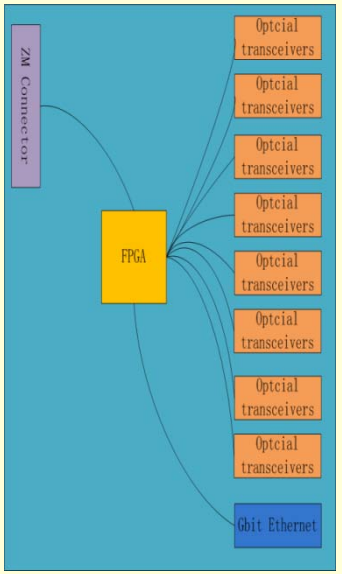
- **Compute Node**
  - A general high availability and high performance data acquisition and trigger system
- **But, not satisfied in**
  - Memory capacity
  - Timing and control capabilities
  - xTCA for physics compliant (IHEP is a co-sponsor of this standard)
- **xTCA is a good choice for next generation**
  - 1 ATCA Carrier Board with high bandwidth switch + AMC modules (xFP)
  - Custom AMC modules for different applications
  - Low cost, easy upgrade
  - Flexibility for maintaining

Development of Carrier Board

- The carrier board
  - based on xTCA
  - allowing backplane data transmission
  - 4 AMC connectors
  - FPGA0 for switch
  - IPMC routing
  - Clock/trigger/ distributions
  - Power conversions
  - RTM reservation(xTCA compliant)
- Status
  - Schematic is amended for xTCA specification ‘draft’
  - PCB layout almost finished







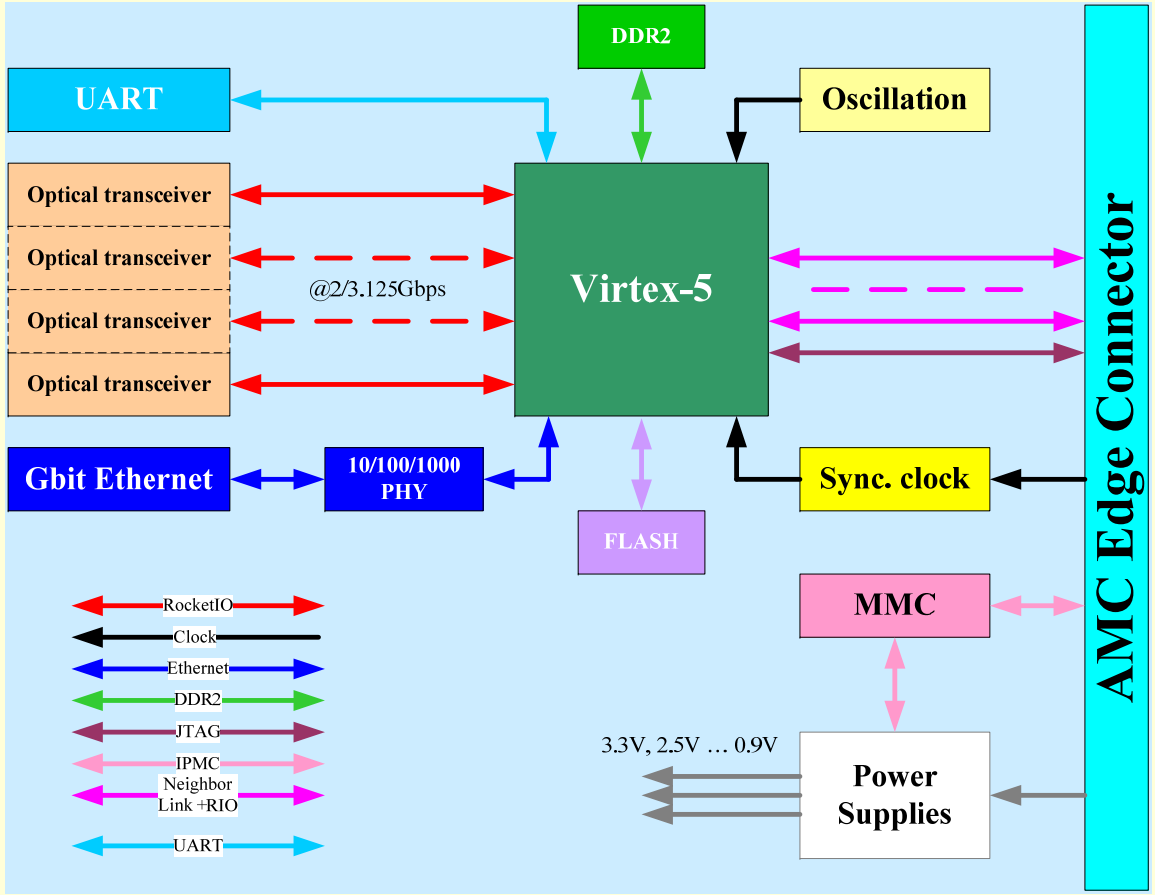
AMC Connector Pins Definition (for xTCA compatability)

40 signal pairs allocated to the Fabric Interface: 20 inputs + 20 outputs

- Connection with neighbor AMC modules, total 2x(1x3 + 2x3) = 18
  - In: 1 MGT channels + 2 IO channels
  - Out: 1 MGT channels + 2 IO channelsh
- Connection with switch FPGA
  - In: 2IO channels
  - Out: 2IO channels
- Connection with RTM
  - In: 3 MGT channels + 2 IO Channels
  - Out: 3 MGT channels + 2 IO Channels
- FPGA download
  - In: 4 single-end
  - Out: 4 single-end
- Control
  - In: 4 single-end
  - Out: 4 single-end

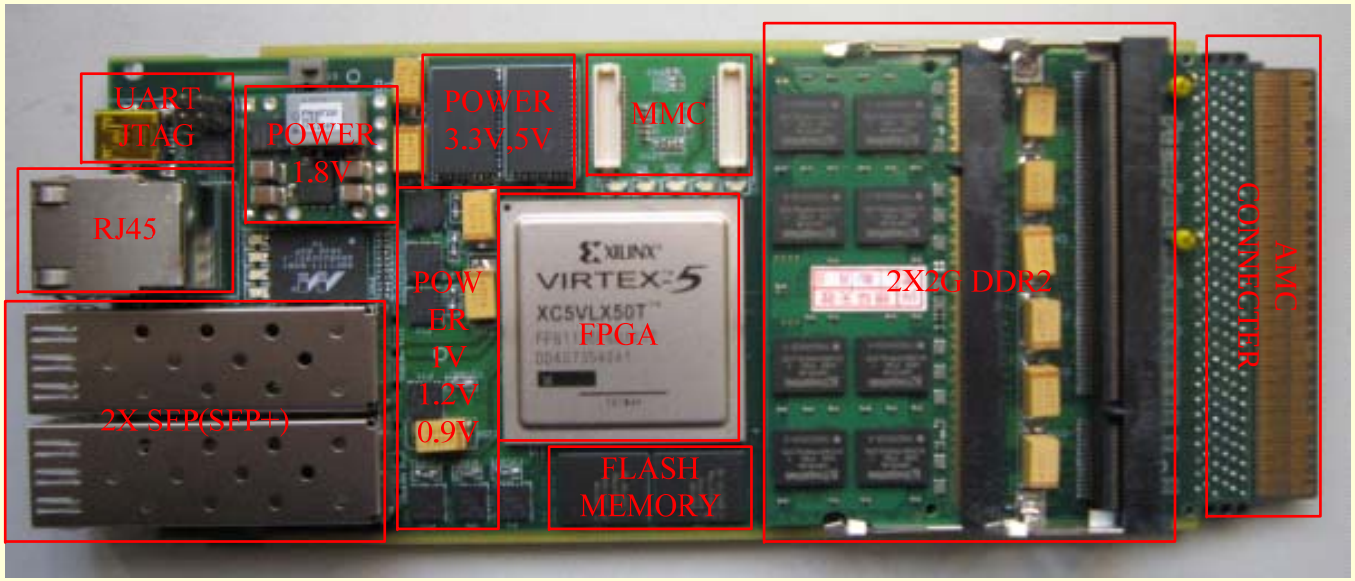
The Structure of the xFP Card(AMC)

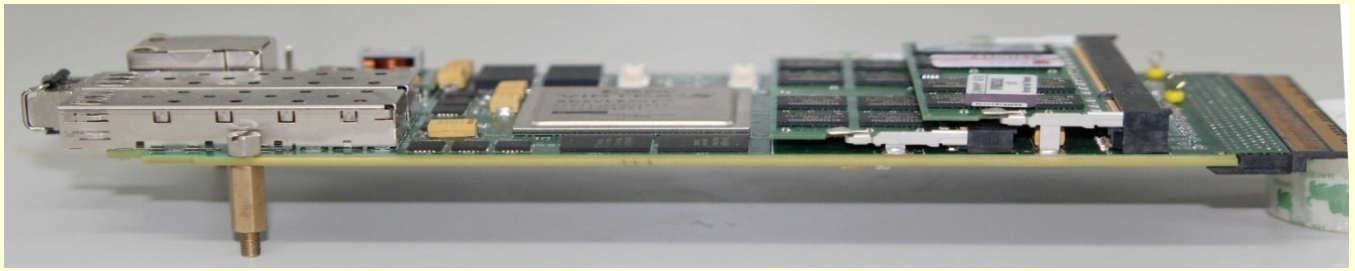
- 2 x 3Gbps optical link
- 2 x 2GB DDR2 SDRAM
- 64MB Flash Memory
- 1x Gbit Ethernet
- 1 UART
- 1 IPMC/MMC



AMC/xFP is Ready

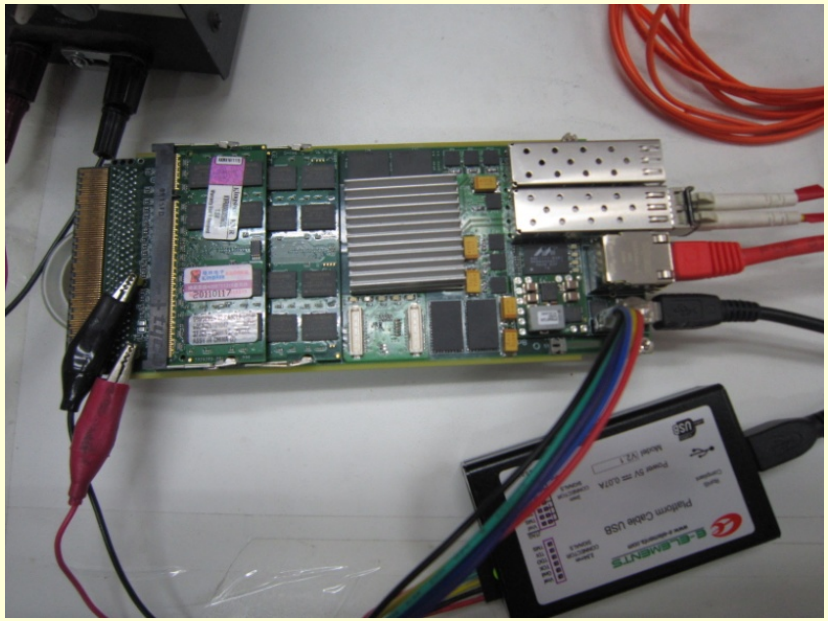
- FPGA:
  - XC5VLX50T

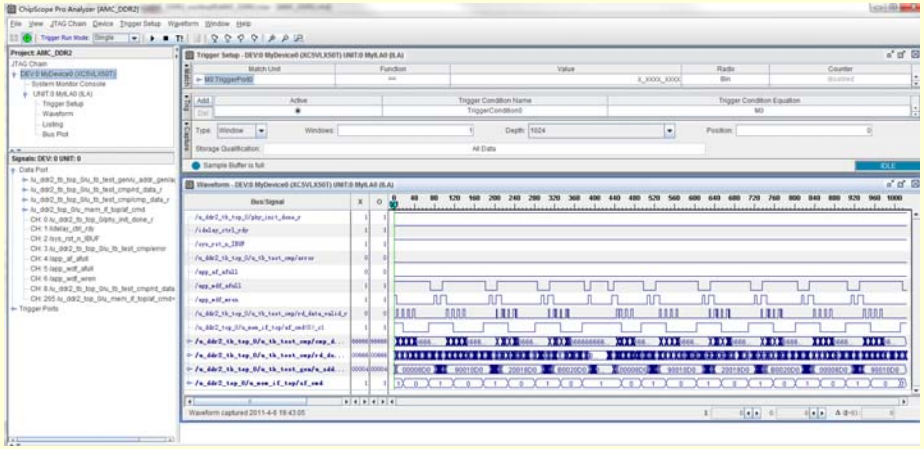


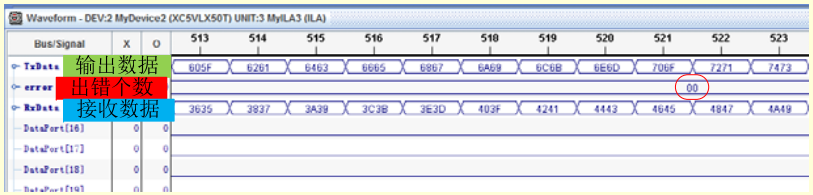


Test Results with AMC/xFP

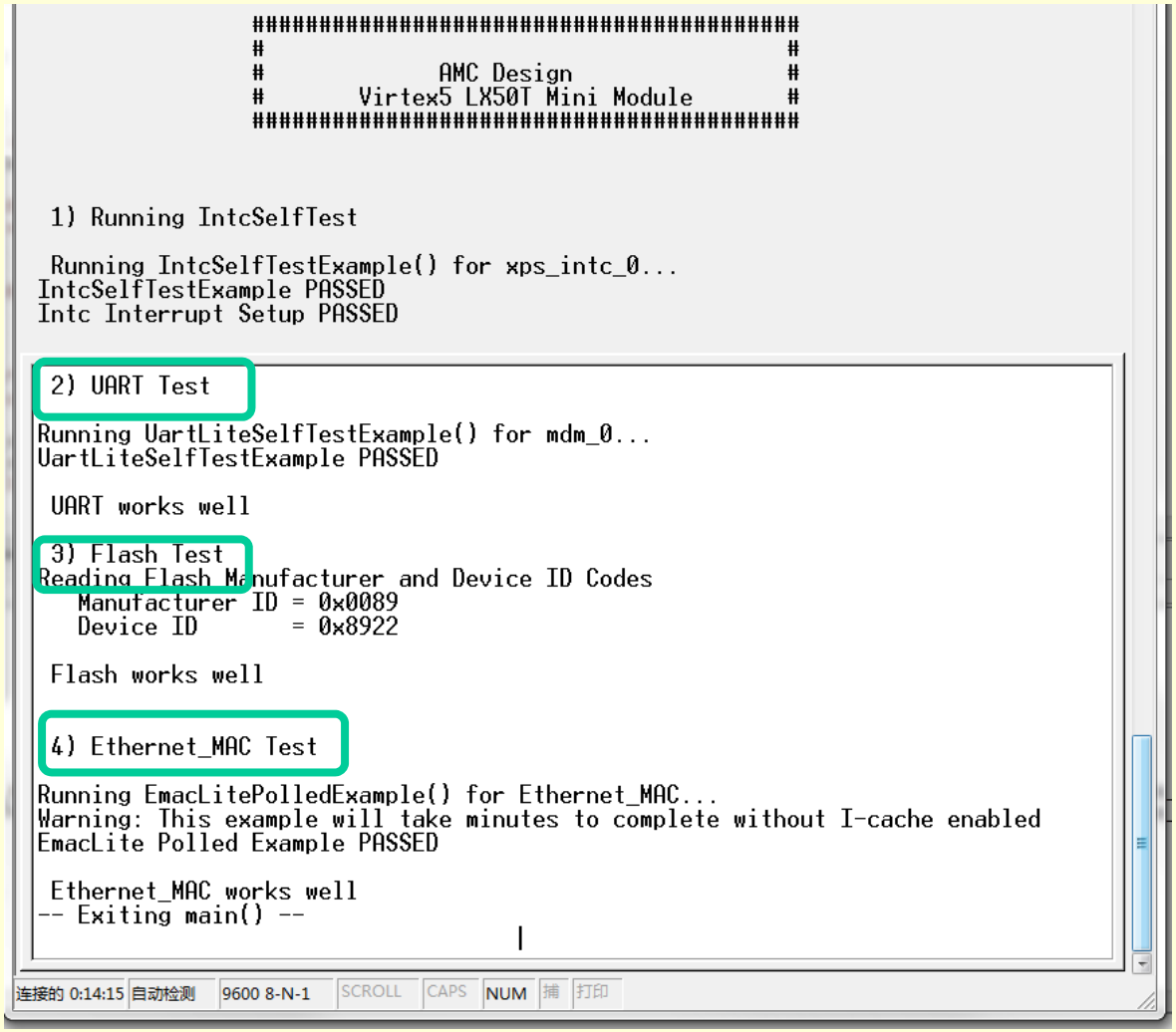
- Optical link @3.125Gbps
  - Tested about 1 hour with pseudo random data
  - Estimated BER < 8.6X10e-14
- DDR2 SDRAM
  - 2 x 2GB DDR2 @177MHz







Peripherals Test with Microblaze



PowerPC Version of xFP

- Required for the Memory/IO throughput
- XC5VFX70T with PPC
  - PCB compatible
  - Soldering, to be back in this week
- Test results will be ready for June PXD DAQ workshop

Development for SVD Concentrator

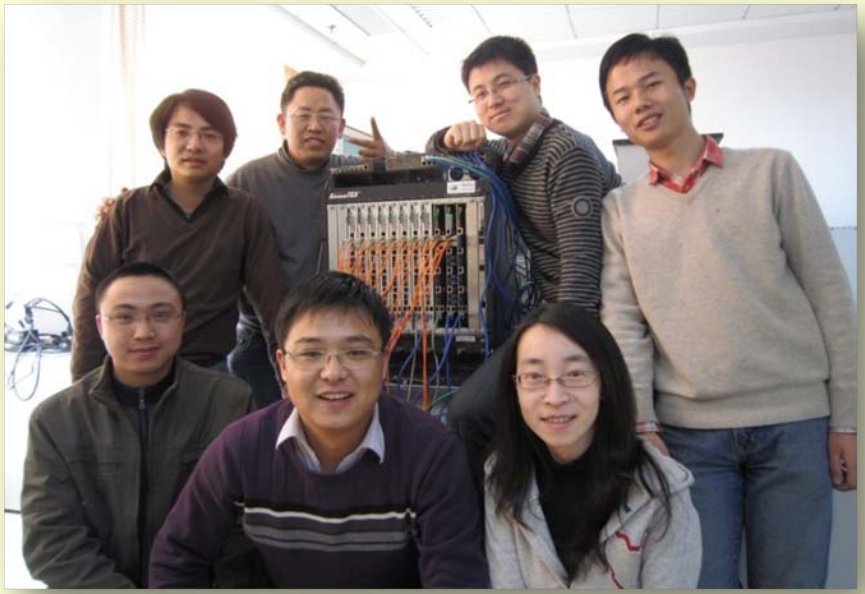
Discussed with Soeren, Carlos and Michael

- A possible approach: based-on the xFP module
  - 4 optical link inputs
    - 2 more transceivers needed
  - Considering tight space limitation, we have to remove
    - One DDR2 memory slot
    - Ethernet Jack and PHY chip
- Difficulties
- Positive on this collaboration
  - IHEP/U.Giessen/U.Bonn
  - More discussion will be made in June

Summary

- CN production in good shape
  - Hardware ready for firmware development
  - Good results for data throughput(even not satisfactory)
  - Algorithms development on CN going well
- xFP works well and new board with XC5VFX70T will be ready in 2 weeks
- Development for SVD started

Thank you for your attention !



Backup Slides