DEPFET pixel stability

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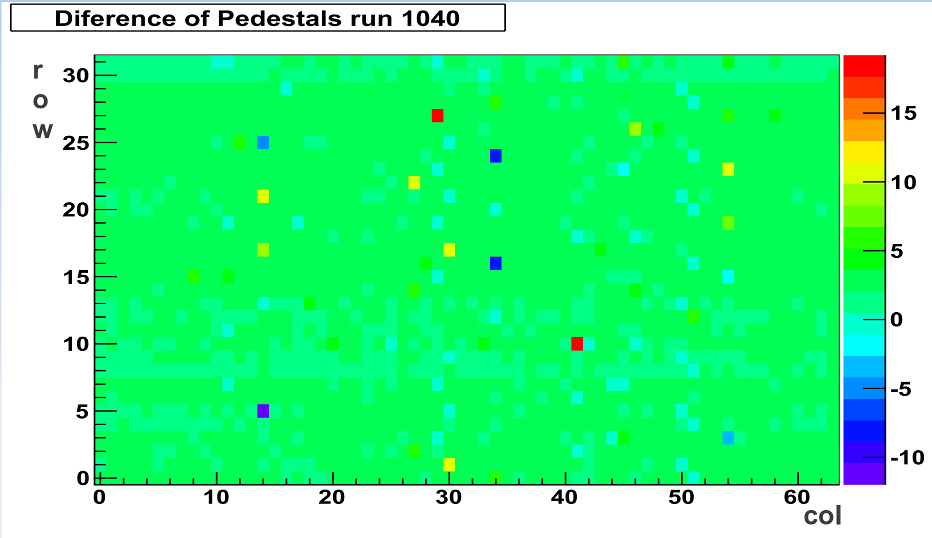
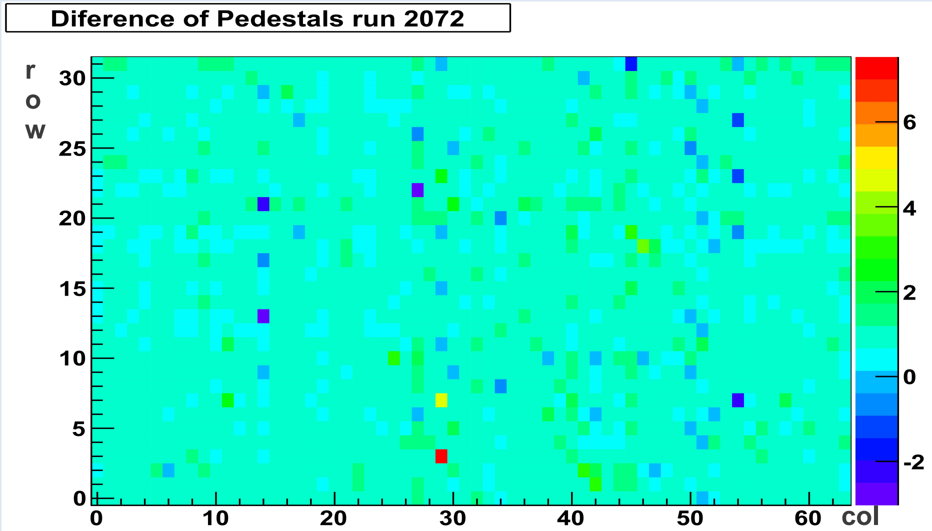
Pedestal Stability





- Difference of pedestals calculated between the first 5000 and the last 5000.
- Variation in run 1040 →

  2.3 ± 0.6
- Variation in run 2072 →

  0.9 ± 0.4
- This is a real error, because the statistical error is $\mathcal{E}_{ped} \approx 0$

Status Map

- Status Map changes from one run to other, noisy map even in the same run depending where we take the measures
  - Hot pixels and Noisy pixels are not always the same pixels
- Fixed Hot pixel cut comparing with a binomial distribution
- Noisy pixel cut fixed at 1.5 ADC units

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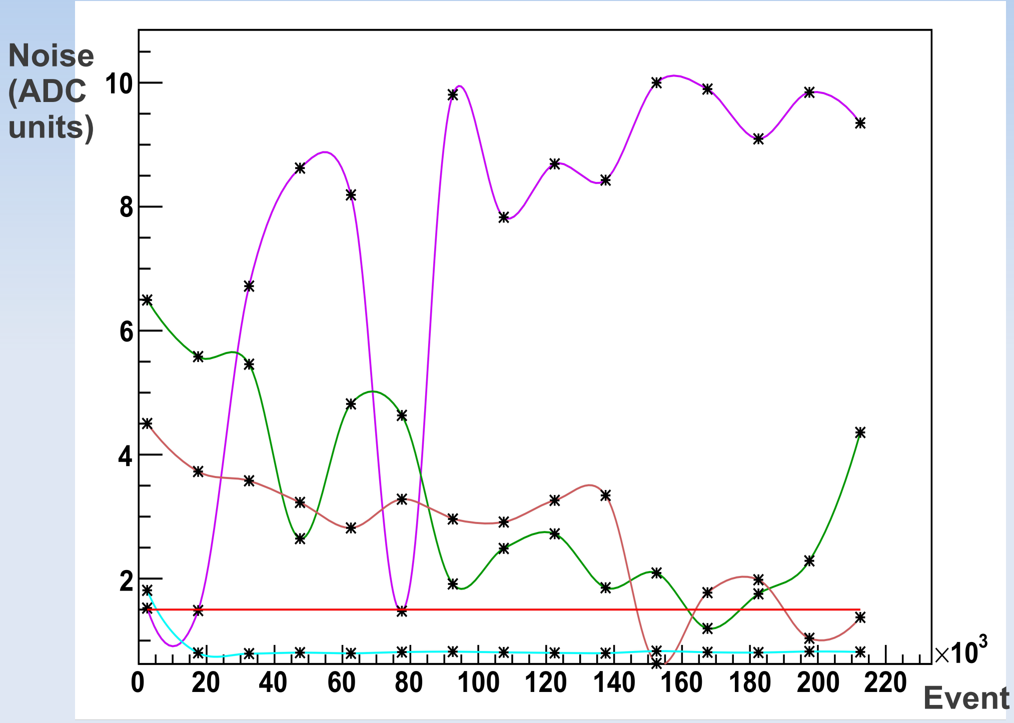
Noisy Map

- Studying the variation in one run we find that,
  - Bad pixels (always) ~ 3.9%
  - Very variable pixels ~ 0.5% (diference of noise > 1 ADC unit)
  - Variable pixels ~ 1.1% (diference of noise ≤ 1 ADC unit)
  - Good pixels ~ 94.5%
- Studying variation in different runs with same voltages (2072 and 2061),
  - Bad pixels (always) ~ 2.1%
  - Very variable pixels ~ 3.2%
  - Variable pixels ~ 1.9%
  - Good pixels ~ 92.8%

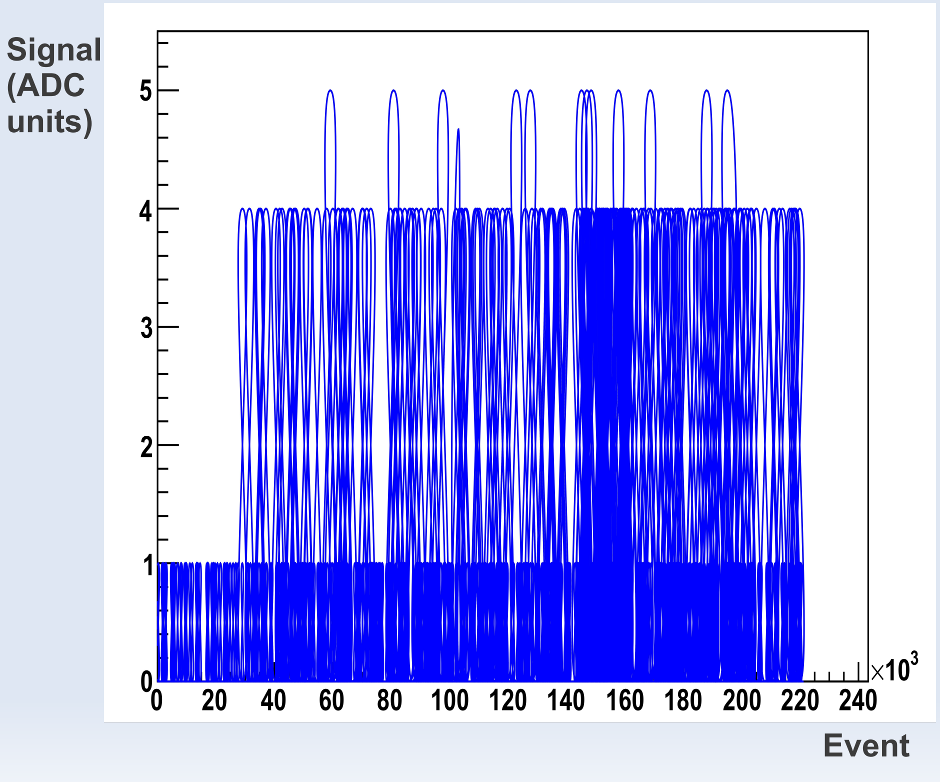
Noisy Map



- Noise measured with 5000 events in different places of run 2072 for 4 very variable pixels, seems that there's not an uniform behavior.

Hot Map

- Studying variation in diferents runs (same voltages),
  - Bad pixels (always) ~ 0.05%
  - Variable pixels ~ 1.4%
  - Good pixels ~ 98.5%



- ADC counts for a hot pixel, the values oscilate between 0 and 5 ADC counts, we measure the noise with the first 5000 events where there's low variation of counts.
- Only one hot pixel of diference calculing hot map with the first 50000 and the last 50000 events, it seems that some adc changes its behavior when initialize the device

Trailing Frames

- Trailing frames are runs in which we save four consecutive lectures of the matrix.
- This was implemented in the DAQ by Sergey Furletov and his team in the test beam of 2010.
- The measurements were performed at MPI by Christian Koffmane.
- The data available on Bonn server.
- This data allows us to measure the clear efficiency in a clean way.

Trailing Frames

- Measures taken with Cd-109 source.
- Clear voltage scan: all voltages are referred to source.

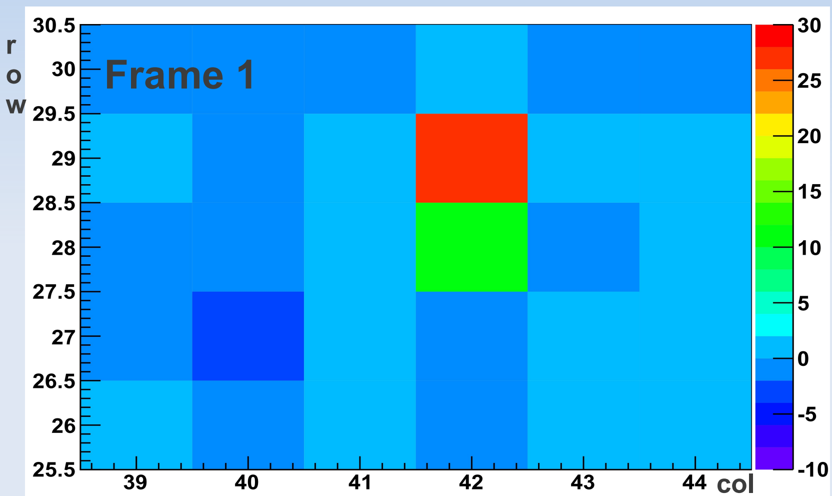
Date	Run	CCG(V)	ClearHi(V)	ClearLo(V)	GateLo(V)
15/2/2011	2072	-1.5	18	2.5	-3.65
28/4/2011	3007	-1.5	17	2.5	-3.65
28/4/2011	3008	-1.5	15	2.5	-3.65
28/4/2011	3009	-1.5	13	2.5	-3.65
28/4/2011	3011	-1.5	22.5	2.5	-3.65
28/4/2011	3012	-1.5	20.5	2.5	-3.65
28/4/2011	3013	-1.5	24.5	2.5	-3.65

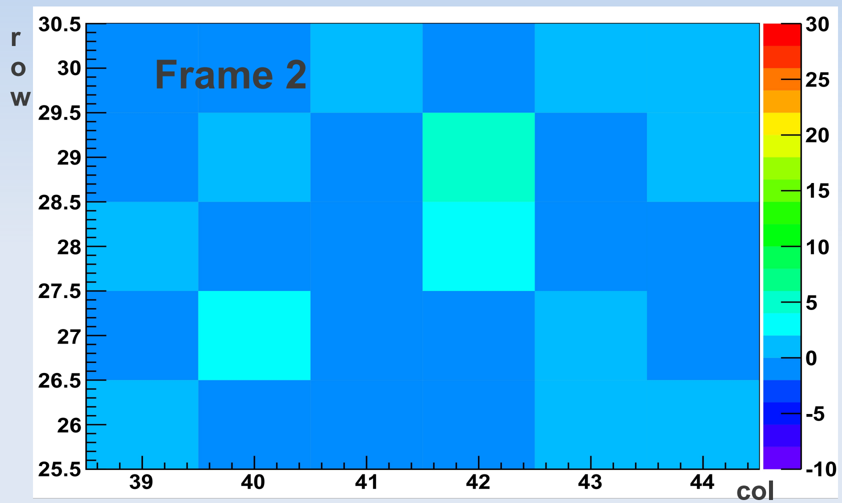
Trailing Frames

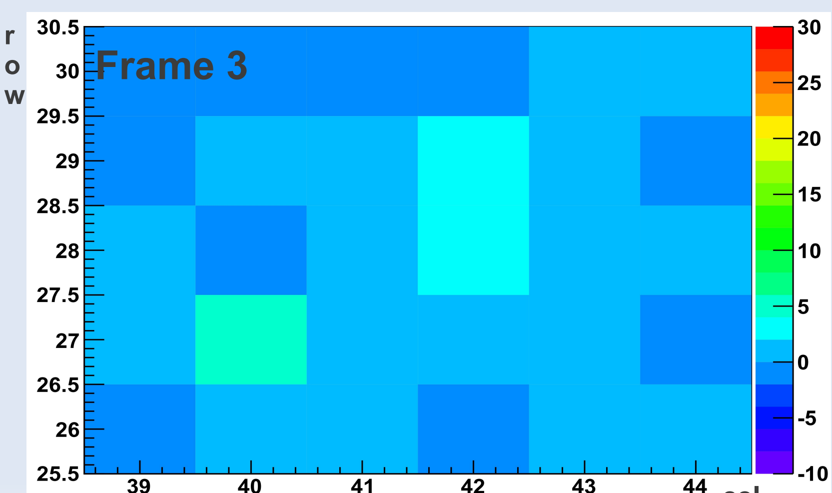
- A faint ”shadow” of the signal is visible after clear pulse.

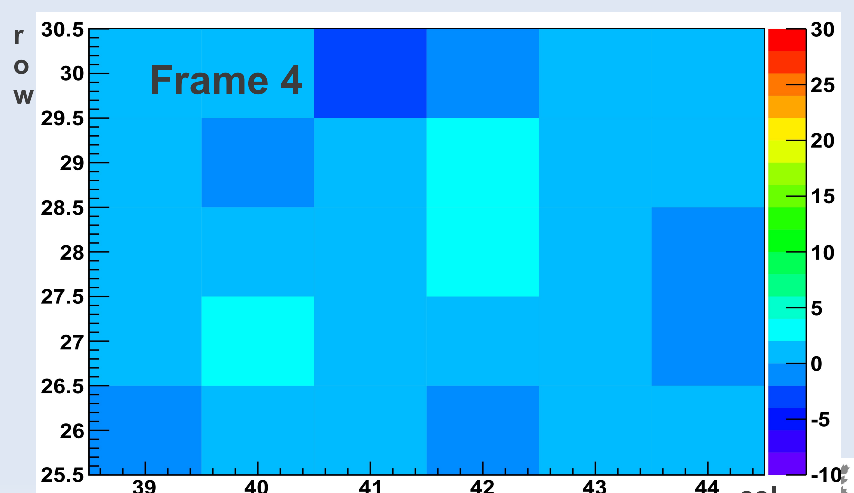
Run 2072

$$V_{CL}^{eff} = 15.5\,V$$









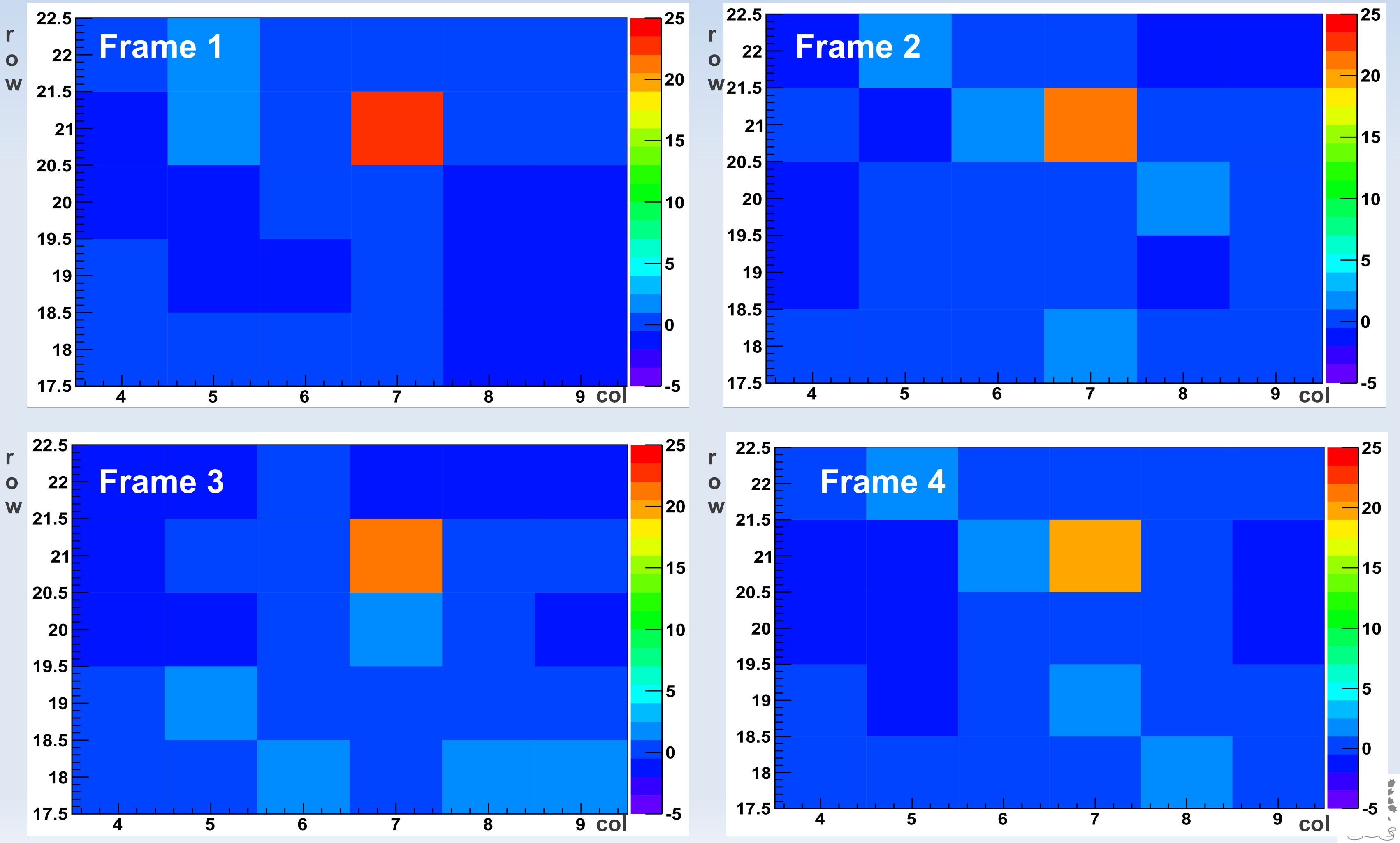
- ADC counts after common mode and pedestal correction for four consecutive frames.

Trailing Frames

- For low clear voltage, the signal remains large in multiple frames

$V_{CL}^{eff} = 10.5\,V$

Run 3009

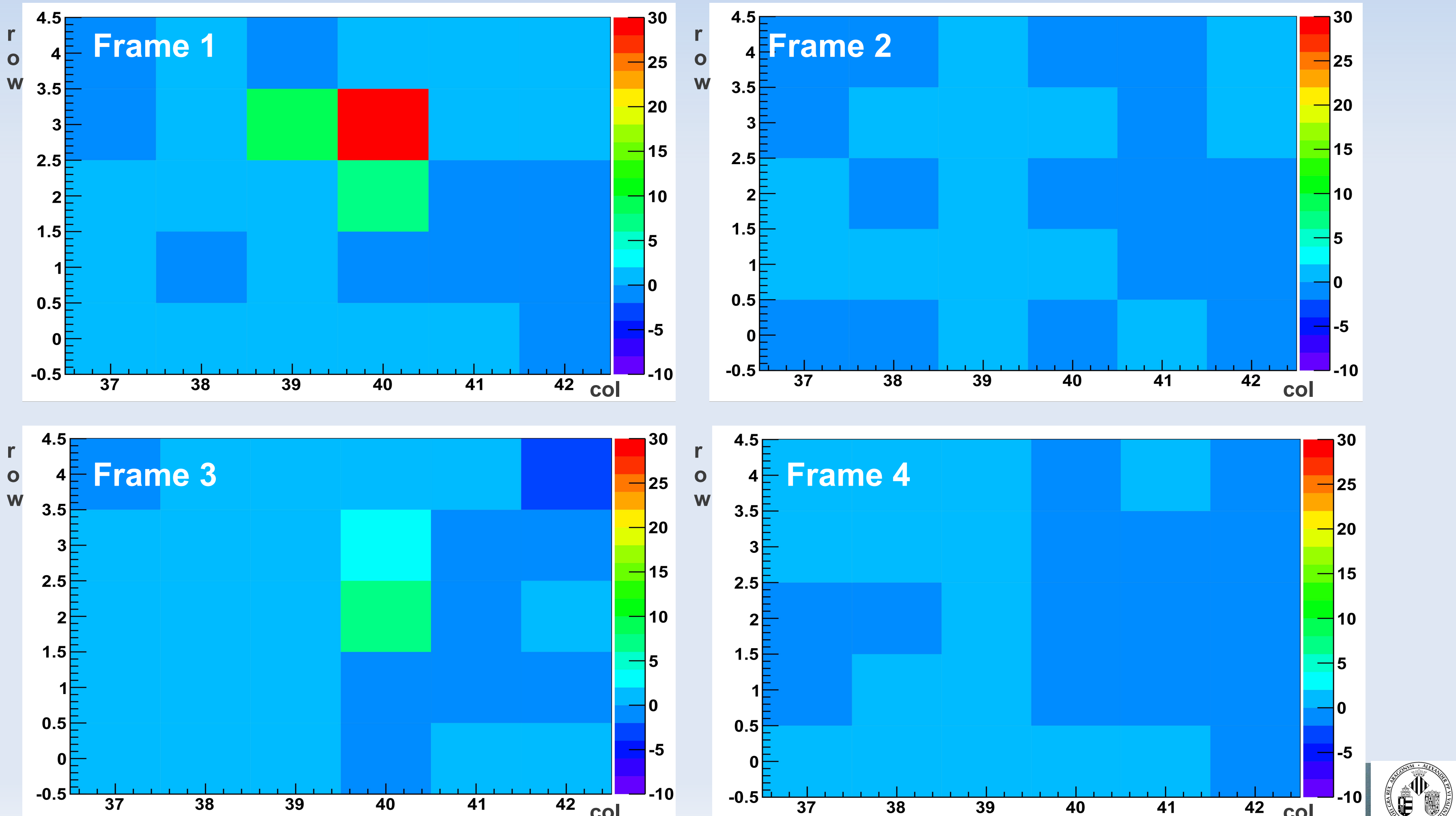


- # Clusters increases strongly when V_{CL}^{eff} diminishes. As the clear is inefficient we see the same cluster more than once.

Trailing Frames

- Raising the clear voltage, a complete clear is achieved

Run 3013 $V_{CL}^{eff}=22\,V$

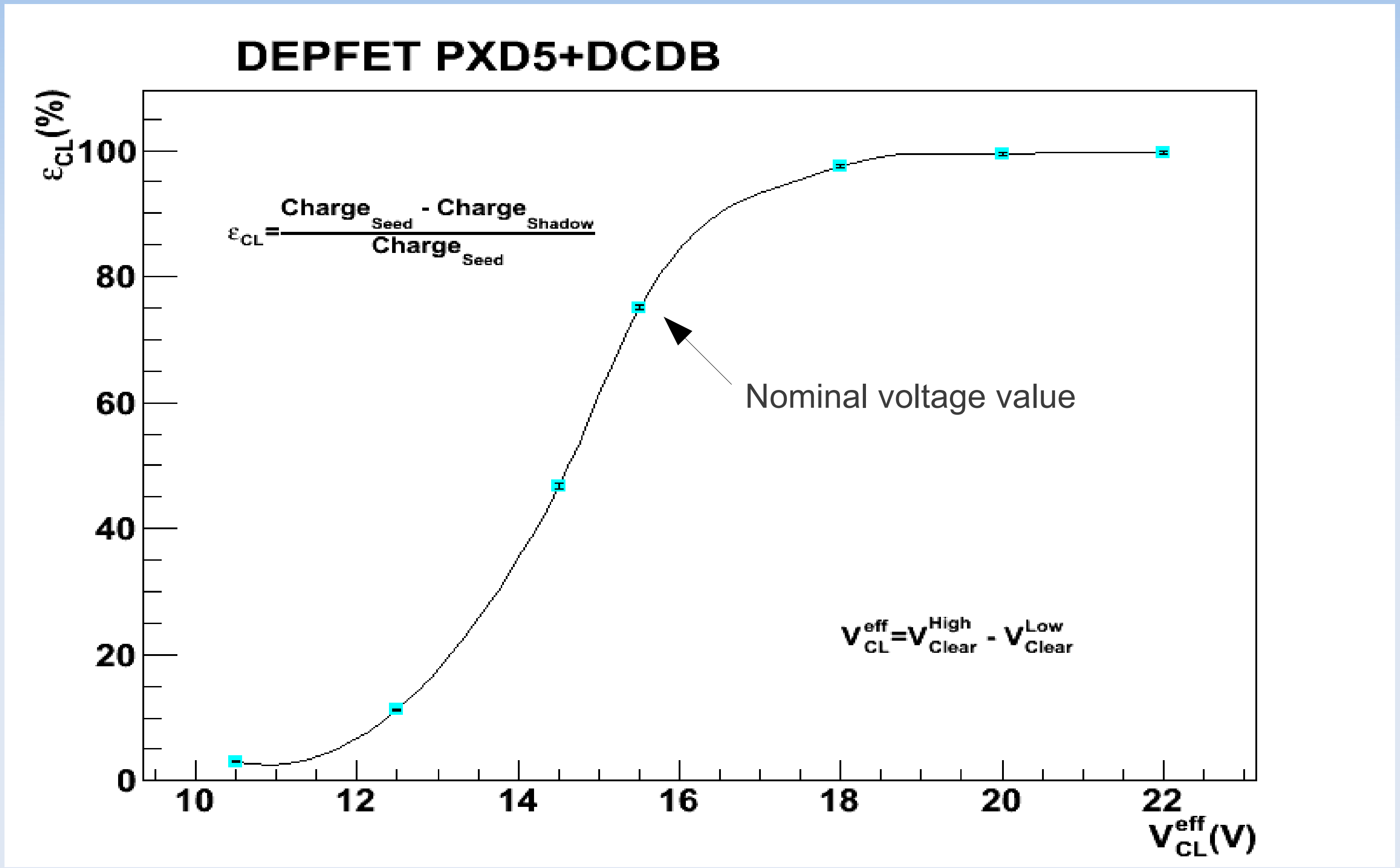


Trailing Frames: Clear Efficiency

- We measure the clear efficiency by comparing the signal on the seed pixel before and after applying the clear voltage.
- Measure clear efficiency vs. Clear voltage

$$Clear\ Efficiency = \frac{Seed\ Charge - Shadow\ Charge}{Seed\ Charge}$$

Clear Efficiency



- We've measured a sligth dependence on clear efficiency vs. seed charge.

Conclusions

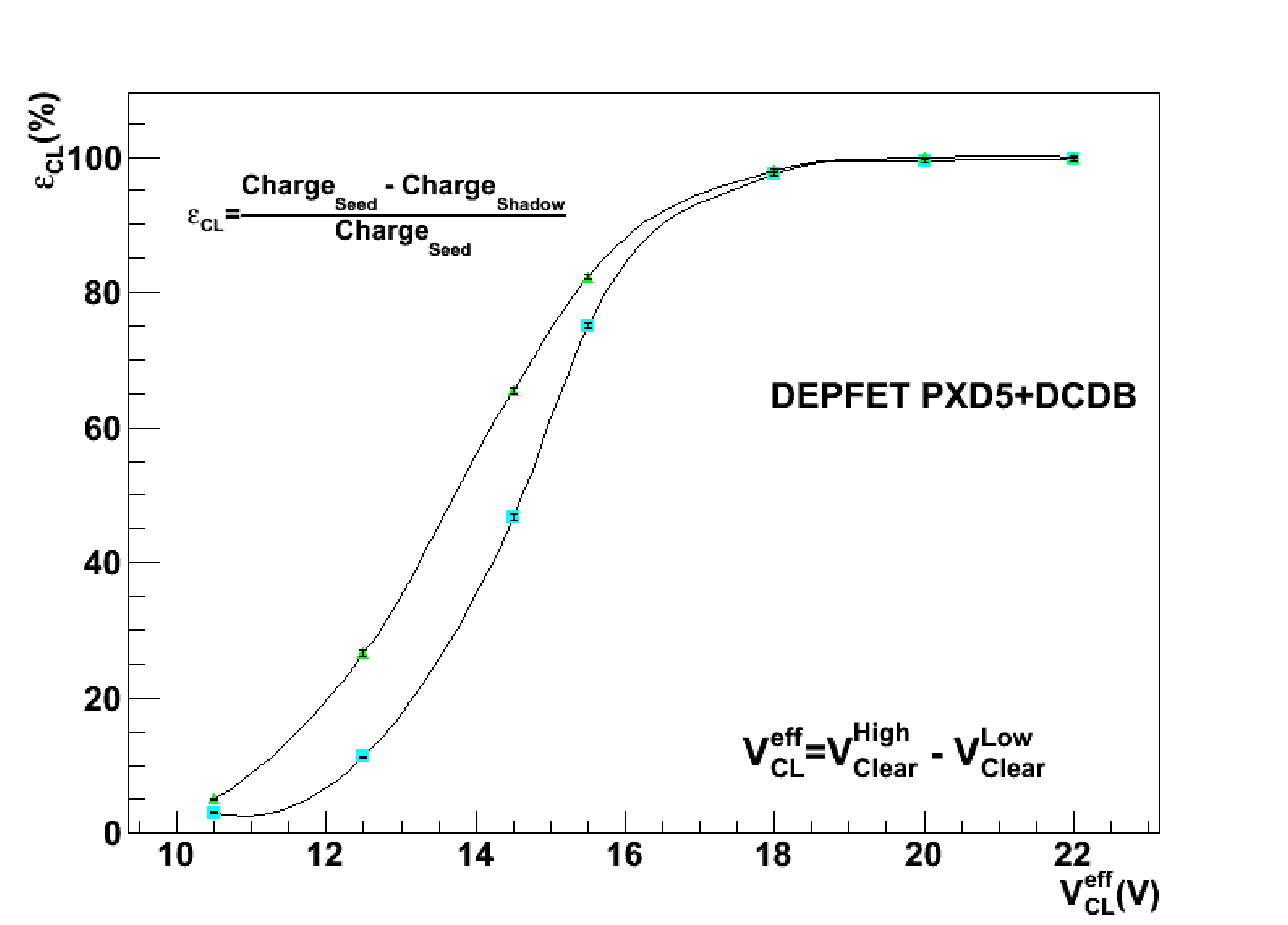
- There are ~5-7% of bad pixels on PXD5+DCDB
  - See Benjamin's talk Bonn 2011

- This DCDB allows characterization of PXD6 sensors

- Source runs with trailing frames allow us to measure the clear efficiency vs. V_{CL}^{eff}

Back up slides

Clear Efficiency vs. V_{CL}^{eff}



- Blue: Calculated with all seeds.
- Green: Calculated with seeds higher than 20 ADC counts.