LMU München - Excellence Cluster Universe

UPDATE on PS development

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Overview

- Organization
- Updates on requirements
- Engineering aspects
  - System overview
  - Multichannel prototype
  - PS form factor & space needs
  - HV – channel
- Outlook

PS Development – Organisation

- Group from Krakow interested to join the PS development effort
  - Started with hardware tests
  - Will look into Overvoltage protection / Hardware safety system
  - Organizing a longer stay of a designer in Munich
- Manpower
  - More and more students are interested to work in our group
  - Helpful support for testing & Labview programming
- Firmware development is ongoing

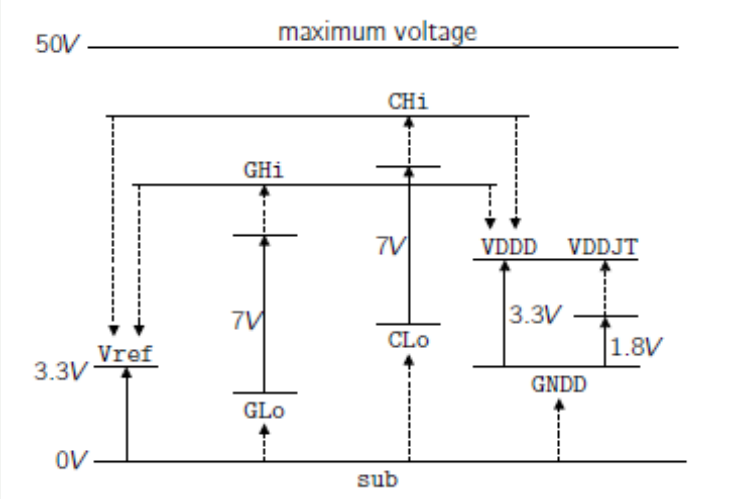
  → See my next talk

Update on requirements

- New input from HLL → have to be prepared for threshold voltage shift
  - Segmentation of MOS-structures
    - 3 Gate_On – 3 CCG - voltages
  - Range of voltages has increased (CCG, Gate)
  - Ability to put Gate_On below GND
  - Gate_OFF needs bipolar output (~ +5 to -5V)

→SW_SUBS can‘t be put on GND anymore

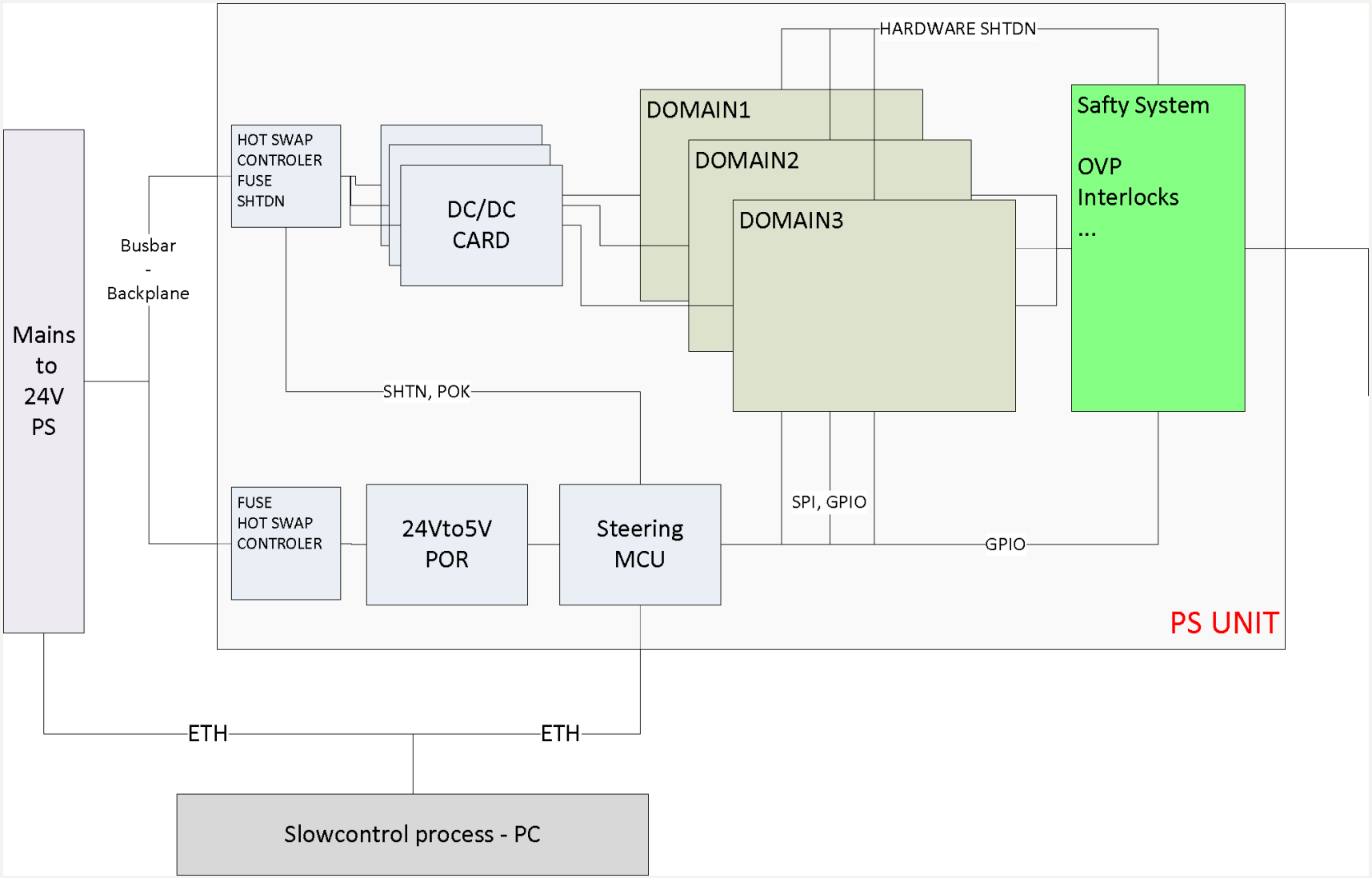
[from SWB manual]



Old biasing:	New biasing:
VREF : SW_DVDD	VREF : -10V + 3.3V
SW_SUB : GND	SW_SUB : -10V

- Need 6 additional voltages
- With this scheme steering voltages can be easily applied with respect to source

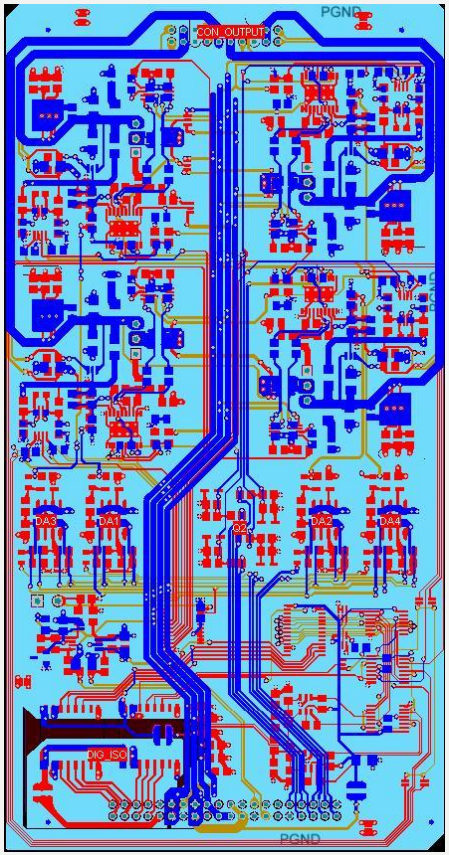
System overview



PS Development – Multichannel prototype

- Design of multichannel prototype finished – “Analog Prototype”
  - Digital interface via DAC-PCI card and ADC
  - Organized in 4 modules with 4 channels
  - 4 layer PCB, 75*145mm2

- Flexible design:
  - With/without remote sensing
  - Positive- or Negative Output, sink or source
  - Flexible over current protection
  - Clear_OFF can be derived form Clear_On
  - Monitoring of currents and voltages
  - Status outputs



PS Development – Multichannel prototype

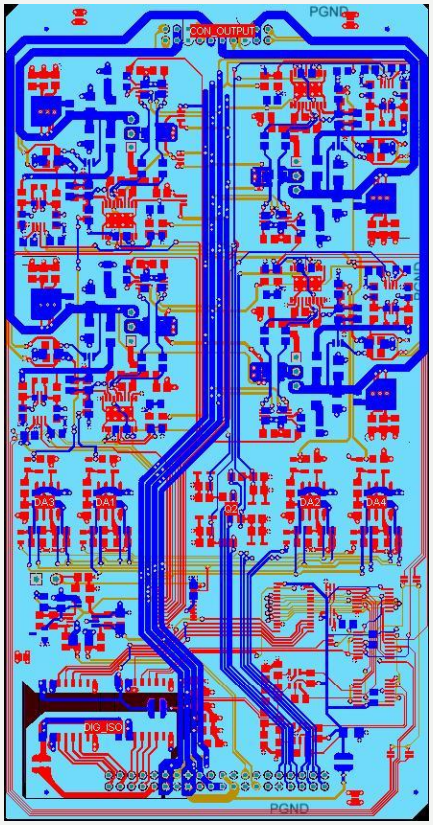
- Compact channel (~9cm2)
  - Regulator (~2.5 cm) + pass element (.5cm2)
  - Space for heat sink (~2cm2)
  - Monitoring (~2.5cm2)
    - Current sense
    - Voltage sense
  - Current source @ each output (.8cm2)
    - Allows the regulator to sink current
    - Interesting for DCD_AVDD, steering voltages

- Auxiliary circuitry
  - Digital isolators (now for steering of MUX, later for SPI)
  - Range adjustment for the DAC output
  - Common shutdown

→ Layout is there and will serve as baseline for the next iteration

→ Based on this we can make a first estimate on system-size

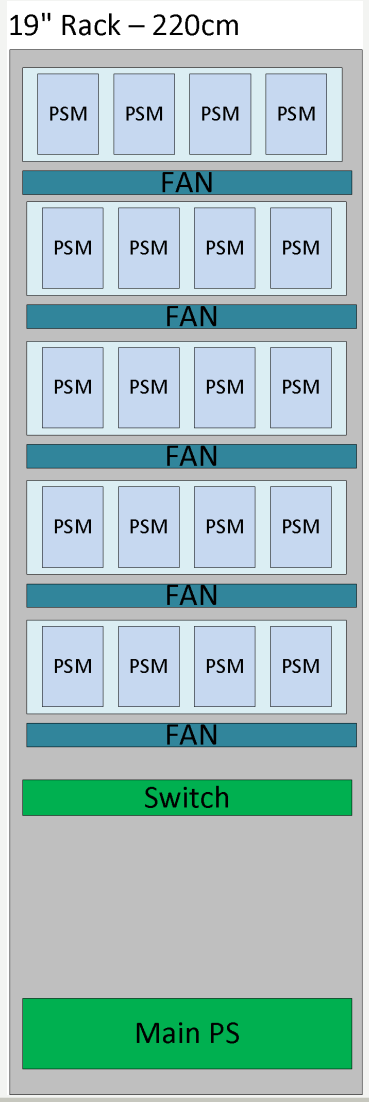
→ After commissioning first tests with DEPFET-system can be done



PS form factor & system size

- Baseline for electro-mechanics
  - → Use of standard 19" components
  - → Good HF properties
- 24V Main power supply (e.g. TDK-Lambda GENSYS, 2U)
  - 3 kW (ε - DC/DC, ε – regulator, auxiliary)
  - 24V power distribution via bus bar + backplane
- PS modules – standard cassettes 6HE-21TE → 10 crates
- Cooling - 19" fan unit 1U → 1 per crate
- Connectivity – ETH - Switch ~2U
- Cooling interlock via backplane
- Connectivity (ETH, JTAG, Detector output) on front-side of PS-module

→ First estimate: 2 two racks - more precise estimate by Autumn



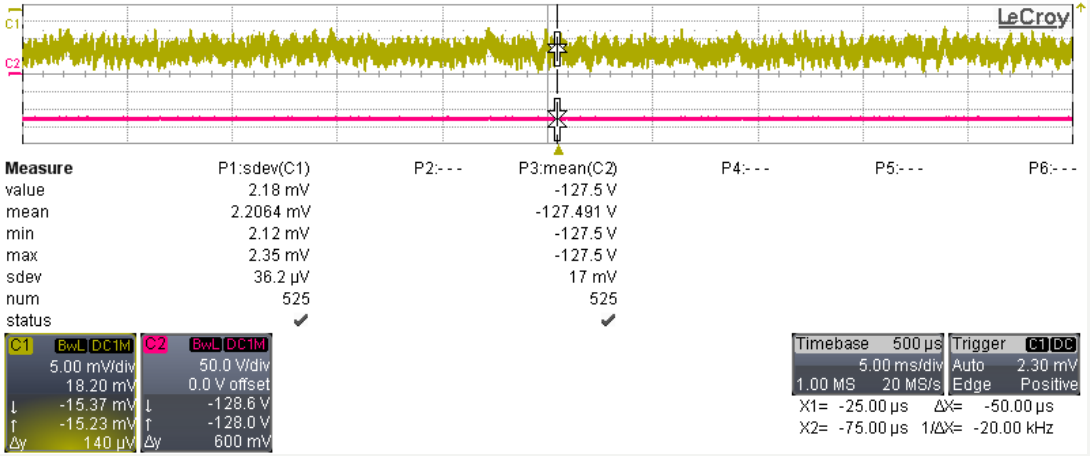
HV - channel

- First prototype ready & tested
  - HV DC/DC converter
  - Shunt post regulator

- Specifications
  - 0-200V output settable
  - 1mA output current
  - Precise current and voltage monitoring

- Performance
  - Noise 2.2mVrms (0.1Hz-20MHz)
  - Still switching remnants visible 8mVpp

  →Second iteration with better filtering should solve this problem



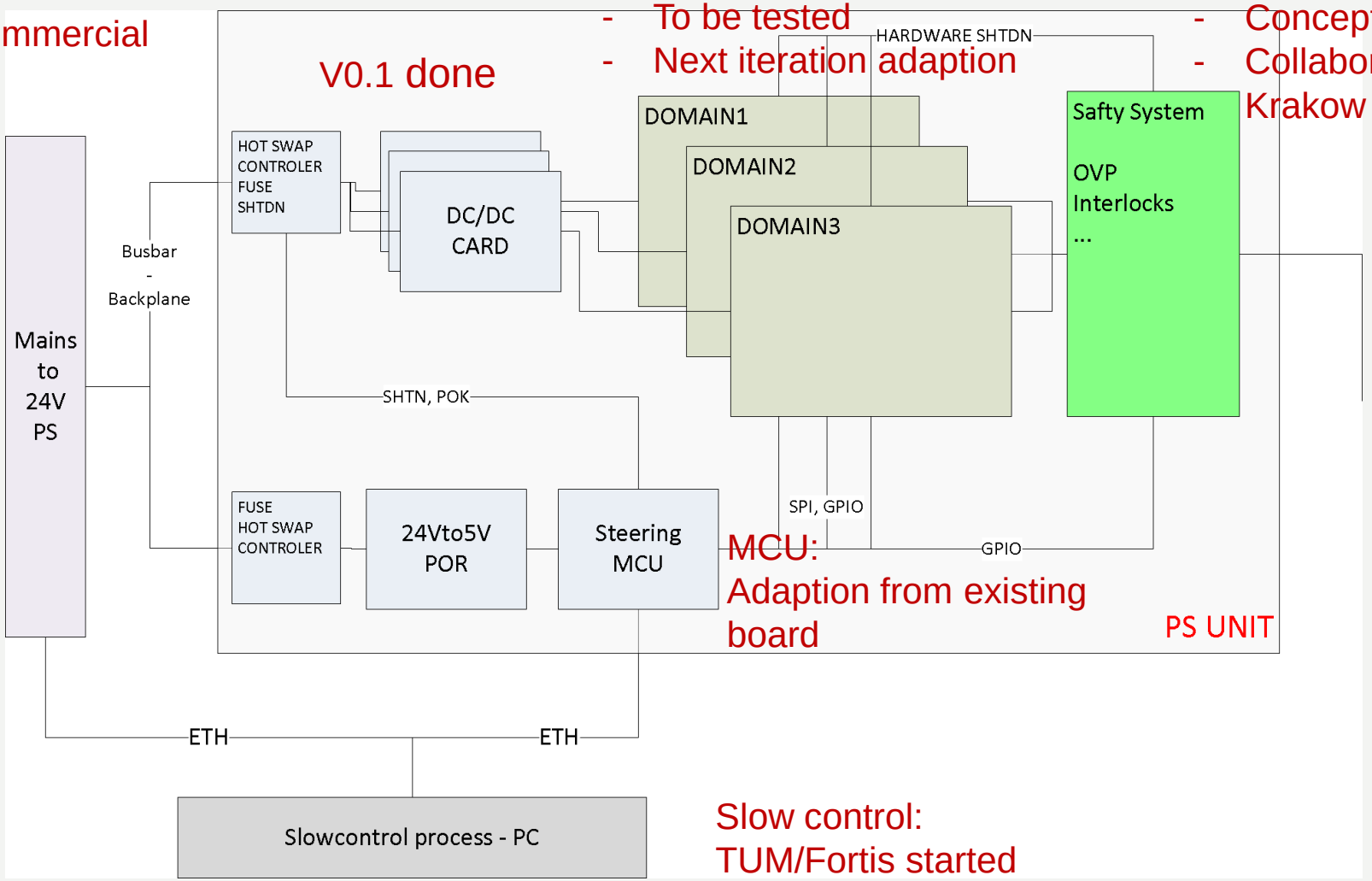
Status - Overview

Commercial

V0.1 done

16Ch prototype done:
- To be tested
- Next iteration adaption

Safety:
- Concept done
- Collaboration with Krakow



MCU:
Adaption from existing board

Slow control:
TUM/Fortis started

Next steps

- Next steps
  - Integrate DAC/ADC into Multichannel prototype
    - → Adaption of existing design
  - MCU – Steering card
    - → Adaption of evaluation board
  - Hardware safety – OVP
    - → Krakow

- Since our last Ringberg meeting in May 2009 we made significant progress

- Full scale electrical prototype by end of this year