UNIVERSITÄT
HEIDELBERG

DCDB Performance and Operation Updates

Schaltungstechnik
und Simulation

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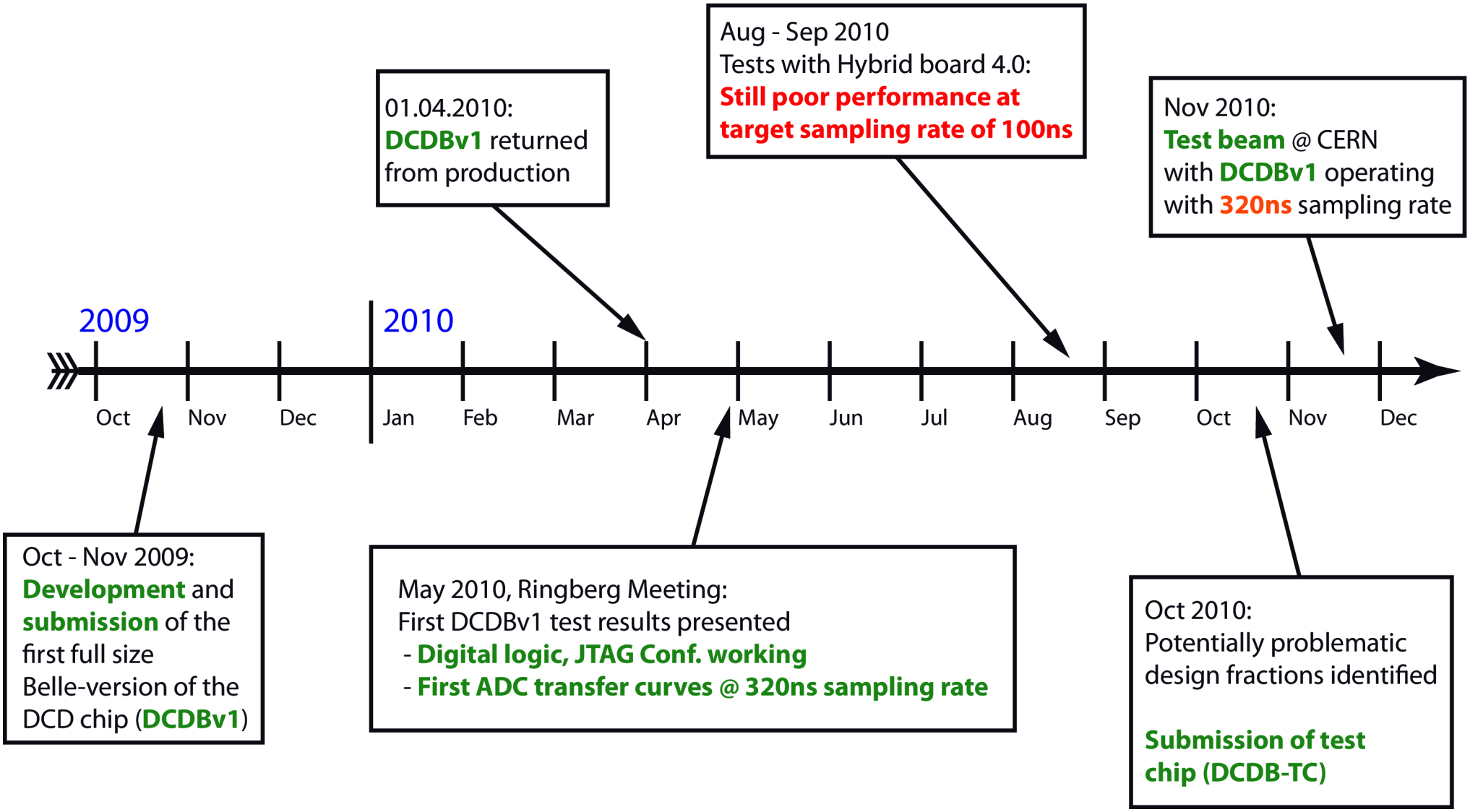
Agenda

- Introduction: History of the DCDB Development
- Part I: Latest Improvements in DCDBv1 Performance
- Part II: DCDB in DEPFET Readout Operation - Dynamic Offset Compensation
- Part III: DCDB-TC Measurement Results

Introduction: History of DCDB Development

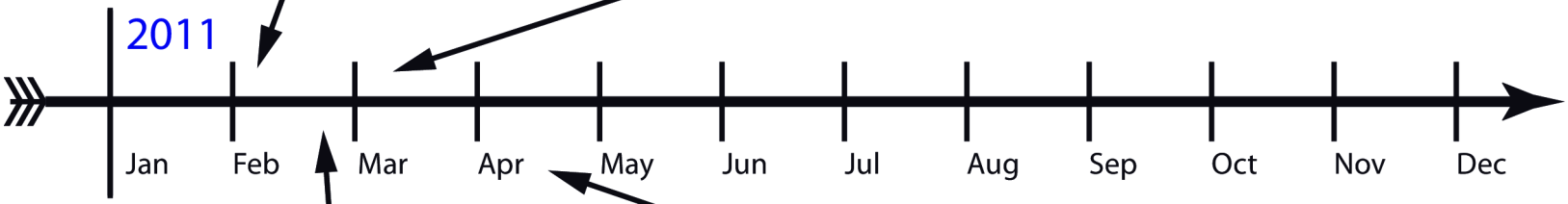
History of DCDB Developments (1/2)



History of DCDB Developments (2/2)

Feb 2011:
DCDBv1 Operating **@100ns** with **reasonable performance**

Mar 2011:
The next full size chip, **DCDBv2**, was **submitted**

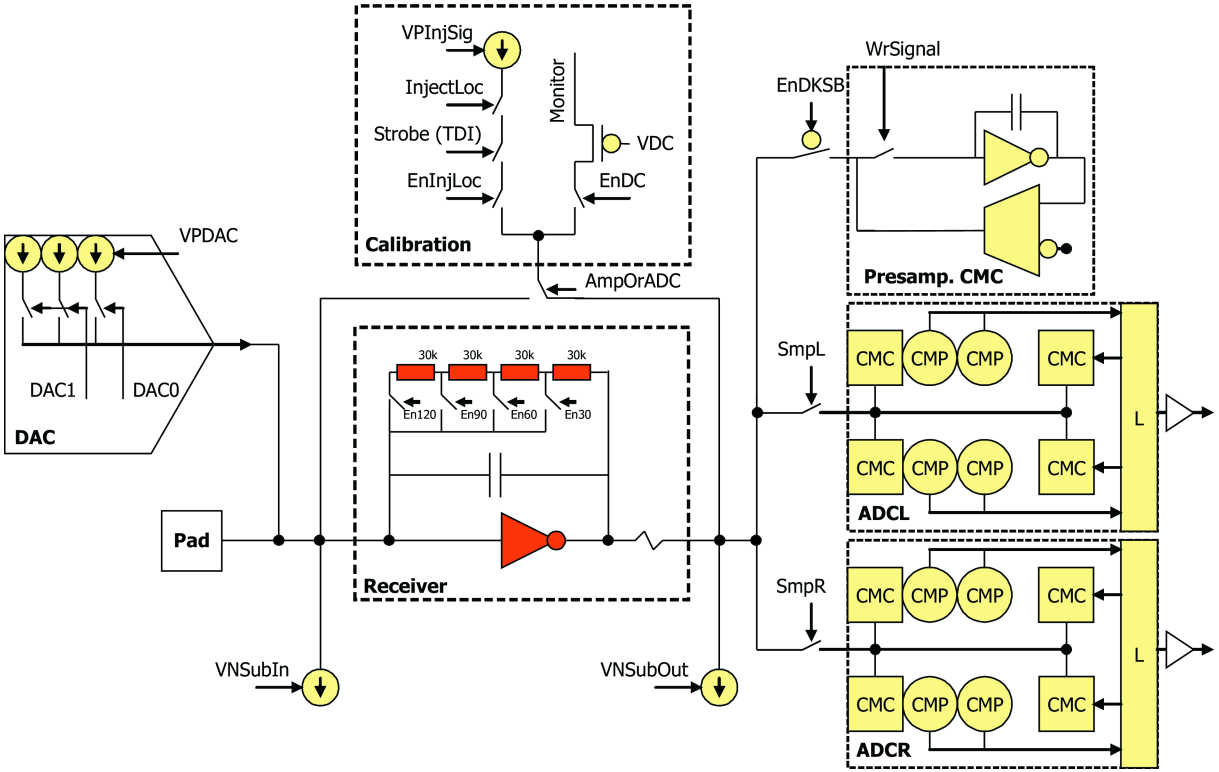


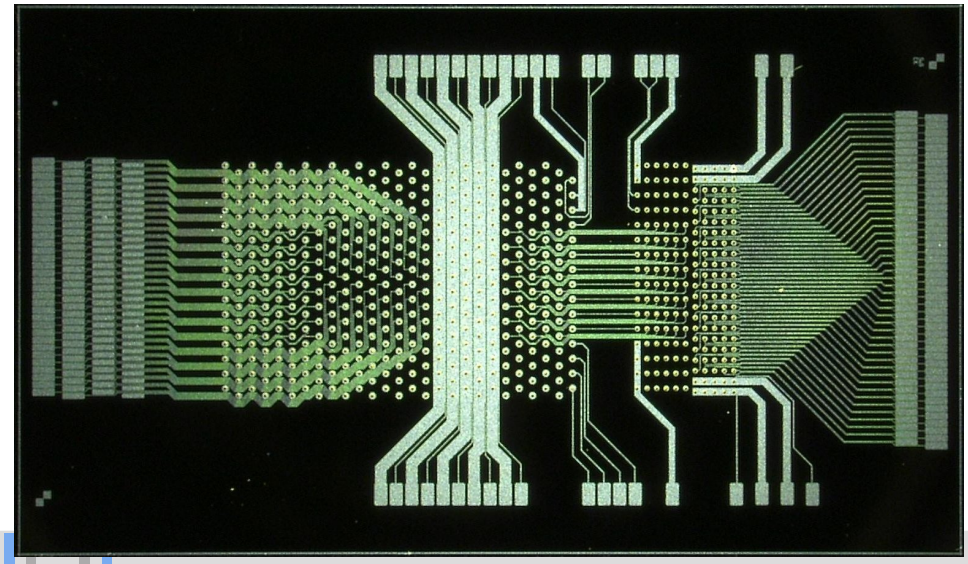
Feb 2011:
DCDB-TC returned from production

Apr 2011:
Significantly improved performance of the DCDBv1 at target sampling rate of 100ns

Part I:
Latest Improvements in DCDBv1 Performance

What Led to the Improvements?





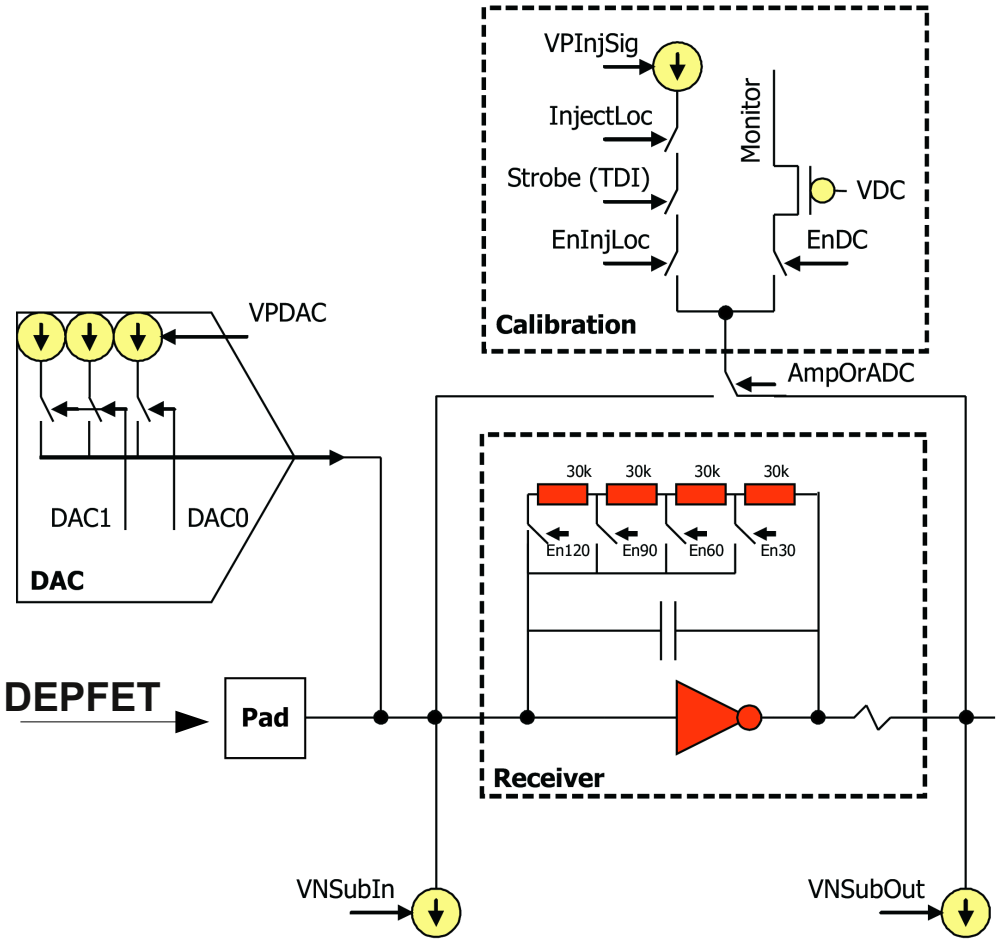
Get better understanding by detailed measurements:

- Potential of internal nodes
- TIA Characterization
- ADC's Current Memory Cell Characterization

Results:

- Suboptimal bias of TIA
- Voltage drop, **NOT primary inside the chip but on the WB**

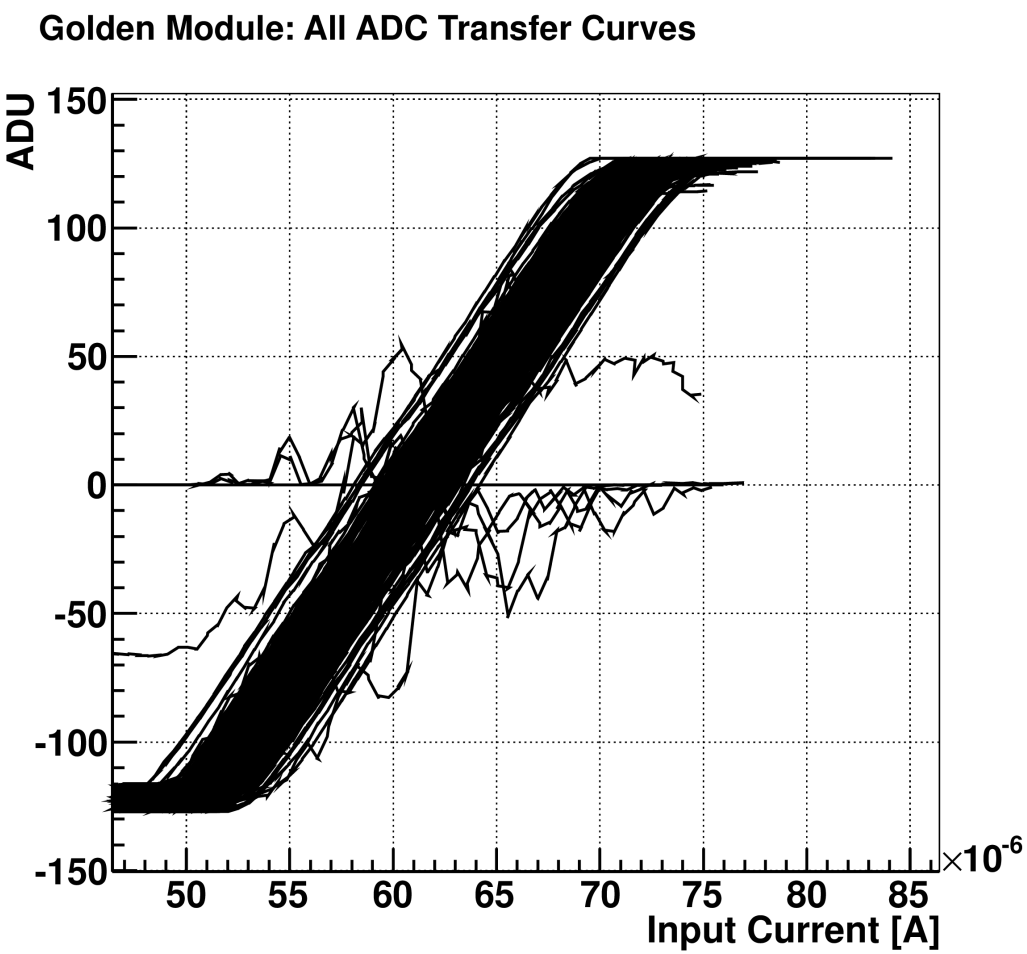
Measurement Setup



Scenario:

- TestBeam 2010 Module used!
- Signal sampling rate : **100ns**
- Single matrix row is constantly activated.
  → Offset Current (with variation)
- Offset is subtracted by current source **@max!**
  (VNSubIn = 127) → Realistic!
- Signal is generated by internal source, each calibrated via SMU.

The DCDBv1's Current Performance (1/5)



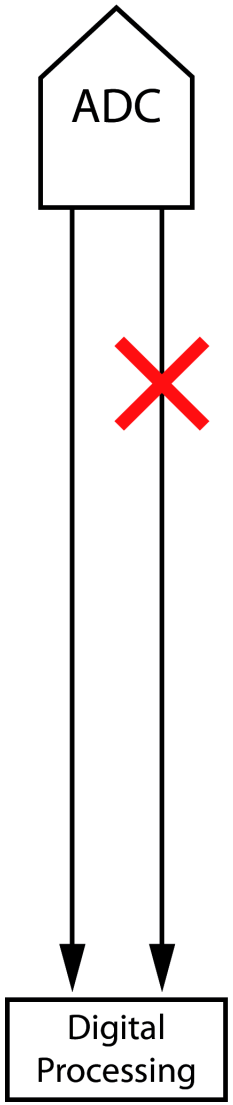
Facts:

- 100ns sampling rate!
- Transfer curves of all 256 accessible ADCs
- Each point is the mean of 100 samples
- **Here: 1ADU = ~84nA**

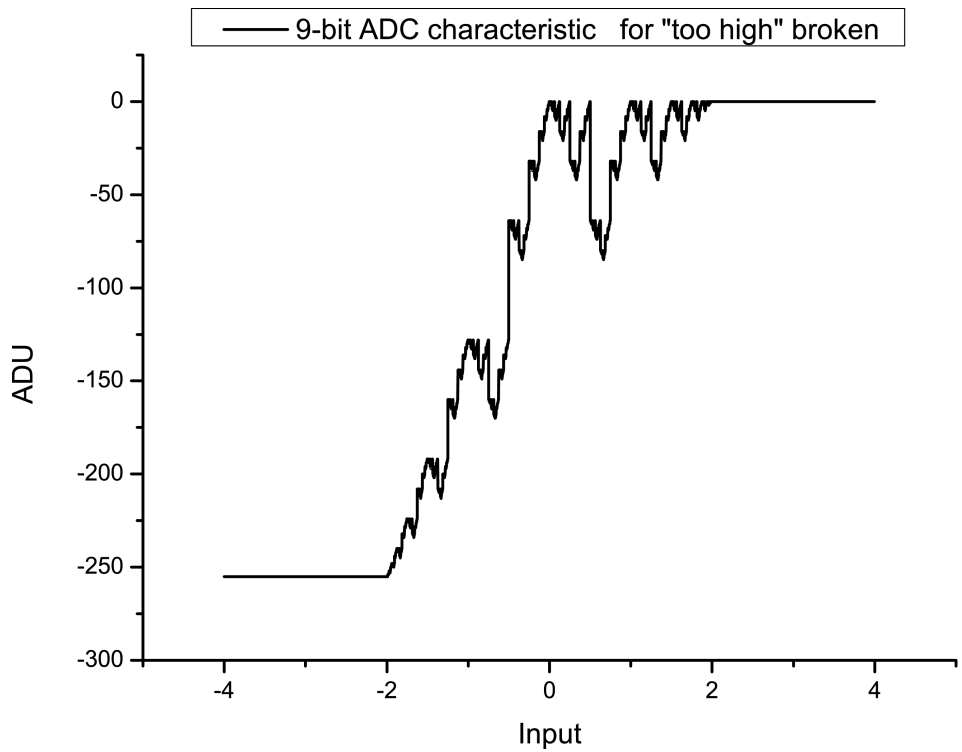
Conclusions:

- 8 bad ADCs have already been identified during TB2010 analysis.
- Vertical dispersion: ~73LSB. Note: This includes DEPFET variations!

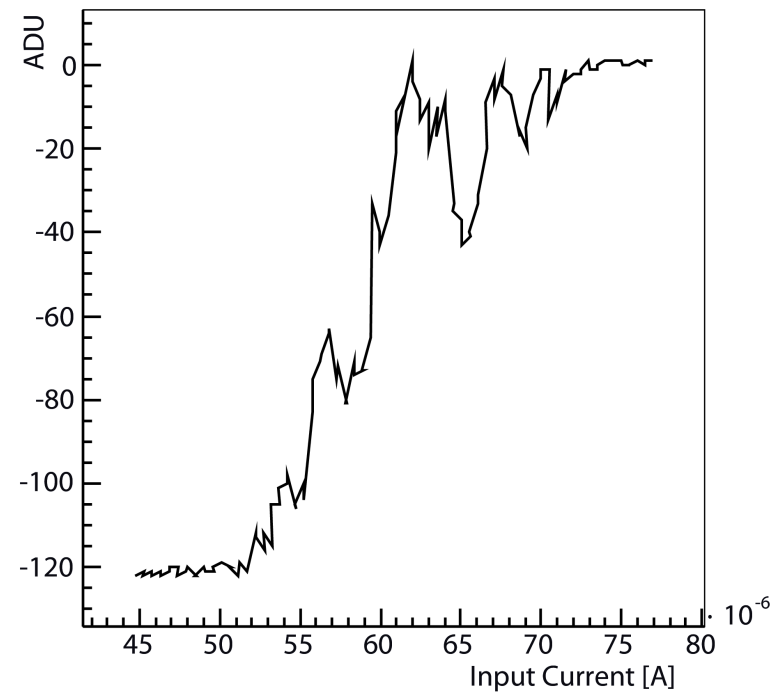
A Propos: Bad ADCs



Simulation of the ADC transfer curve with one of the two lines being broken.

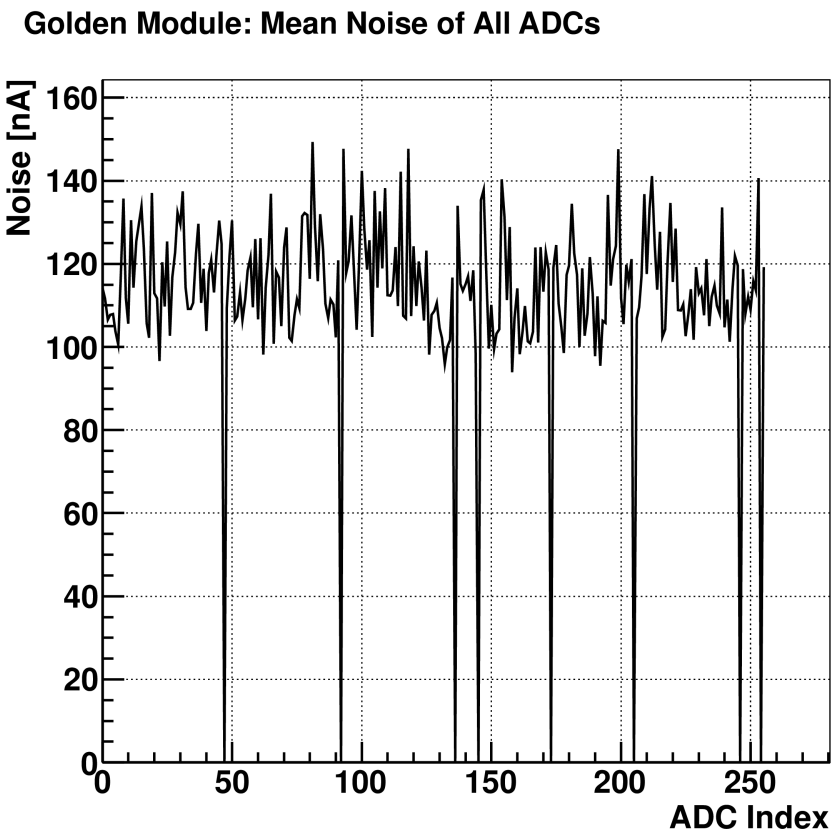


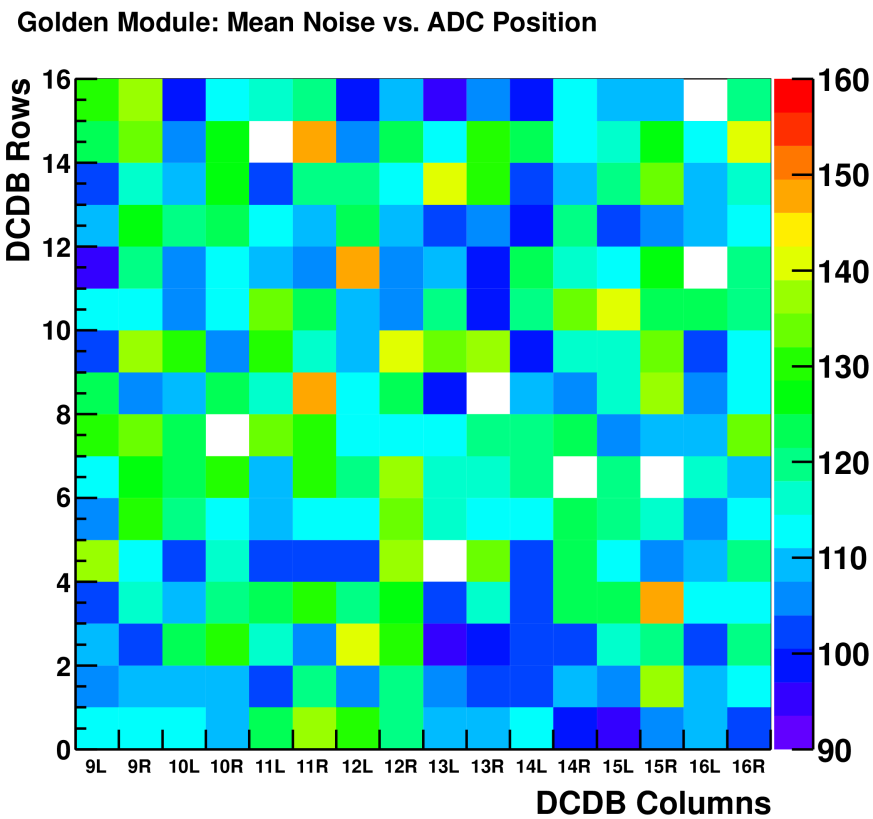
Measurement: Bad ADC's Transfer Curve



→ Fits to at least 6 of the broken ADCs of the Golden Module.

The DCDBv1's Current Performance (2/5)



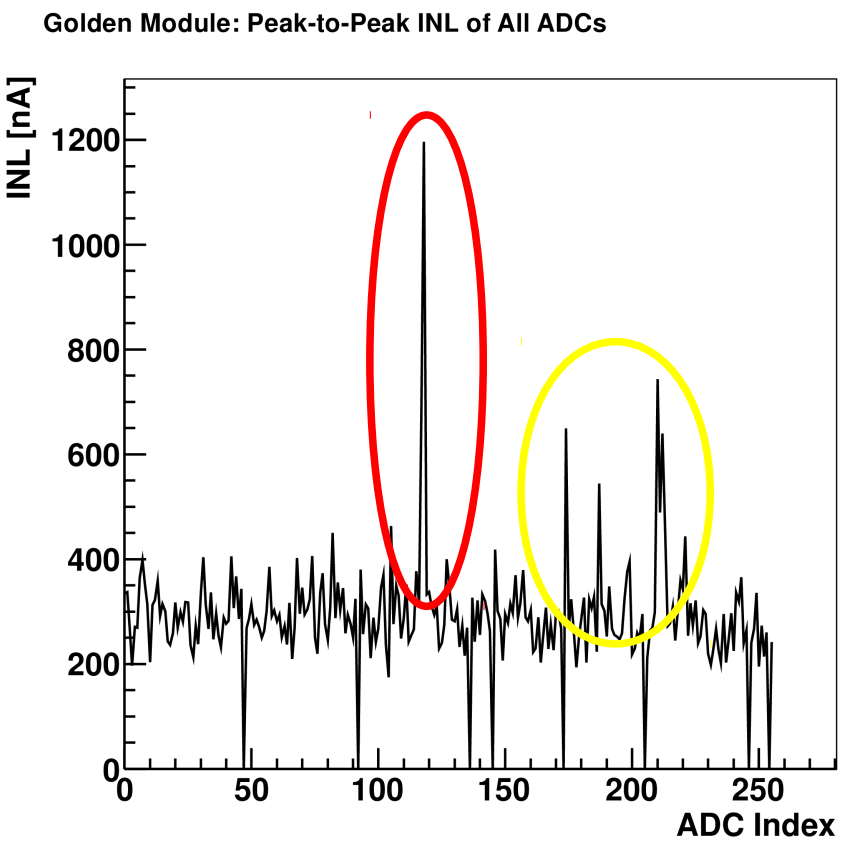


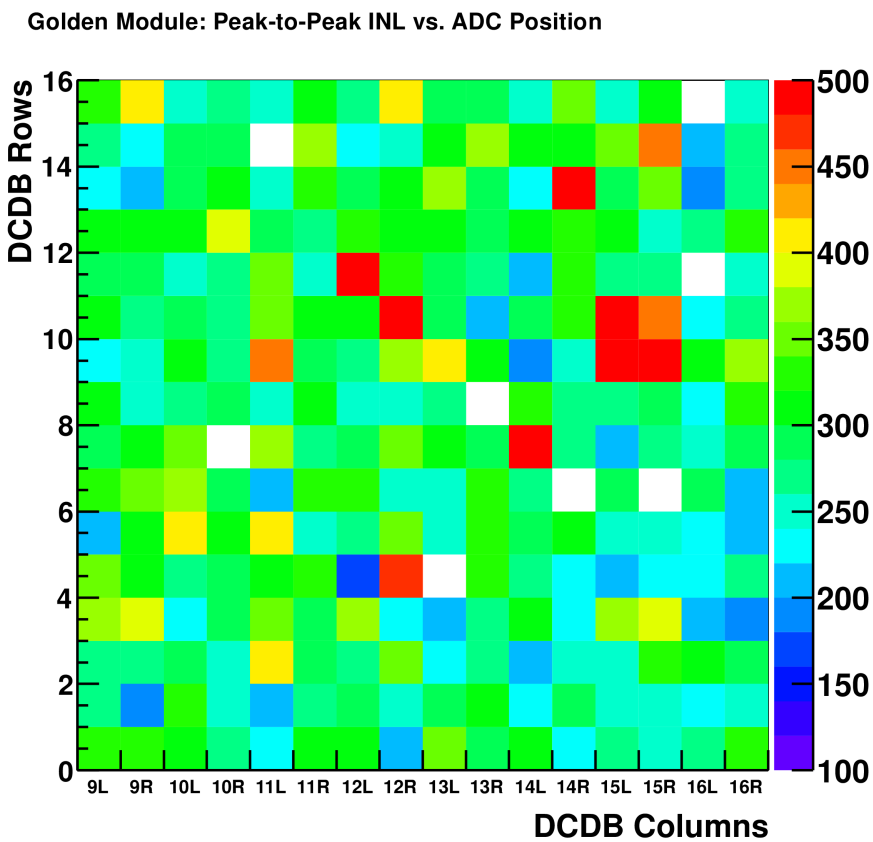
- Mean ADC noise is homogeneous all over the chip.
- Main source of noise is NOT the ADC but rather the TIA.

  → These numbers are based on 30k TIA feedback resistor.

  → Noise almost halves with 60k!

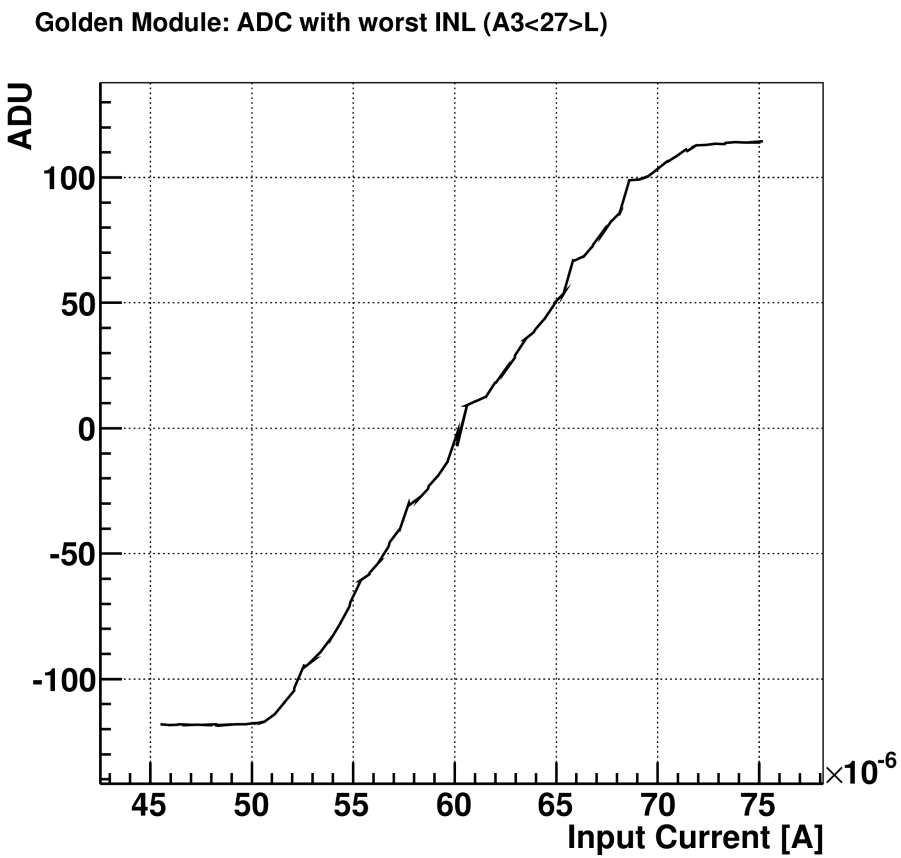
The DCDBv1's Current Performance (3/5)

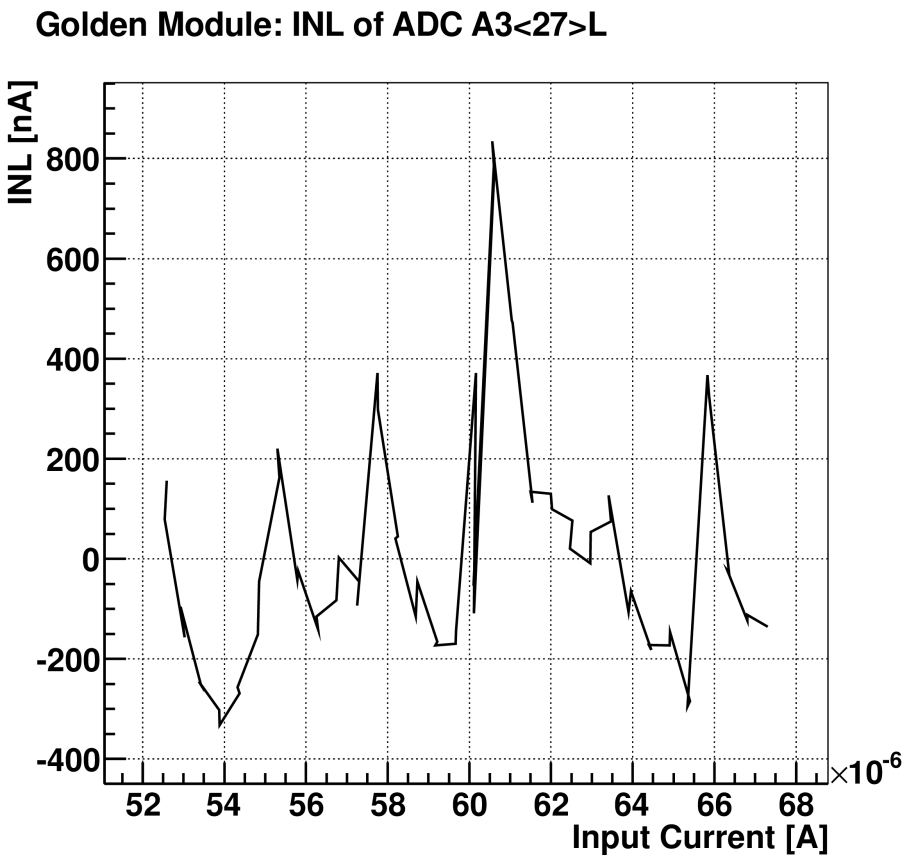




- Integral non-linearity (**peak-to-peak**) is roughly in the order of 2x noise.
- Homogeneous distribution over the chip.
- ~5 ADCs with fairly increased non-linearity. (→ next slide)

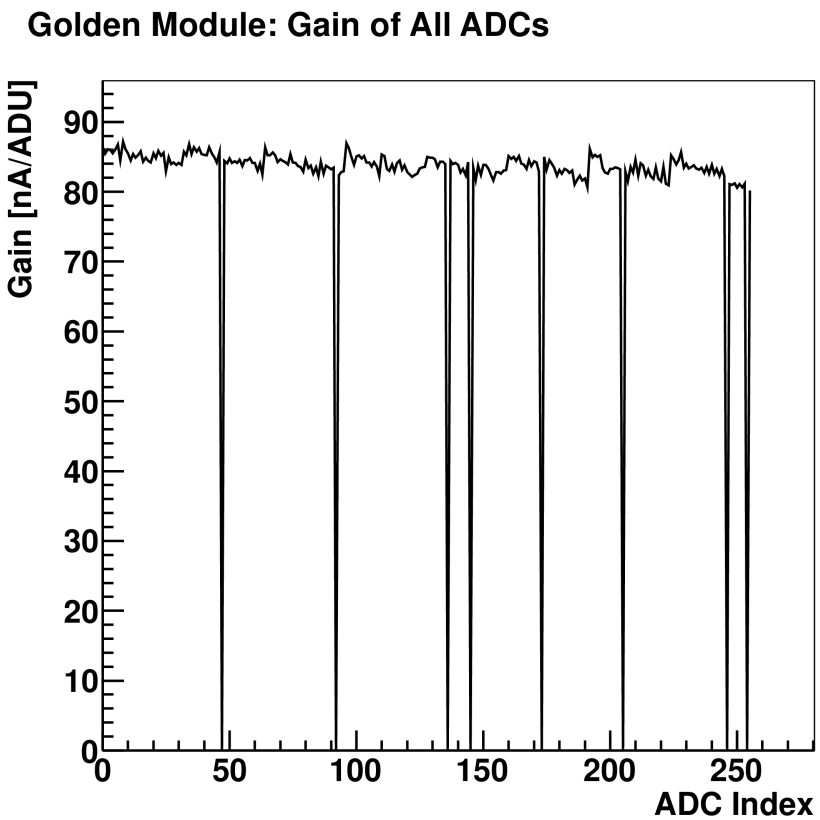
The DCDBv1's Current Performance (4/5)

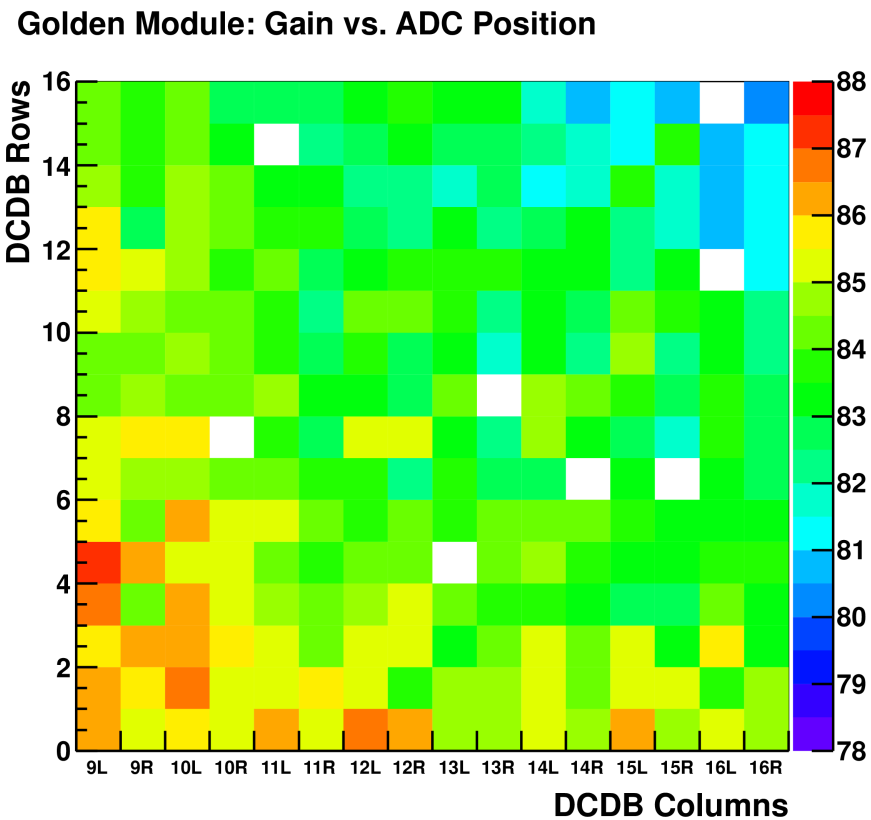




- Non-linearity is caused by steps in the ADC's transfer curve.
- Could be another yield issue.

The DCDBv1's Current Performance (5/5)



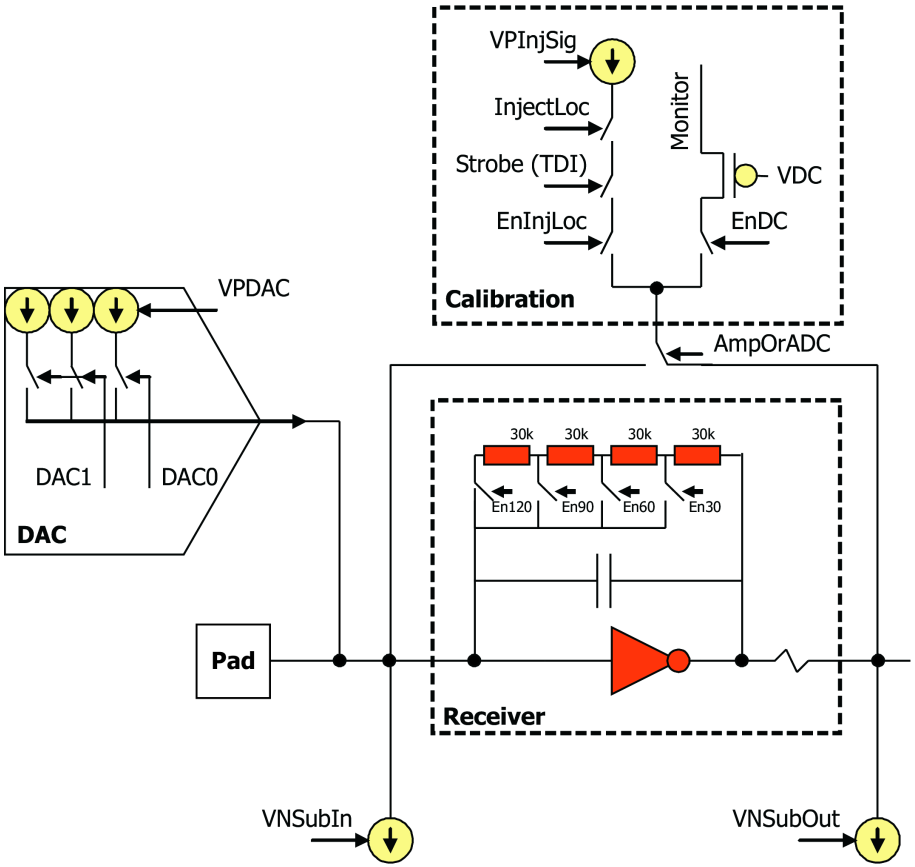


- Gain for applied bias settings and 30k TIA feedback resistor: ~ 84nA/ADU
- There are two clear but quantitatively small gradients!
  → Vertical gradient might be on-chip voltage drop.
  → The reason for the horizontal gradient is unknown. (Chip layout is symmetrical!)

Part II:

DCDB in DEPFET Readout Operation - Dynamic Offset Compensation

Dynamic Offset Compensation – Principle of Operation

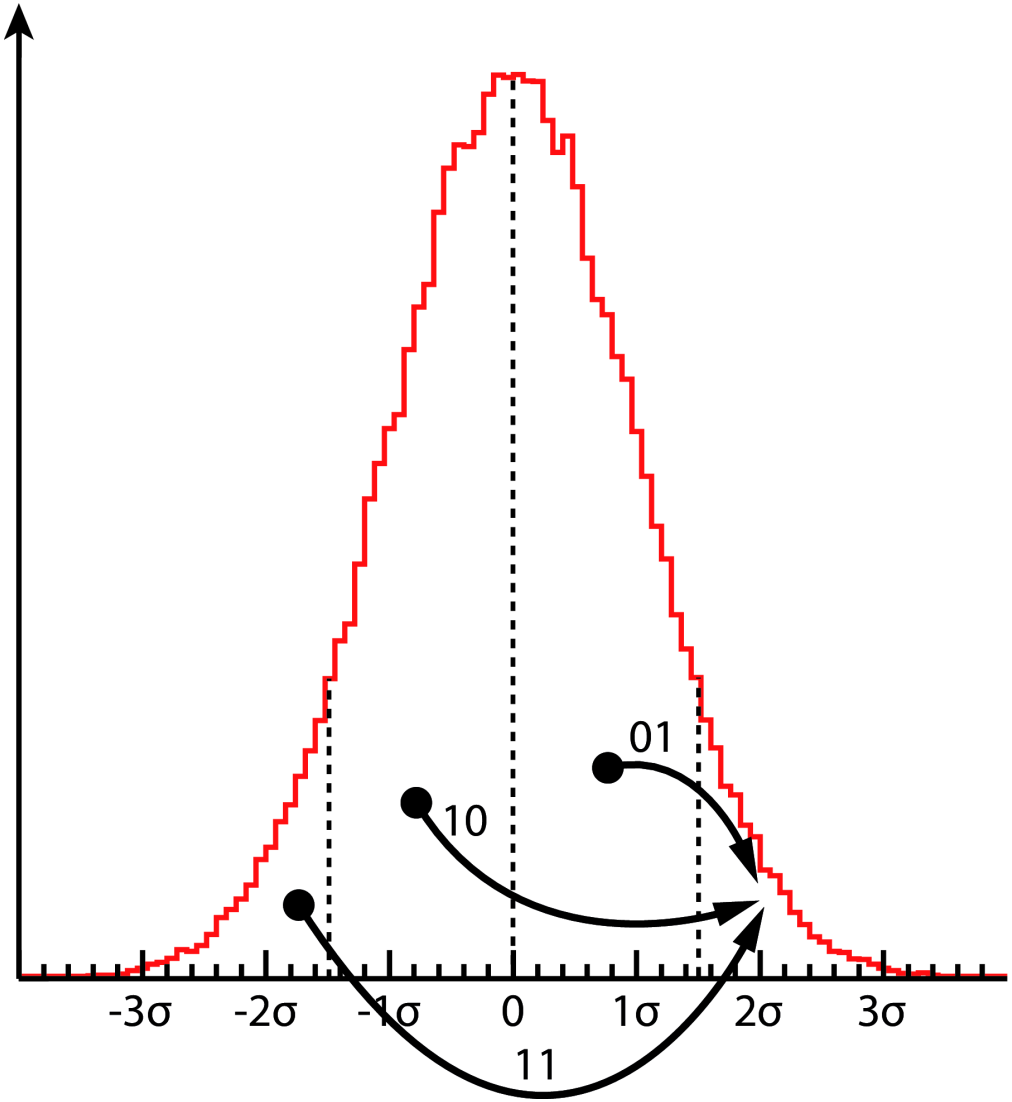


- **Current is dynamically added (!) to the input signal from the DEPFET.**
  - The lower the pixel's offset, the more current is added.

- **<u>Technical realization:</u>** There are three identical sources, each constantly delivering a unit of current. An additional 2bit factor defines the multiplication between 0x and 3x.

- **<u>Parameters to define:</u>**
  a) Unit current (per chip)
  b) Multiplication factor: 0-3 (per matrix pixel)

Expected Influence on Measurements (1/2)



Strategy:

"Bring the effective offsets of all pixels into the uppermost bin."

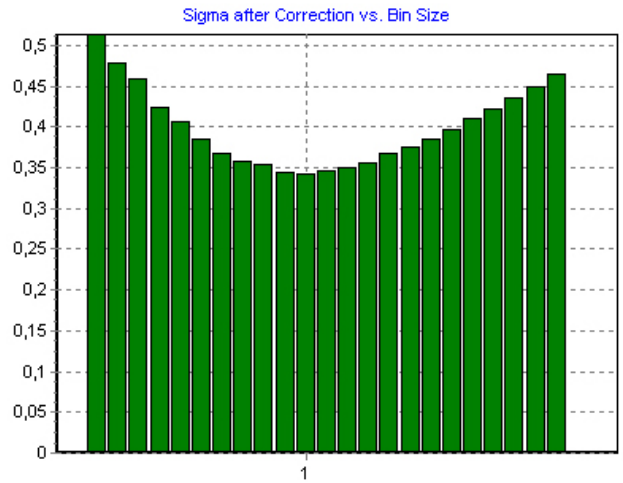
Question:

How to set the bins?

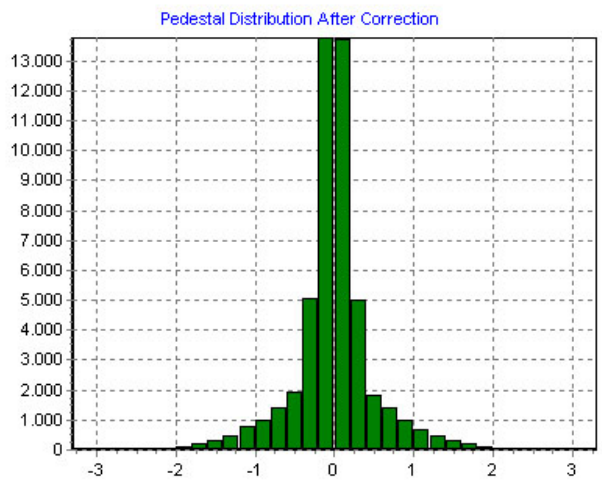
Expected Influence on Measurements (2/2)

Simulation:

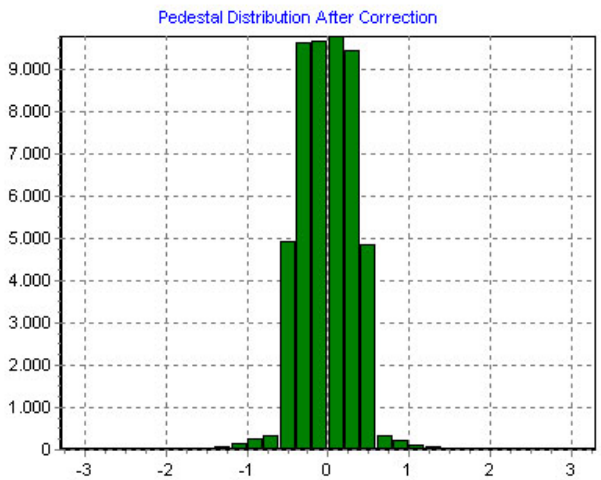
- Assuming uncorrected pedestal distribution with σ = 1
- Perform correction based on bin sizes between 0.5σ and 1.6σ
- Calculate σ of resulting corrected distribution



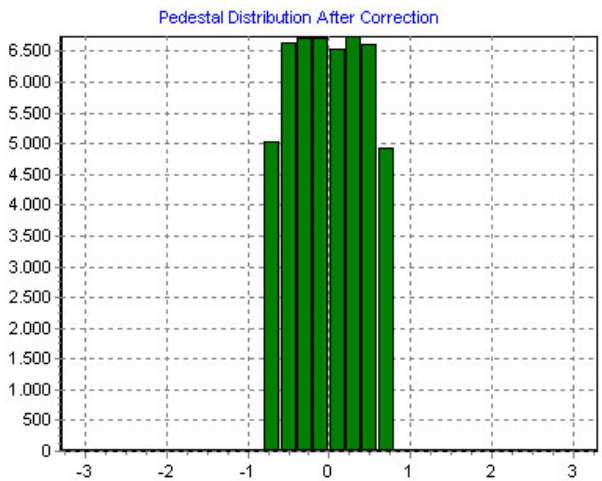
Bin: 0.5σ



Bin: 1.0σ



Bin 1.5σ



Corrected Distribution:

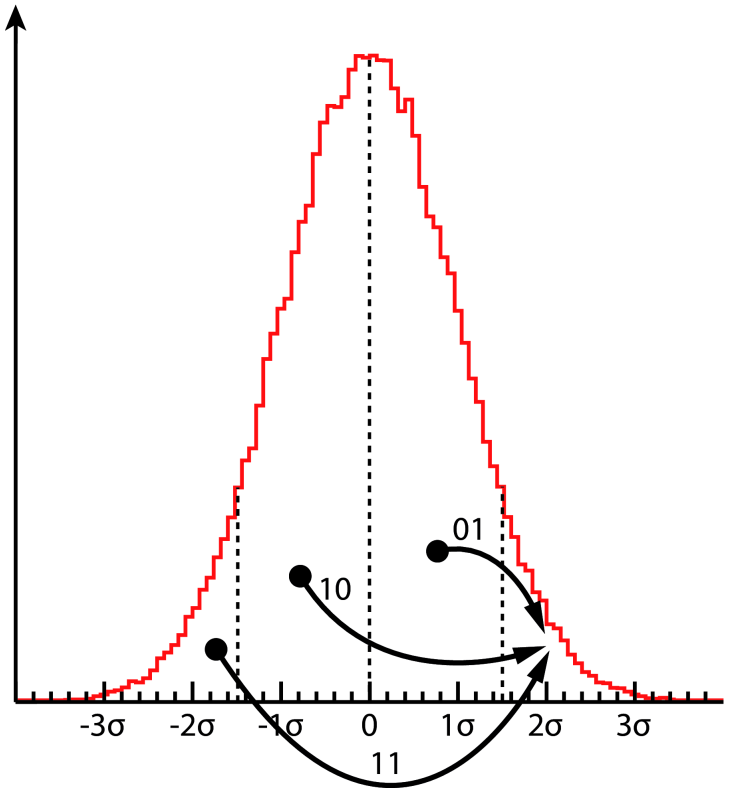
σ = 0.51 σ = 0.34 σ = 0.44

The Optimization Algorithm

I. Scan: Measure ADU for every combination of
   a) Matrix pixel
   b) Unit current
   c) Multiplication factor

   → Brute force algorithm

   → DC Measurements



II. Calculate σ for raw distribution (= correction off)

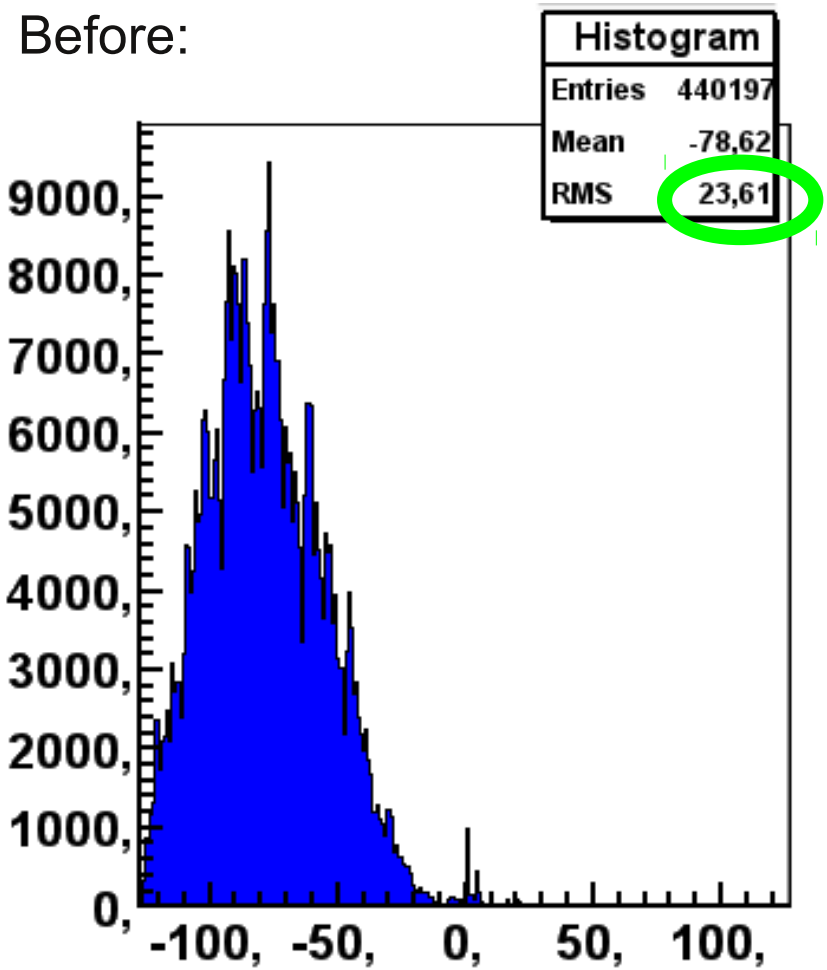
III. Define bin width

IV. Find best multiplication factor map for each unit current

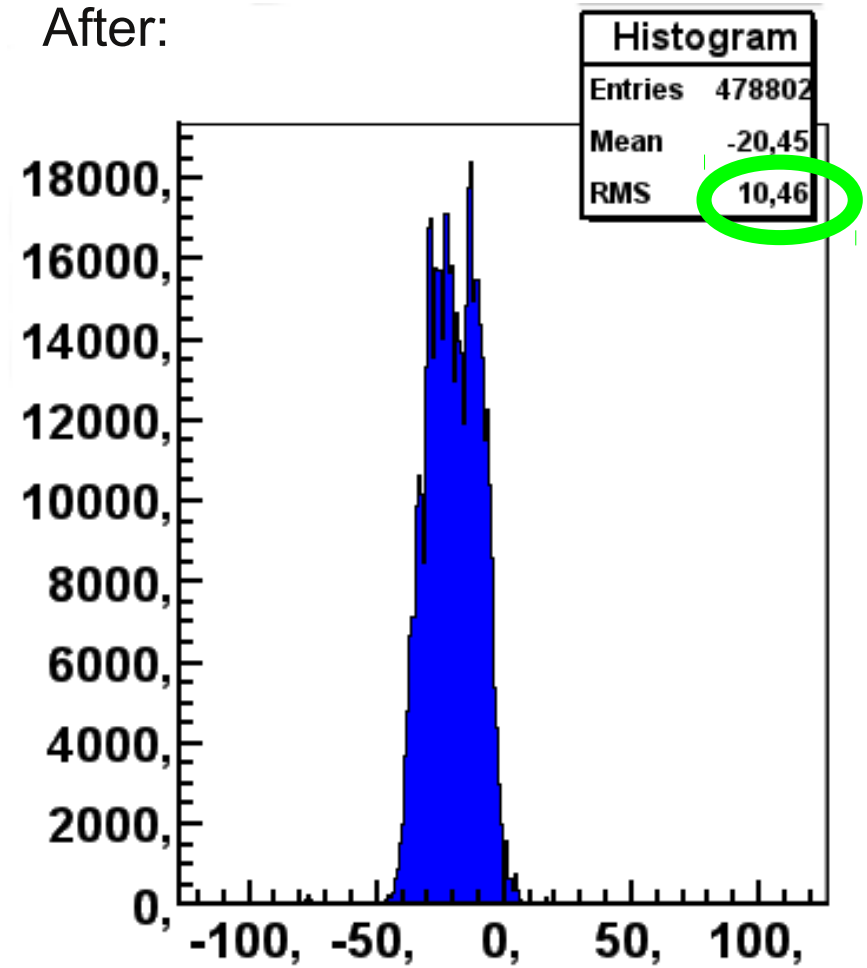
V. Pick unit current with lowest remaining σ

Dynamic Offset Compensation – The Results

Before:



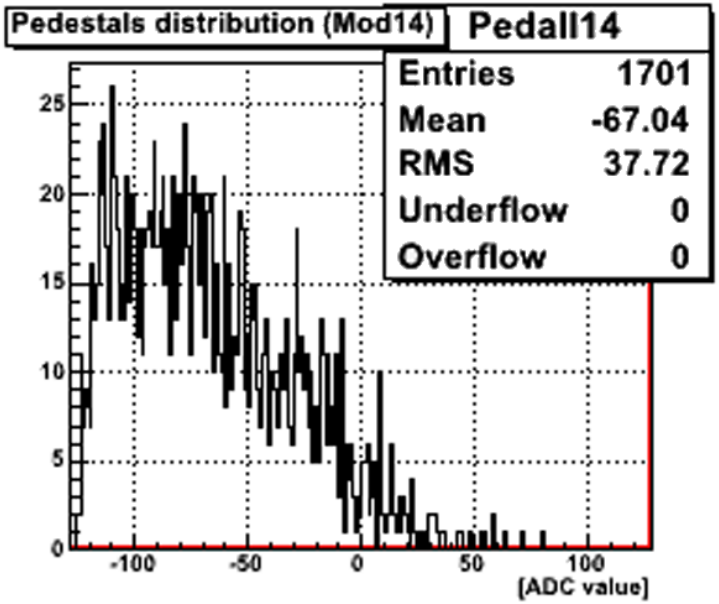
After:

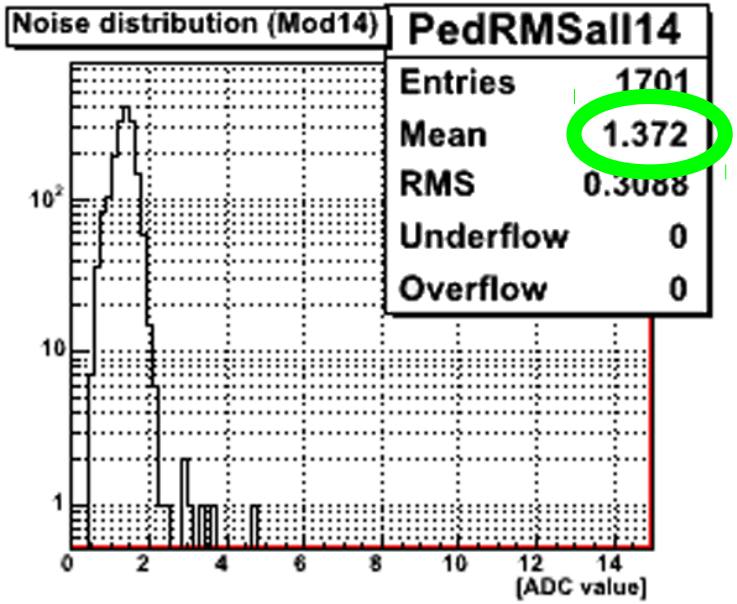


- Same settings and speed as for the DCDB characterization (100ns).
- Here: Bin width = 1.5σ → Expected reduction = 44%, Measured reduction = 44.3%
- → **Indirect prove of TIAs dynamic performance!**

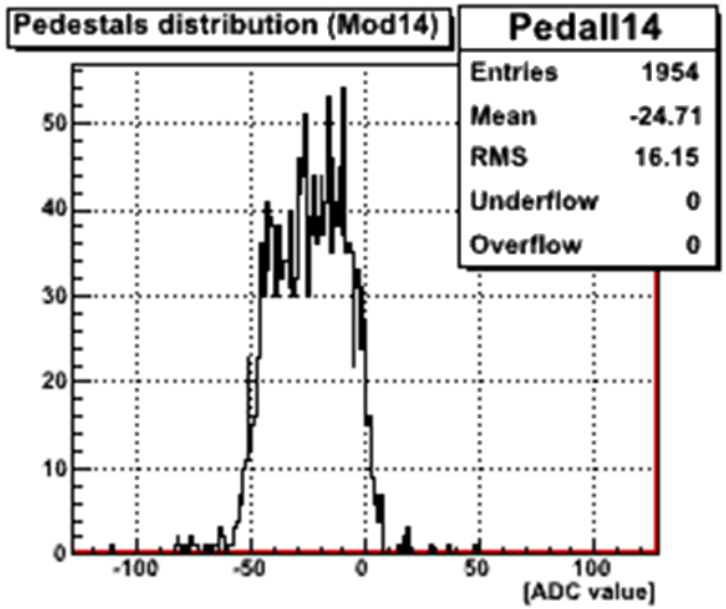
What About the Noise Introduced by Dynamic Offset Compensation?

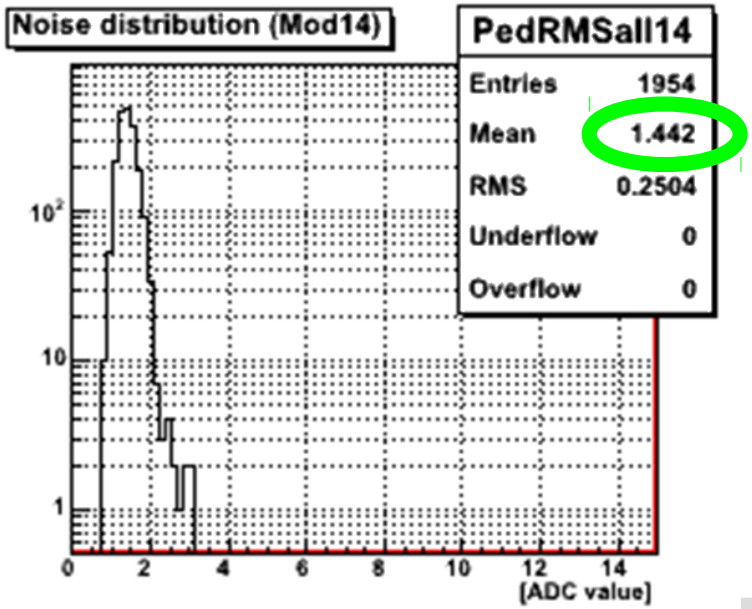
Before:





After:





Part III:
DCDB-TC Measurement Results

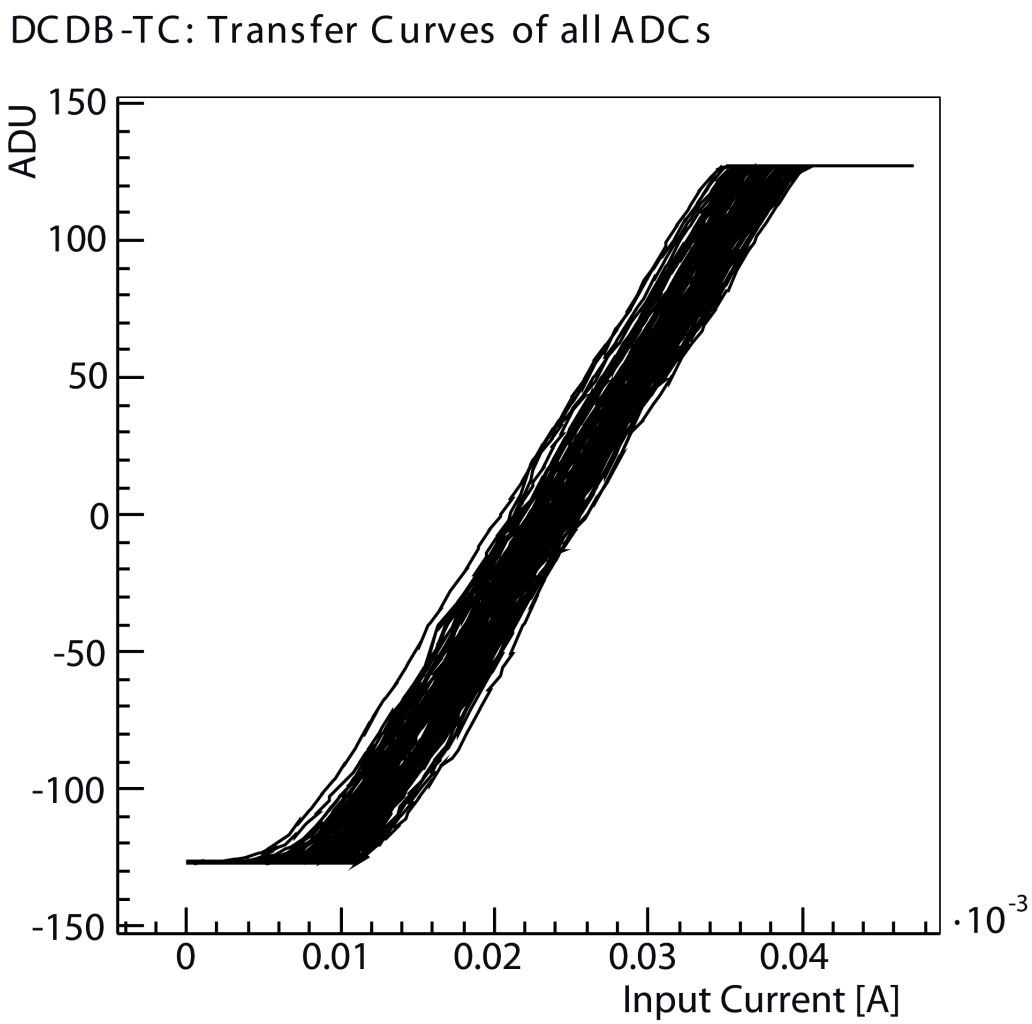
DCDB-TC: Fact Sheet

- Why did we submit a DCDB test chip at all?
  → Because we thought the DCDBv1 would have serious issues...

- Major changes / improvements in DCDB-TC
  - 32 Channels only, standard technology without bumps
    → smaller & cheaper, faster production
  - Delay bias generator was made stronger
  - Separate bulk potential for switch transistors
  - *Modified ADC switches: Low-Vt transistors used*
  - Input subtraction source doubled (VNSubIn)
  - Internal voltage drops measurable

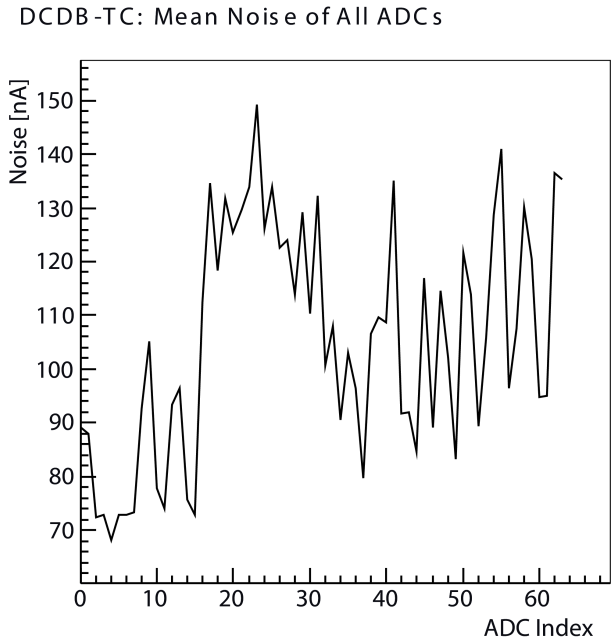
- Production details:
  - Developed & submitted in October 2010
  - Expected delivery ~Jan 2011, the chip arrived end of Feb 2011!
    → Only very few days of testing before DCDBv2 submission!

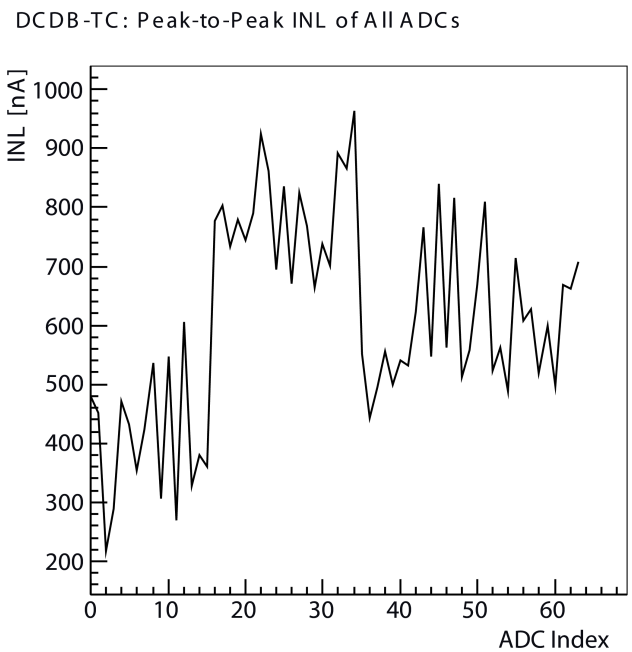
DCDB-TC Measurement Results (1/3)



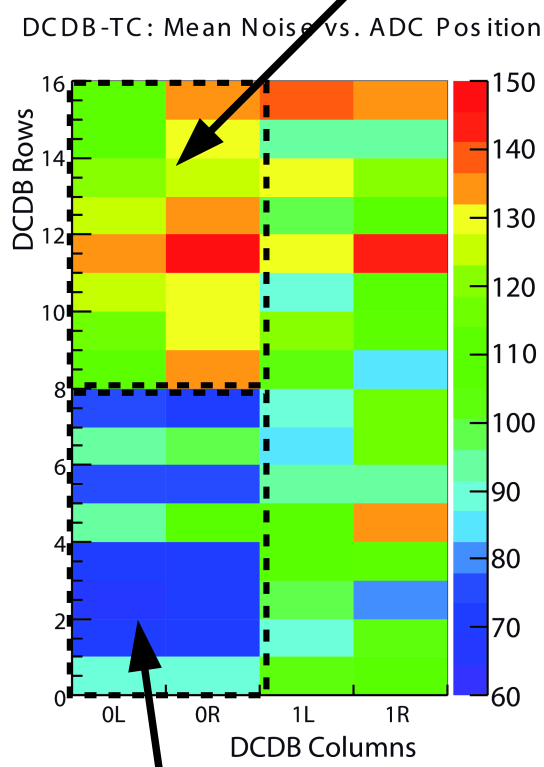
- Operation speed: 400MHz → **80ns** sampling rate
- Internal signal source, calibrated via SMU
- Each point is the mean of 100 samples
- Vertical dispersion: 53 ADUs

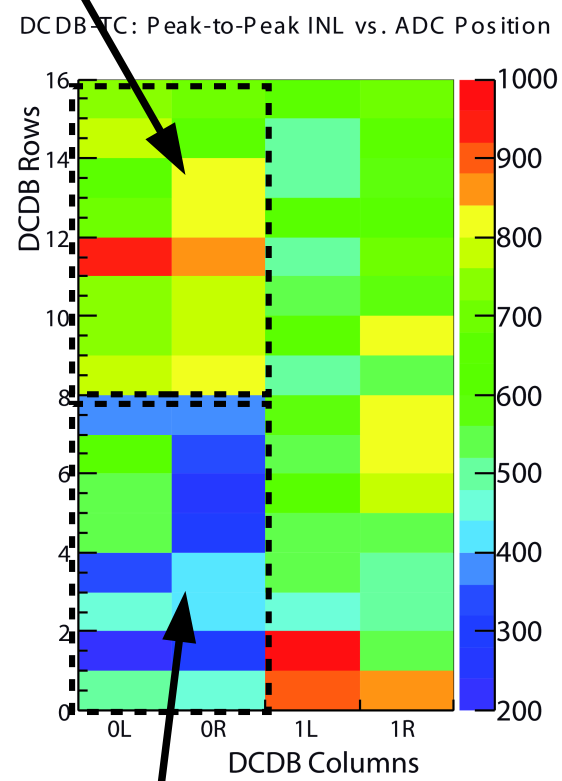
DCDB-TC Measurement Results (2/3)





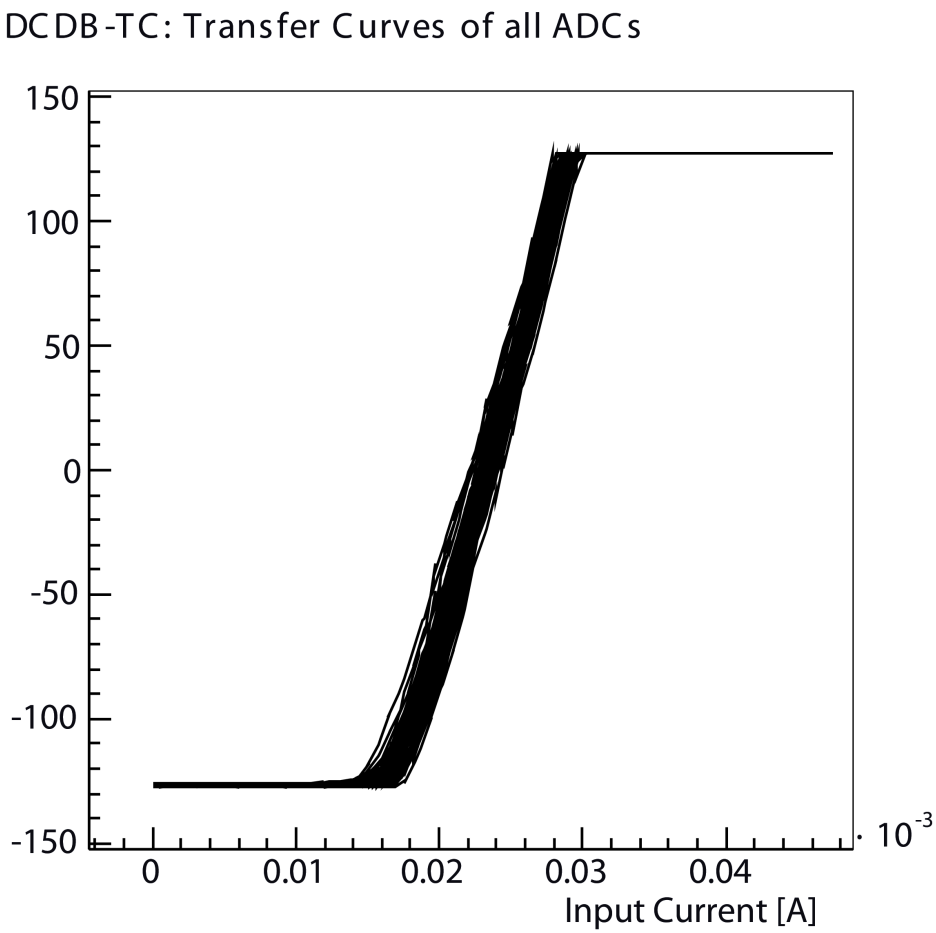
Like DCDBv1

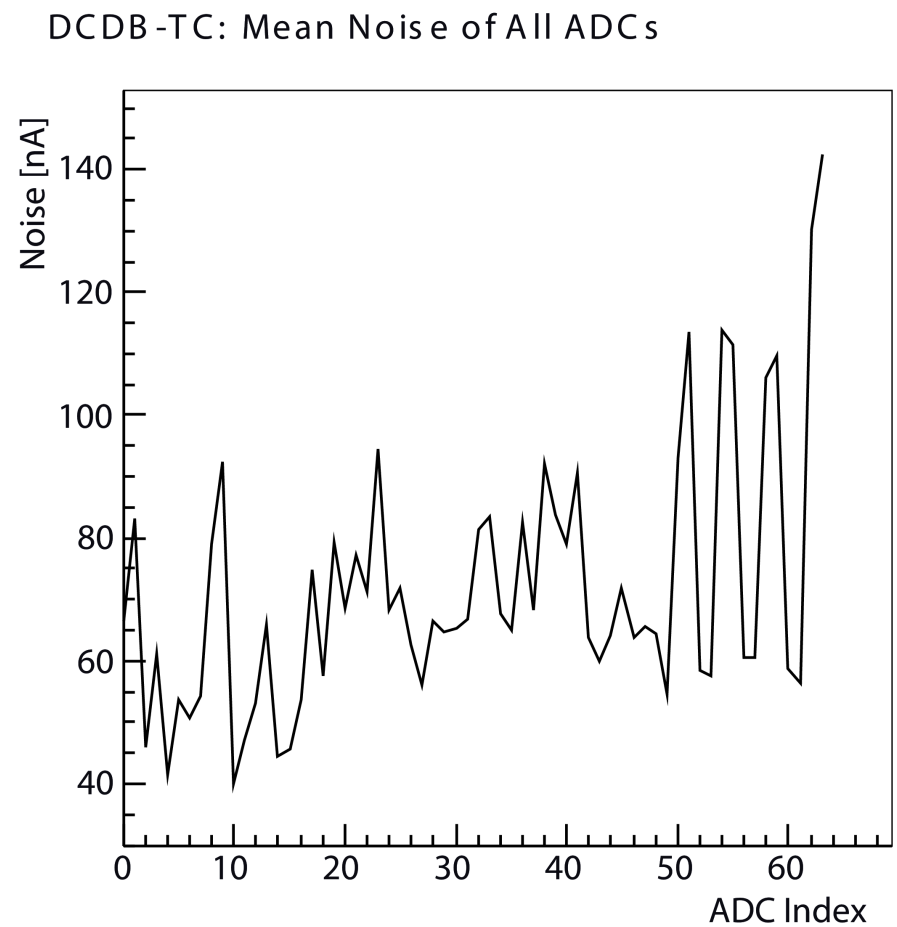




This implementation is used for DCDBv2

DCDB-TC Measurement Results (3/3)





Here: 60kΩ TIA feedback resistor

→ Smaller dynamic range but better noise performance.

Summary

Summary

- DCDB-TC measurements
  - Improvements in noise and linearity
  - DCDBv2 (next full size chip) benefits from this achievement.

- Dynamic Offset Compensation
  - Characterization algorithm exists
  - Measured reduction fits perfectly to the expectations
  - Noise performance is not influenced

- Latest DCDBv1 performance measurements @ lowest TIA amplification:
  - 100ns sampling rate
  - ~115nA mean noise
  - ~270nA non-linearity (peak-to-peak!)
  - ~22uA dynamic range

Good News!!

<u>No magic or fundamental fixes!</u>
<u>The DCDBv1 has been working ever since!</u>

Thank you!