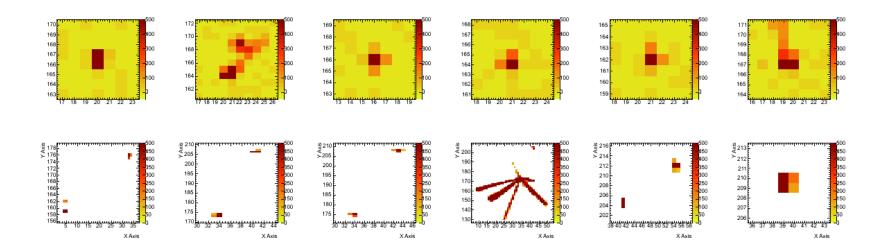
DEPFET TB 2010/2011



DEPFET TB 2010/2011

7th DEPFET workshop, Ringberg castle – May 10th 2011 -

Marcel Vos, IFIC Valencia

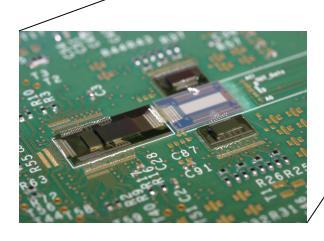




Some history: TB2010

DCDB-based PXD5 DUT (on hybrid 4.1)

- (Nearly) full-speed read out row rate/nominal ~ 3, compared to several orders of magnitude with previous system)
- Relevant pedestals, common mode but custom power supplies, cables, no dynamic offset correction



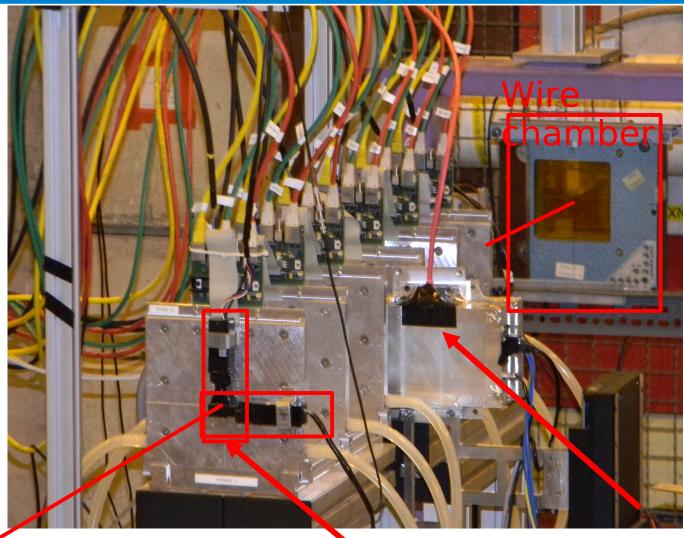






TB2010, our beam period: 15-21 November Last slot of the season, after SiLC, EUDET telescope requested

TB setup



SPS H6 beam

Scintillator triggers

DEPFET DUT

line

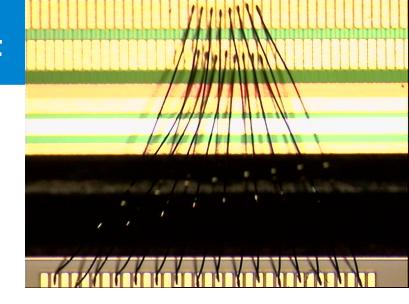
TB2010: with some hindsight

SwitcherB operated successfully during TB2010,

- after two SwitcherB chips died on first hybrid
- 4.1 (one after brief period with life signs)

Bonding errors lead to inefficient and undefined sequence

- data not usable



DCD Pedestal spread over 2/3 of dynamic range

- subtraction DACs not yet available... will be there for next TB!!!
- Source for offset current subtraction too weak → gate on voltage must be too low.

DCD pedestal variations

- Variations with time of a few counts observed due to temperature drift
- otherwise stable to within

DCD noise:

- 0.8 LSB noise before TB and in H6 when run with same parameters in TB DCD ADC response:
- instabilities in fraction of ADCs confirmed by more detailed studies

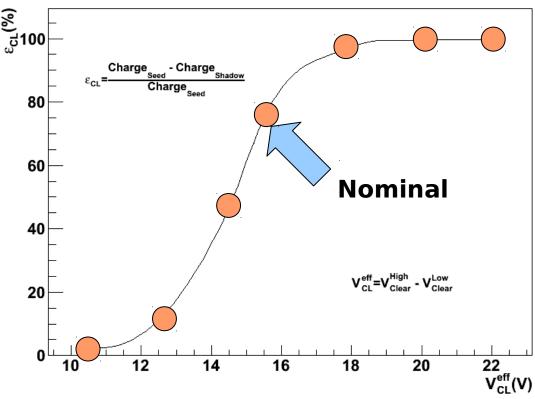
Jochen's talk yesterday: this module is now behaving nicely. I wish we had a few more!



TB2010

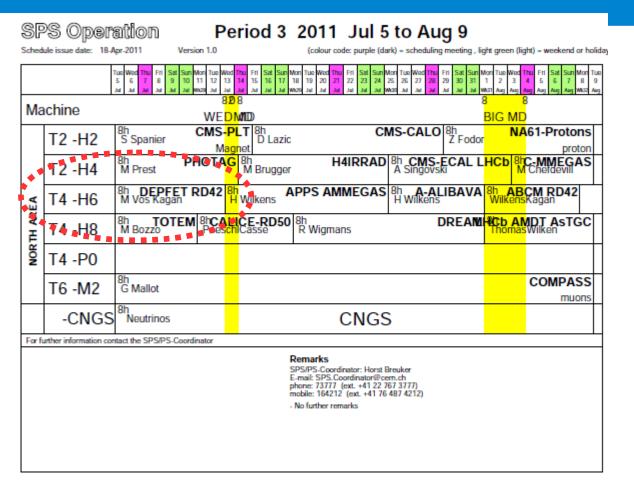
Trailing frames – a new feature of the DAQ developed by Sergey and team for TB2010 – allow unambiguous measurement of signal remaining (or not) after applying clear voltage. Source data taken by Christian Koffmane at MPI after repair.







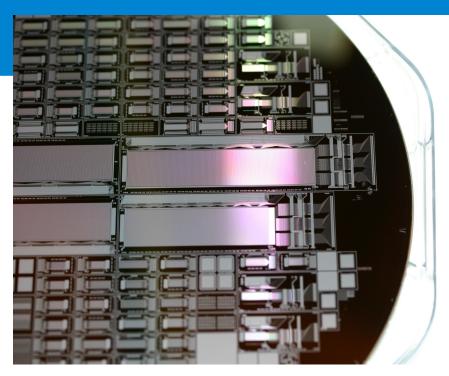








TB2011



DCDB module

- full-speed or at least high speed read-out
- live with V1 features (ADC issues, offset correction, see next slide).

PXD6 module

- mm² ILC design → first thin DEPFET, comparison with previous results
- mm² Belle-II design → resolution, digitizer validation
- full-length ladder → final demonstrator



DUTs - continued

PXD5/DCDB module (golden module)

- was in TB2010
- from Jochen's talk, the PXD5 module we had in 2010 looks ready for a TB!
- This module has a Switcher problem that prevents it from running full-speed

PXD6/DCDB module (platinum module)

- seems perfect

- - -

- Any DCDBv1 module has limited offset correction current and will have to be run with a GATE ON voltage that is sub-optimal $\rightarrow g_\alpha$ will be too low
- Test chip hard to use in TB. DCDBv2 expected in October. Is reading out with CURO going to be any easier than reading out DCDB? Or possible at all?





Power supplies



Power supplies 2010:

- Semi-automated start-up sequence
- Remote control & monitoring

Power supplies 2011:

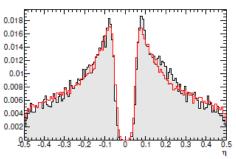
- prototype system available and debugged? Question in this direction from Stefan Rummel.

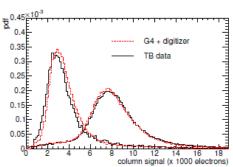




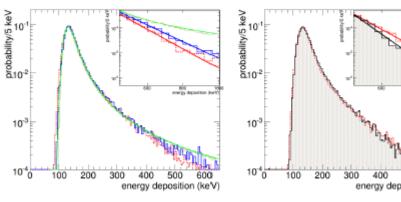
Digitizer validation

Charge sharing



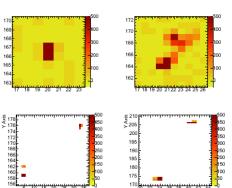


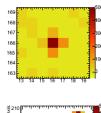
FLUKA/GEANT4/Bichsel

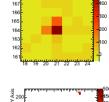


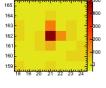
Impact of digitization

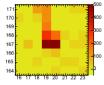
A lot of material exists on ILC-type design allows for very precise characterization of Si-based detector response. Must validate the digitizer used for physics studies. Repeat with BASF?



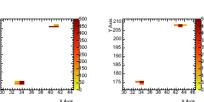


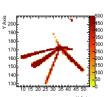


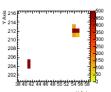


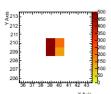












Nuclear interactions

Conclusions

TB2010: development of new tools, debugging of new system

- Several developments still ongoing: DCDB yield, two-bit DAC...
- TB data now abandoned, but TB-like analysis of source data after DUT repair provides interesting results.

TB2011: demonstrator of thin Belle-II design DEPFET sensor with high-speed read-out

- Not just (or even primarily) to convince the outside world we are able to build the best detector ever; this is an important test of the full system performance. Important feedback we should have as early ASAP.
- Not to be done in a rush, with something that's not carefully characterized. But, we want to be able to raise an alarm signal before submitting new sensor design. Stick to July or delay until September/October?

More issues:

Power supplies: when?

Digitizer validation: use BASF set-up to reproduce old results

