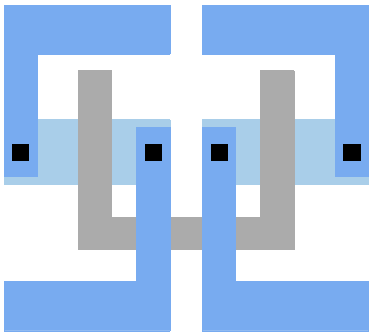
UNIVERSITÄT
HEIDELBERG

Preliminary DCDB Updates



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DEPFET Collaboration

EVO-Meeting

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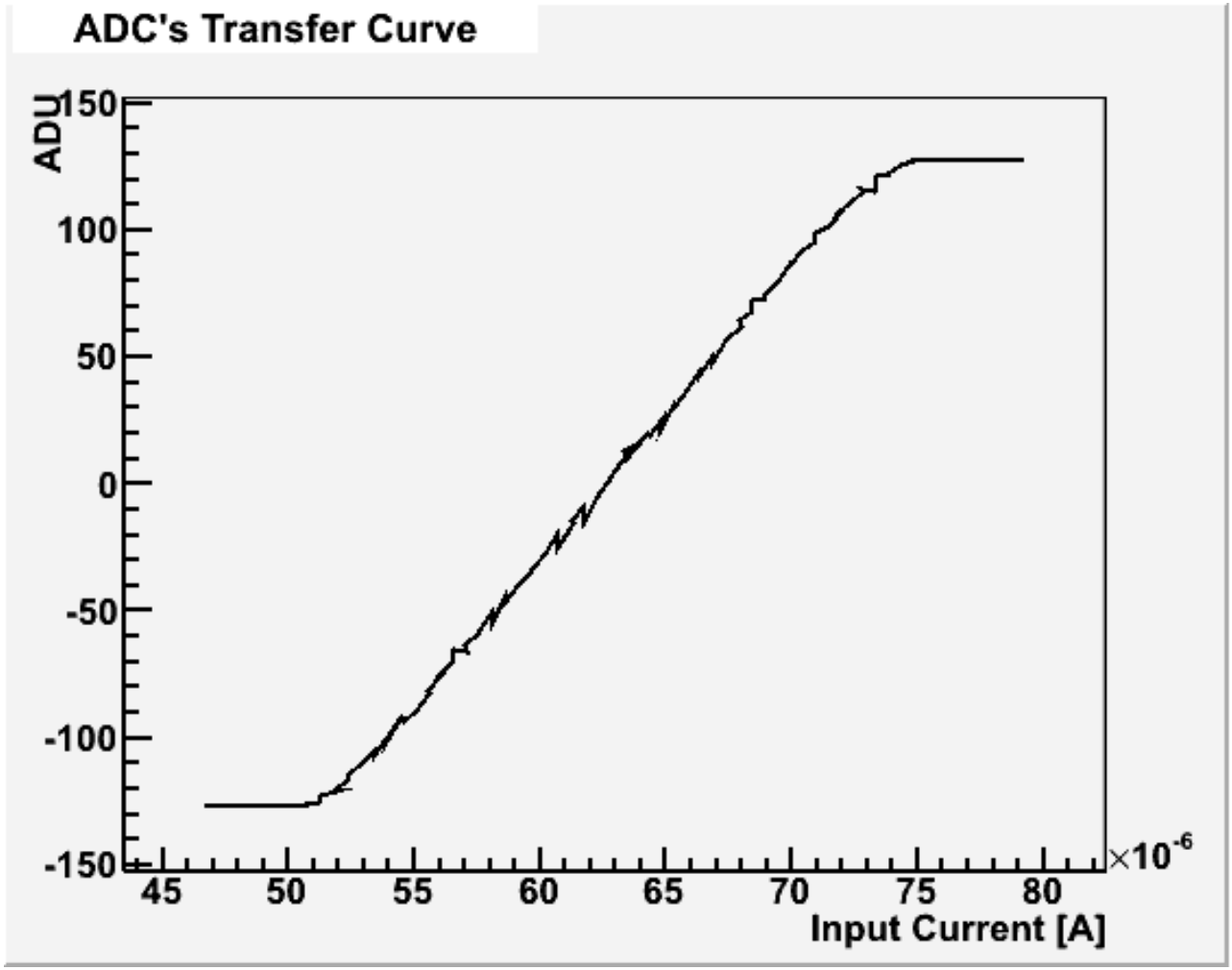
Major Achievements During Last Weeks

- DCDB**v1** is running at target speed: 320MHz = 100ns sampling rate
- With PXD5 matrix attached (TB2010-Module)
  → Maximum input offset subtraction (VNSubIn = 127)
- Noise and non-linearity improved significantly!
- Offset DAC is working dynamically

→ See the plots on the following slides!

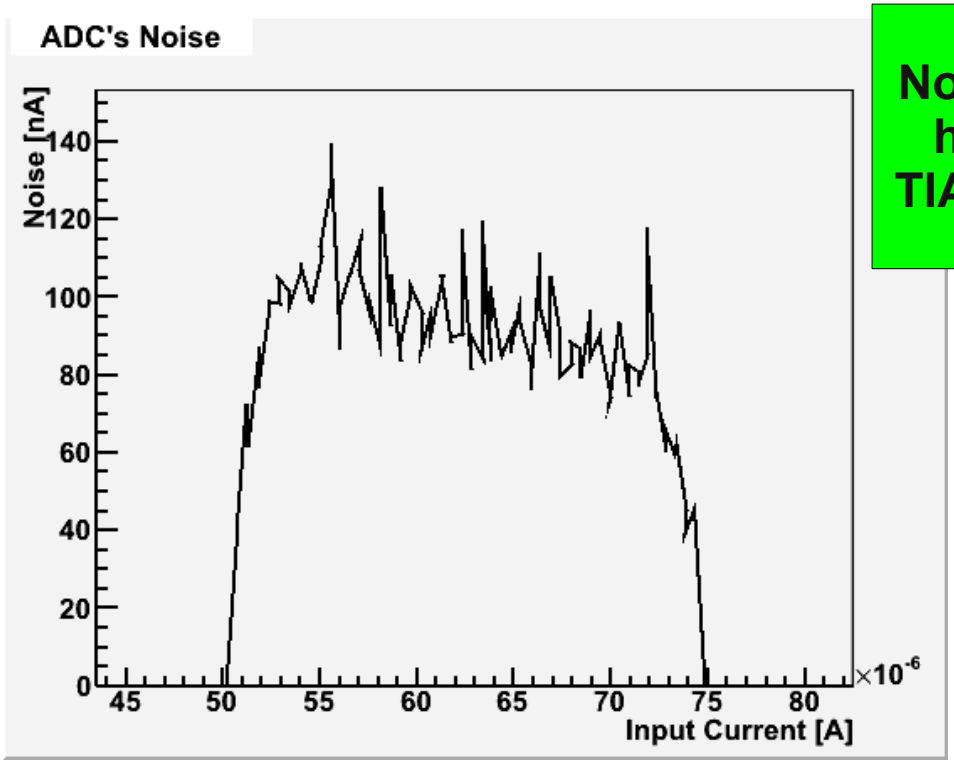
Current DCDB Performance



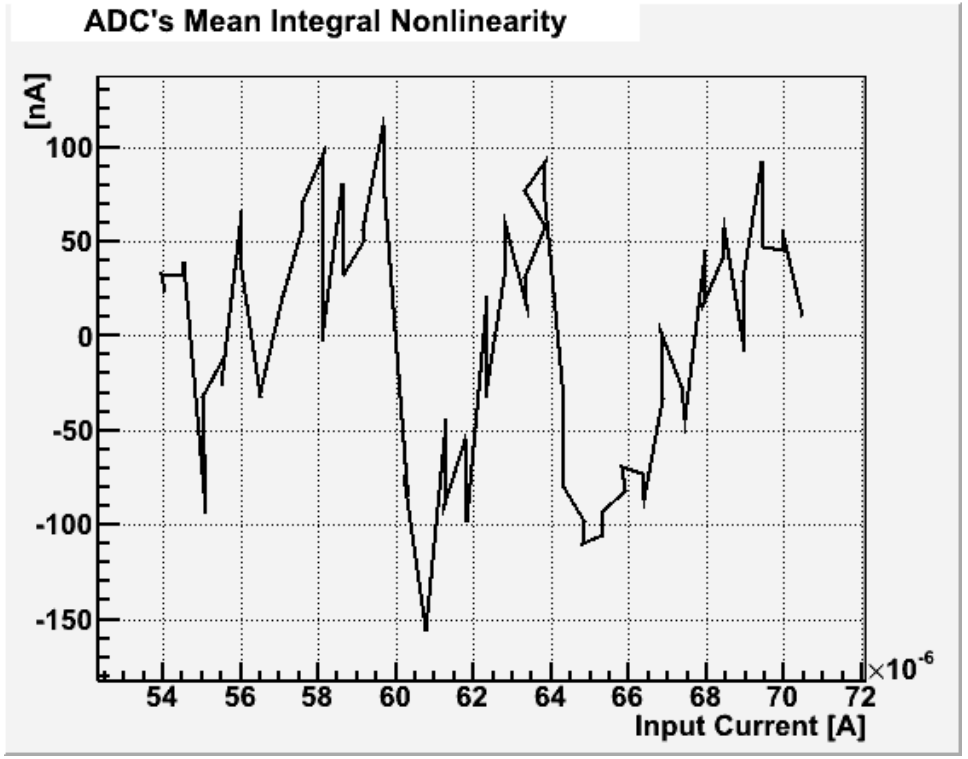
Facts:

- Single sample per point.
- 30kΩ TIA feedback res
- Sweep via internal source
- ADC: column 5, pixel 0, left

Current DCDB Performance

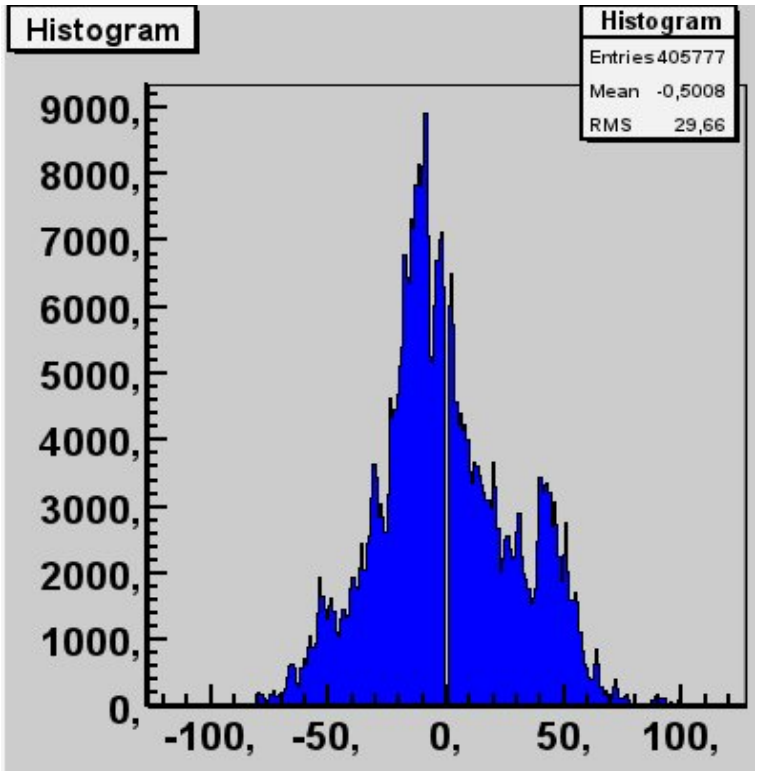


Noise can be almost halved with 60kΩ TIA feedback resistor

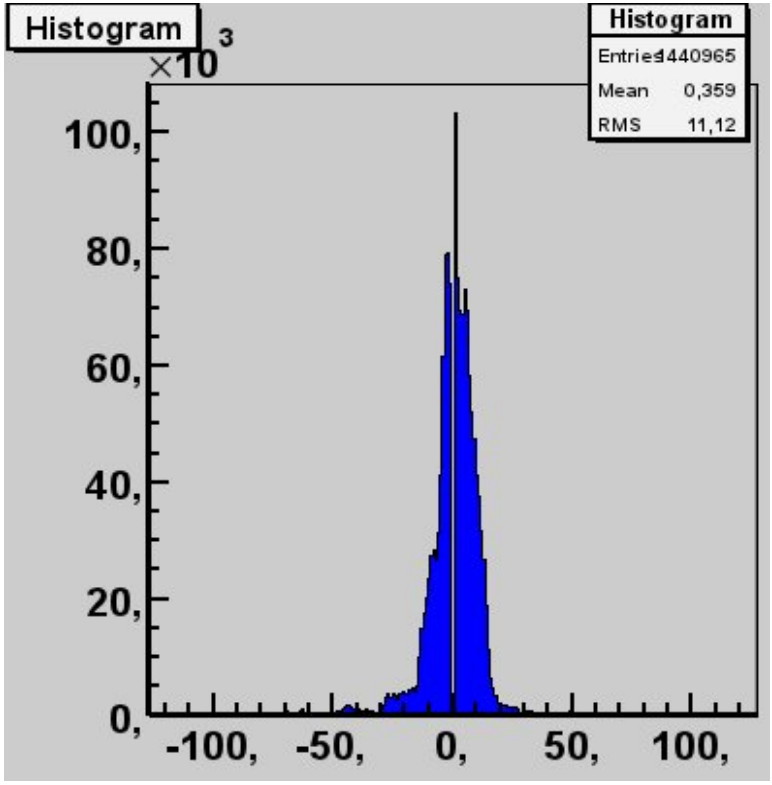


Peak-to-Peak INL ~ 250nA

Minimizing the Pedestal Dispersion



Pedestal Compensation applied



RMS of pedestal dispersion is reduced from ~30 to ~11 ADU → ~37%

Thank you!