Development of High Speed Sampling ASIC Analog Memory Cell for Imaging Atmospheric Cherenkov Telescope

IMPRS workshop
2011/5/2 in München

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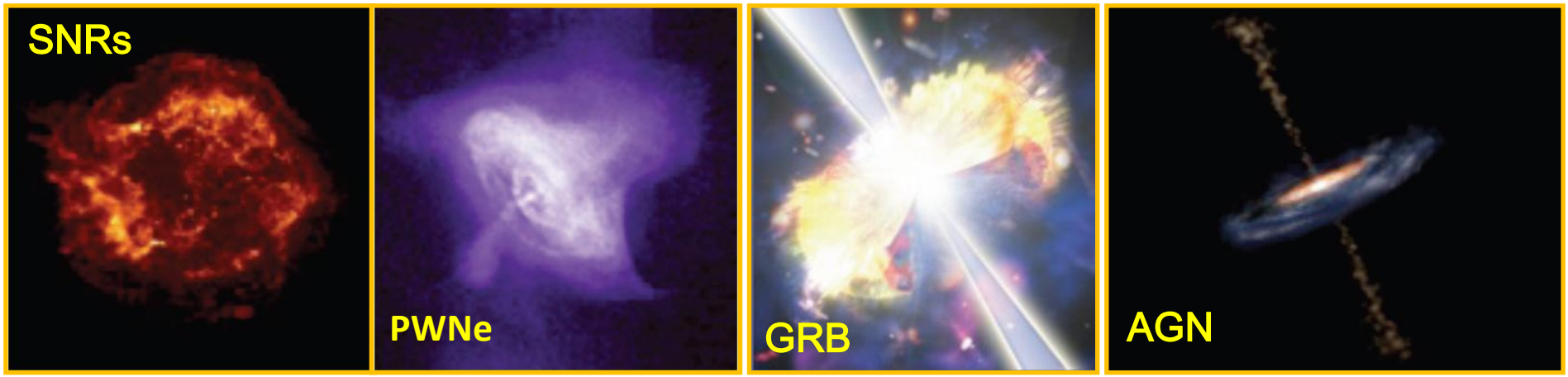
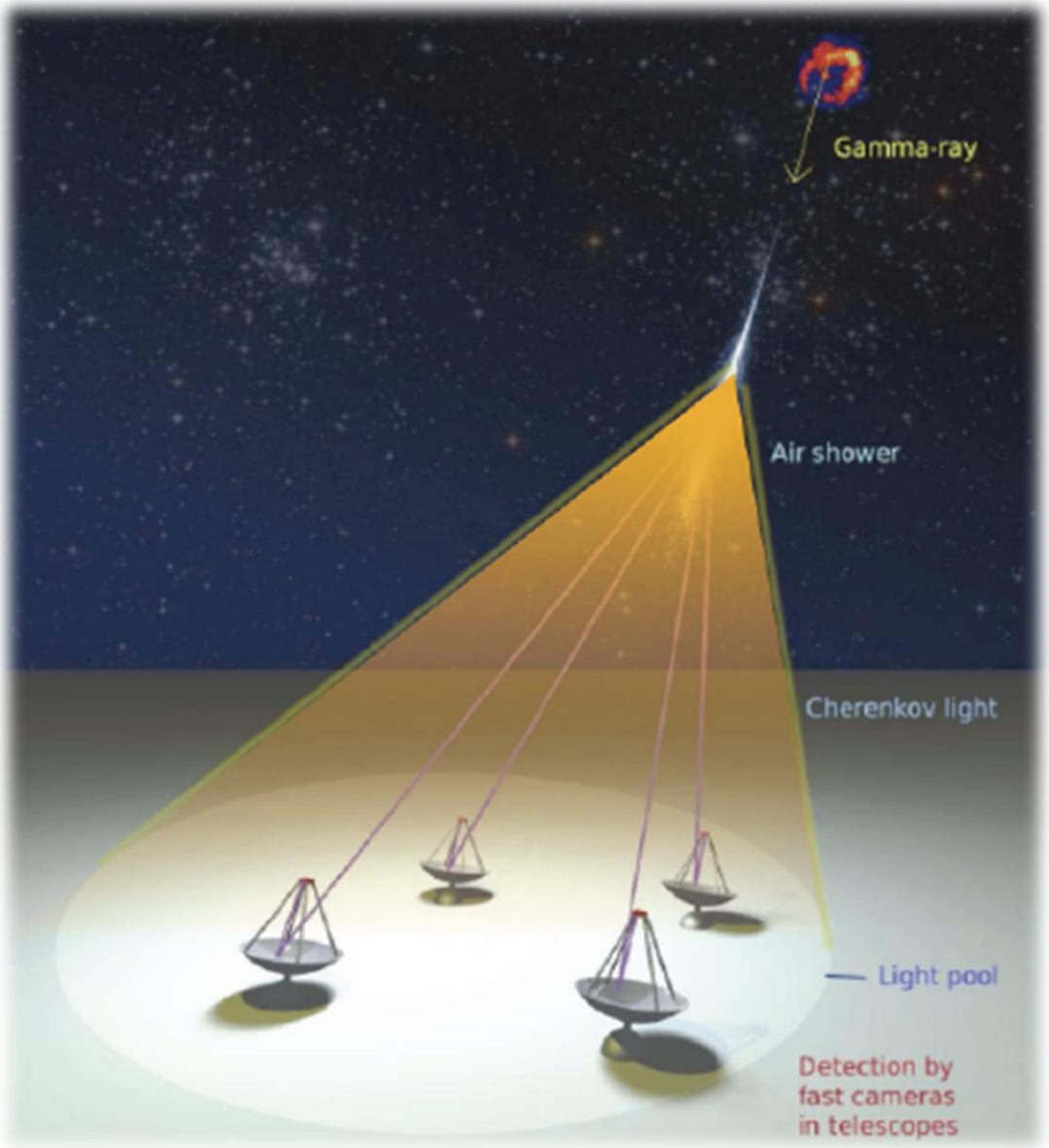
Very high energy gamma ray astronomy

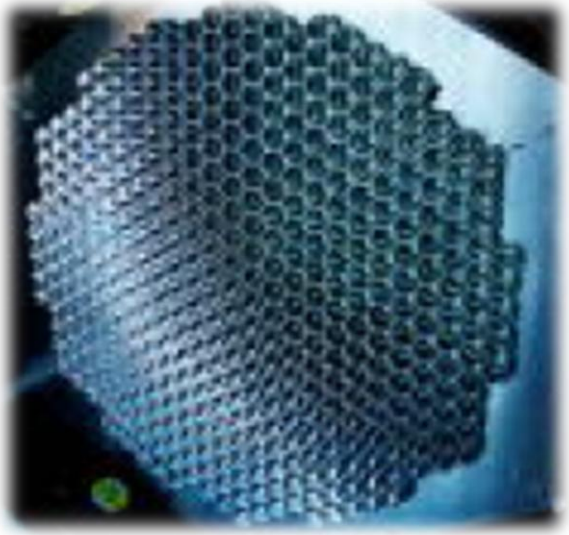
- A hundred of TeV gamma ray sources have been detected by Imaging Atmospheric Cherenkov Telescopes
  for example, PWNe, GC /, AGN , star burst galaxies and UnIDs



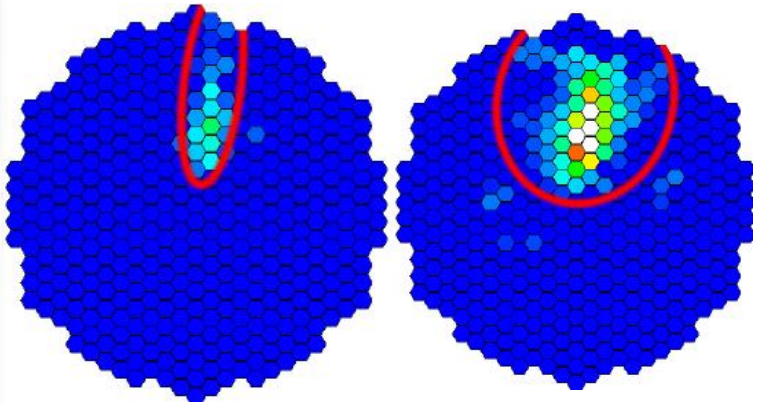
- These lead to understanding radiation mechanisms
- In particular, low energy (<50GeV) observations enable us to study the early universe

IACT observation system





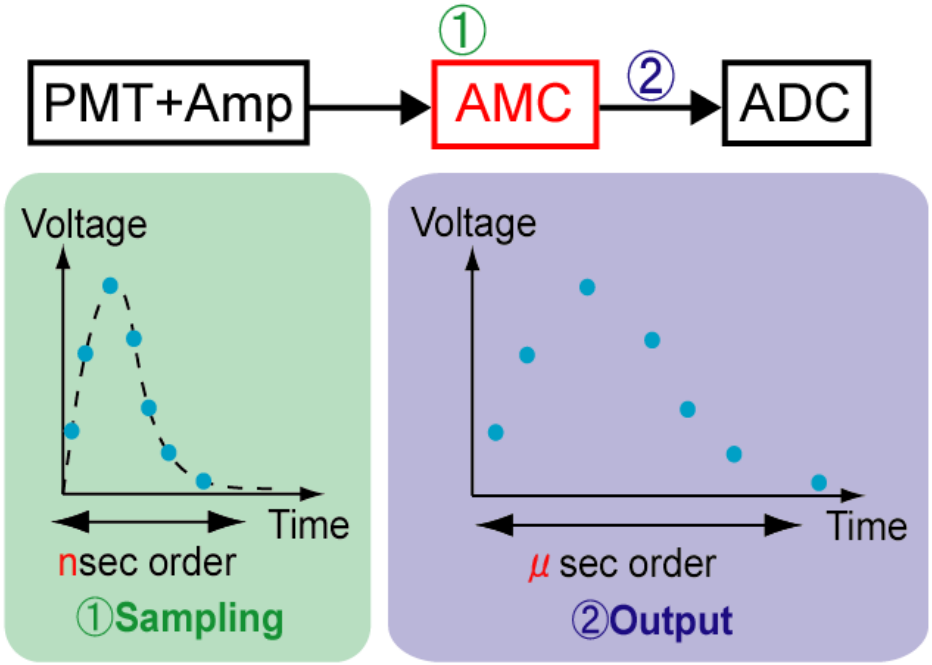
PMT camera



Event of gamma ray

Event of hadron

Analog Memory Cell(AMC)



①Samples wave form with fast speed 1GHz and high precision over 10bits

②Reads out sampled data with slowly <50MHz

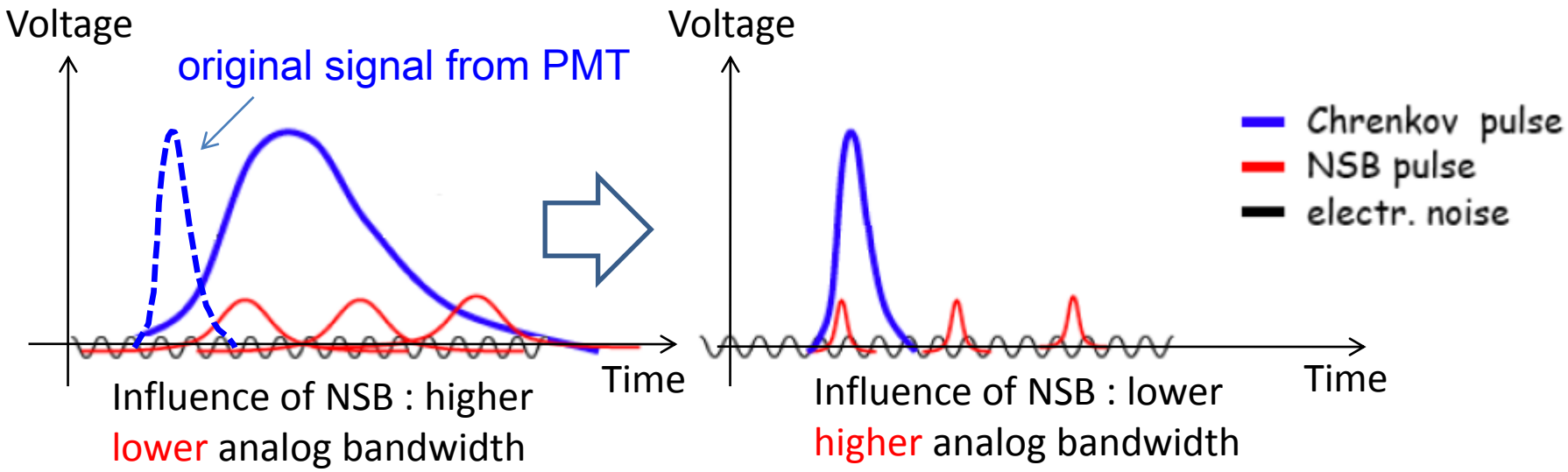
- Slower ADC can digitize the readout data

Why did we select not FADC but AMC system?

- better precision(>10bits)
- lower power consumption (order of mW)

  (cf: power consumption of FADC is a few W)
- compact (locate AMC with PMT)

Signal to noise ratio



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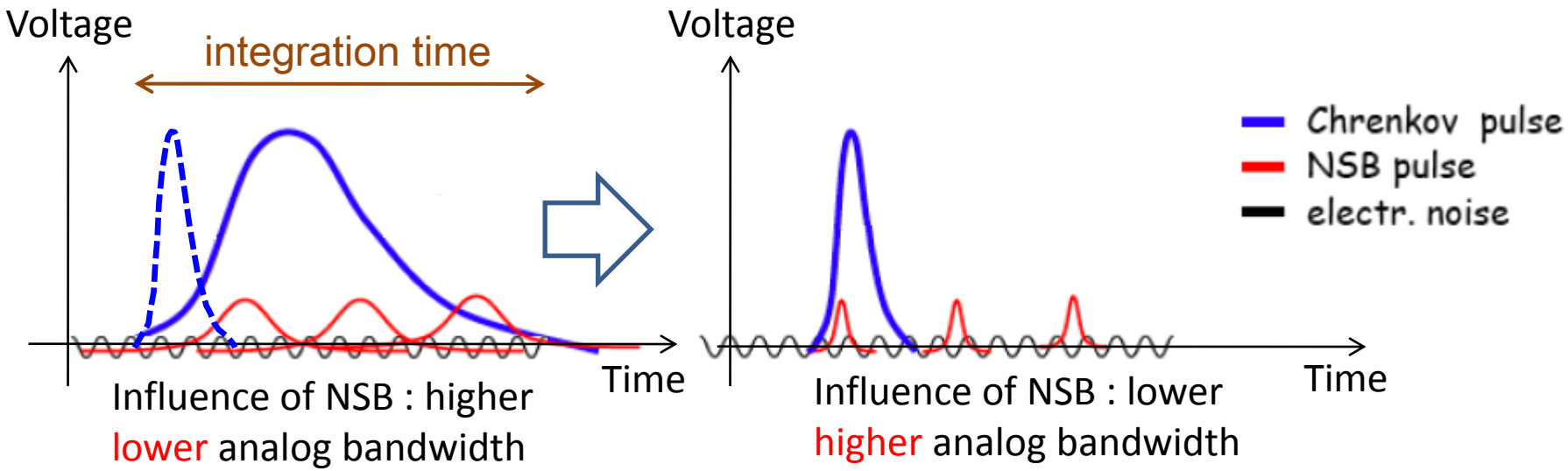

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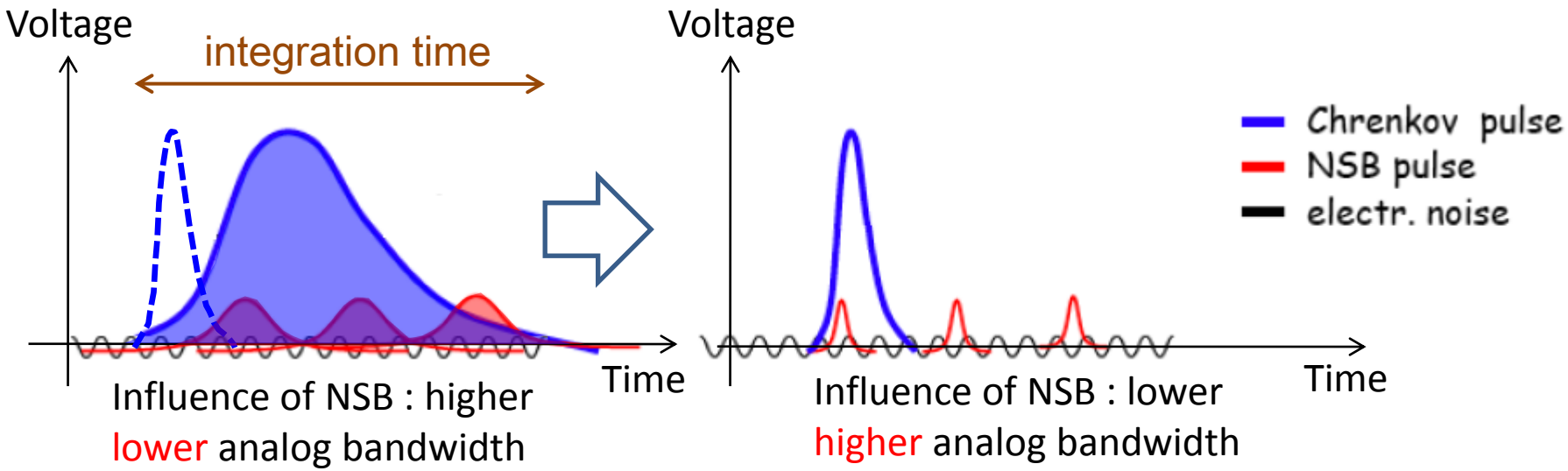

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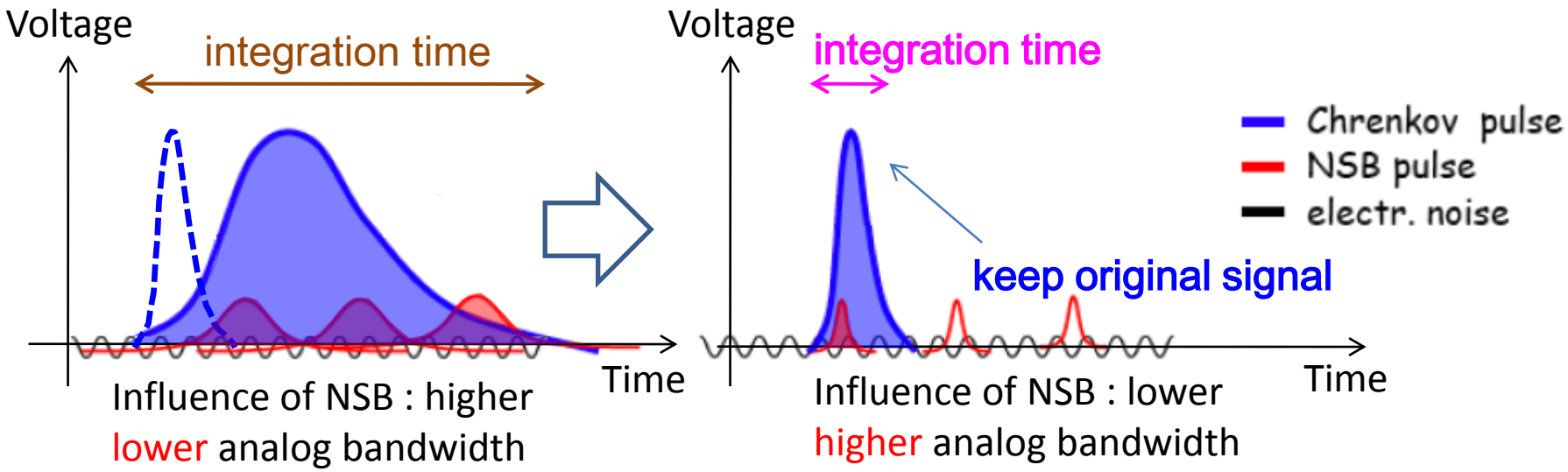
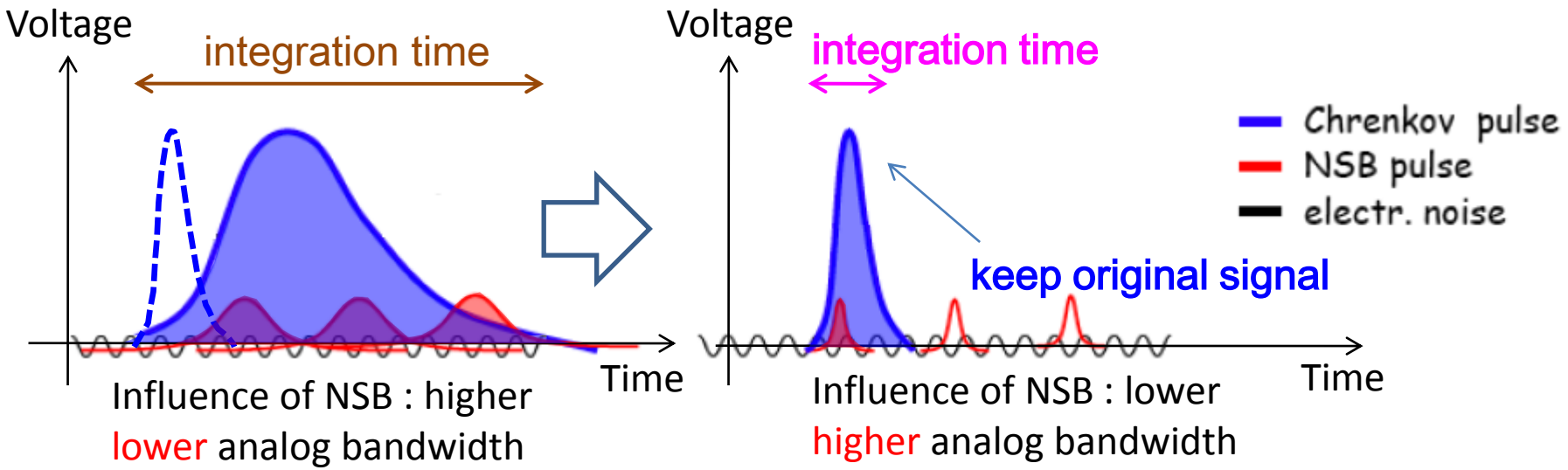


- Sampling with high analog bandwidth & minimizing the integration time
  1 reduce the influence of Night Sky Background

Signal to noise ratio



- Sampling with high analog bandwidth & minimizing the integration time
  1 reduce the influence of Night Sky Background
  2 improves shower image finer
  3 leads to lower threshold energy, better sensibility, better angular resolution and better energy resolution

Target specification

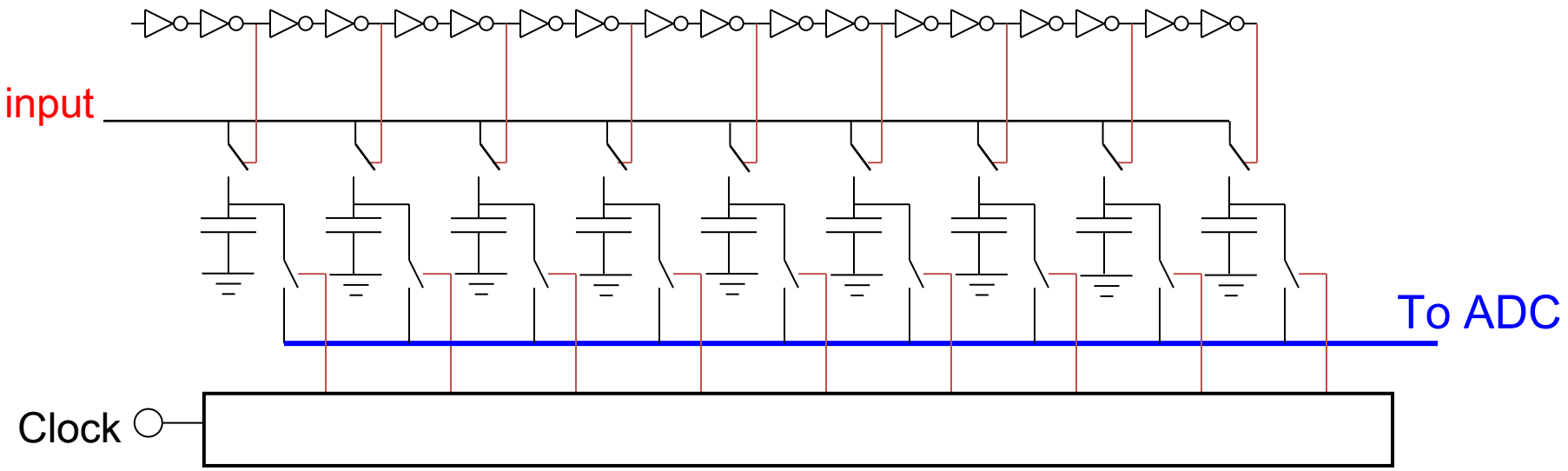
AMC processed by 0.25μm technology

- charge resolution (10 bits)
- Sampling speed (1 GHz)
- Analog bandwidth (300 MHz)
  - enough to record original shapes of Cherenkov light signals

We can measure quantity of Cherenkov light correctly

How AMC sample voltage

- AMC has mainly



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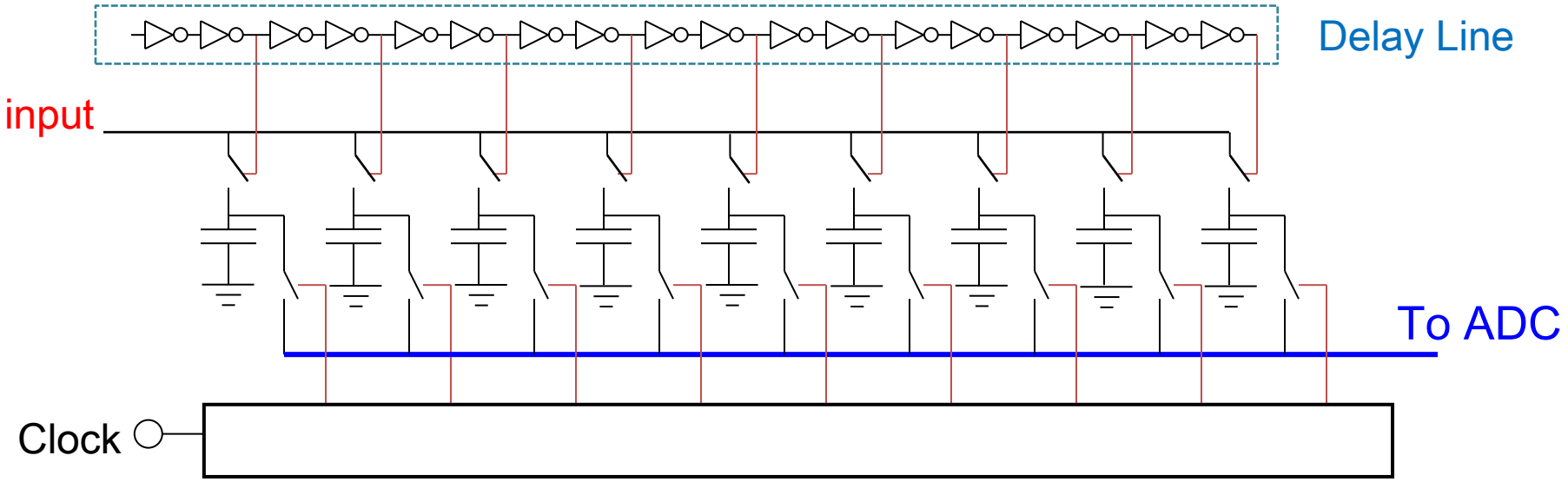

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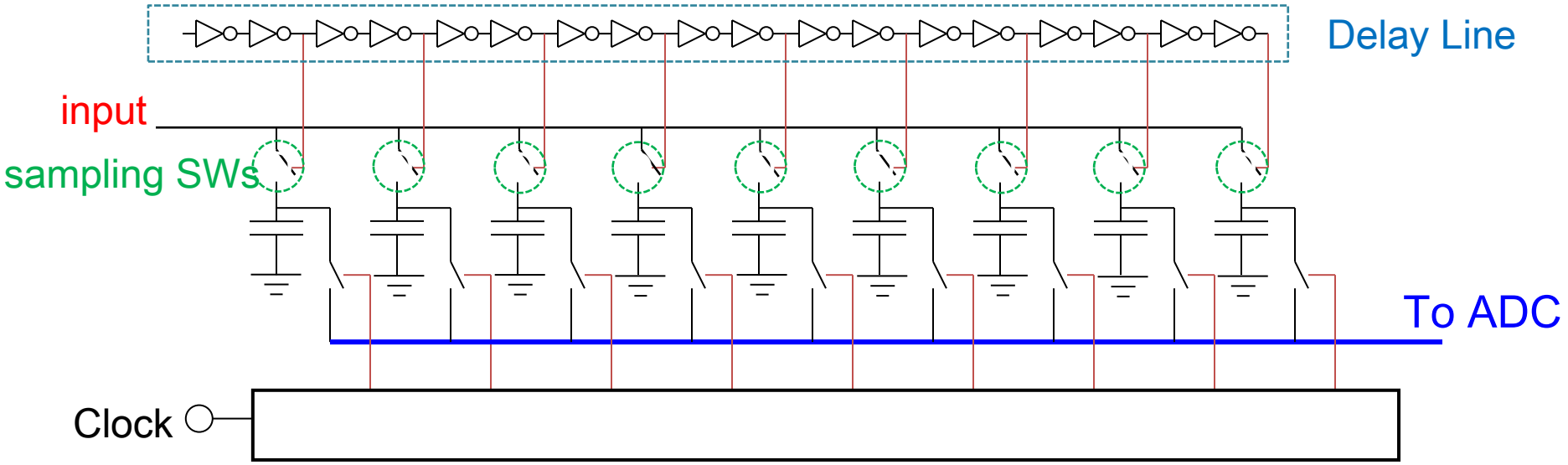

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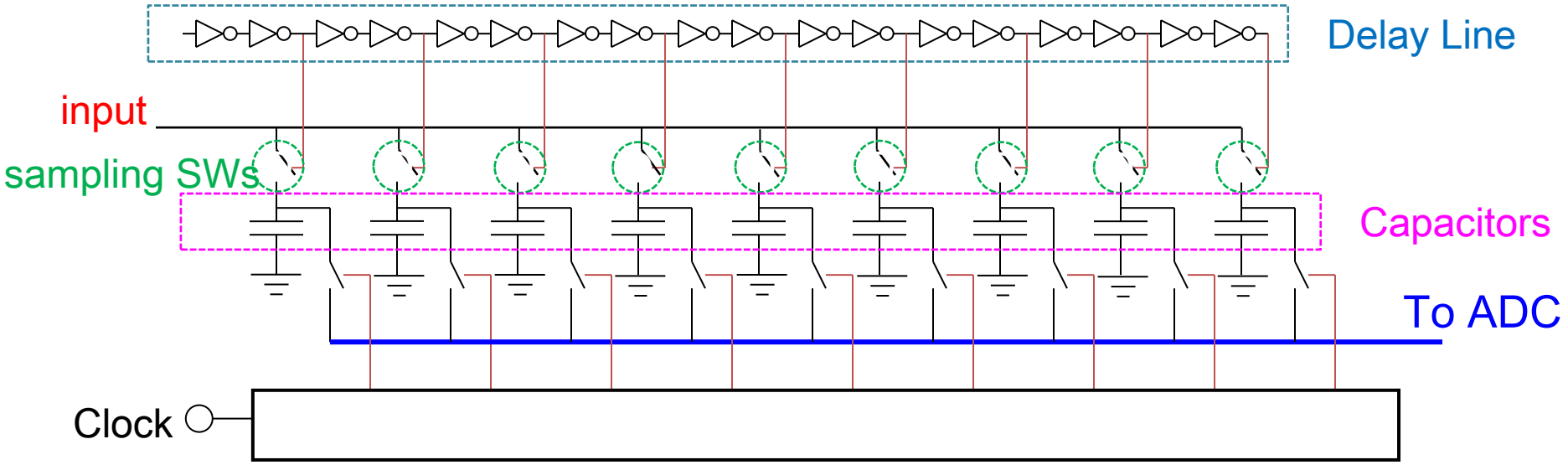

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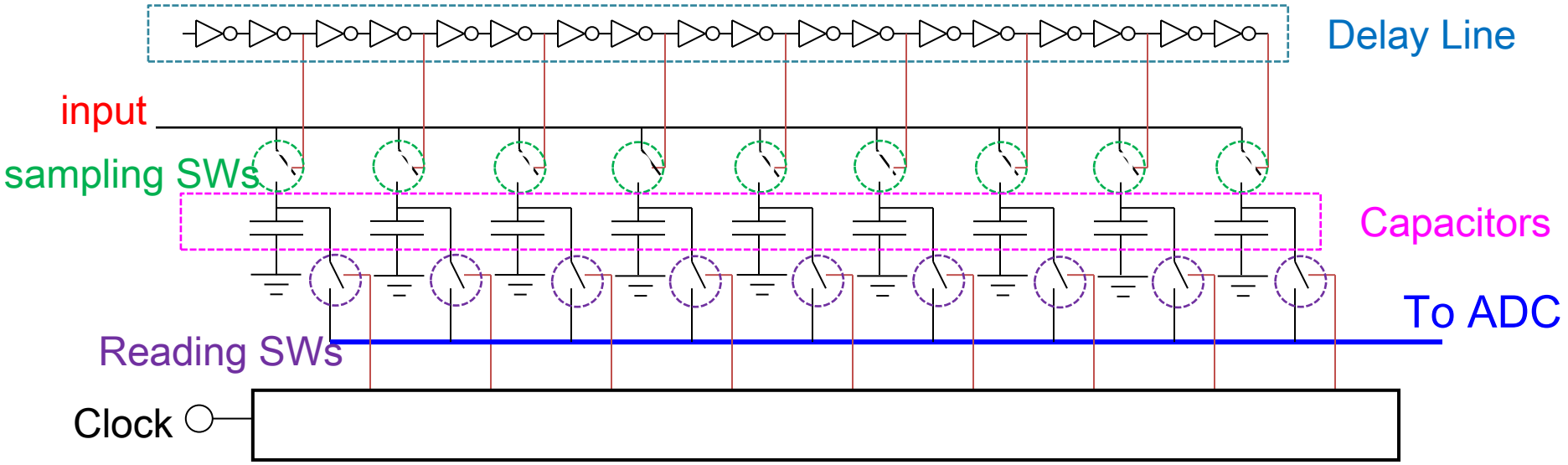

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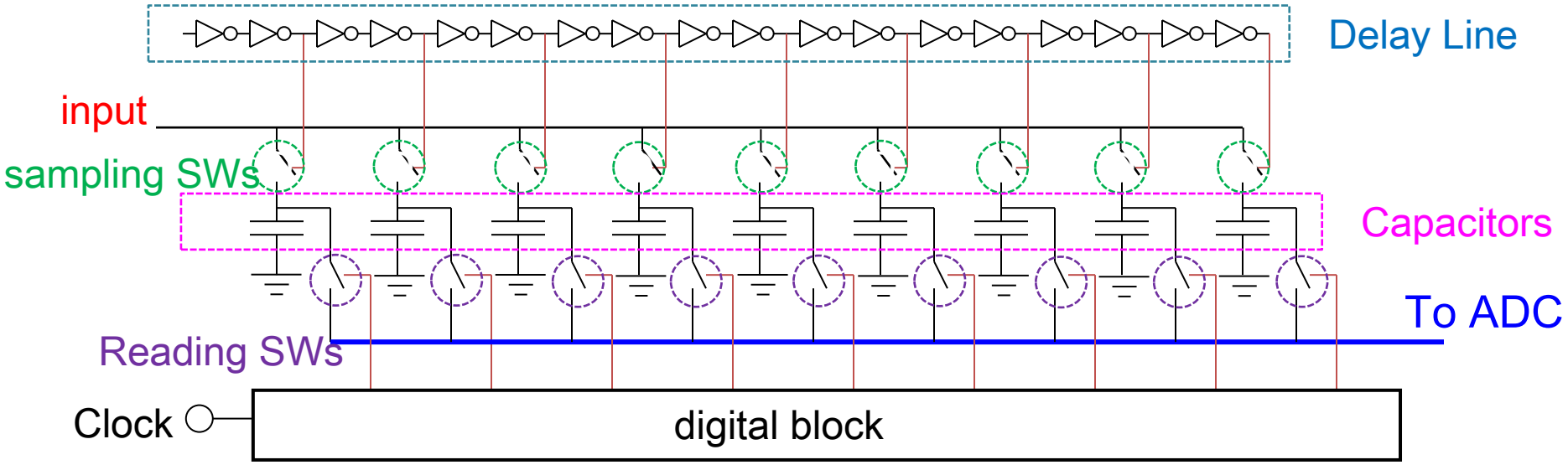

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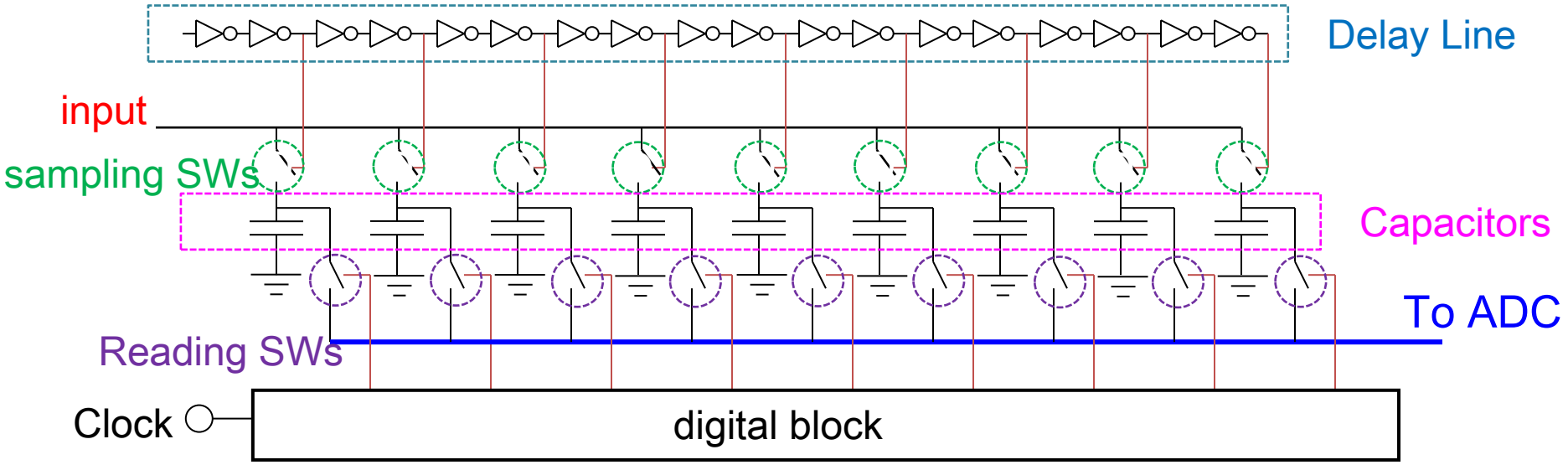

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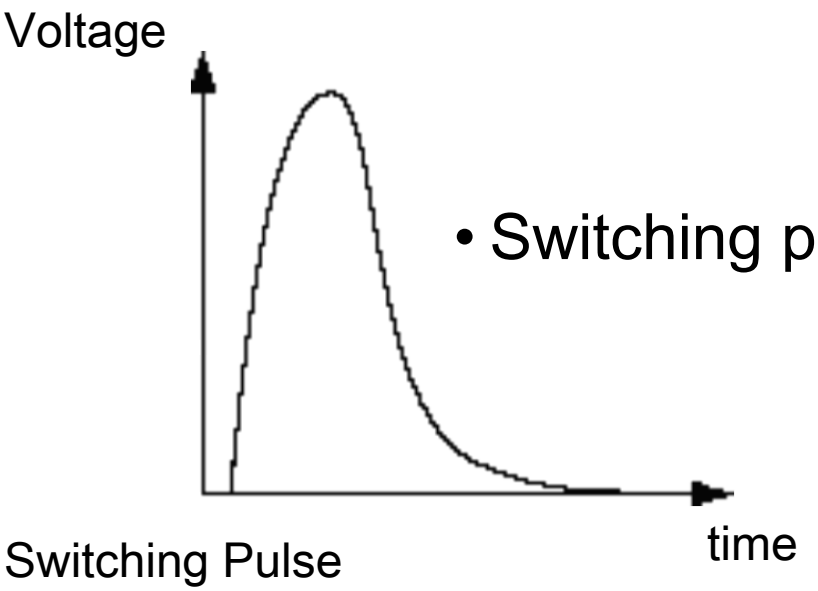

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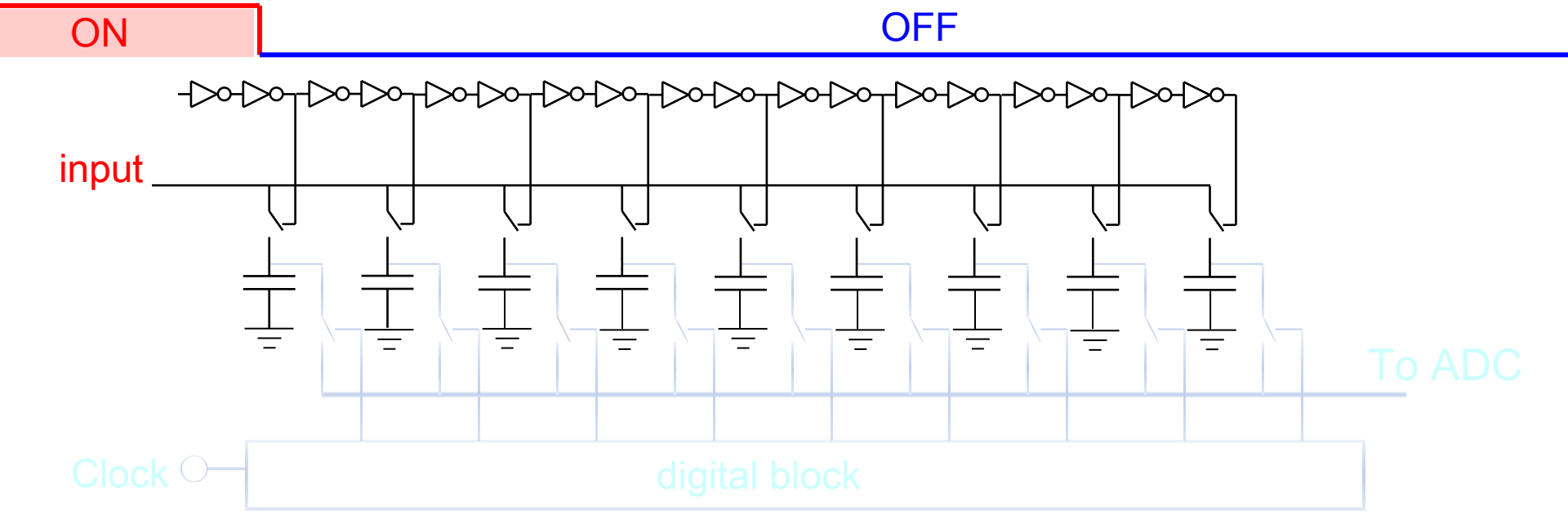

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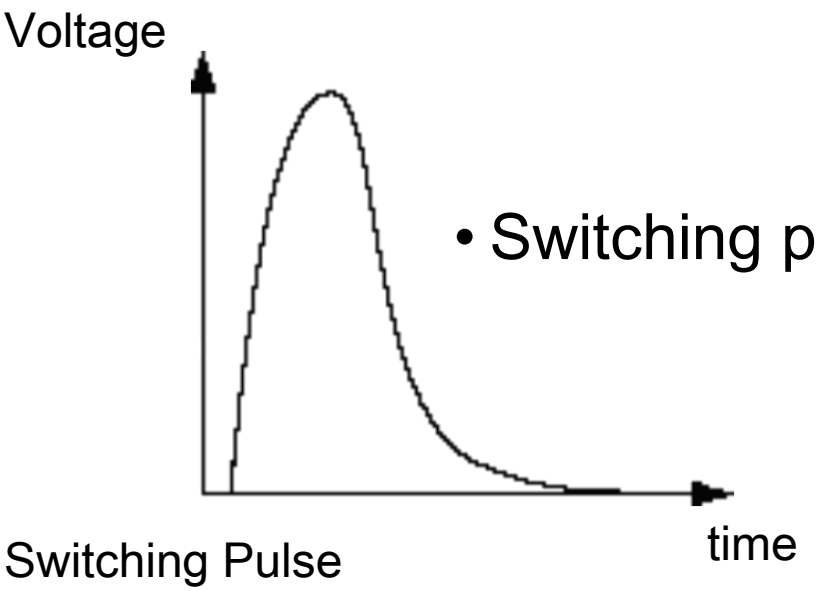

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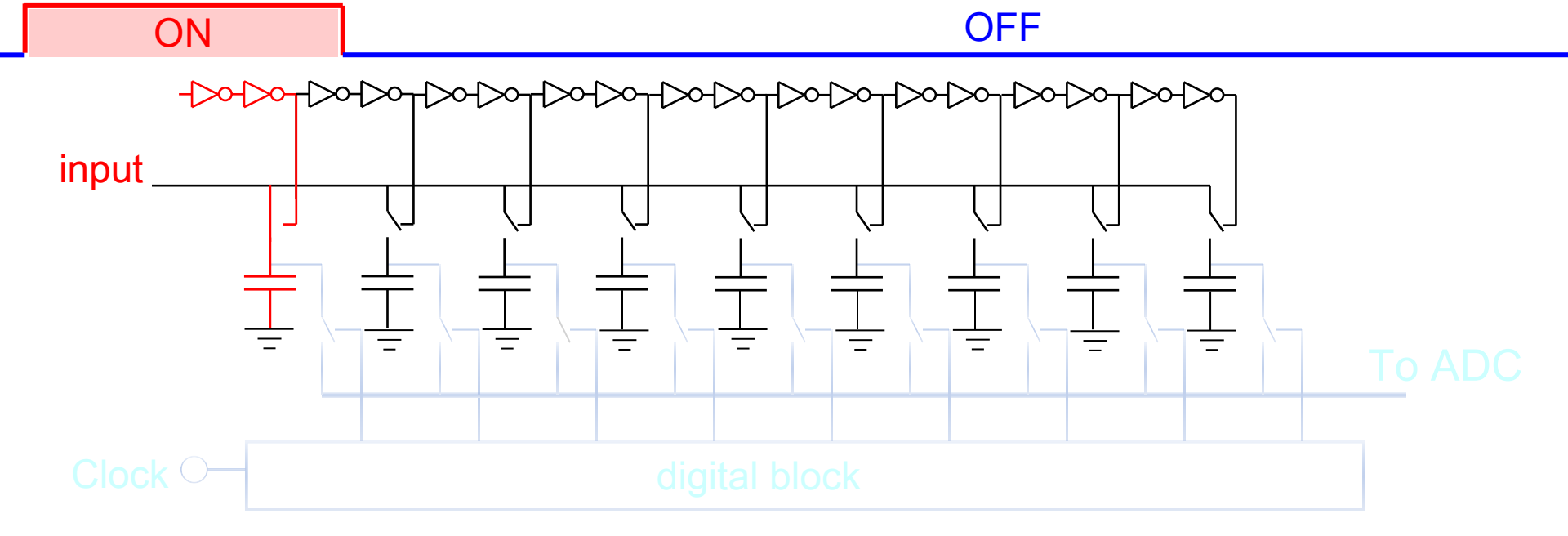

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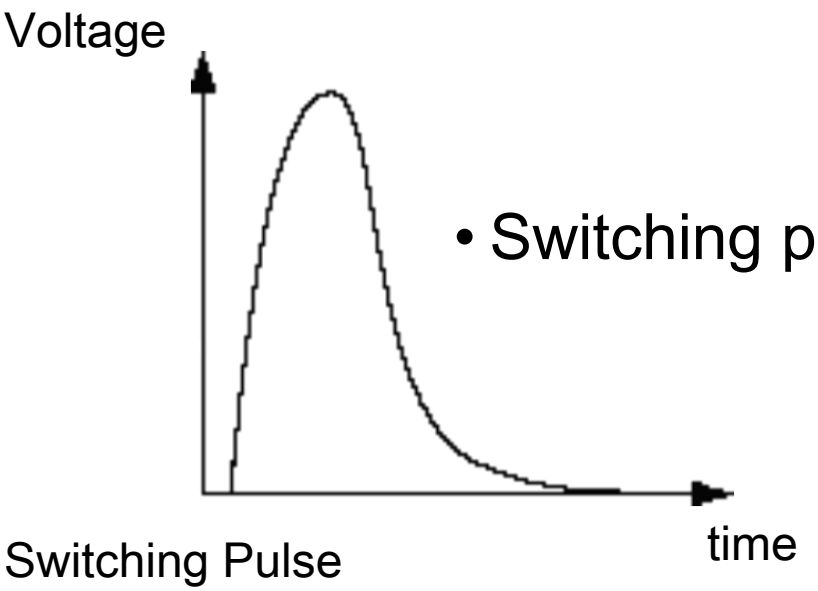

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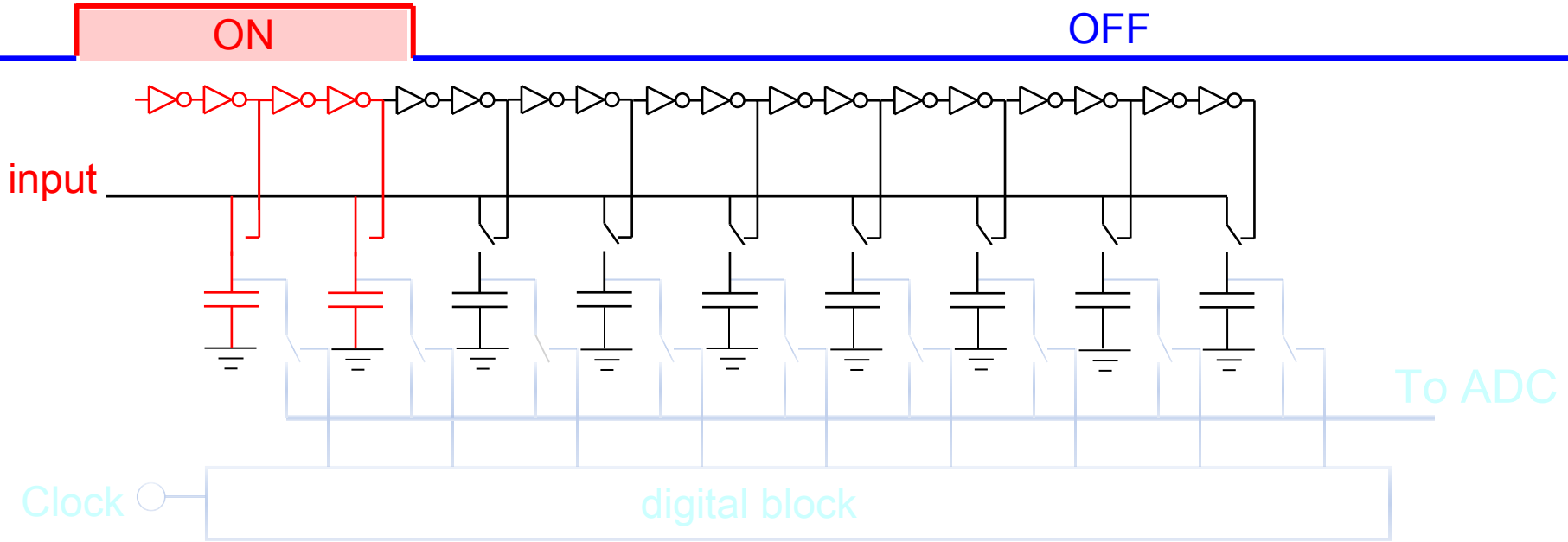

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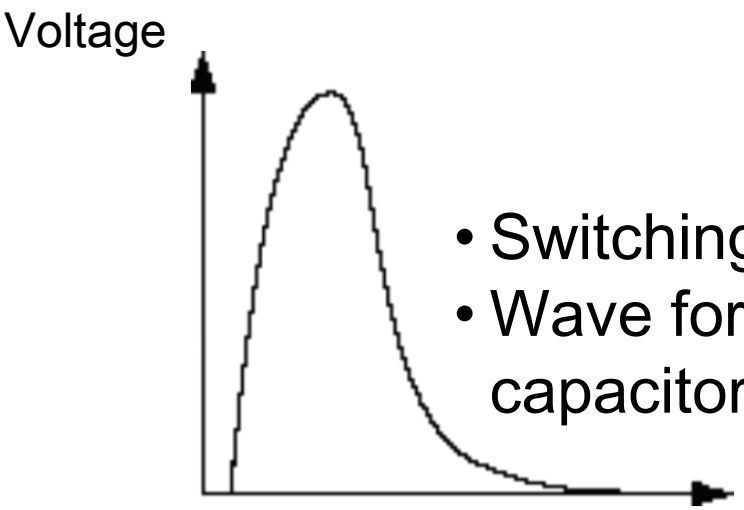

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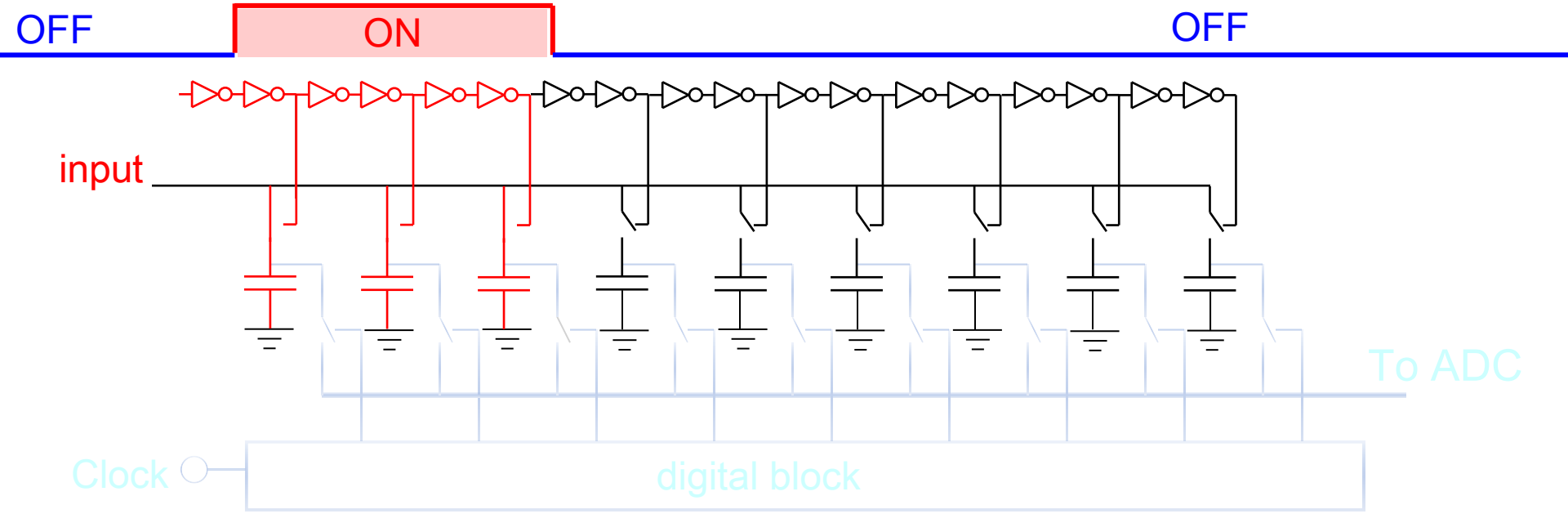

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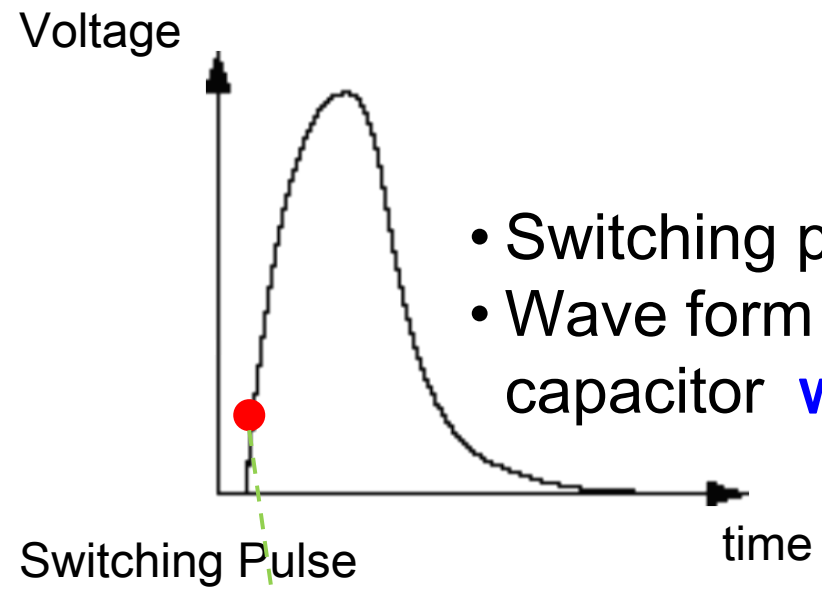

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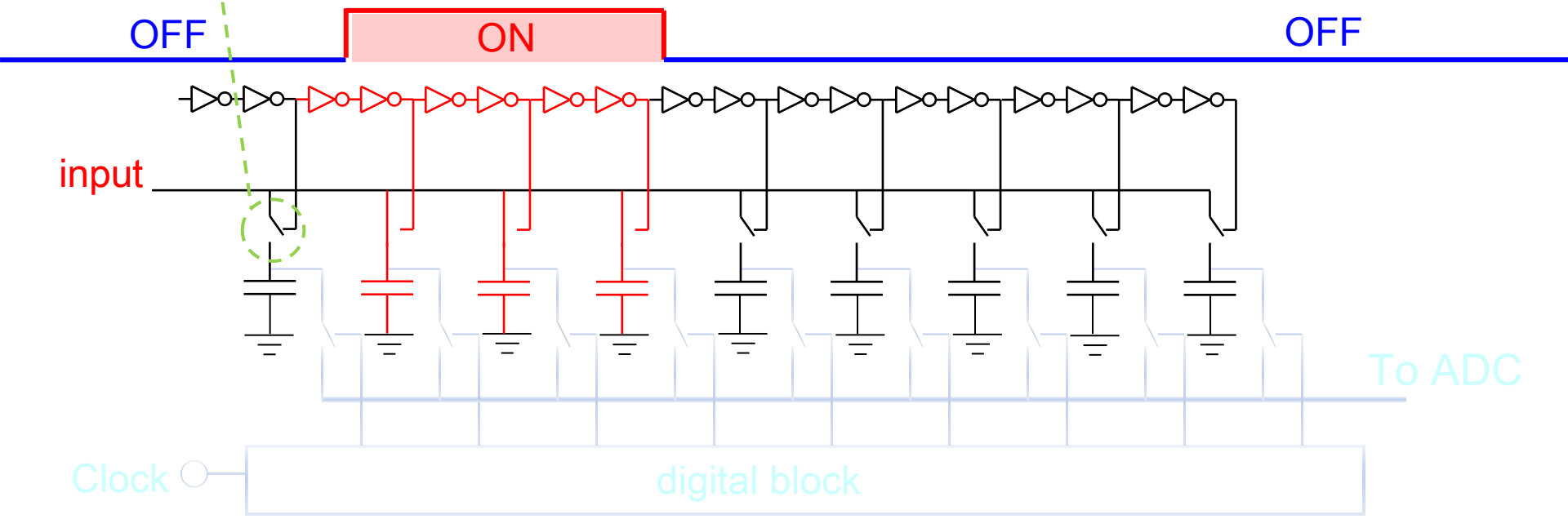

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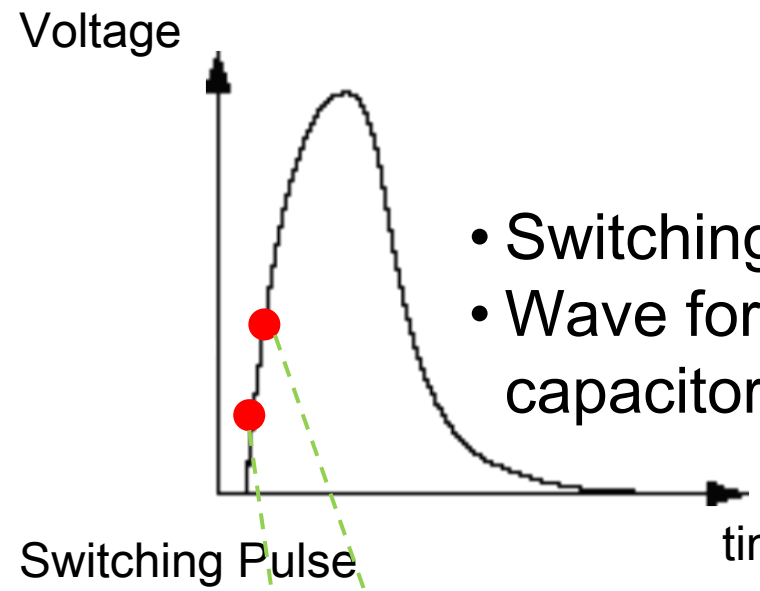

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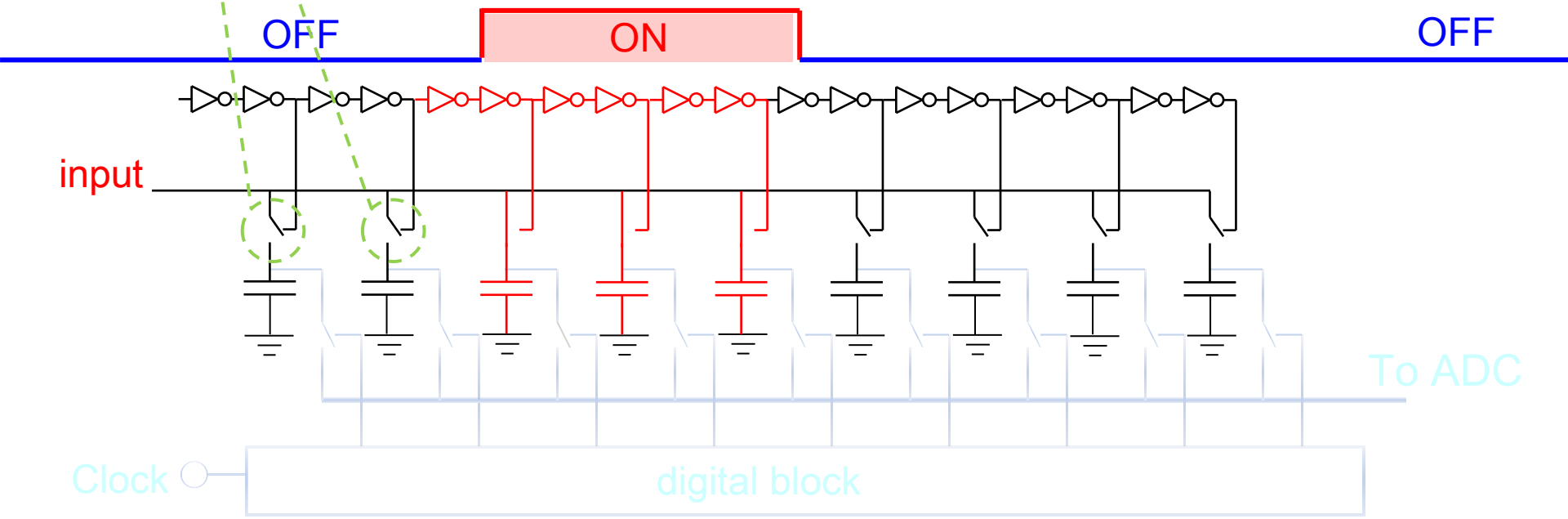

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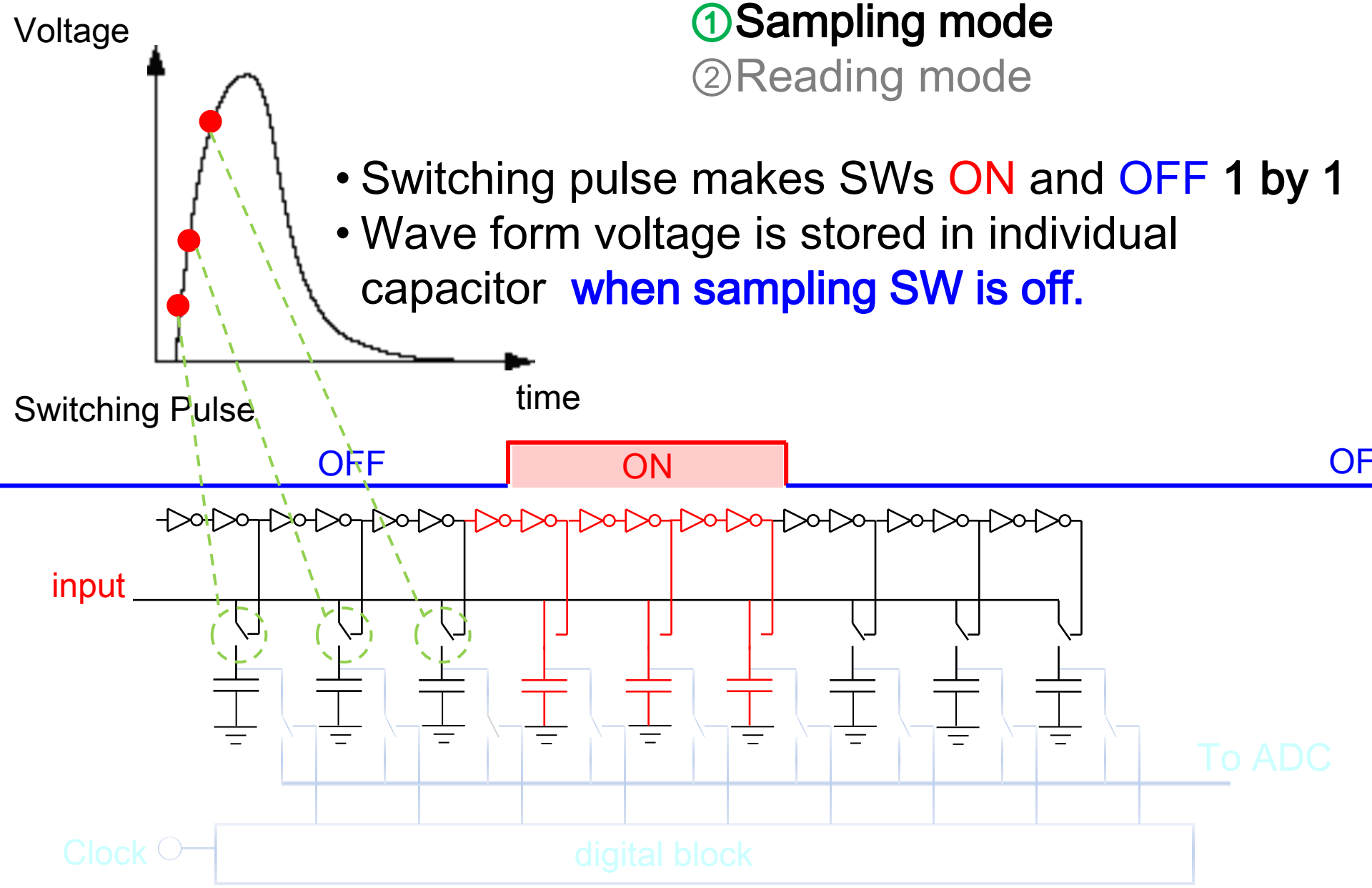

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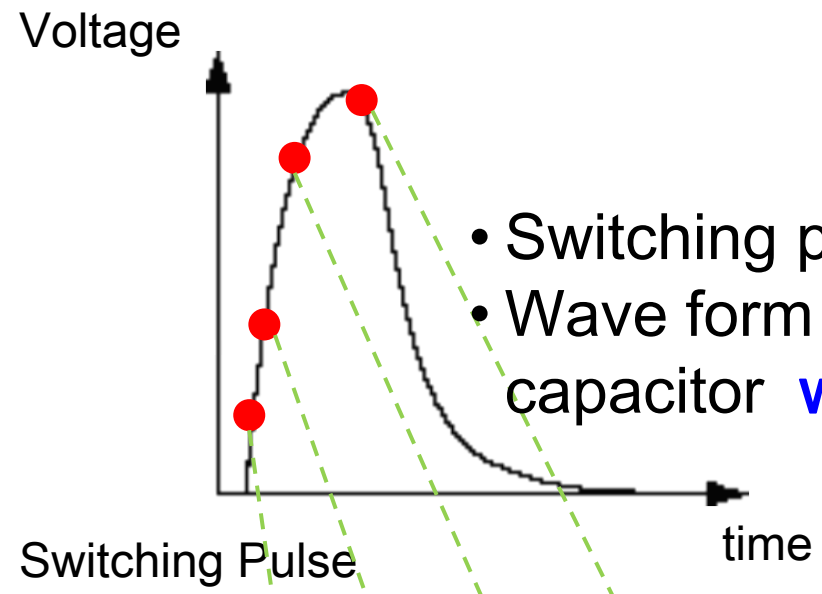

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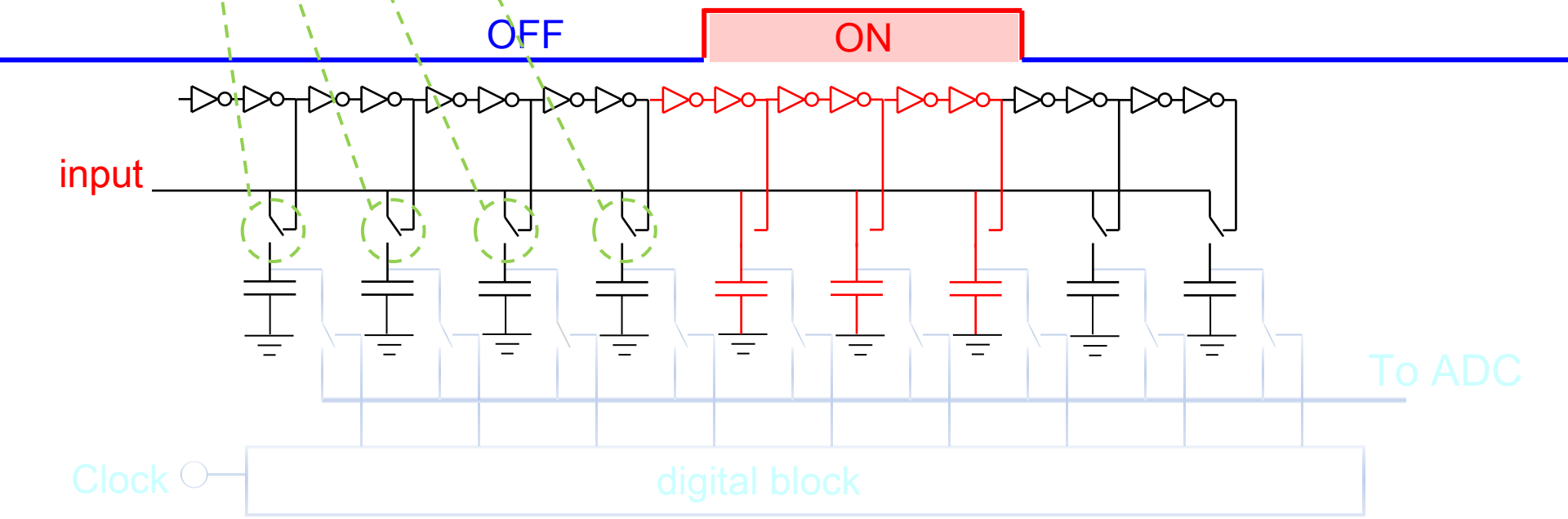

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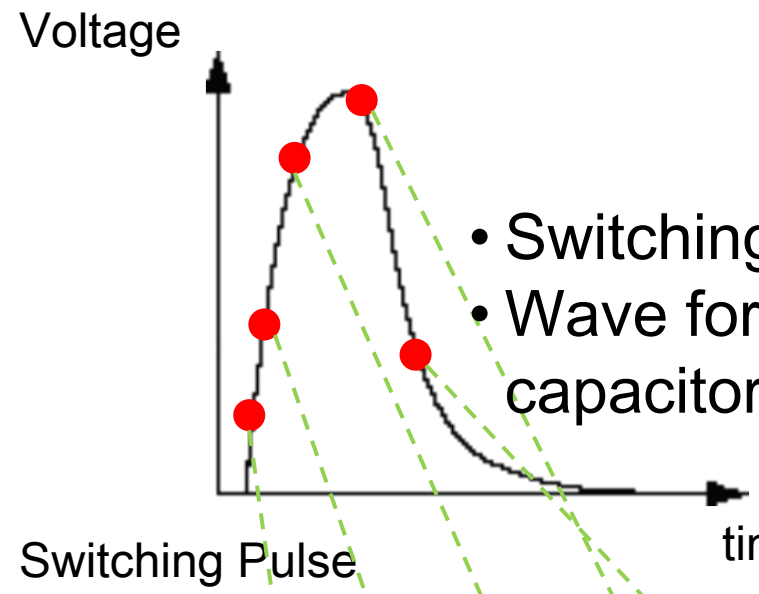

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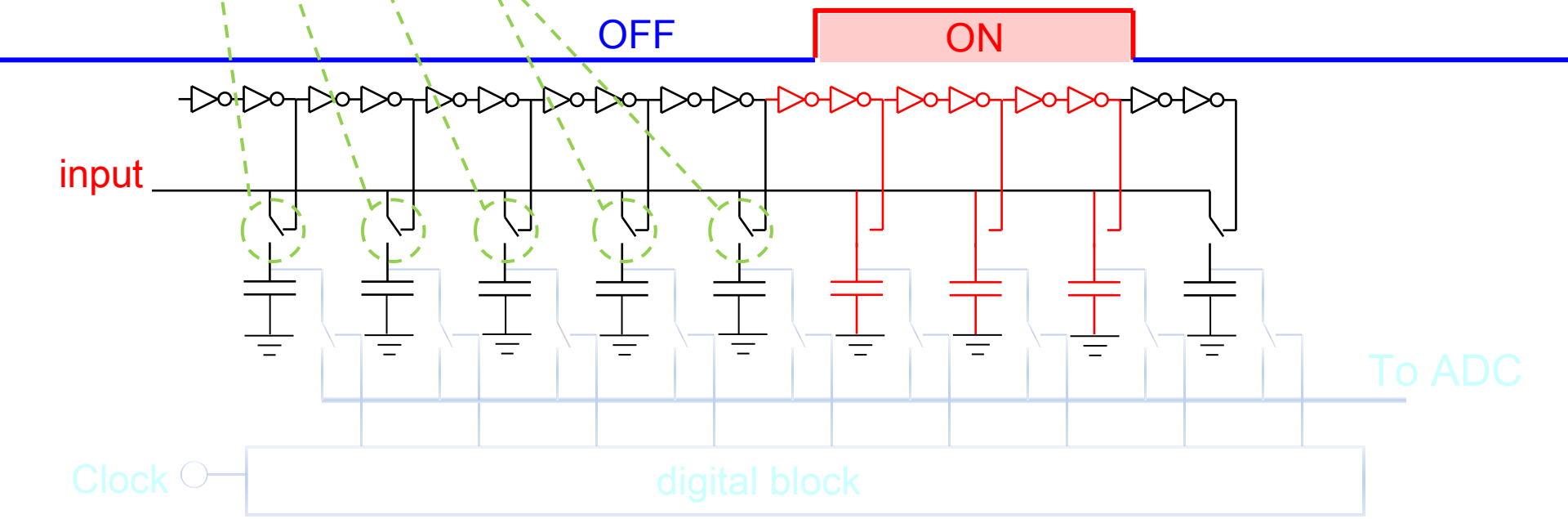

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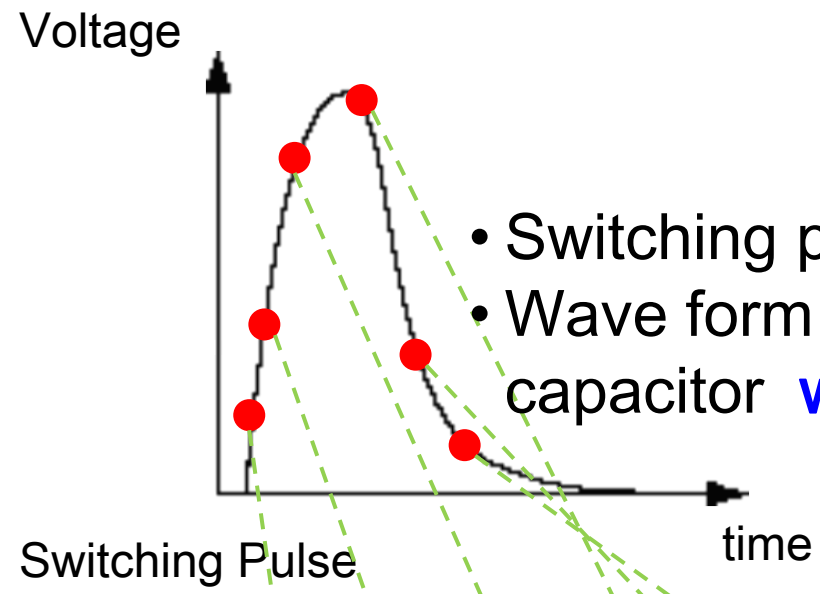

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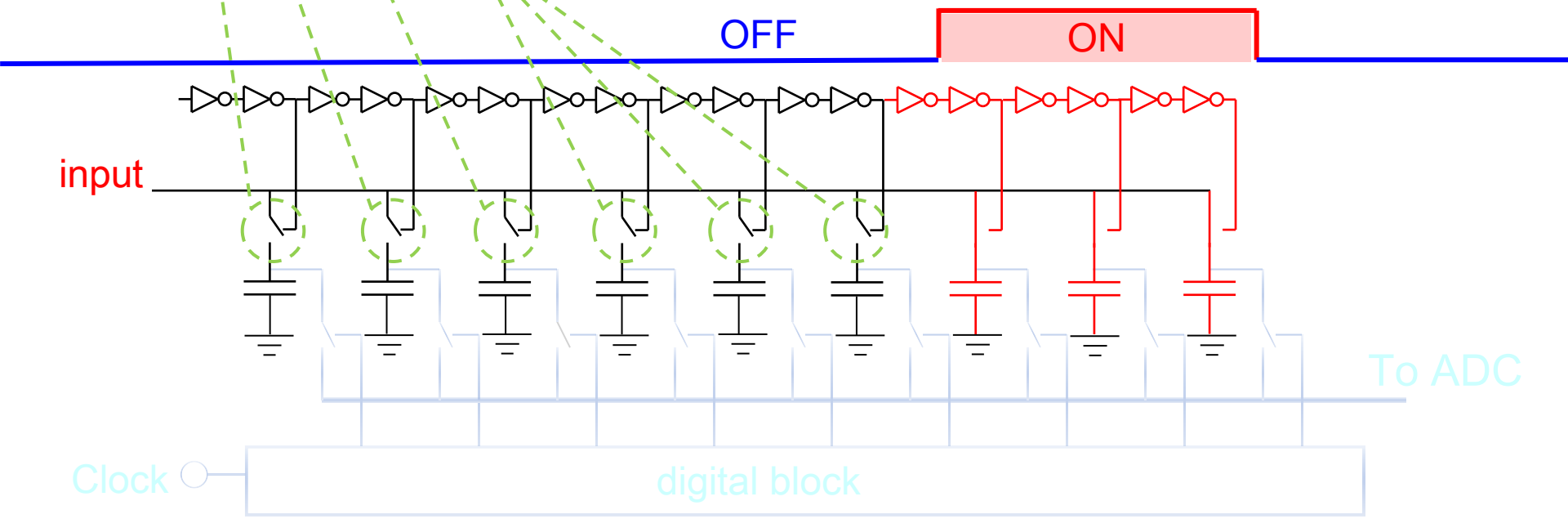

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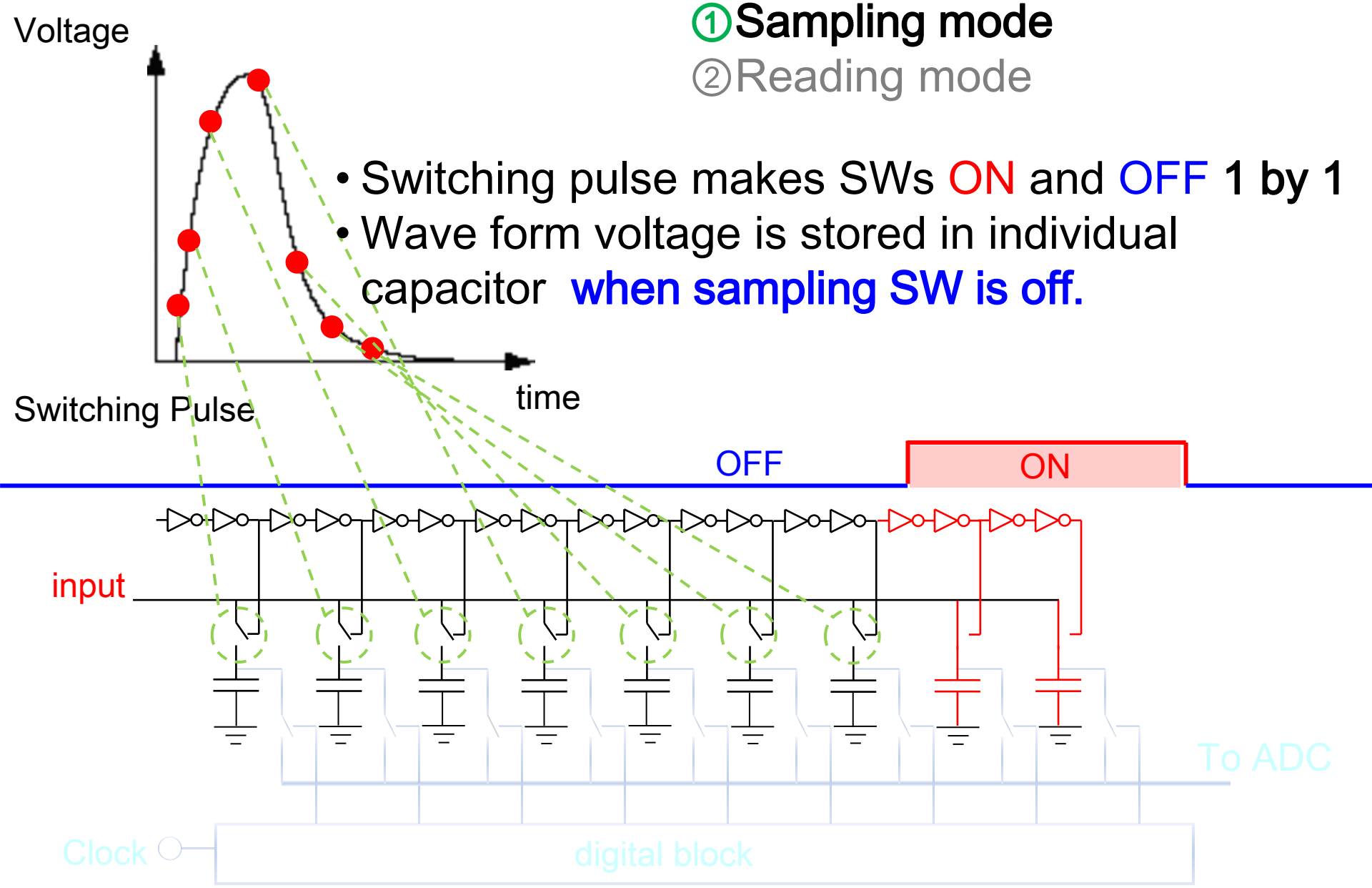

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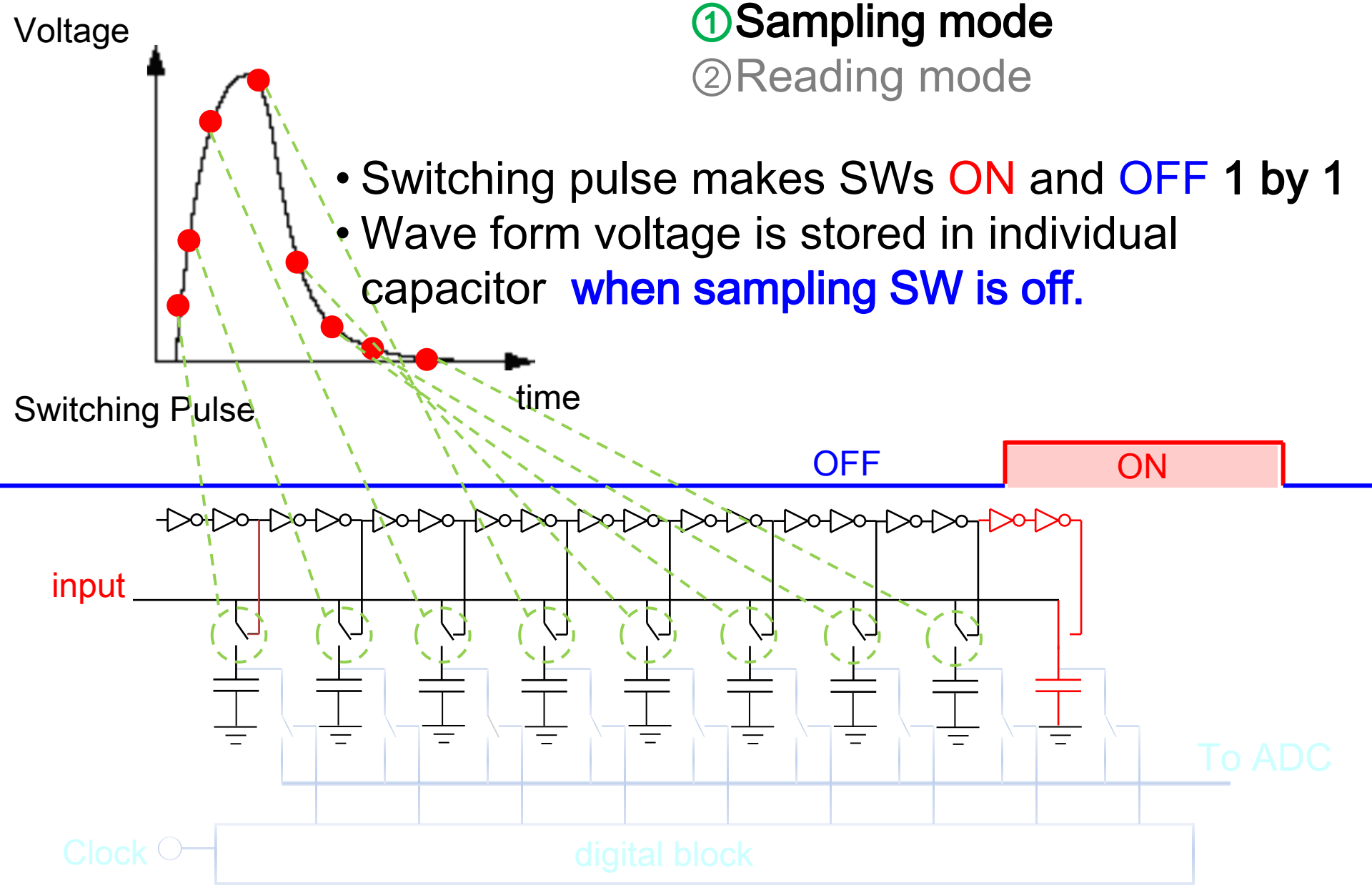

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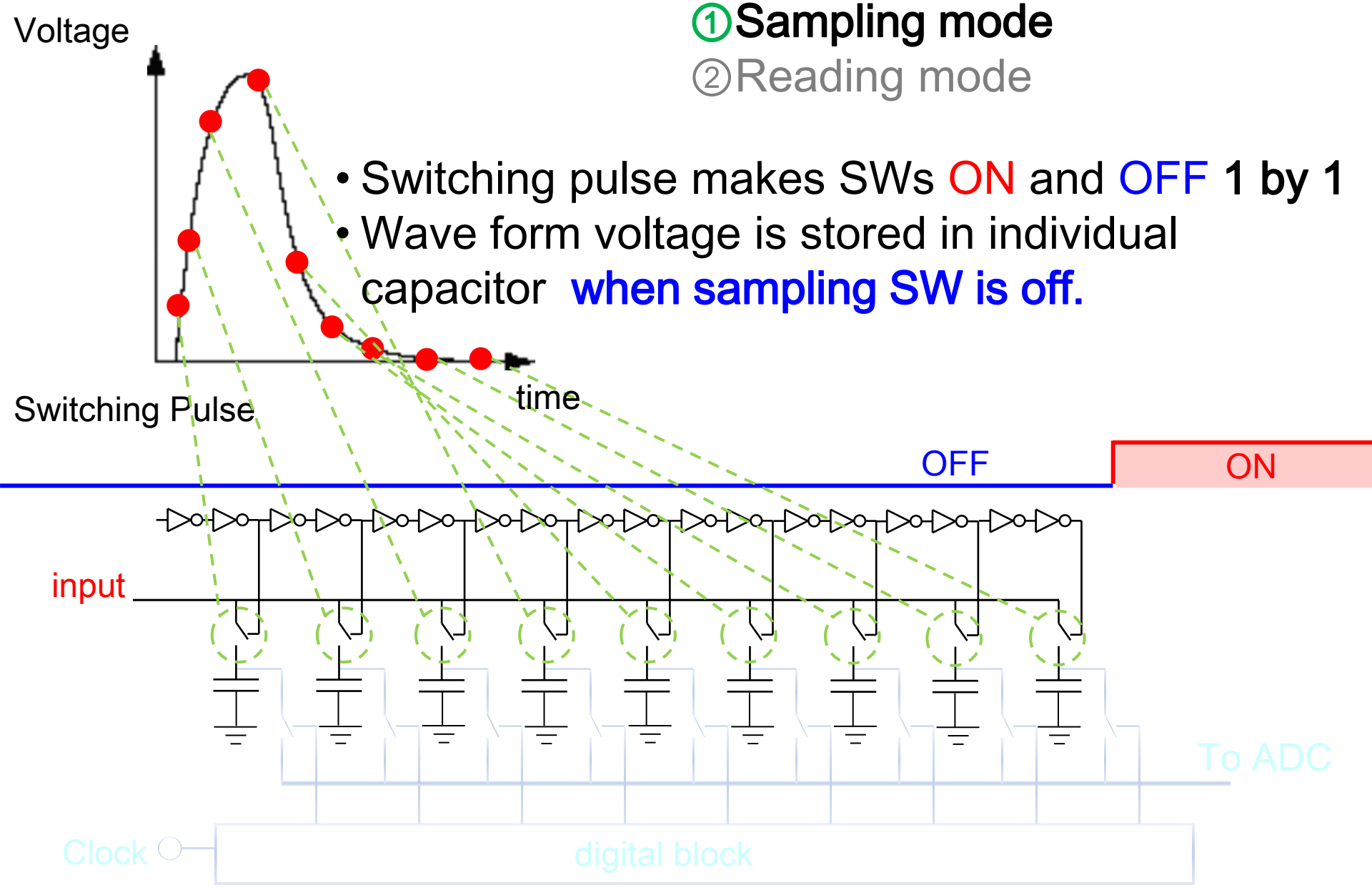

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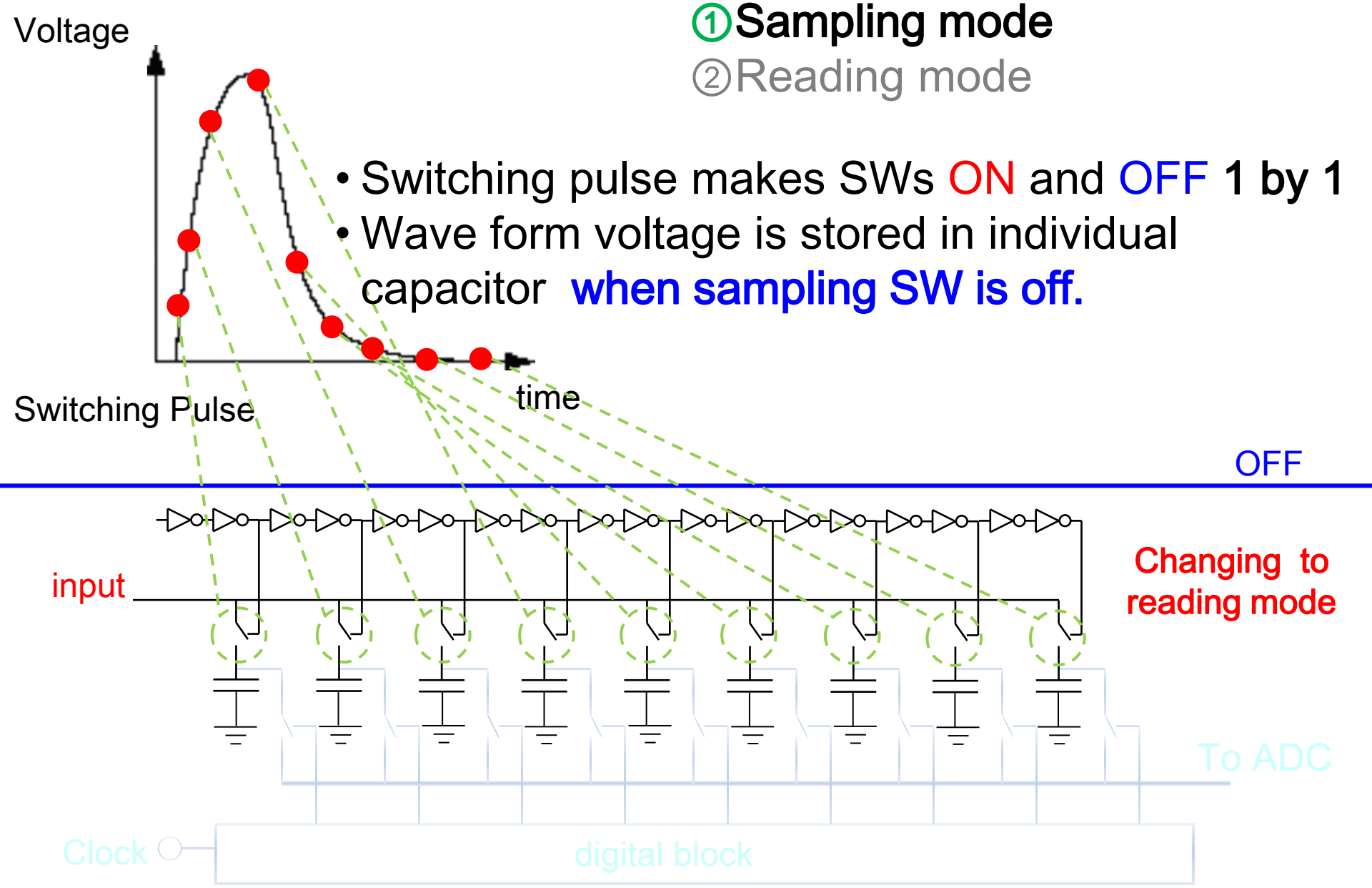

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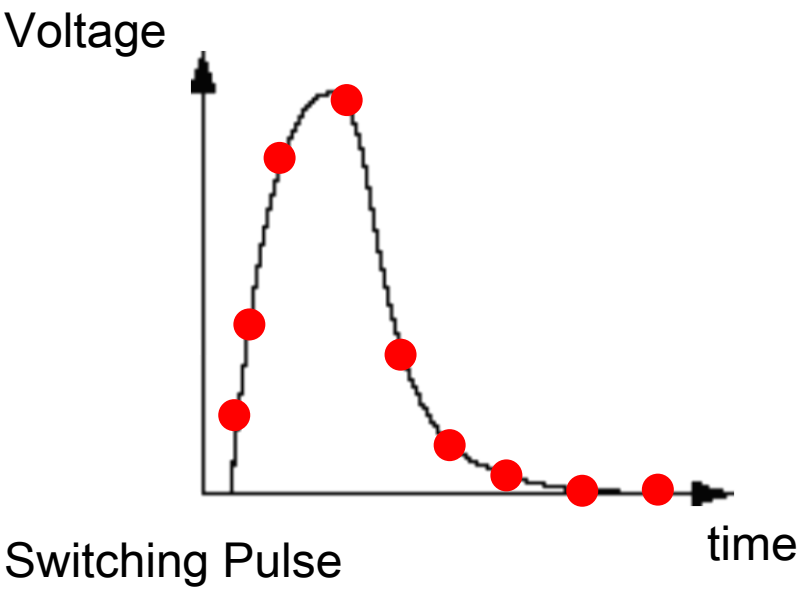

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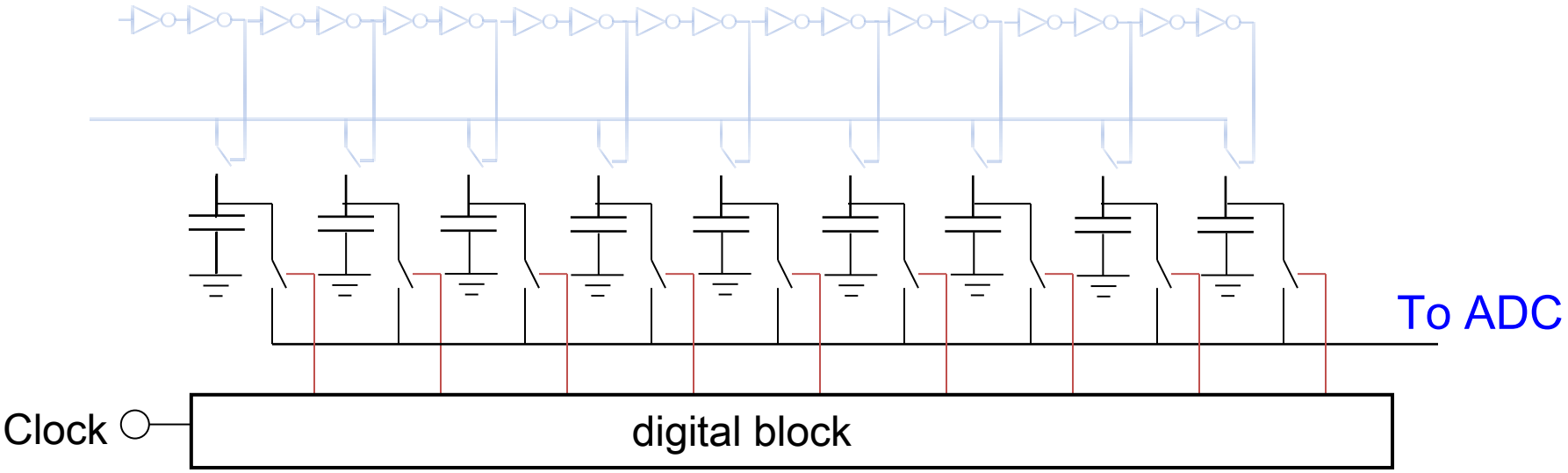

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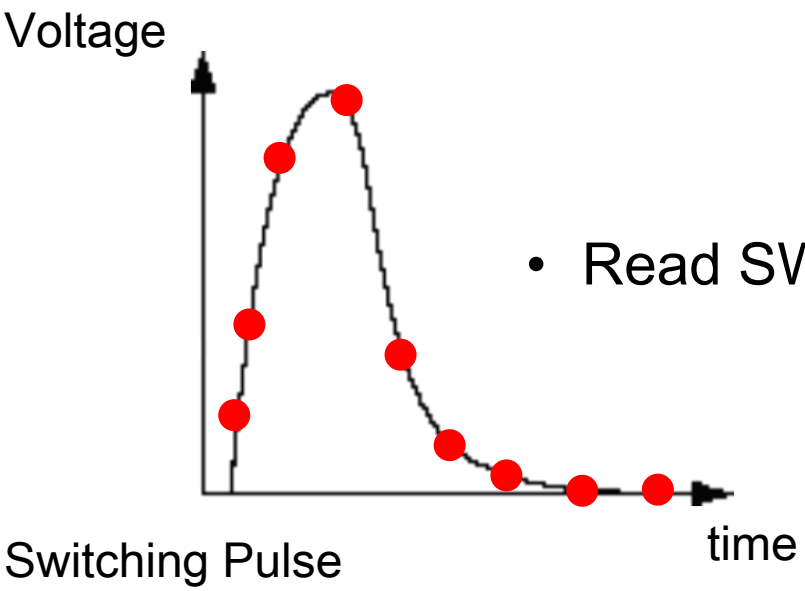

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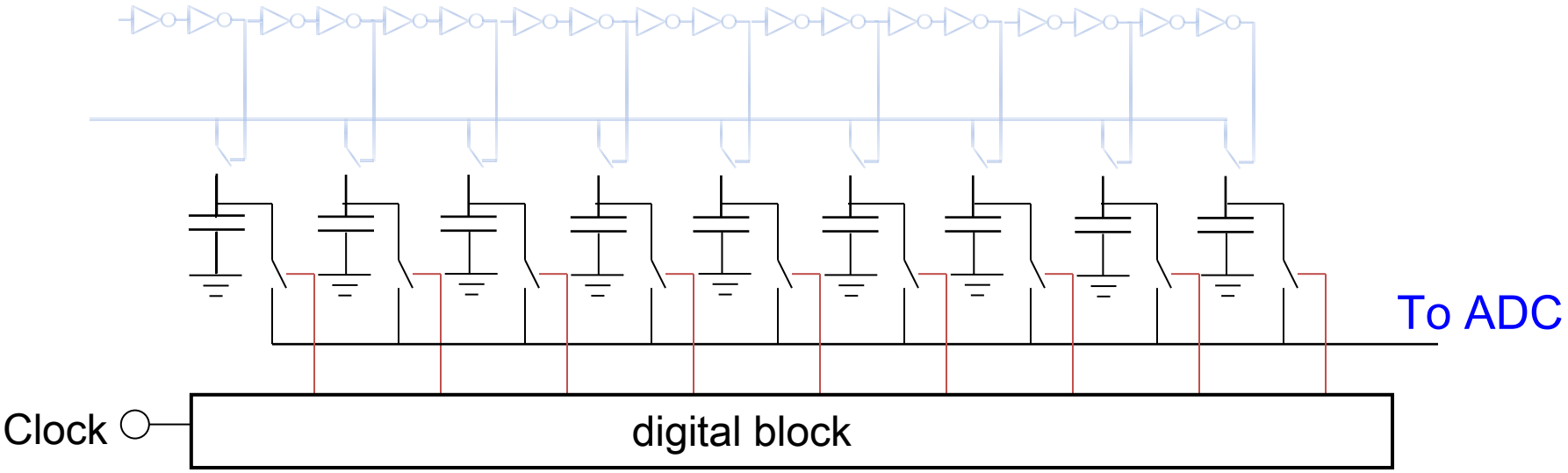

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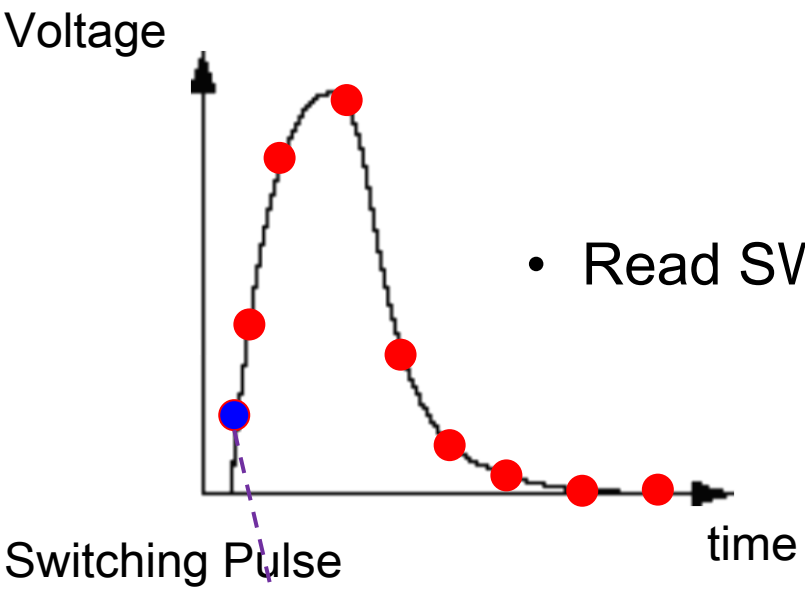

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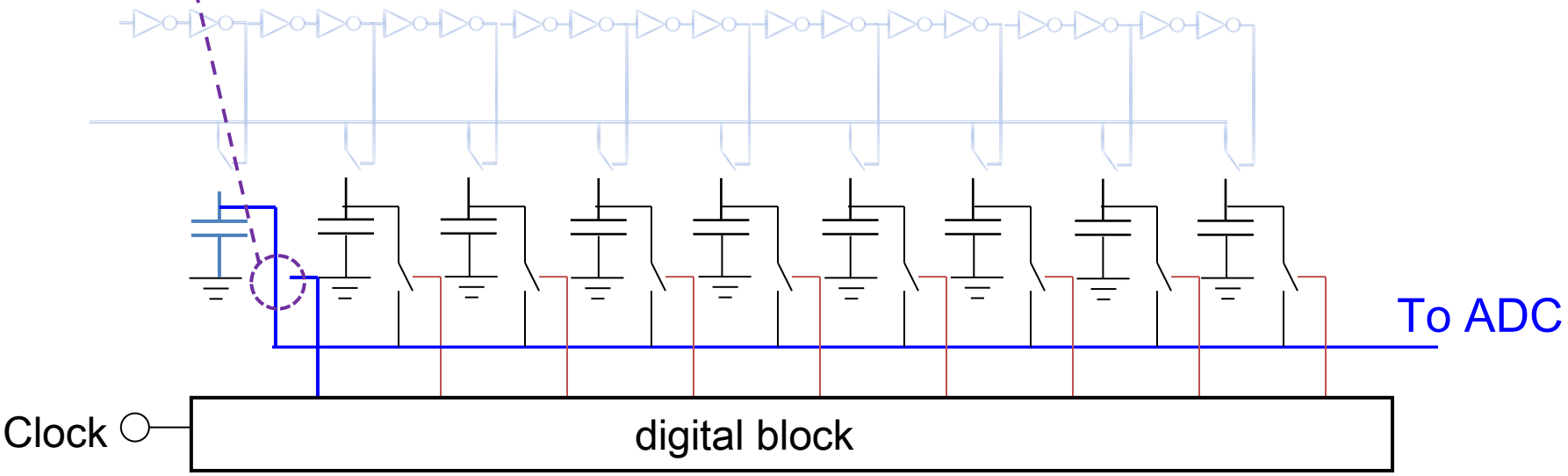

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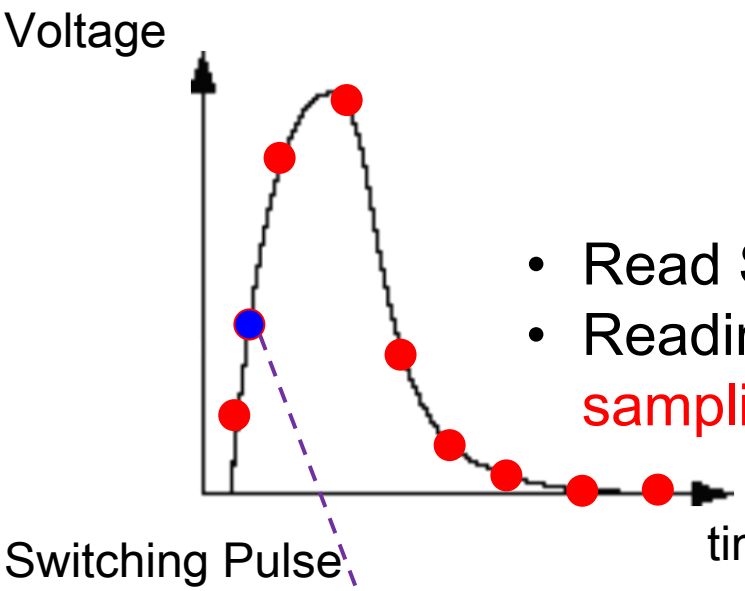

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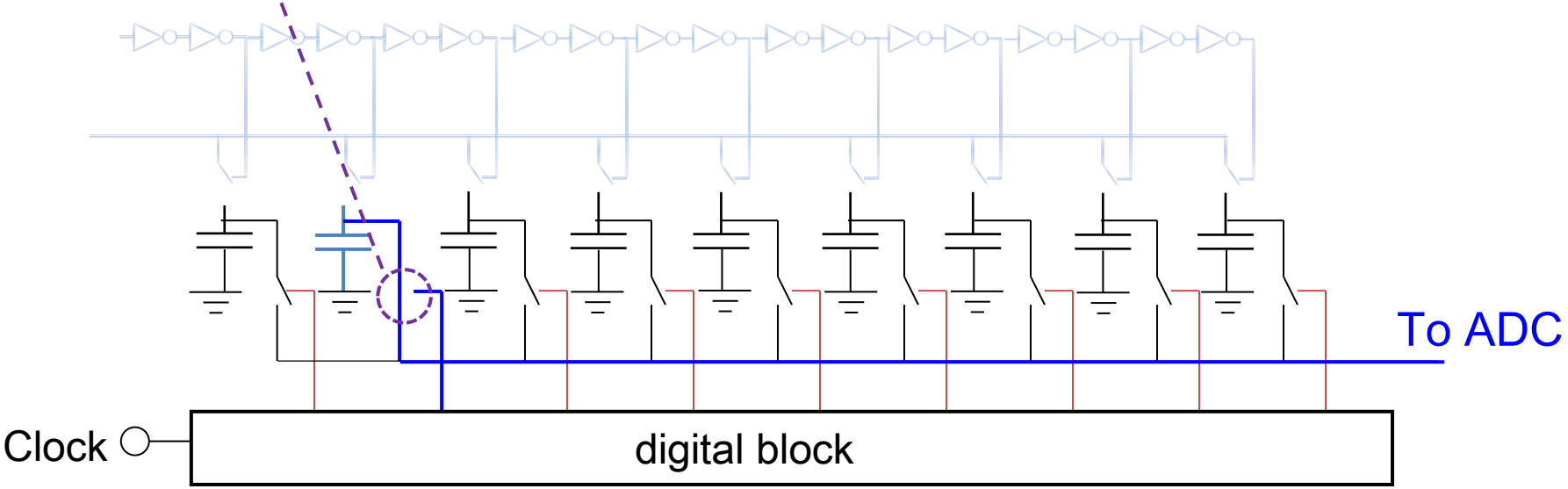

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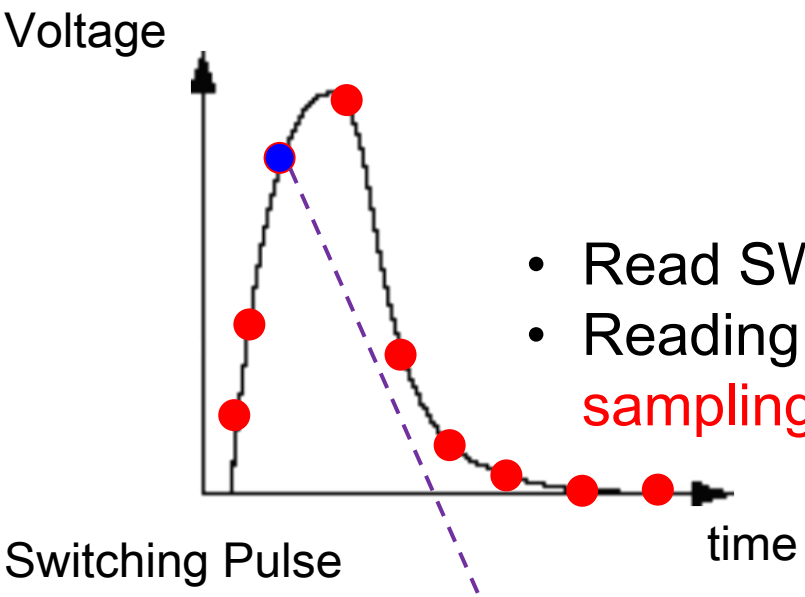

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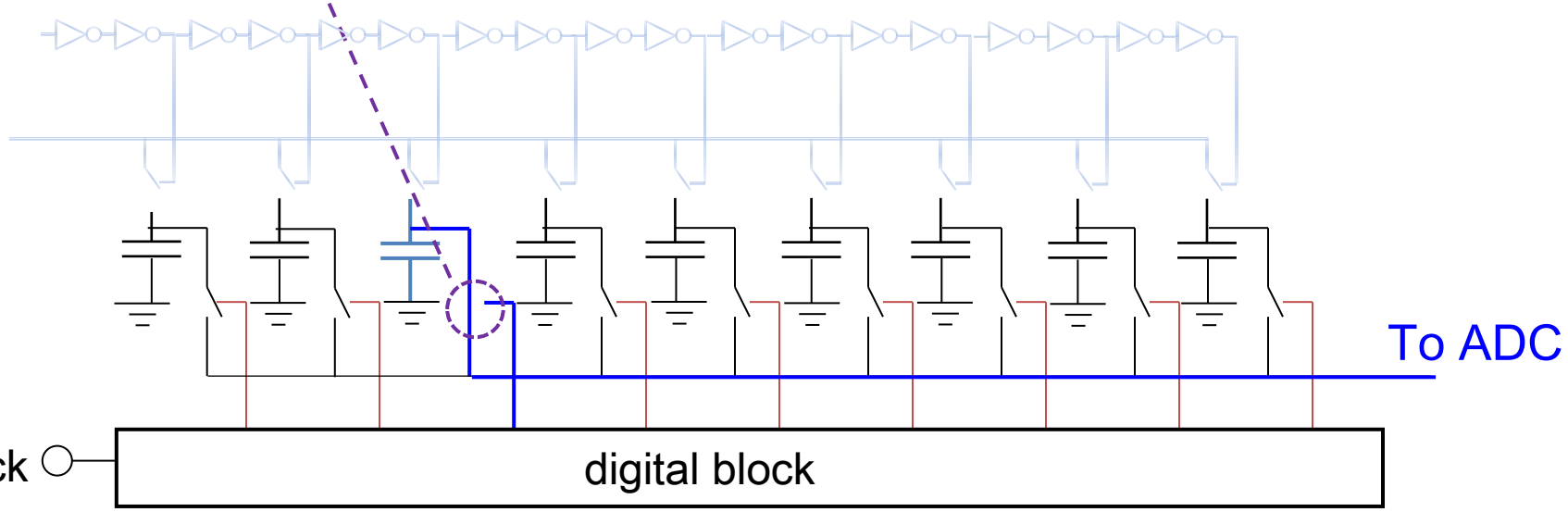

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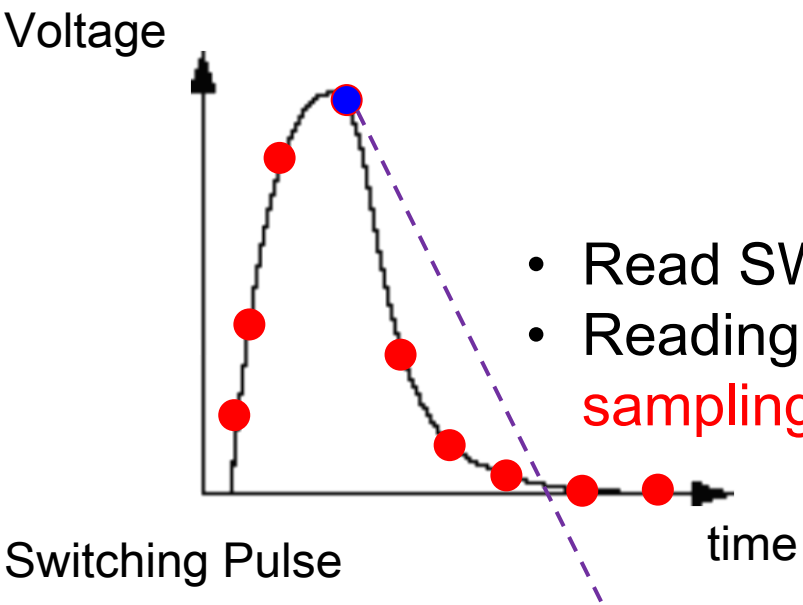

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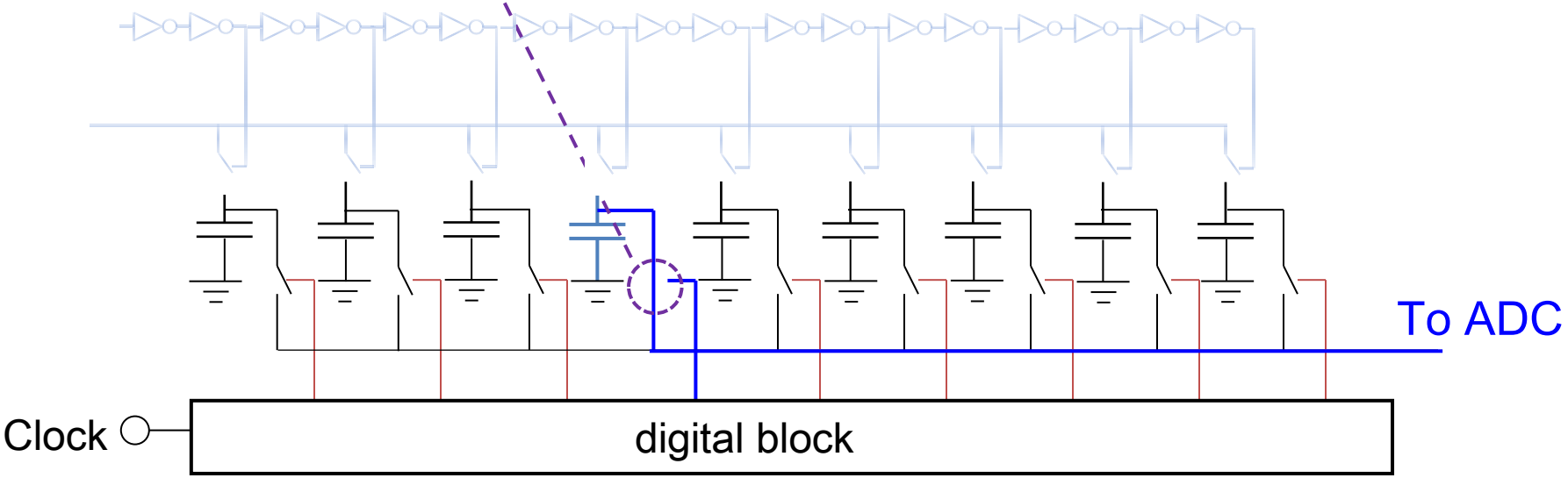
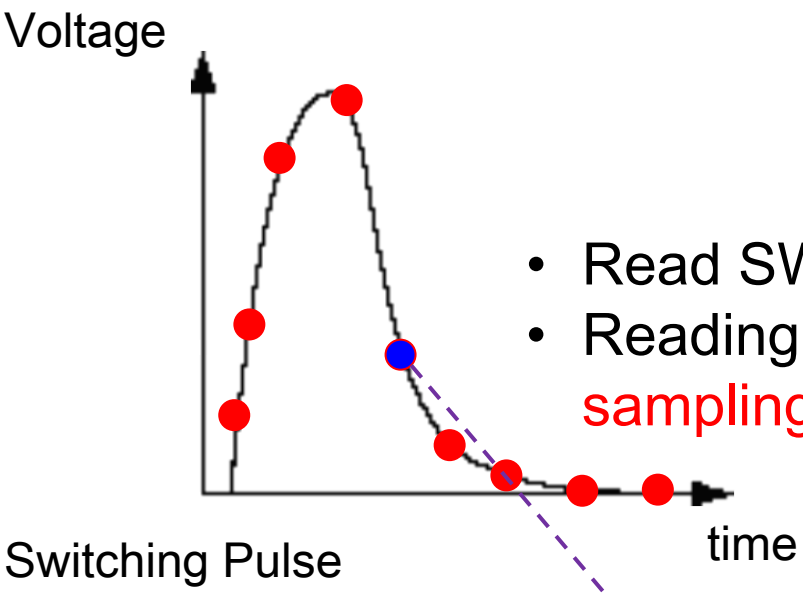
- Read SWs are ON 1 by 1 to digitize stored data
- Reading speed is slowly (<50MHz) than sampling speed (1GHz)



How AMC sample voltage



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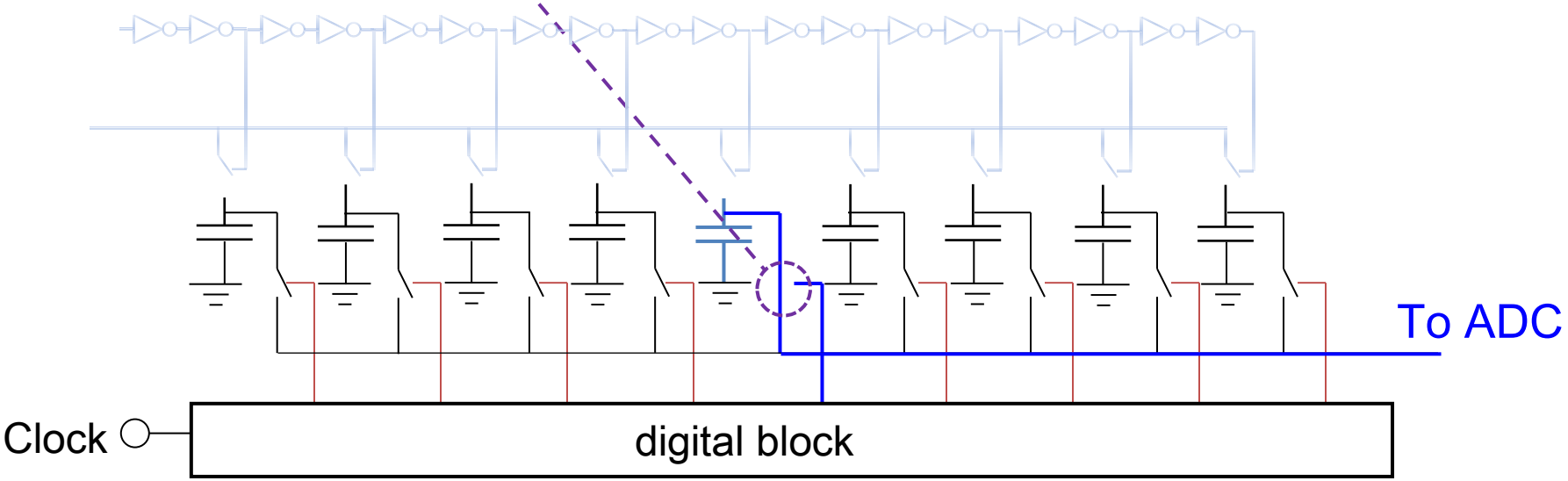
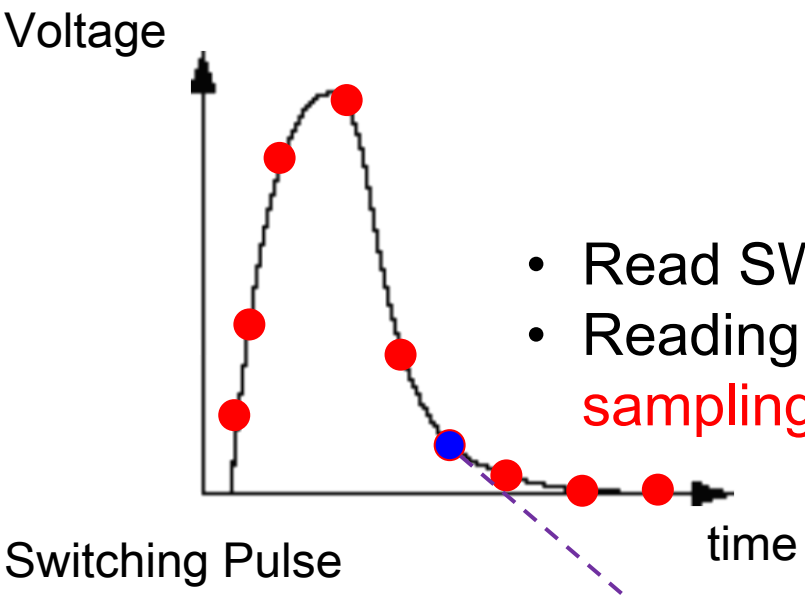


How AMC sample voltage



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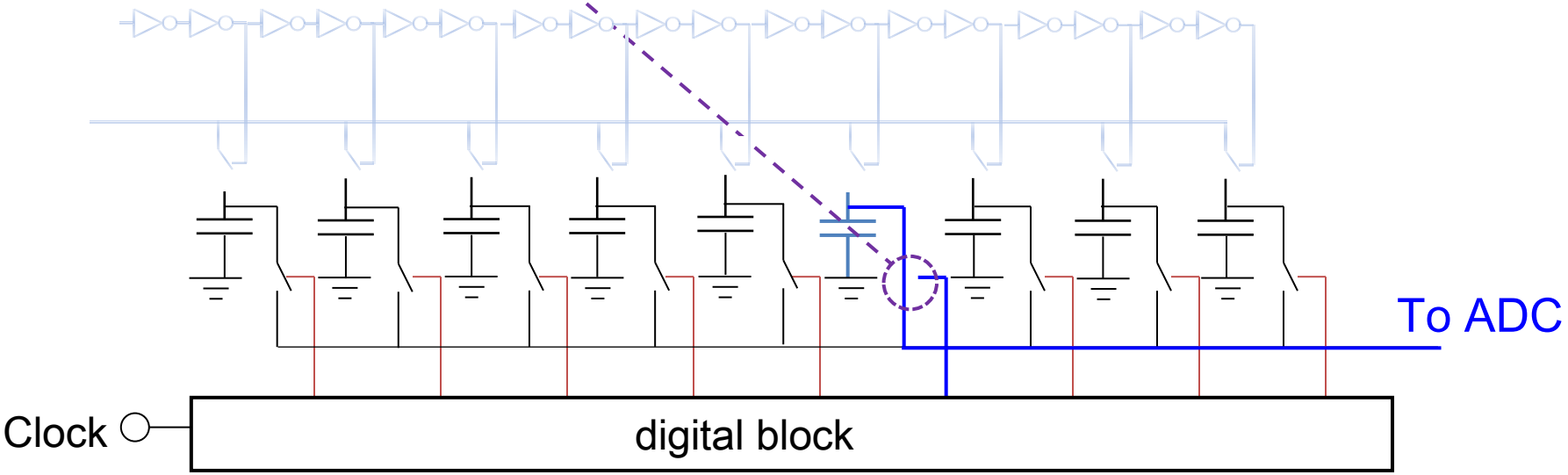
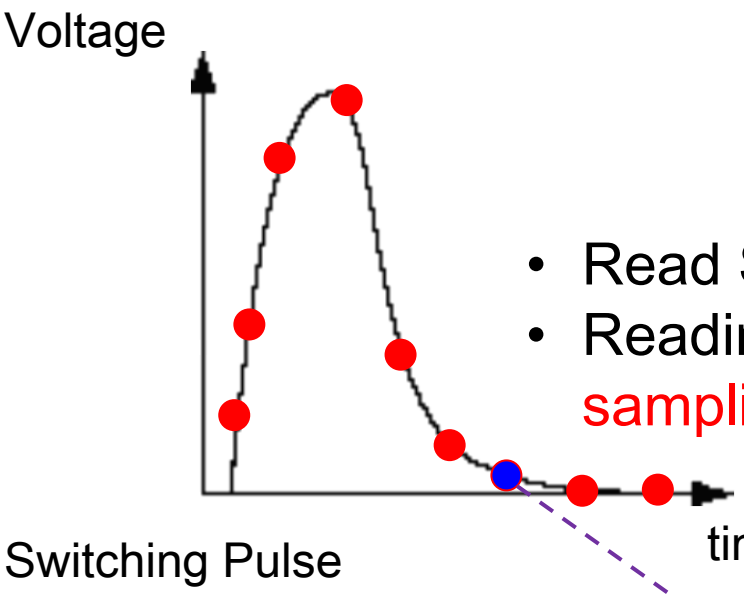


How AMC sample voltage



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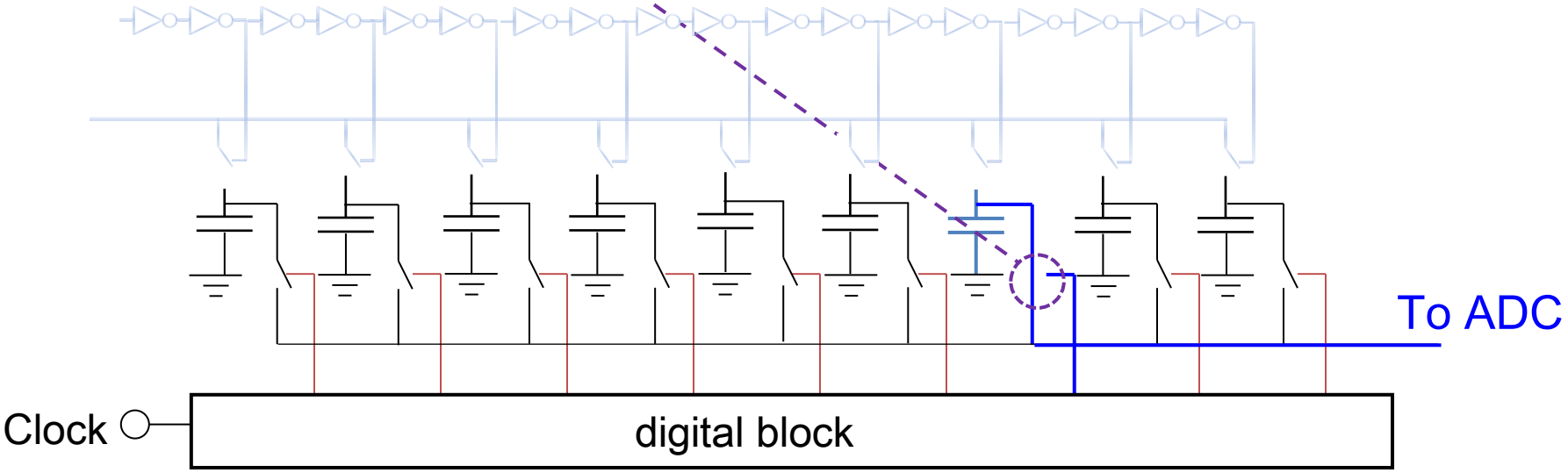
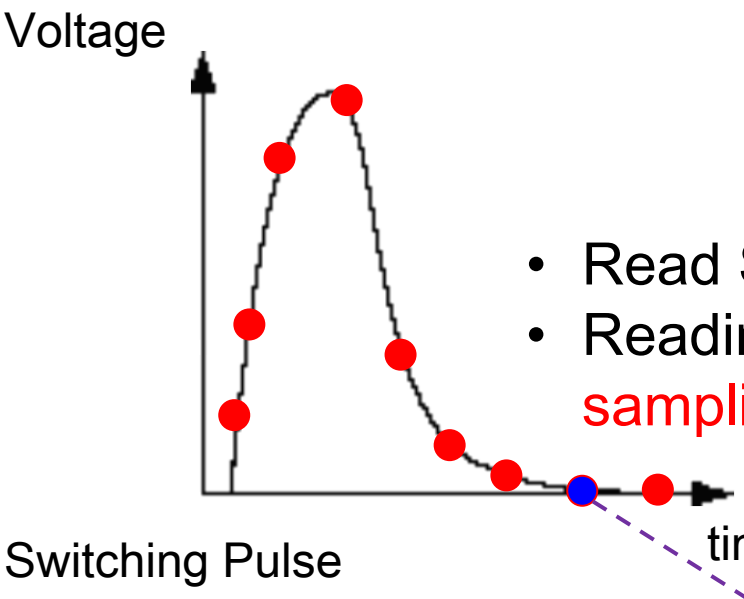


How AMC sample voltage



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②**Reading mode**

- Read SWs are ON 1 by 1 to digitize stored data
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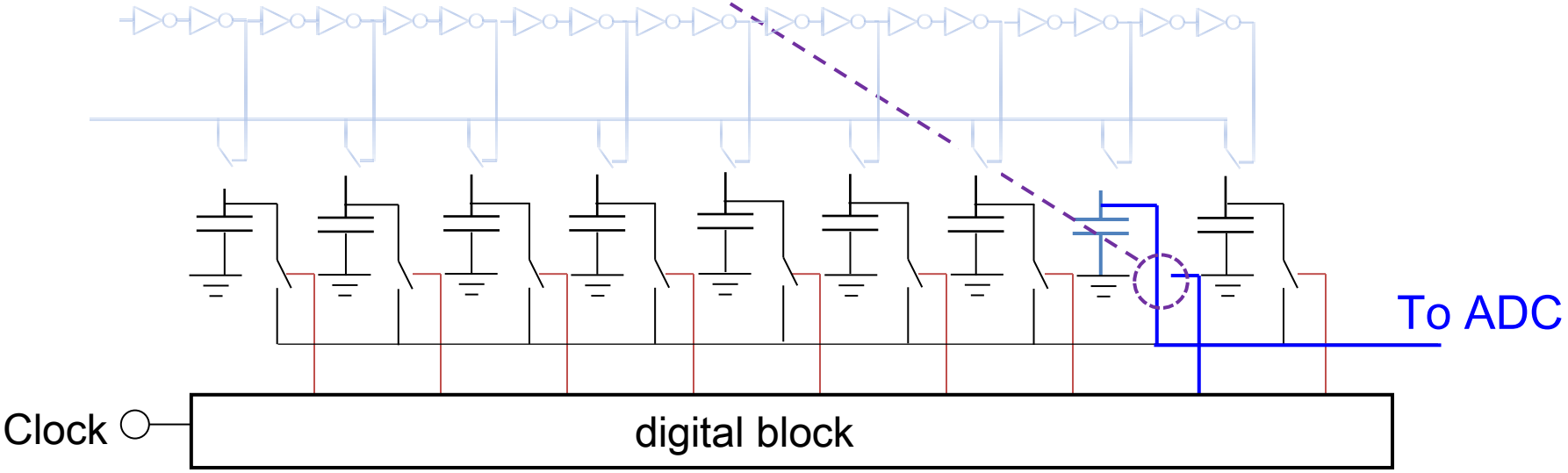
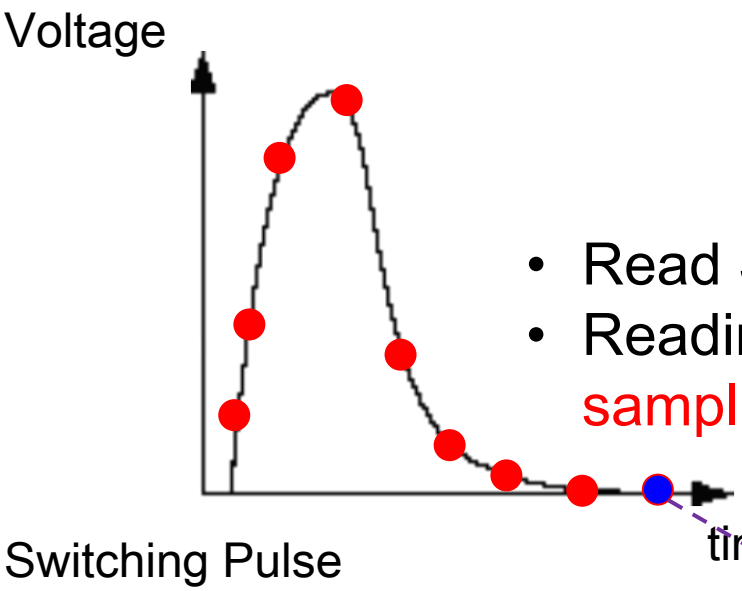


How AMC sample voltage



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- Read SWs are ON 1 by 1 to digitize stored data
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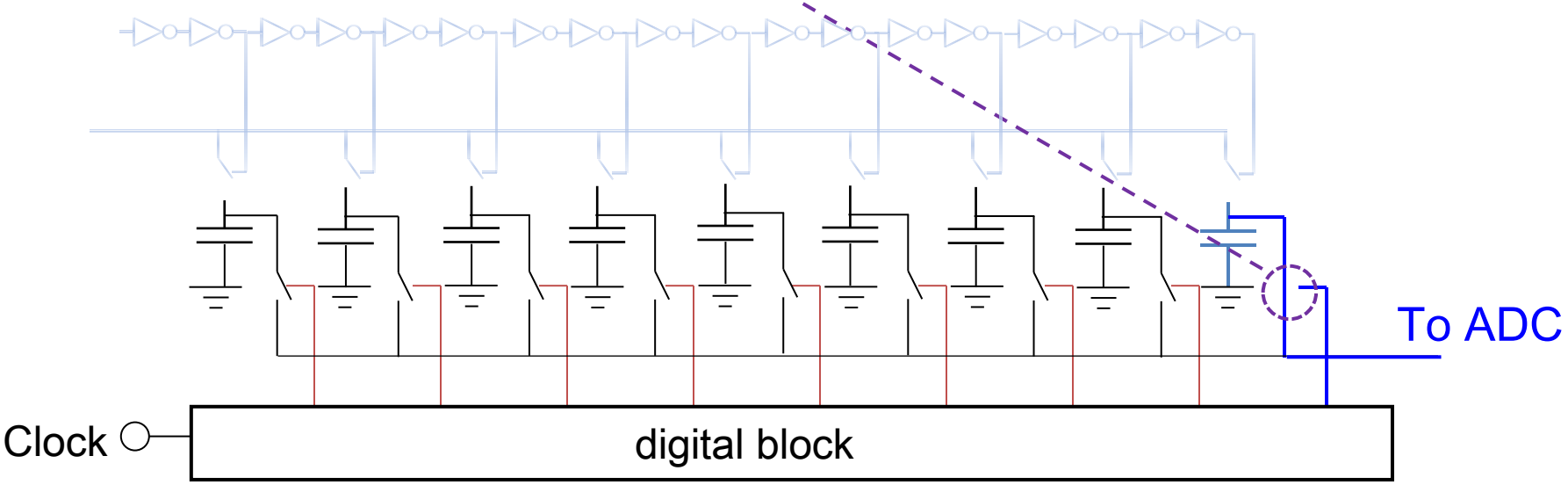
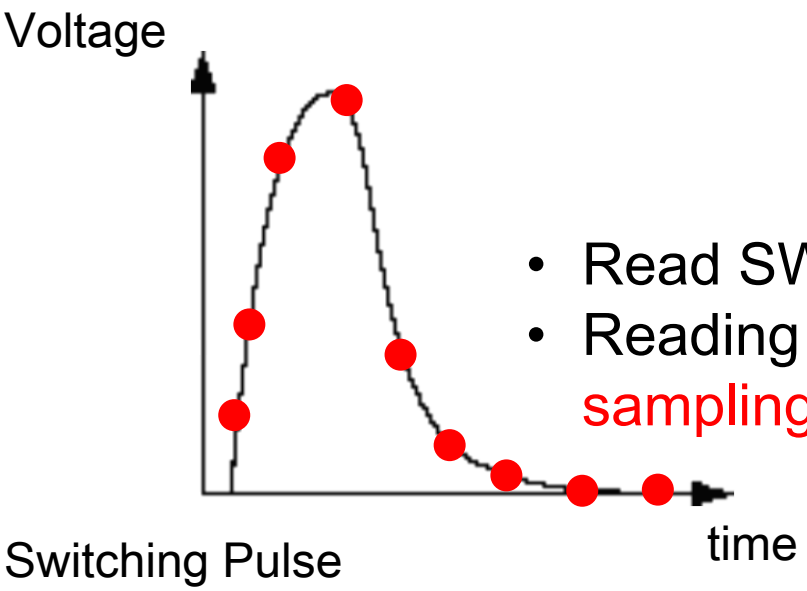


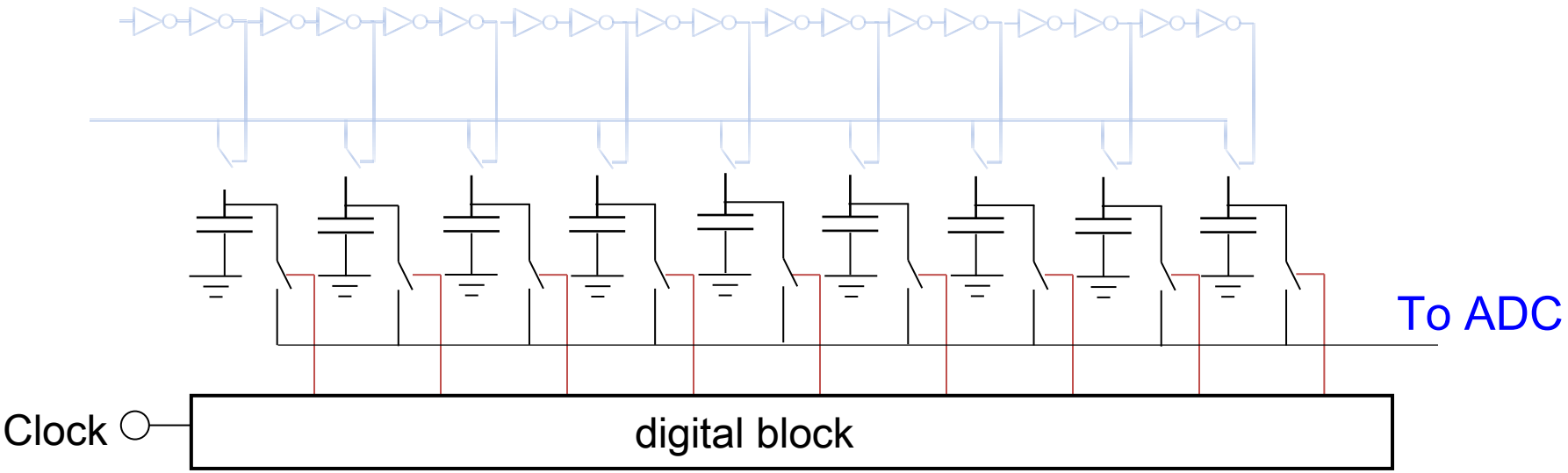
How AMC sample voltage



①Sampling mode
②Reading mode **Finished**

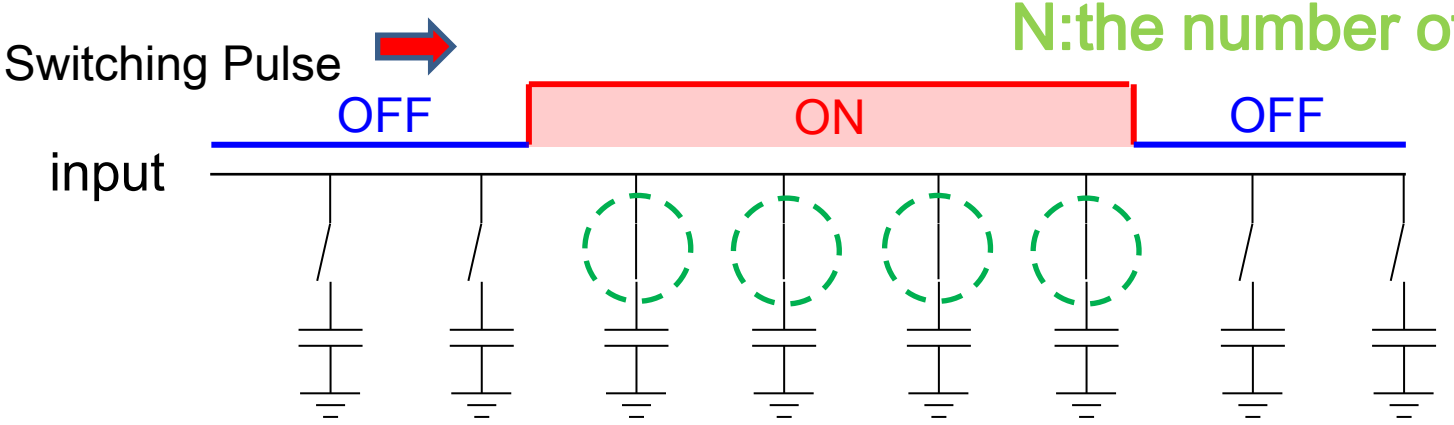
- Read SWs are ON 1 by 1 to digitize stored data
- Reading speed is slowly (<50MHz) than sampling speed (1GHz)

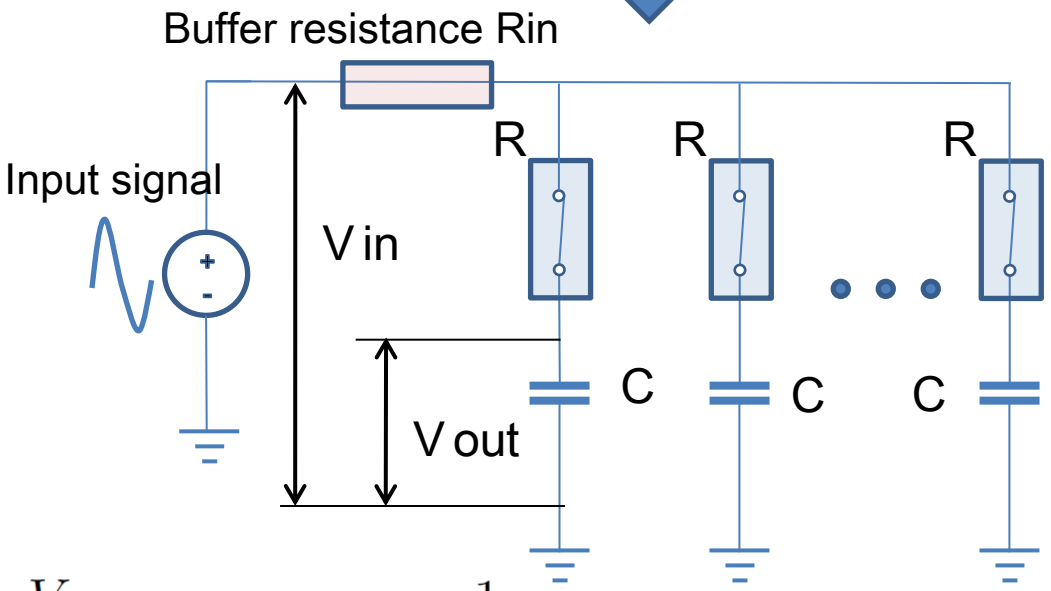
Signal from PMT is digitized



Design ~analog bandwidth~

N:the number of ON switches





$$\frac{V_{out}}{V_{in}} = \frac{1}{1 + j\omega RC + j\omega NCR_{in}}$$

Analog bandwidth : f (-3dB)

$$f = \frac{1}{2\pi(RC + NR_{in}C)}$$

R : SW ON resistance

C : capacitance

R_{in}: resistance of output buffer

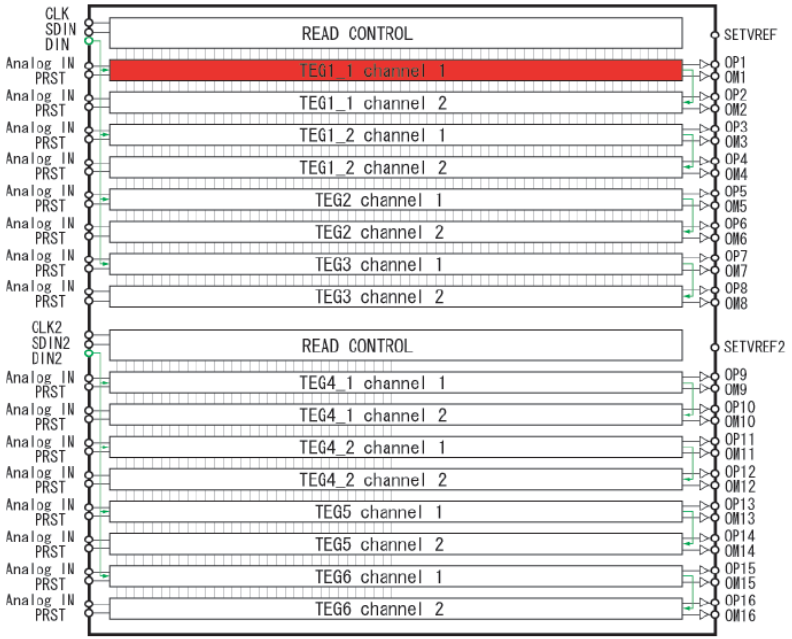
N : the number of ON switches

-keep low N to improve f

Test Element Group(TEG)

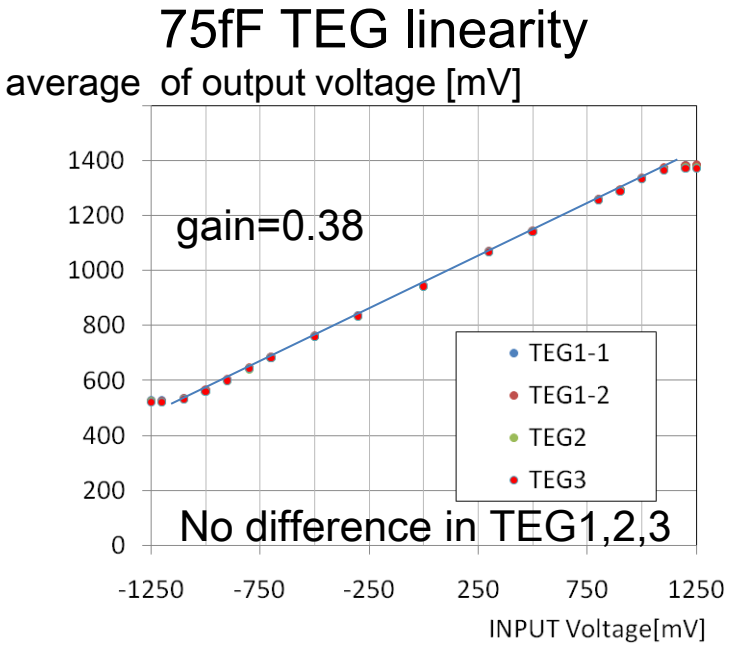
- We Fabricated 6 types Test Element Group as test pieces
- TEGs have different capacitor and architecture

	capacitance	Architecture
TEG1	**75fF**	**Typical**
TEG2		**Symmetry**
TEG3		**Simple**
TEG4	**400fF**	**Typical**
TEG5		**Symmetry**
TEG6		**Simple**

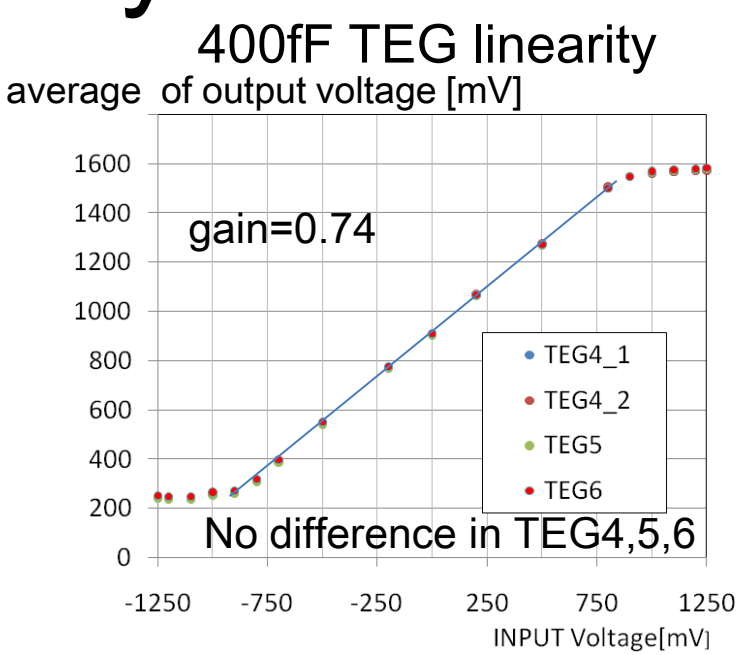


Linearity

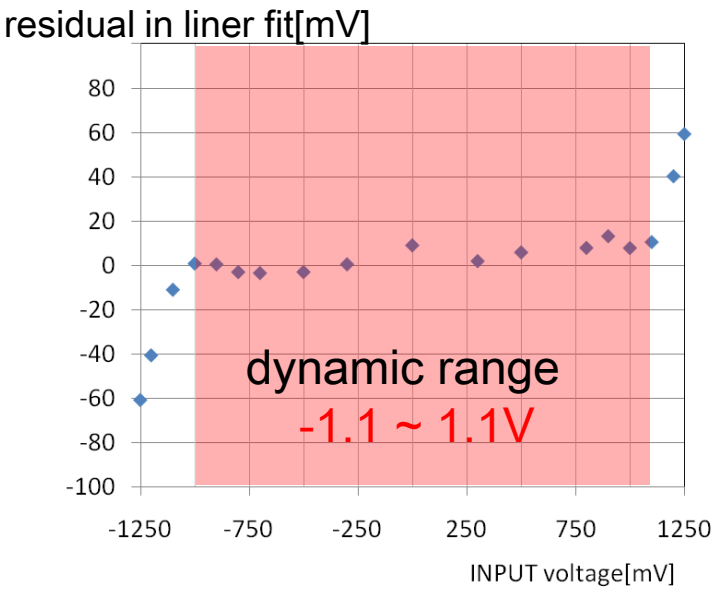
75fF TEG linearity



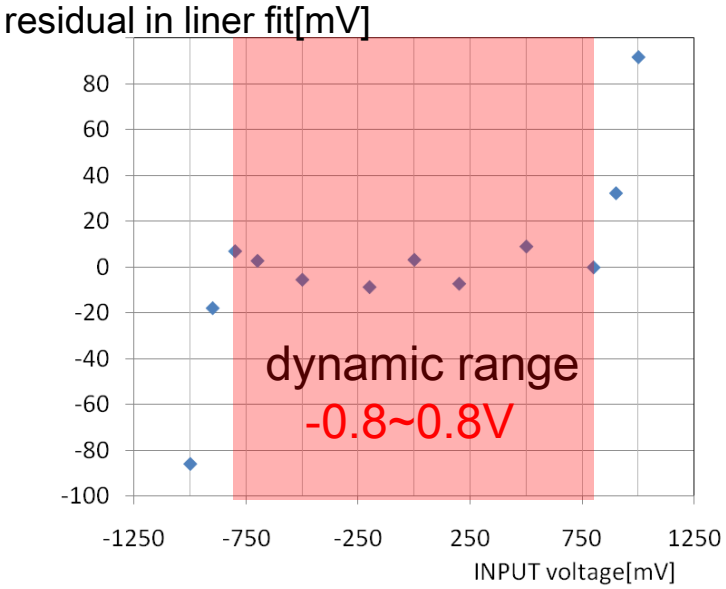
400fF TEG linearity



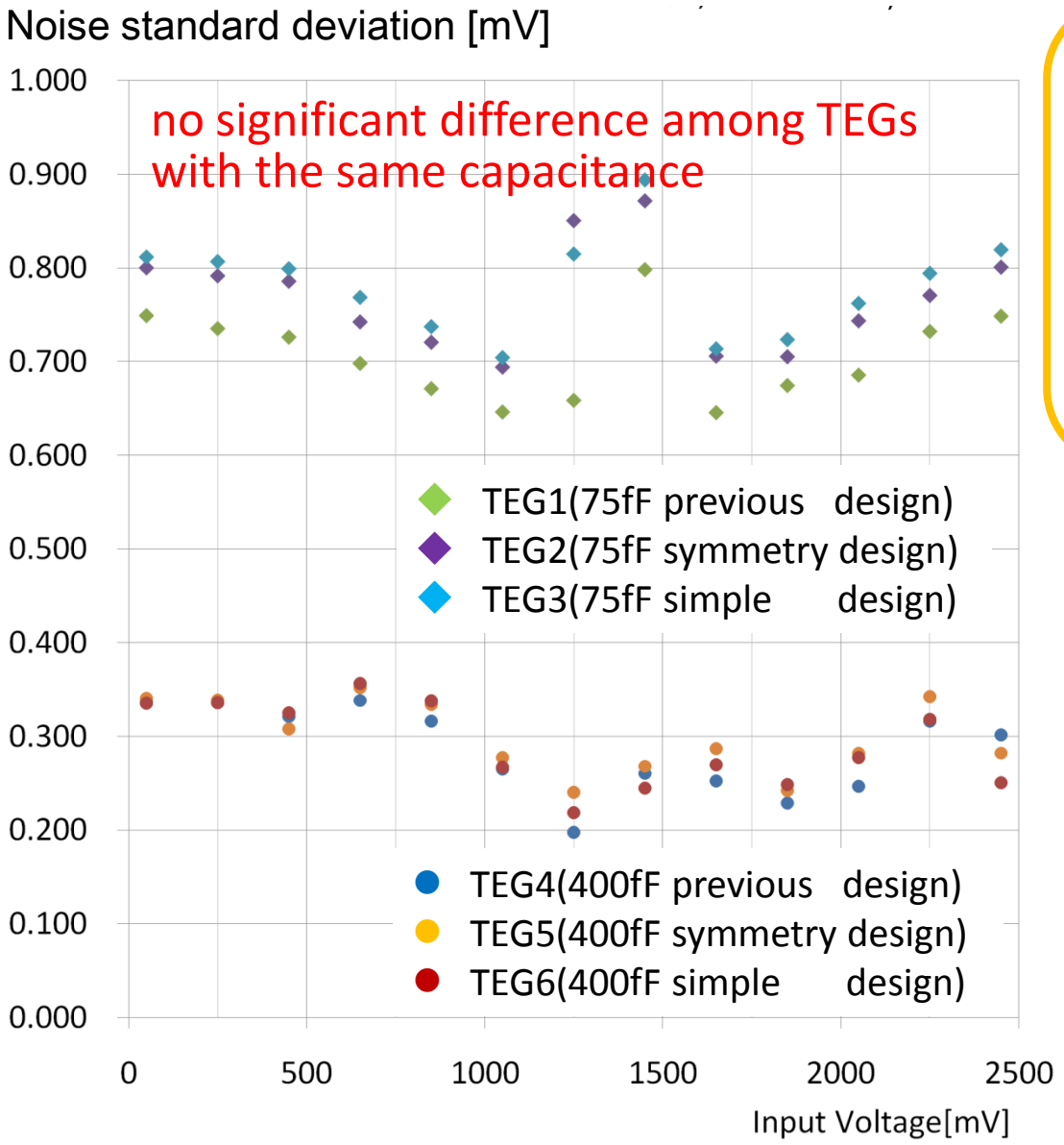
residual in liner fit for75fF TEG



residual in liner fit 400fF TEG



Noise(RMS of measured voltages)



X axis:
input voltage

Y axis:
standard deviation of output voltages in 32 cells for 1000 events with the constant input voltages

Typical noise voltages

σ=0.8mV 75fF TEG1,2,3

σ=0.4mV 400fF TEG4,5,6

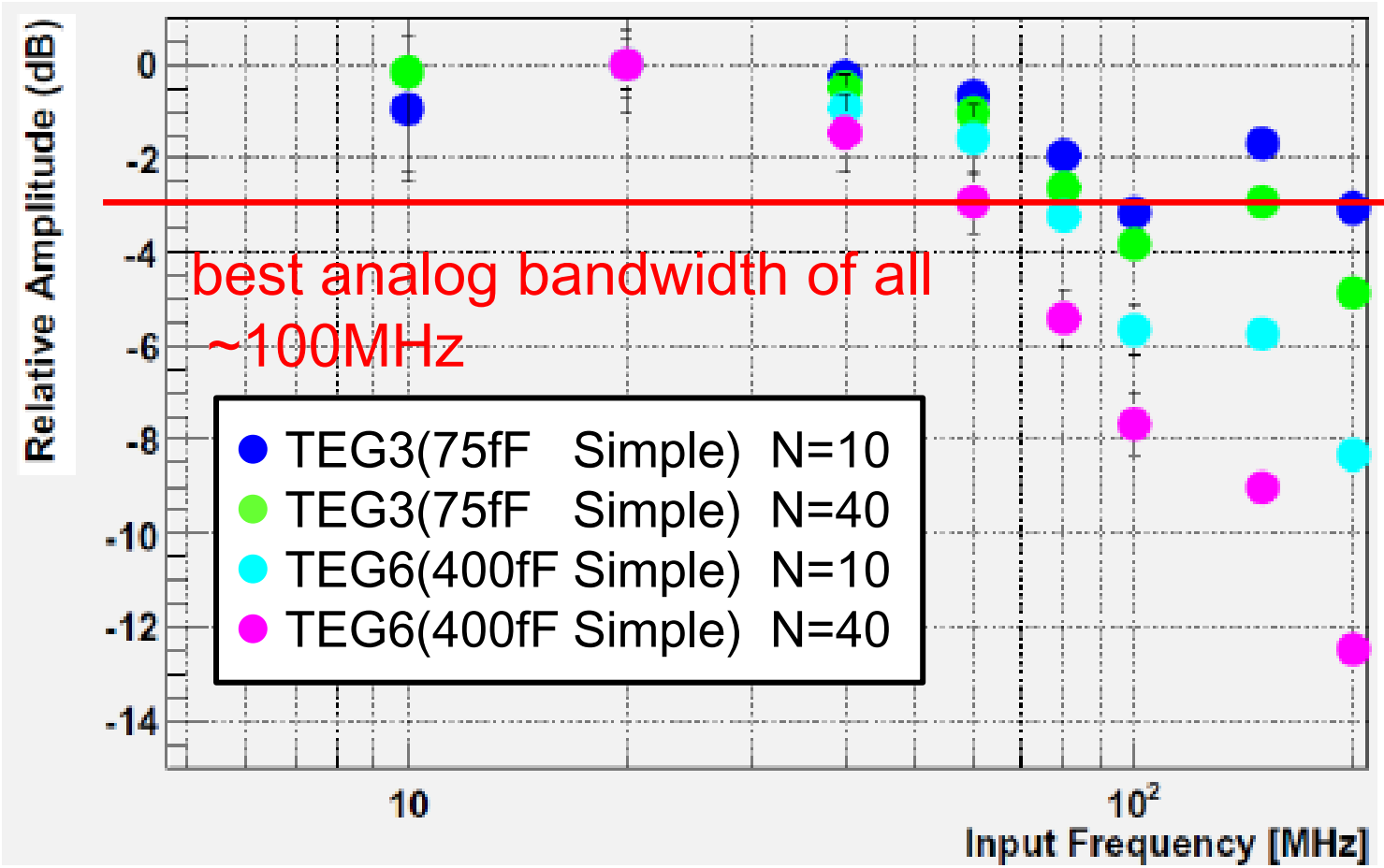
resolution for 75fFTEGs
2.2V/0.8mV~10bits
resolution for 400fFTEGs
1.6V/0.4mV~11bits

Achieve target 10bits!

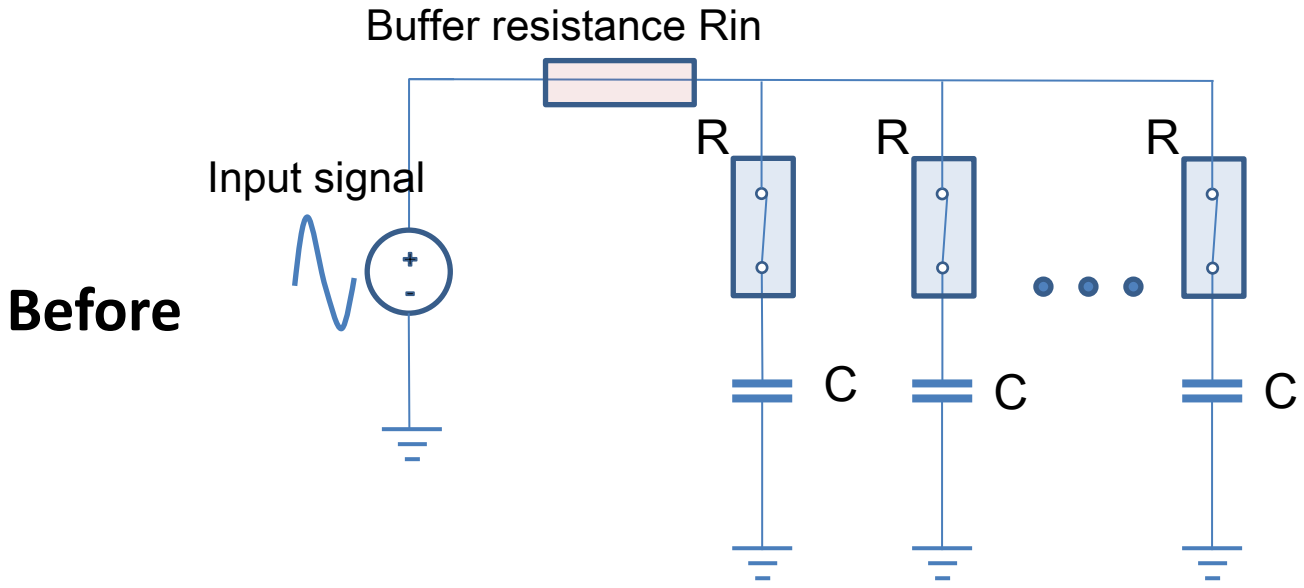
Analog bandwidth

- TEG3 is the best among TEG1~3 ,TEG6 is the best among TEG4~6
  -Simple TEGs show the best analog bandwidth
- The better Analog bandwidth is shown in the operation with the smaller N

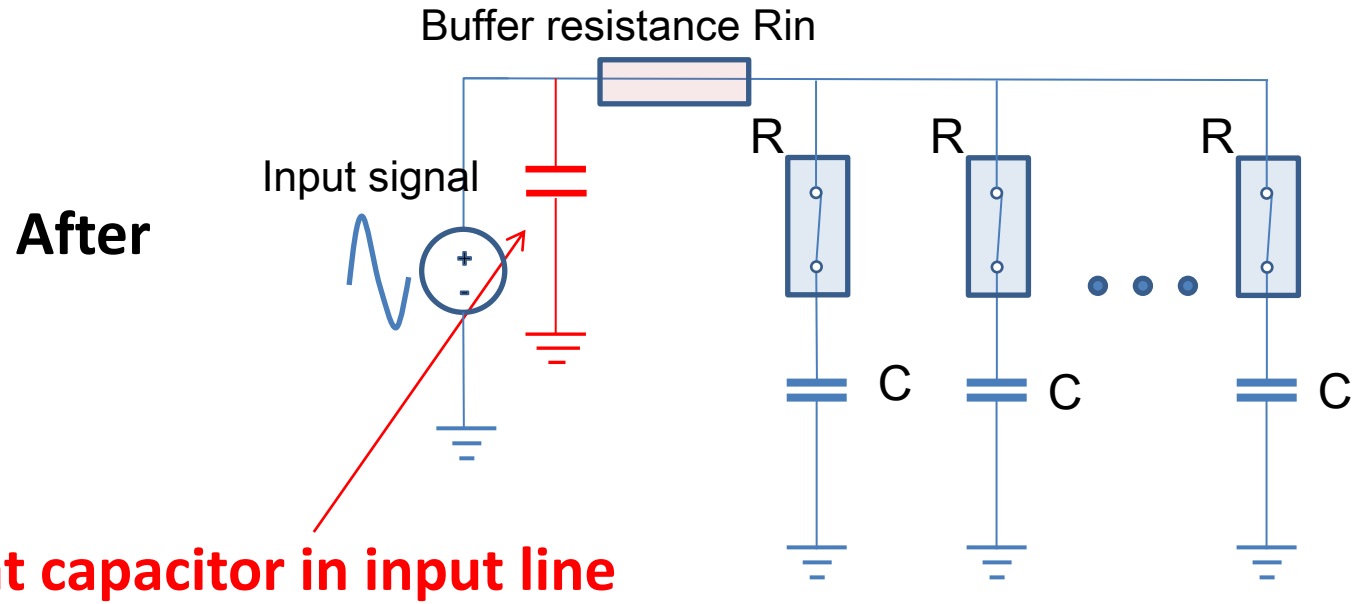
N is the number of ON switches



Simulation of analog bandwidth



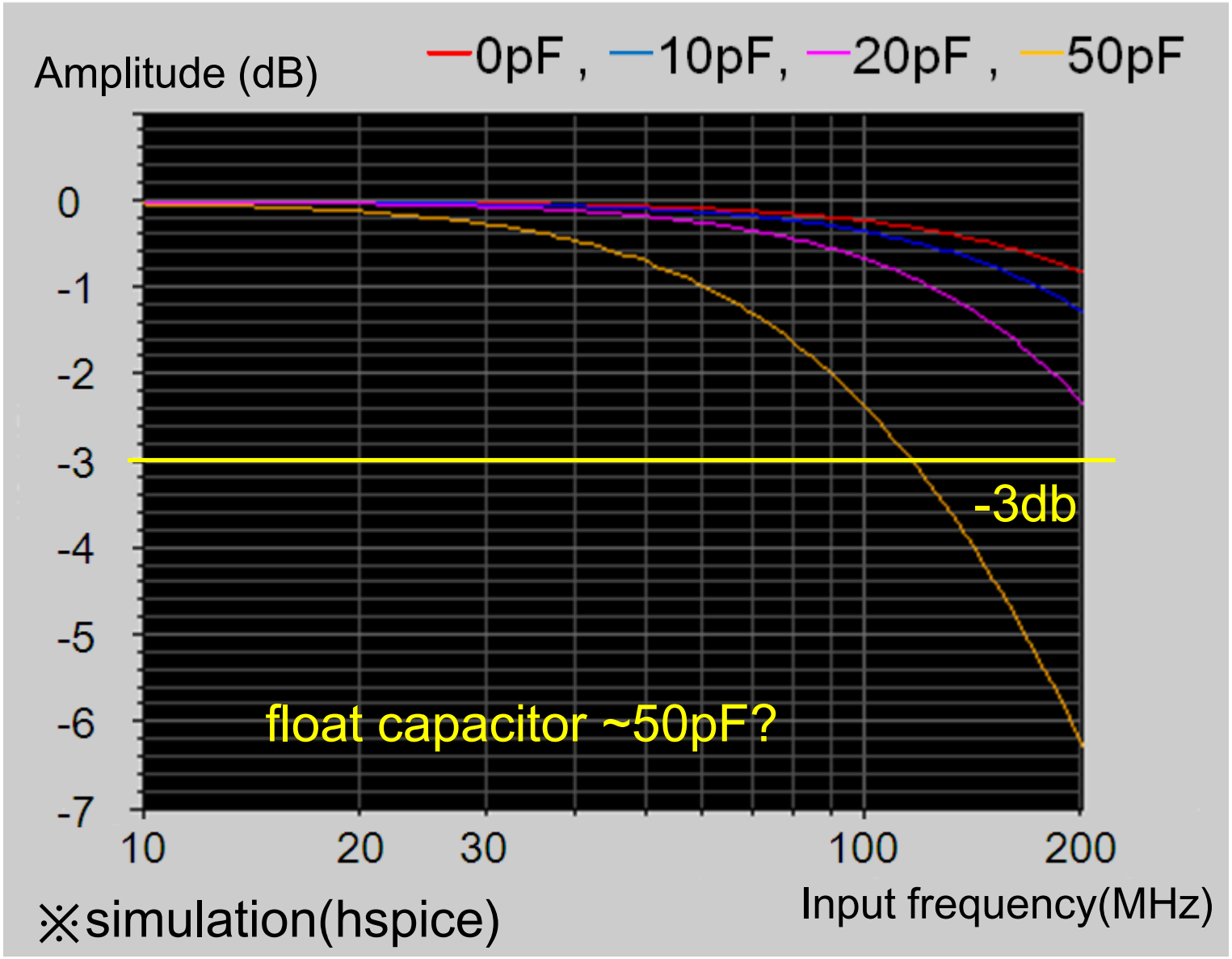
Before



After

float capacitor in input line

Simulation result



※simulation(hspice)

Summary

- AMC contributes to lower threshold energy
- Good results except for analog bandwidth
- Analog bandwidth of 100MHz should be improved
  - extra capacitance and resistance limit analog bandwidth
  - The smaller N gives a better analog bandwidth
- Simple Designs like TEG3 and 6 make analog bandwidth higher

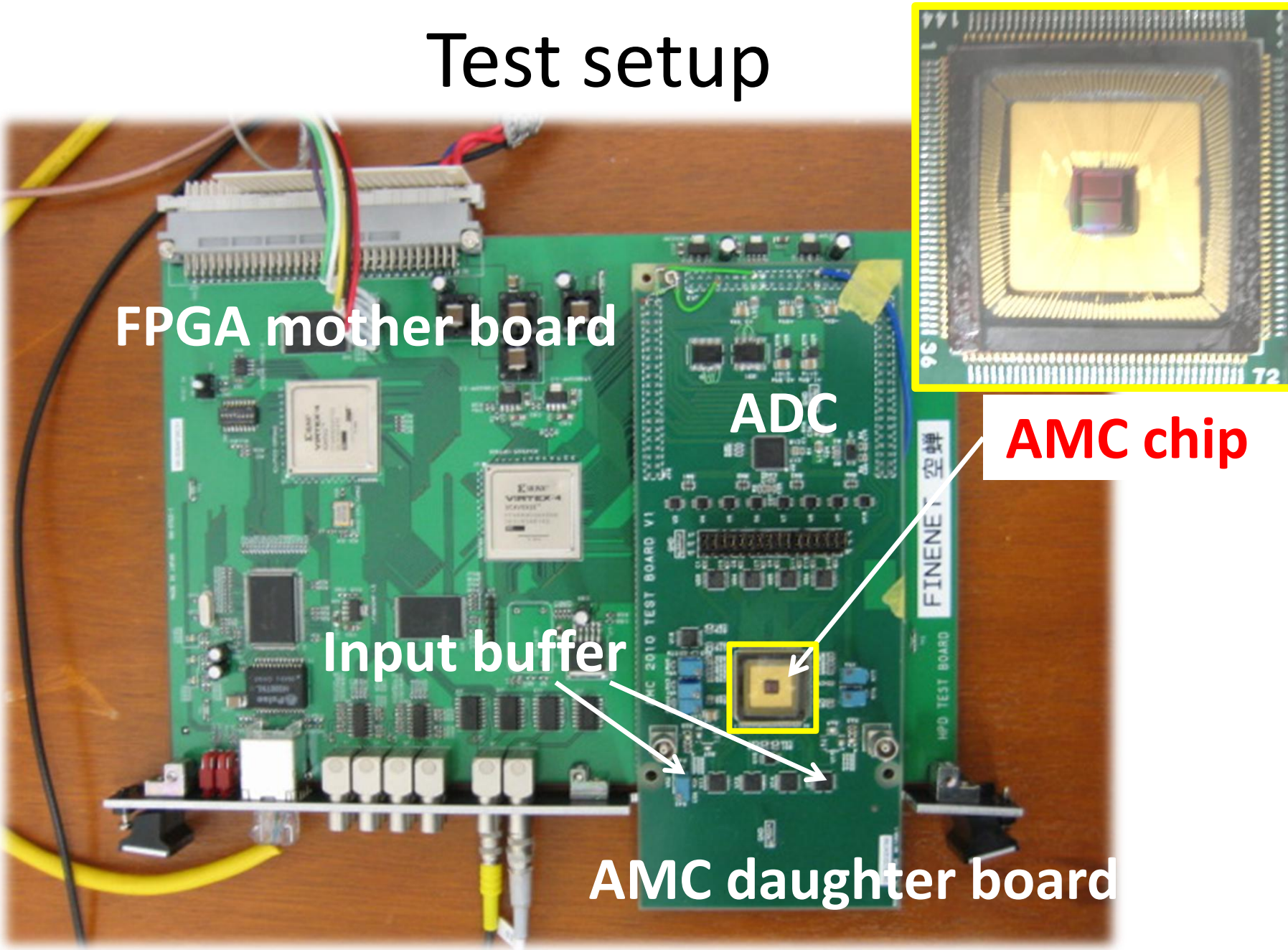
Future plans

- I would like to contribute to design study of CTA and the upgrade of MAGIC, especially to the readout electronics with my experience
- I am also motivated to challenge new hardware developments: advanced photo detector SiPM etc
- This development contribute to achieve better sensitivity in low energy especially to study extra galactic sources and fundamental physics


Thank you for your attention

Back up

Test setup

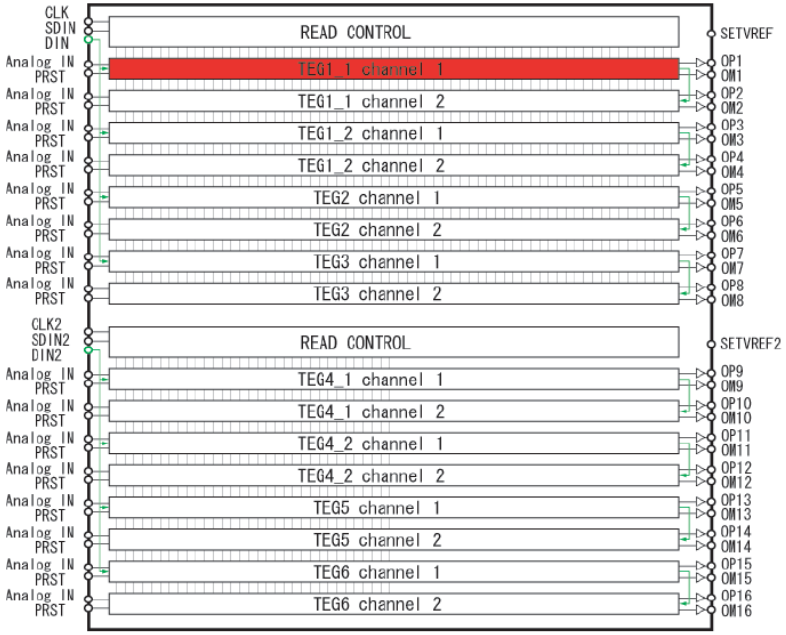

FPGA mother board
ADC
AMC chip
Input buffer
AMC daughter board

Results

		TEG1	TEG2	TEG3	TEG4	TEG5	TEG6
Cell capacitance (fF)		75	75	75	400	400	400
Offset canceling SW		CMOS	CMOS	NMOS	CMOS	CMOS	NMOS
SW formation		Common	1 by 1	1 by 1	Common	1 by 1	1 by 1
Architecture NOTE:		typical	symmetry	simple	typical	symmetry	simple
Switch speed(GHz)		~1	~1	~1	~1	~1	~1
Dynamic range(V)		2.2	2.2	2.2	1.6	1.6	1.6
Linearity(maximum residual) (mV)		15	15	15	10	10	10
Gain		0.38	0.38	0.38	0.74	0.74	0.74
Average of noise(mV)		0.76	0.82	0.84	0.42	0.41	0.42
resolution(bit)		10.1	10.0	10.0	11.4	11.4	11.4
Analog bandwidth (MHz)	N=10	<100	<100	**~100**	<80	<80	**80**

red : clear target spec blue: NOT clear target spec

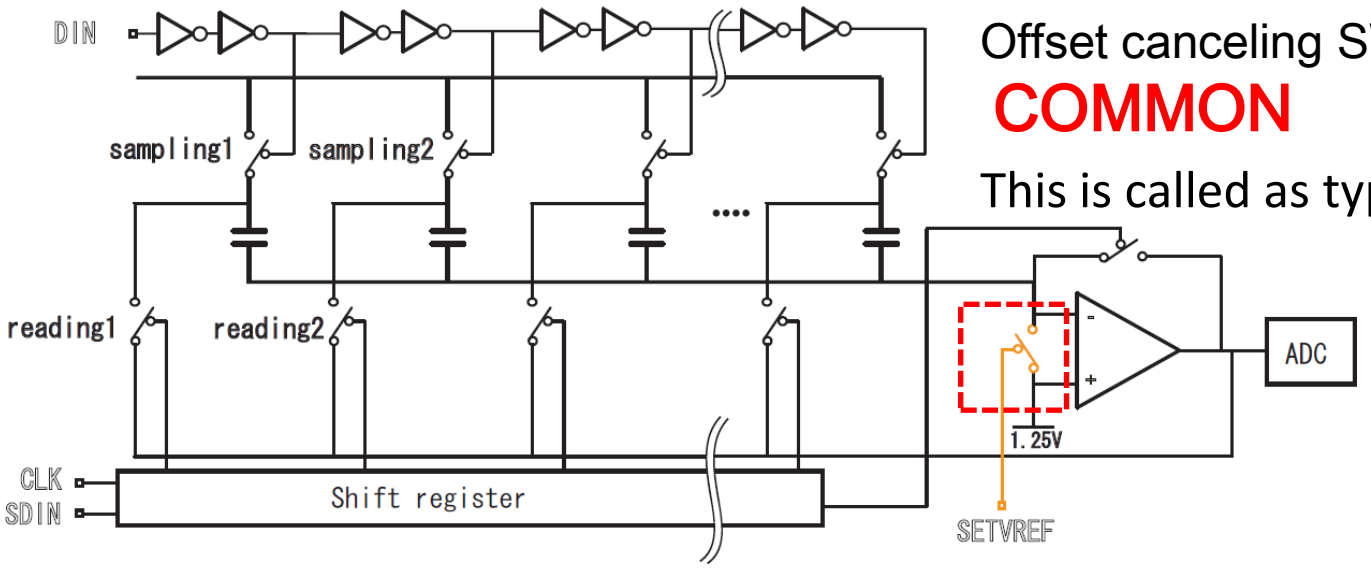
Test Element Group(TEG)



- Fabricated 6 type test element group
  - different capacitor & architecture
- Add to differential system
  - have a clone TEG
  - take a difference between two TEGs
    - -One has a signal with pedestal
    - -The other has a just pedestal for canceling out common noise & offset in chip

	capacitance	Sample SW	Offset canceling SW	Offset canceling SW formation	Cell	Architecture
TEG1	75fF	CMOS	CMOS	Common	128	Typical
TEG2				1 by 1		Symmetry
TEG3			NMOS			Simple
TEG4	400fF		CMOS	Common	64	Typocal
TEG5				1 by 1		Symmetry
TEG6			NMOS			Simple

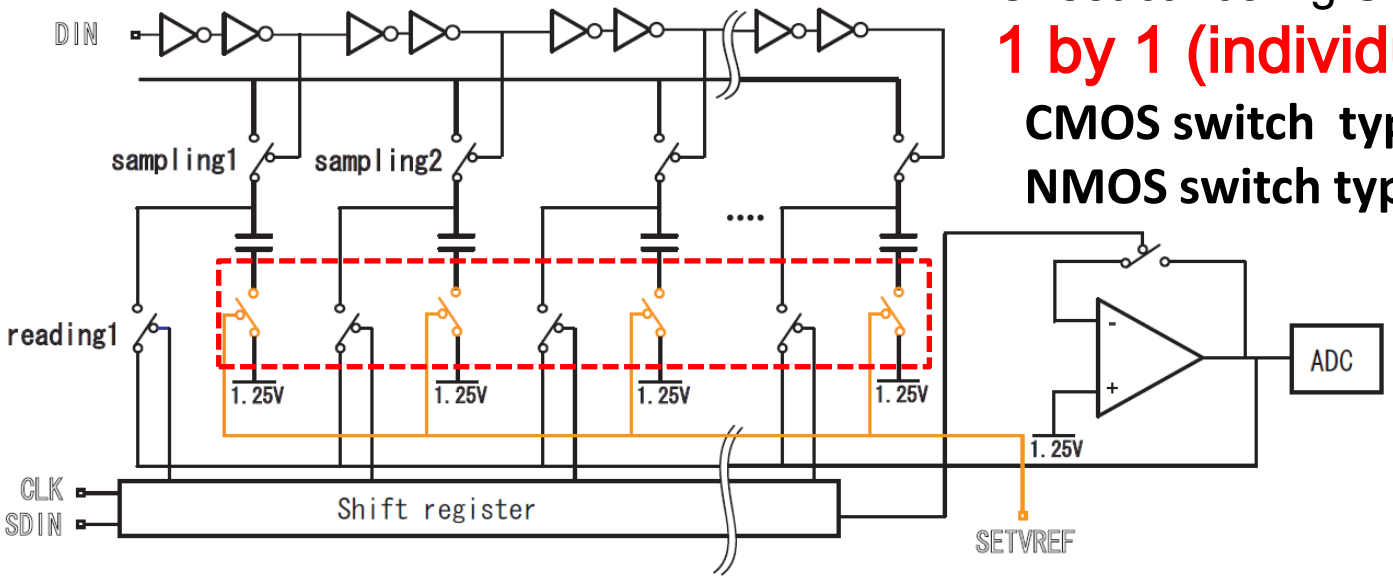
Offset canceling SW formation



Offset canceling SW **formation**

COMMON

This is called as typical.



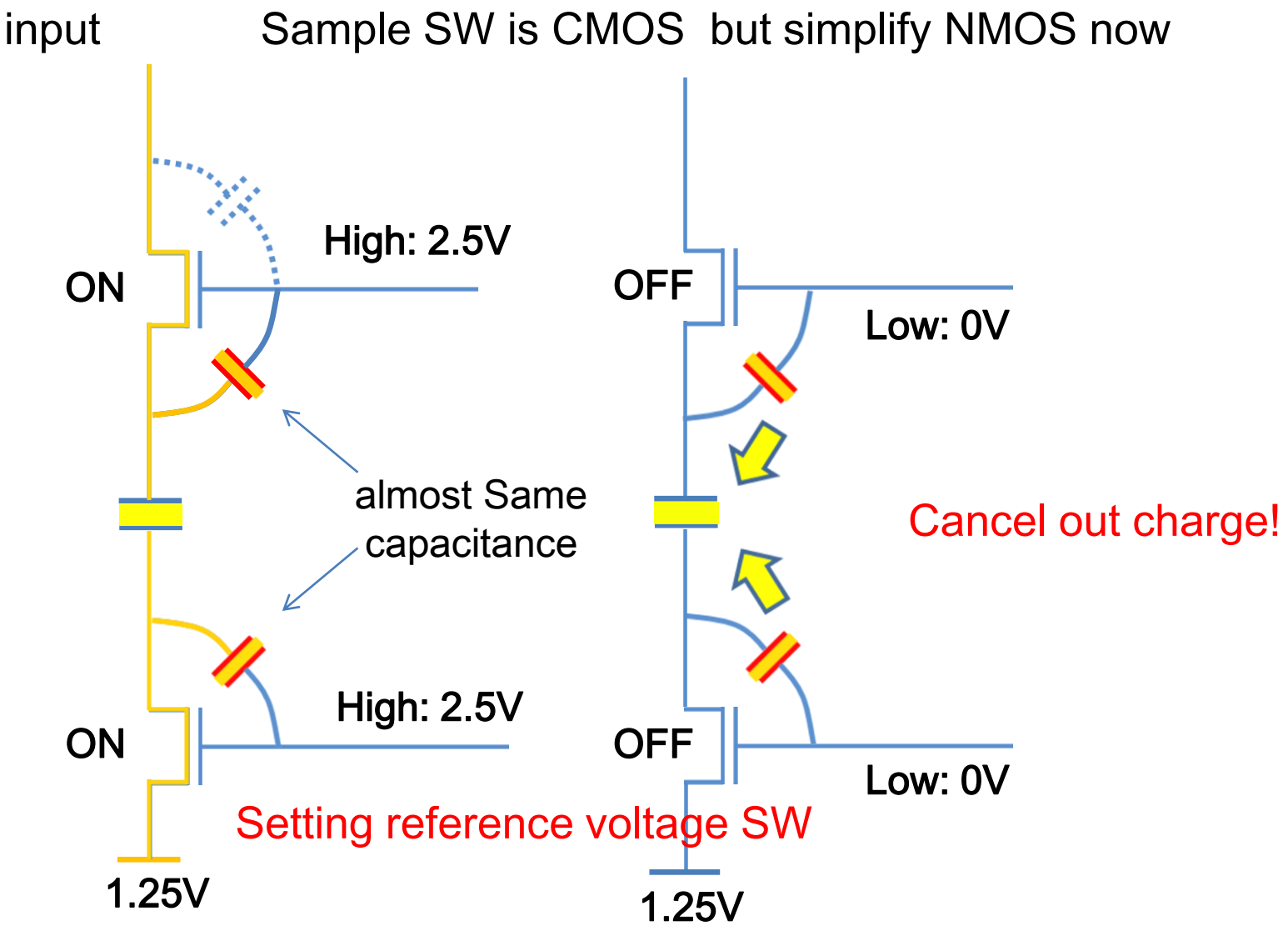
Offset canceling SW **formation**

1 by 1 (individual)

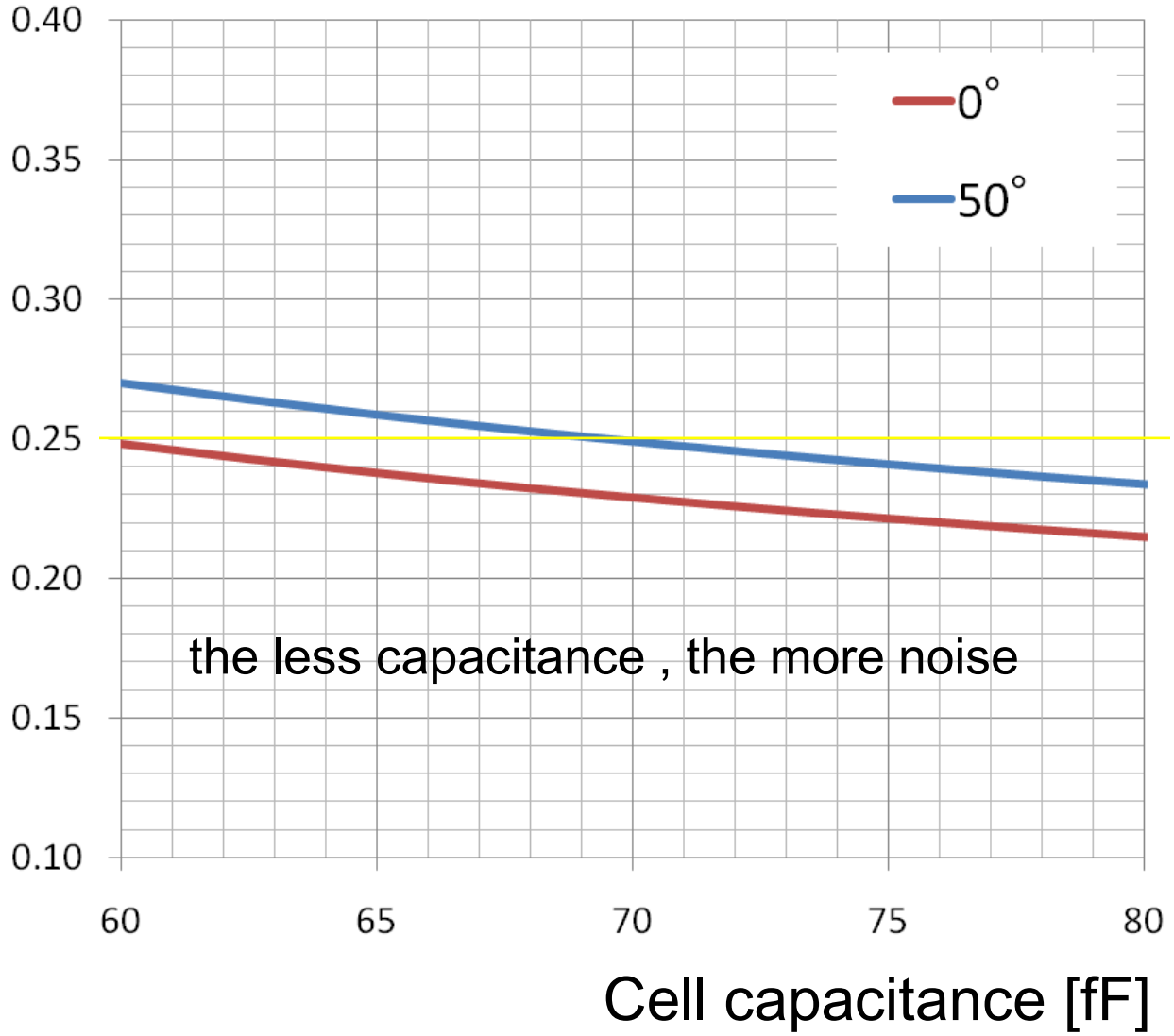
CMOS switch type (symmetric)

NMOS switch type (simple)

Design ~Offset canceling~



Design ~Thermal noise~



$$V_{rms} = \sqrt{\frac{kT}{C}}$$

k:boltzmann constant
C:capacitor
T:temparture

target voltage
Vrms:0.25mV
we safely setting
(dynamic range1V
&12bits)
$1/2^{12}\times$ 1V=0.25mV

select 75fF

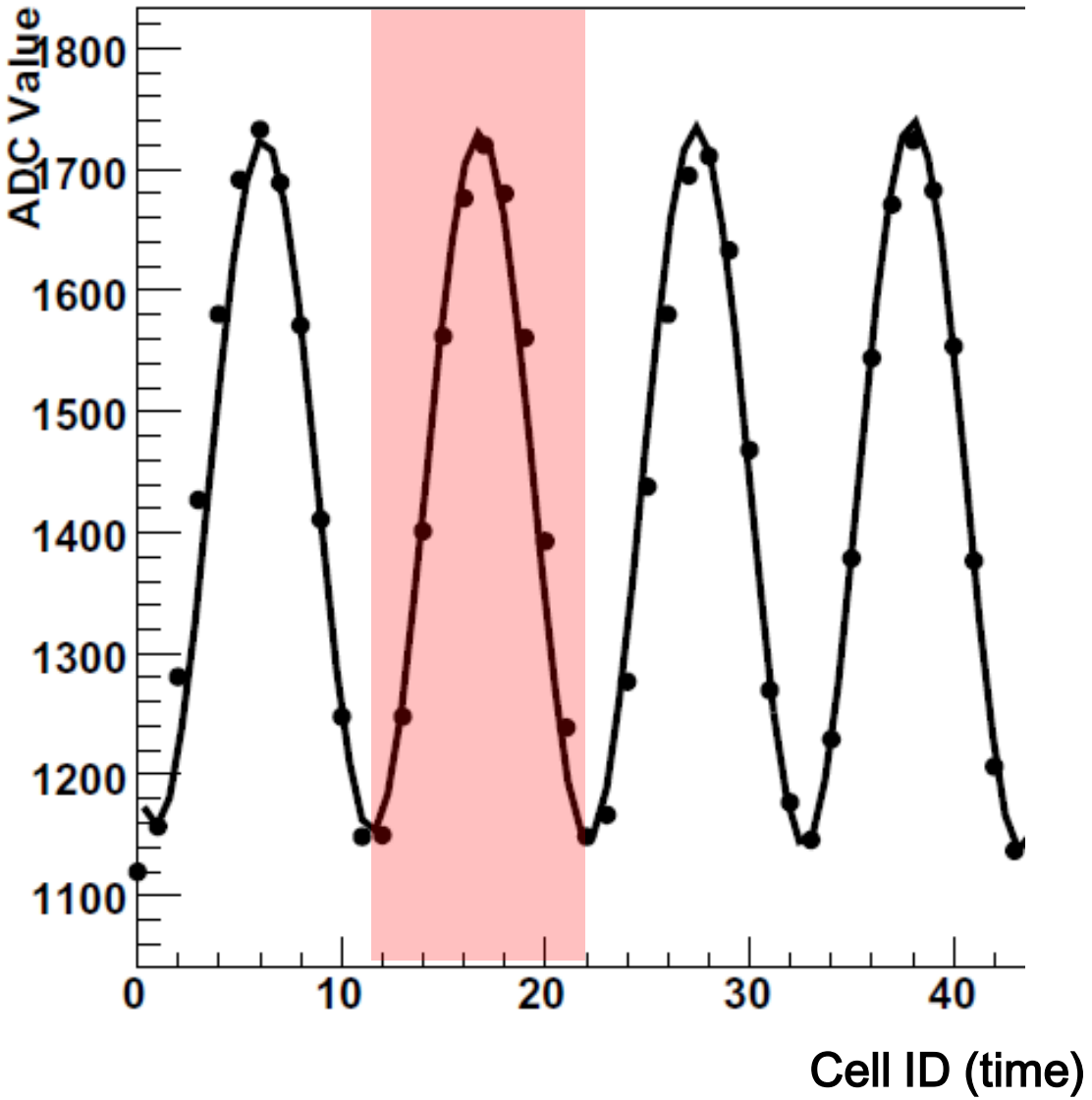
Switching speed

Y axis：ADC count
X axis：Cell ID

Input:100MHz
sinusoidal wave
(period 10nsec)

The number of data
points in 1 cycle
about 10

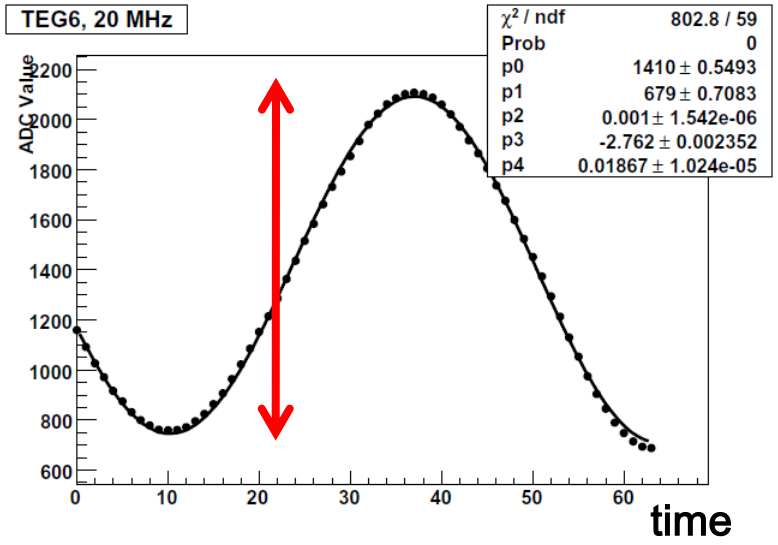
Switching speed
~1GHz

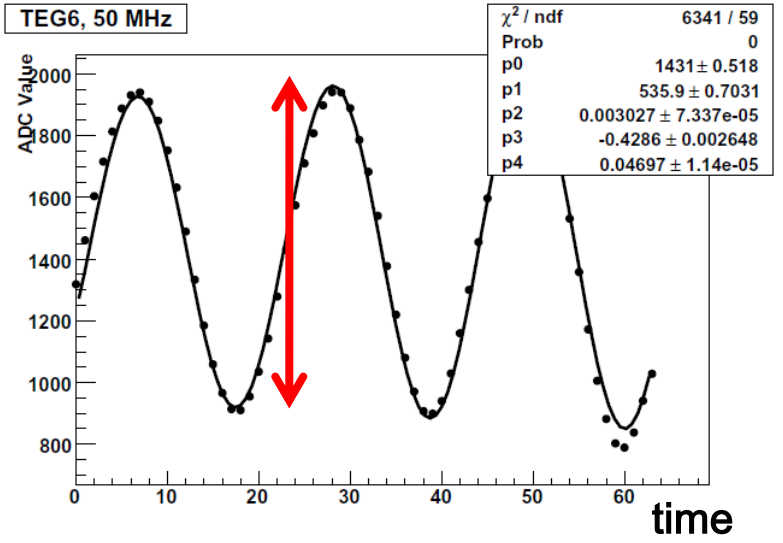


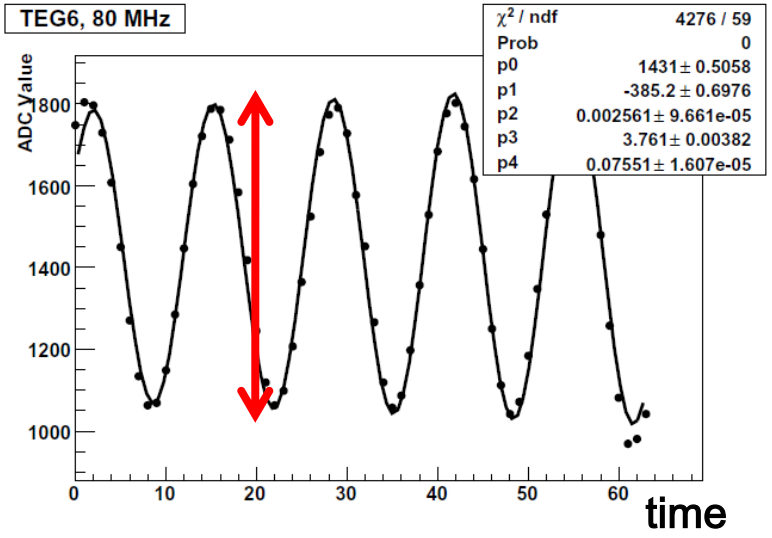
Analysis method analog bandwidth

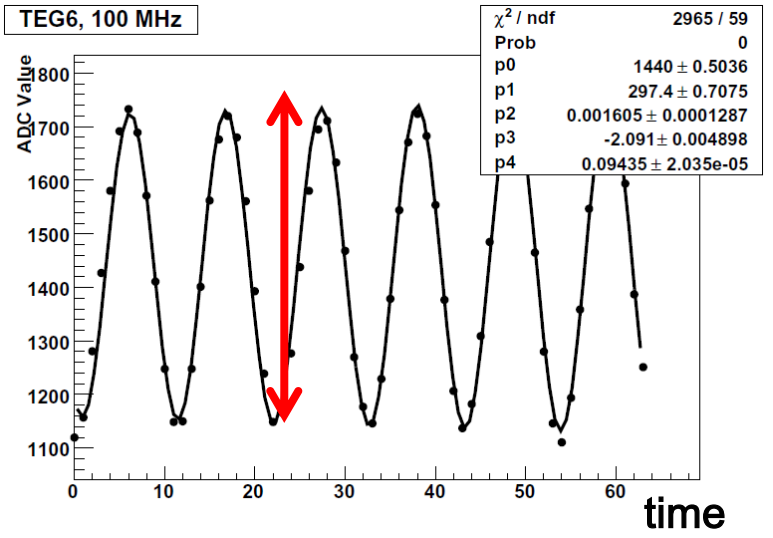
1.Input various frequency wave

2.fitting wave 3.estimate amplitude





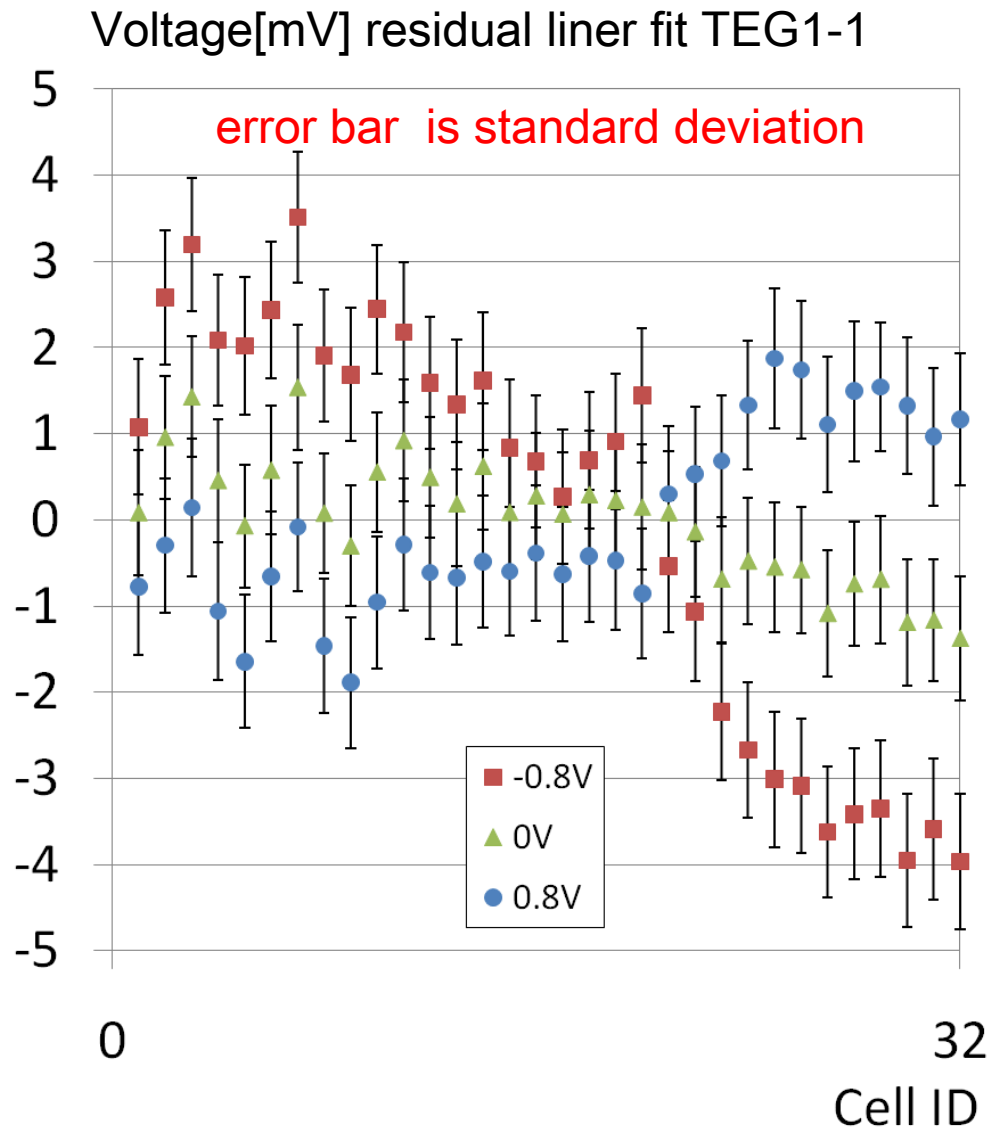




Discussion residual in liner fit

Vertical axis: residual liner fit cell by cell

Horizontal axis: cell ID



different by in put voltage & cell

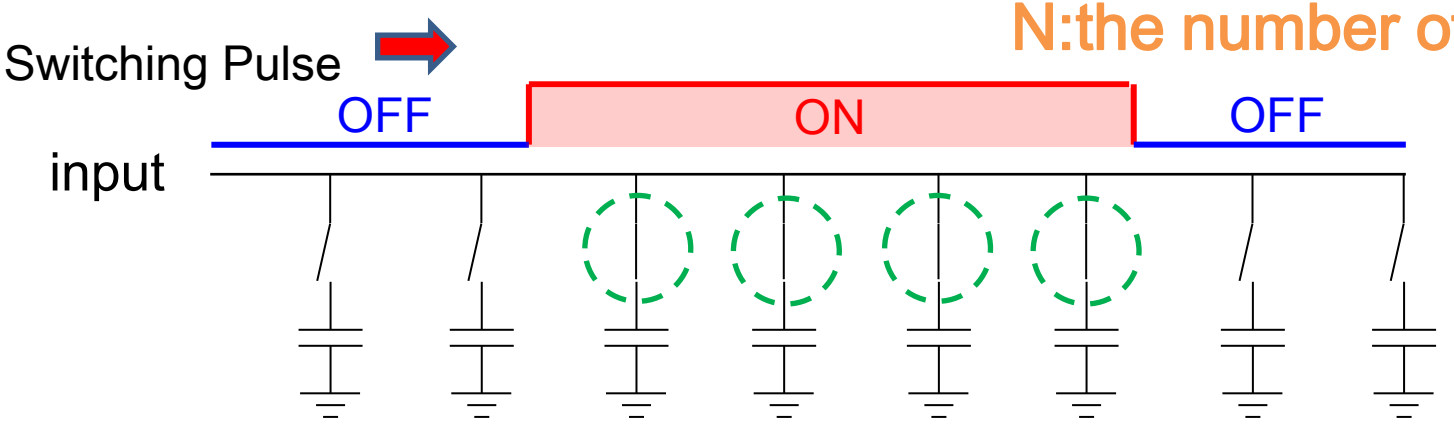
but error bar is not almost different!

We need to know residual by cell & input voltage

Temperature depends on residual? (will check when I come back Japan)

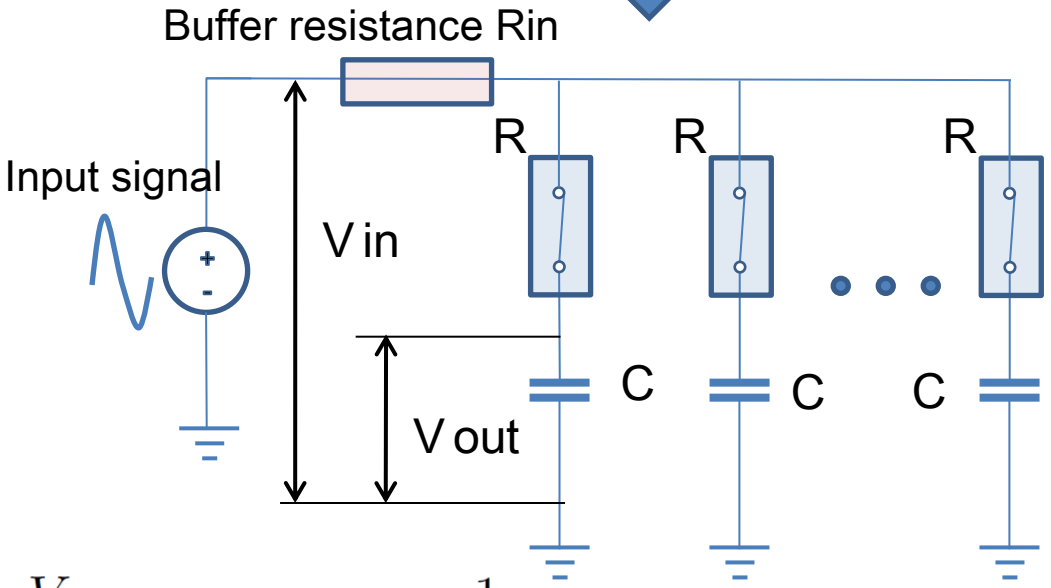
Design ~analog bandwidth~

N:the number of ON switches



Analog bandwidth : f (-3dB)

$$f = \frac{1}{2\pi(RC + NR_{in}C)}$$



$$\frac{V_{out}}{V_{in}} = \frac{1}{1 + j\omega RC + j\omega NCR_{in}}$$

R : SW ON resistance
~2000 Ω

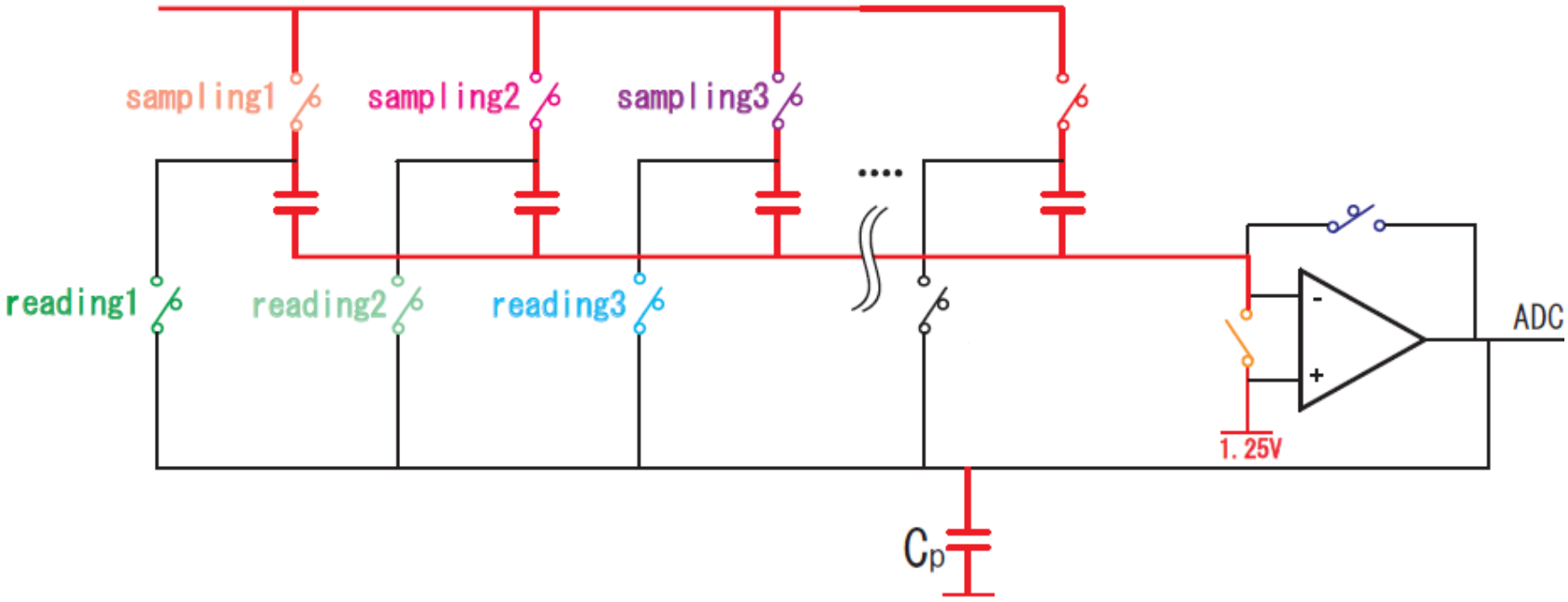
C : capacitance
60~1000fF

R_{in}: resistance of output buffer
~200 Ω

N : the number of ON switches

-keep low N to improve f

Difference of gain



AMC Power consumption

	Power consumption (mW)
AMC+AMC test board +FPGA(reading board)	10400
FPGA(reading board)	7490
AMC+AMC test board	2910

※AMC test board including input buffers(*8) & ADC power consumption

Target specification

AMC processed by 0.25μm technology

- charge resolution (10 bits)
- Sampling speed (1 GHz)
- Analog bandwidth (300 MHz)
  - enough to record original shapes of Cherenkov light signals

We can estimate light of shower correctly