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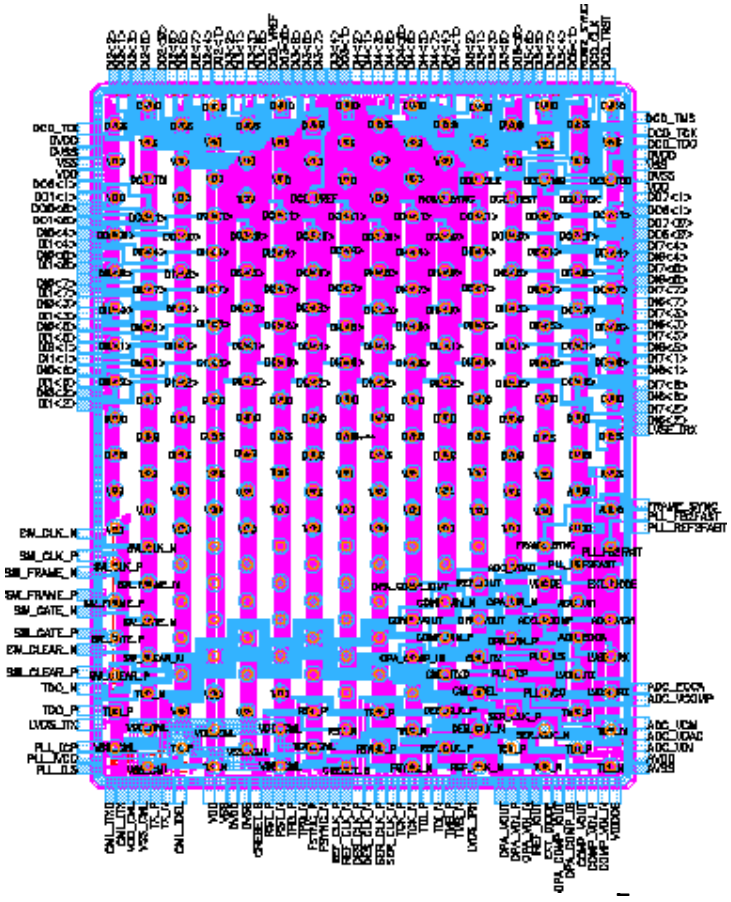
Technology Options for DHP Development

Current Situation

- MOSIS has stopped to offer IBM 90nm (CMS9SF and CMS9RF/LP) MPW runs
- Taxi runs (Engineering runs) are still available at $600-700k per run
- Mai 31st MPW is the last IBM MPW run

➔ This last MPW run will be used to submit the DHP0.2



Technology – Node Size

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- 90nm
  - Vendors: TSMC (MOSIS, Europractice), UMC (Europractice)
  - Worked fine for DHP 0.1 (digital density, high speed link and analog support)

- 65nm
  - Vendors: TSMC (MOSIS, Europractice), UMC (Europractice), IBM/GF (MOSIS)
  - Currently evaluated for LHC & SLHC upgrade developments (TSMC @ CERN)
  - Core voltage (1.2V) as 90nm
  - Could make chip smaller and/or add more buffers
  - Analog design my be more challenging (matching)

Technology – Vendor Choice

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- 65nm (via Europractice)

	UMC	TSMC
mini@asic (3.5mm^2, max. 2 blocks)	2 per year 8k (10k) per block	2 per year 16k (18k) per block
MPW runs	4 per year 45k per 16mm^2 min. size	2 per month (!) 50k for 13 mm^2
C4 bumping	Third vendor (as with 180nm)	From fab, 10k per run (100 samples)
IP avilability	? (ARM standard cells)	Currently being evaluated (ARM, DDR kit: PLL, area IO...)

Prices in EUR

GF (GlobalFoundries, MOSIS) may be an option (compatible to IBM 65nm) but run schedule not known yet

For comparison: DHP 0.2 (13mm^2) in IBM 90nm: 56k + 7k for bumping