Vertical Integration Technology for the ATLAS Pixel Upgrades

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In collaboration with

Fraunhofer
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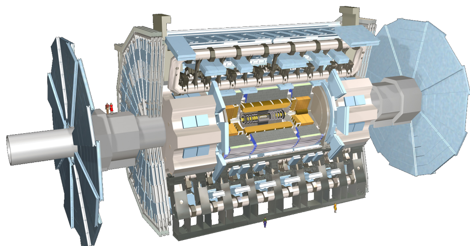
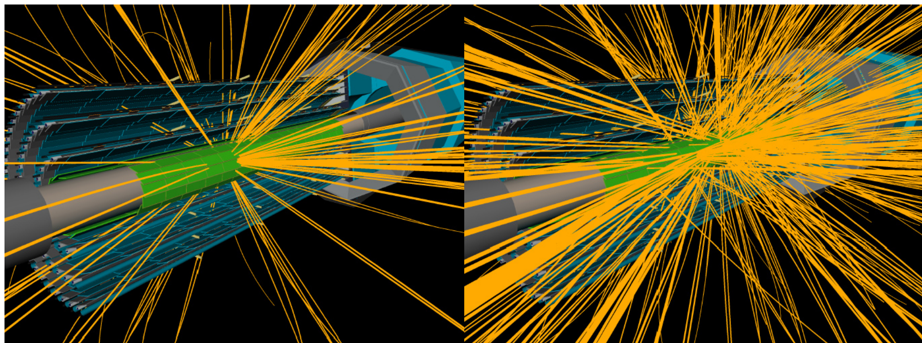


Motivation & Concept

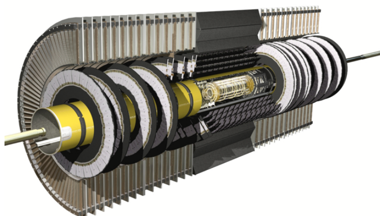
Tracking in a High Luminosity Environment



An increase of the LHC luminosity by a factor of 10 or even 100 leads to challenges for the tracking.

- Denser bunches ⇒ more interactions per bunch crossing
- More bunches ⇒ more remnants for earlier bunch crossings

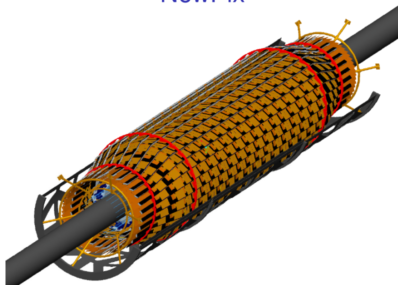
Future of ATLAS and LHC



Keystones for upgrade

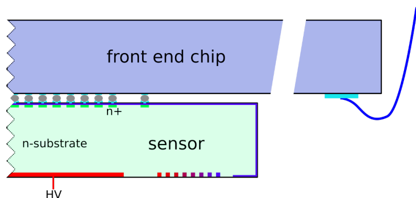
- Twofold Upgrade:
  - Insertable **B-L**ayer ∼2013/4
  - HL-HC/NewPix ∼2018 (Under discussion)
- Luminosity: $(2-3)\cdot 10^{34} - 10^{35}/(\mathrm{cm}^2\mathrm{s})$
- ⇒ radiation dose:
  $\phi_{\mathrm{eq}} \approx 10^{15} - 10^{16}\,\mathrm{n_{eq}}/\mathrm{cm}^2$
- Reduce pixel size to improve on resolution.

NewPix

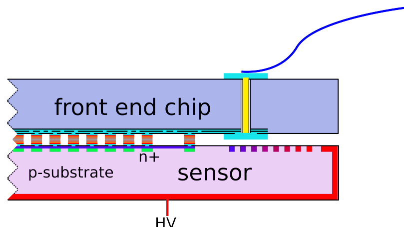


Our Pixel Module Concept

Present design



Thin sensors + ICV-SLID



Four new technologies

- N-in-p bulk material
- Thin sensors (MPP-HLL process)
- SLID: Solid Liquid Inter-Diffusion
- ICV: Inter-Chip-Vias

Advantages of thin sensors + ICV-SLID

- Higher signals after irradiation
- Less multiple scattering
- More compact: „balcony“ for signal-extraction not needed
- Enlargement of active area
- Allows for vertical integration/separation of analogue and digital parts

SLID: Solid Liquid Inter-Diffusion

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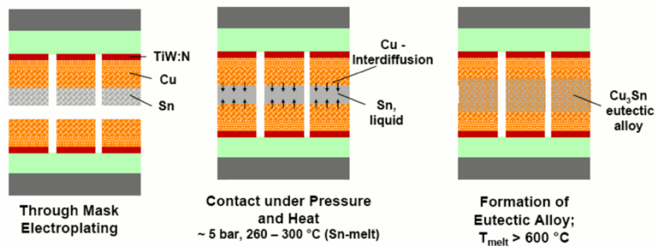
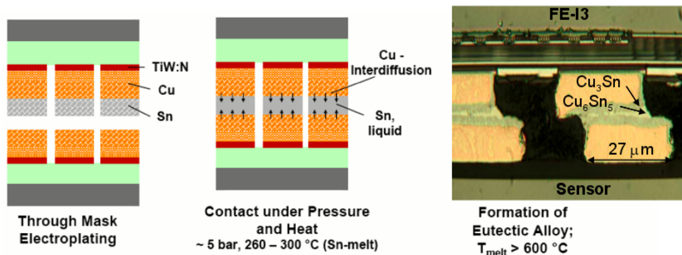


- Alternative to bump bonding (less process steps → lower cost).
- Arbitrary geometries possible, especially smaller pitches.
- Allows for vertical integration (Melting point of Cu_3Sn higher than of Sn).
- Wafer to wafer and chip to wafer possible.

SLID: Solid Liquid Inter-Diffusion



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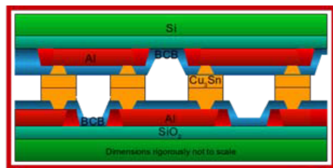
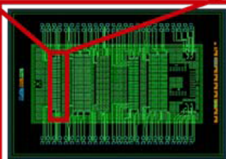
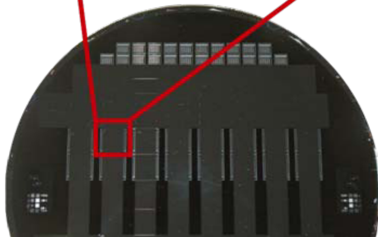
Daisy Chains: Wafer-to-Wafer SLID





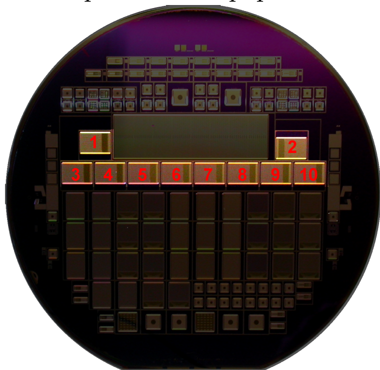


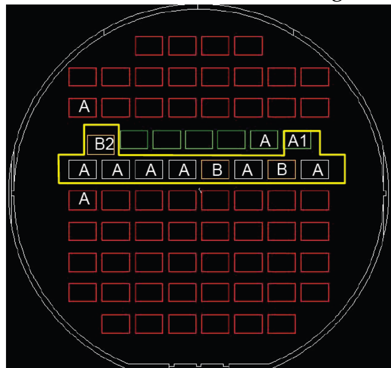
- Aim: Determine the feasibility of the SLID interconnection within the parameters needed for ATLAS pixels.
- Deliberate aplanarity were introduced to study the sensibility $\rightarrow$ Up to 1 μm aplanarities do not affect efficiency.
- SLID efficiencies measured with daisy chains structures (wafer to wafer connections): For ATLAS geometry inefficiency is $(5 \pm 1) \times 10^{-4}$

Chip to Wafer Interconnection

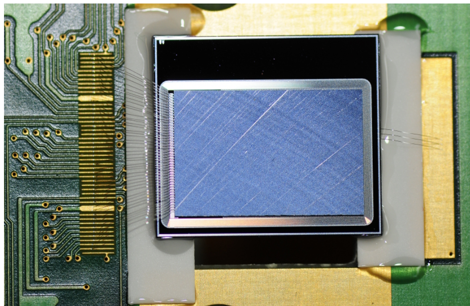
Challenge: Alignment Precision

The chips have to be populated on a handle wafer, then both wafers have to be aligned





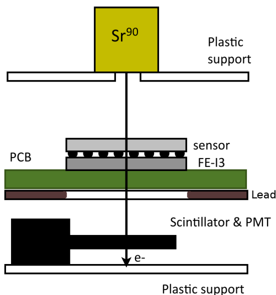
Pad size: $27 \times 60\,\mu\text{m}^2$ and pad distance $23\,\mu$m & $29\,\mu$m respectively.
Alignment precision is $\approx 10\,\mu$m but rotations are also involved.
$\Rightarrow$ Five working Modules.

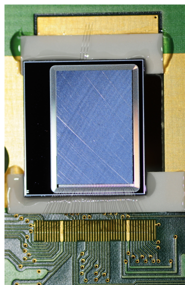


SLID Module Measurements

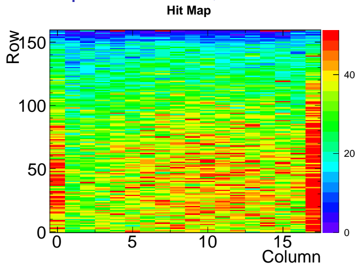
^{90}Sr-Measurement

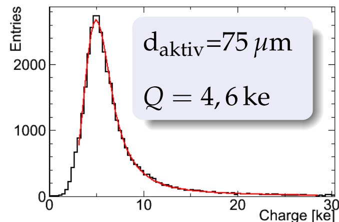
- ^{90}Sr source is used to determine the disconnected channels.
- External trigger via scintillator.
- Excellent performance in terms of collected charge and noise.
- Two bumps correspond to unconnected + noise and connected channels





Example: SLID 10, 250 k events





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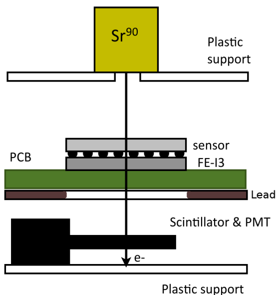

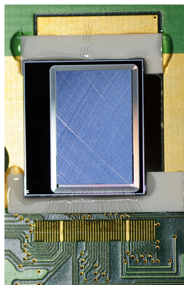

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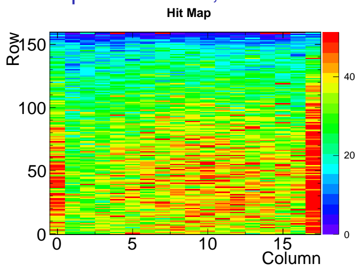

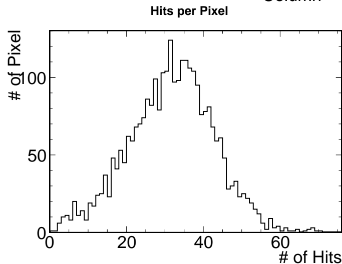

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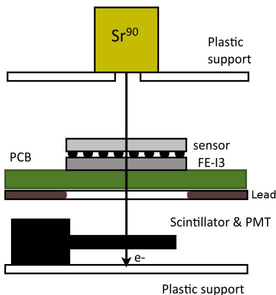
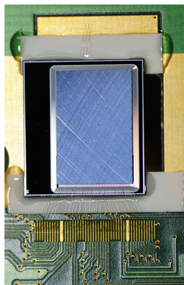
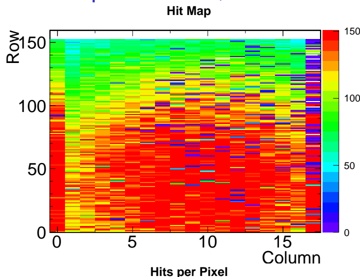
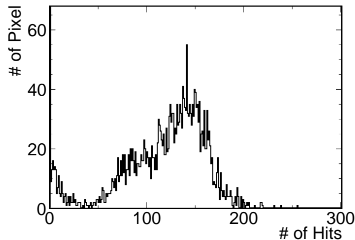




Example: SLID 9, 1 M events





Overview of the SLID Interconnection Efficiency

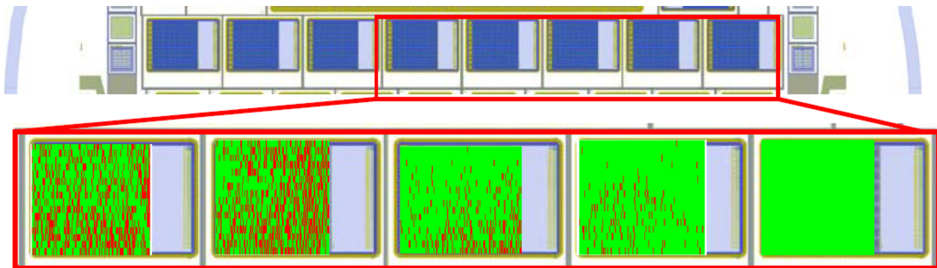
Trend towards centre of the wafer

Chip	Discon. Pixel	%
6	731	30
7	713	29
8	274	11
9	134	6
10	0	0

Percentage given w.r.t not masked channels

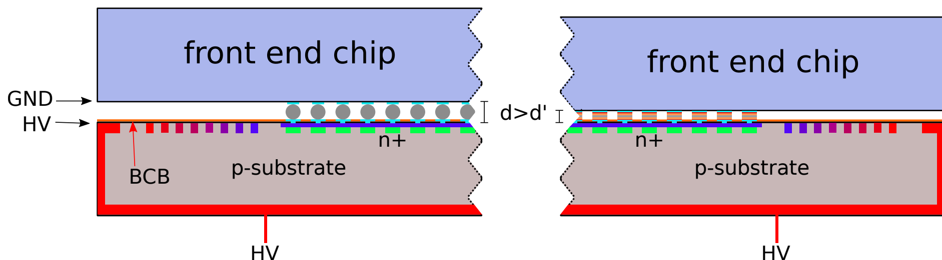
Possible causes:

- x-y alignment: Cannot be the sole reason, since adjacent pixels are not often disconnected.
- z alignment: Thinning down of chips could lead to height differences.
- Imperfections of BCB.



Interlude - BCB (Benzo Clyclo Butene)

n-in-p: HV is on sensor side facing the chip → danger of sparks!



Alternative interconnection technologies like SLID (Solid Liquid Interdiffusion; Cu+Sn pad) further reduce the distance!

Solution: Cover sensor with a thin insulating layer of BCB (Benzo Clyclo Butene)

HV-stability observed @ 1000 V over several hours.

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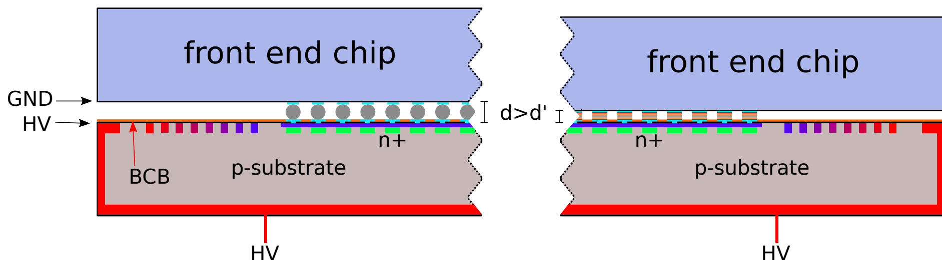

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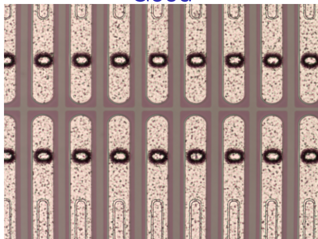
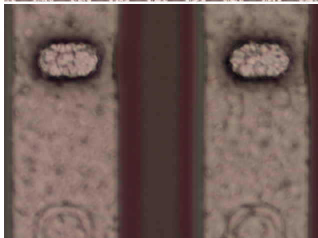
Possible Cause: BCB-Imperfections

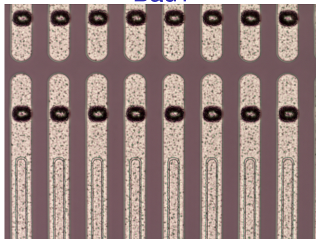
The BCB has to be opened to allow for the contact between chip and sensor. Maybe this operation did not fully succeed.

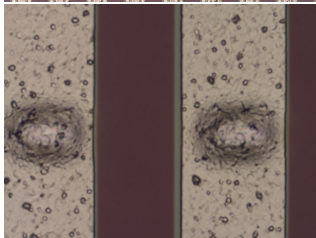
Good





Bad?





Connection Strength

The chips of the lower half of the wafer are ripped off to

- get an idea of the connection strength
- to see if there are systematics, hinting to problems in the process.

Findings:

- Ballpark: 0.01 N per connection. This is roughly what is seen for other technologies too.
- There is no clear correlation between strength and alignment (extreme cases not considered).
- Caveat: Underlying structures are not homogeneous.

Summary & Plans

Summary

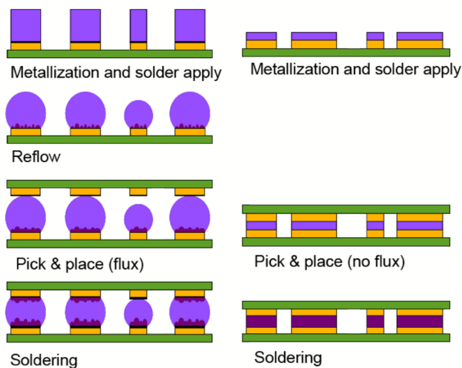
- First single chip modules with SLID interconnection exhibit good performance in terms of charge collection and noise.
- Trend of disconnected channels towards centre of the wafer $\rightarrow$ Reasons under investigation, probably not related to the interconnection technology.

Plans

- Irradiate structures to study the:
  - radiation hardness of the technology
  - charge collection for thin pixel detectors
- Full SLID assembly of sensors and front-end chips including ICV (Inter-Chip-Vias)

BACKUP

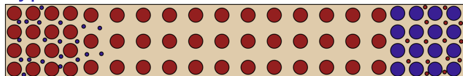
SLID vs. Bumb Bonding



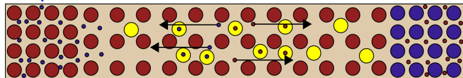
1. Apply metal layer to sensor and chip.
2. For bump bonding, the sensor is heated such that the solder-metal layer melts and become ball like. Smaller pads result in smaller balls (less material).
3. Chip and sensor a brought together.
4. The stack is heated. For bump bonding smaller balls cannot form a good connection.

Radiation damage

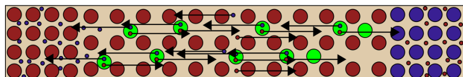
Type conversion



Traps



Carrier generation



Driving variable: Fluece
$\phi_{eq} \sim (1-10) \times 10^{15}\, n_{eq}$

- Acceptor-like defects
  - n-type converts to p-type
  - p-type will get a higher effective doping $\rightarrow$ higher depletion voltages
- Defects can trap free charge carriers:
  - Free pathlength $\ell \sim \phi_{eq}$
- Increased generation and recombination rates $\Rightarrow$ Higher leakage currents $\rightarrow$ higher noise. Can be partly cured by temperatue (annealing)

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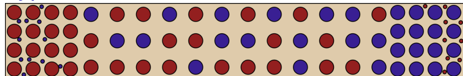

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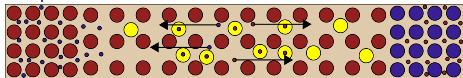

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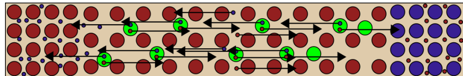

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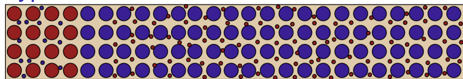

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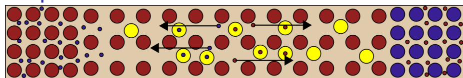

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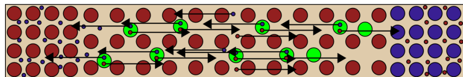

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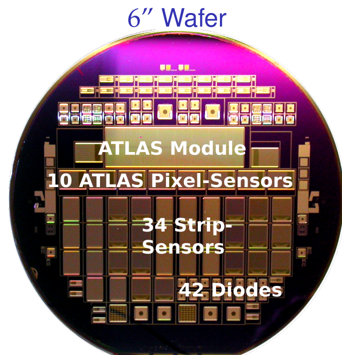
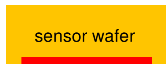
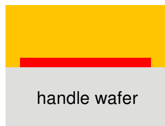
Thin Pixel Production at MPP/HLL



- Four wafers of 150 μm and eight (4×n-in-p & 4×n-in-n) wafers of 75 μm active thickness (on handle wafer)
- Proton & neutron irradiations with fluences up to $10^{16}\,n_{eq/cm^2}$ in Karlsruhe (25 MeV), CERN PS (24 GeV) & Lubljana (reactor)

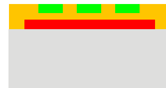


1. Implant backside on sensor

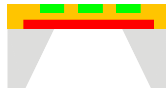


2. Bond sensor wafer to handle wafer

3. Thin sensor side to desired thickness



4. Process on top side



5. Structure resist, etch backside up to oxide