Radiation Hardness of DEPFET Detectors

IMPRS Young Scientist Workshop 2011

Wildbad Kreuth, 25th-29th July 2011

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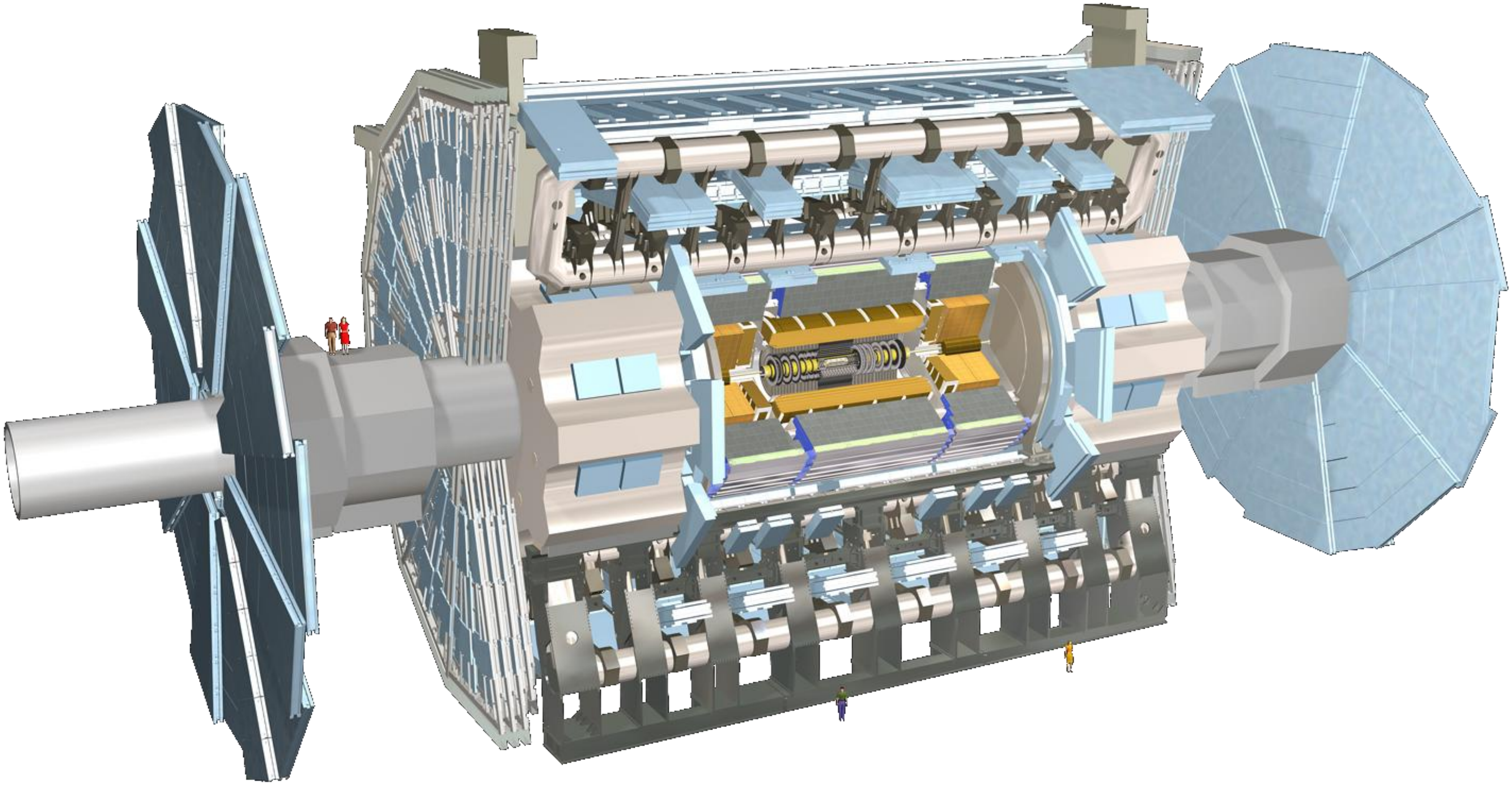
mpi halbleiterlabor

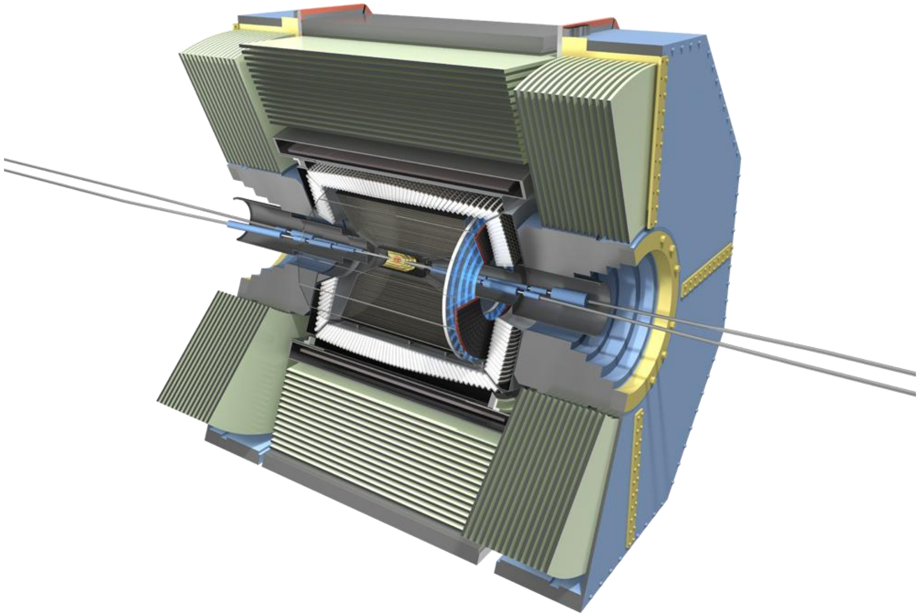
Outline

1. Motivation: DEPFETs for Belle 2
2. What is a DEPFET?
3. Ionizing radiation on MOS devices
4. Possible pixel layout → voltage cross sections
5. Threshold voltage shift dependance on gate voltage
6. Summary and Outlook

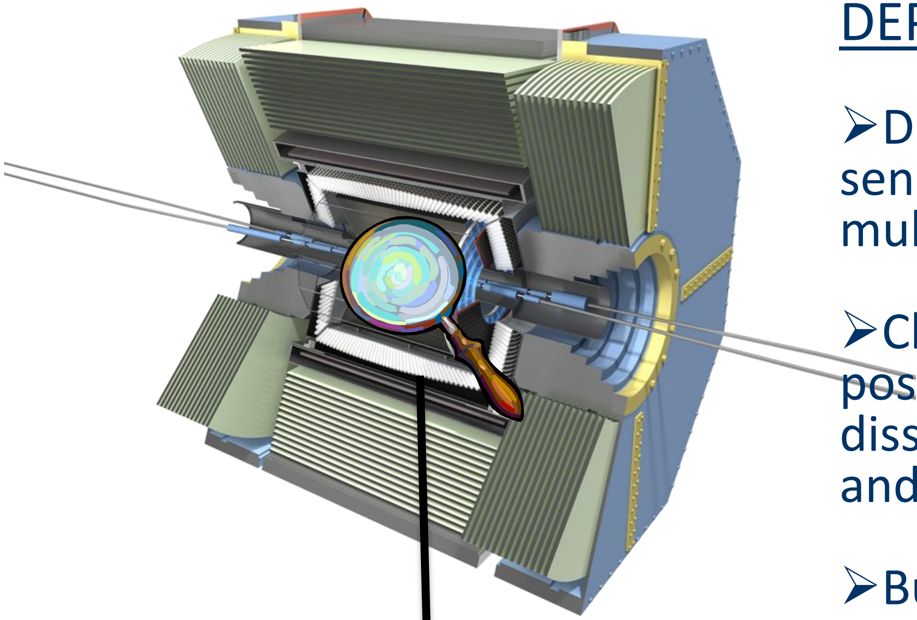
It‘s not about this detector…

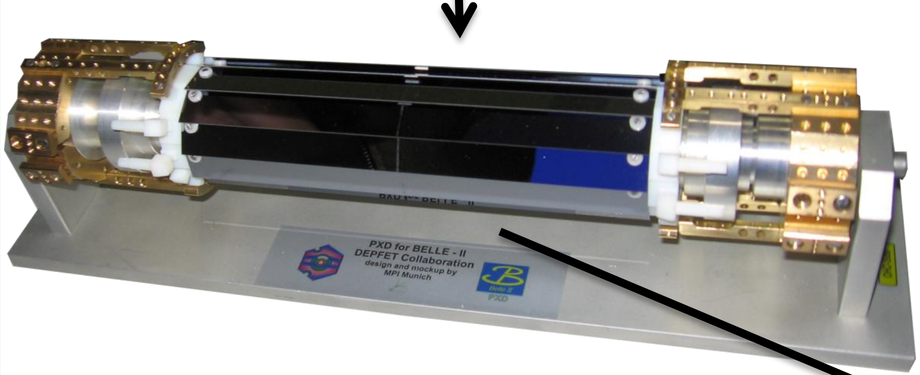


… but about this one (Belle 2)



Motivation: DEPFETs for Belle 2



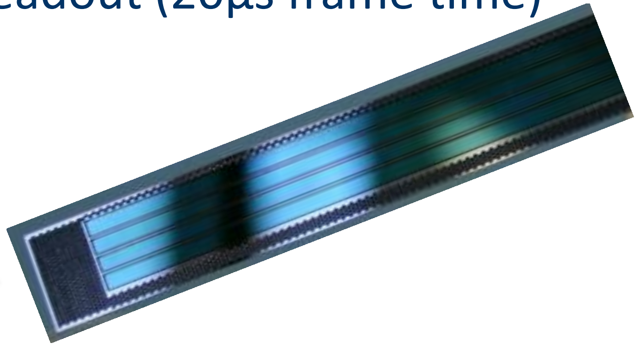


DEPFETs for Belle 2

- DEPFETs have a good SNR → thin sensors achievable (75 µm, avoids multiple scattering)

- Charge collection (next slides…) possible in „OFF“-state → low power dissipation → cooling via end flanges and airflow

- Bulk damage: ~10^{11} neq/(cm² * yr)
  - ~~type inversion~~
  - ~~chargeloss (trapping)~~
  - leakage current, shot noise → fast readout (20µs frame time)



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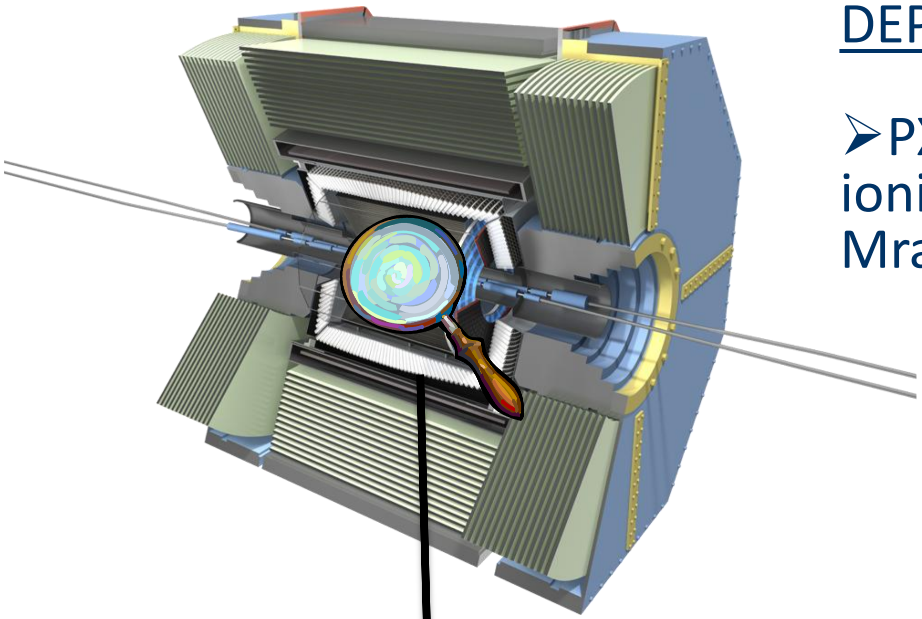
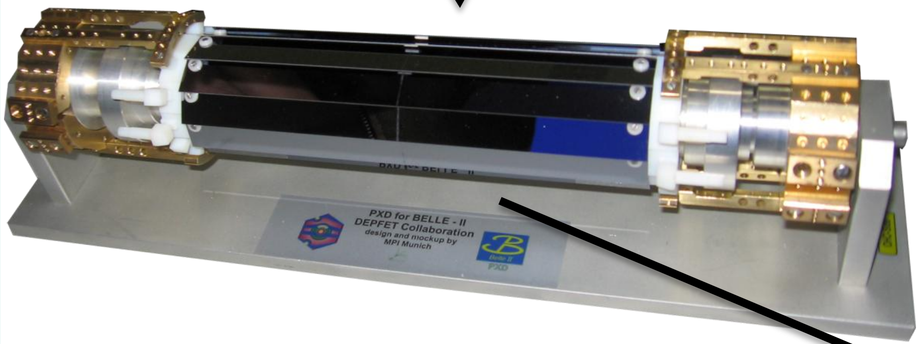
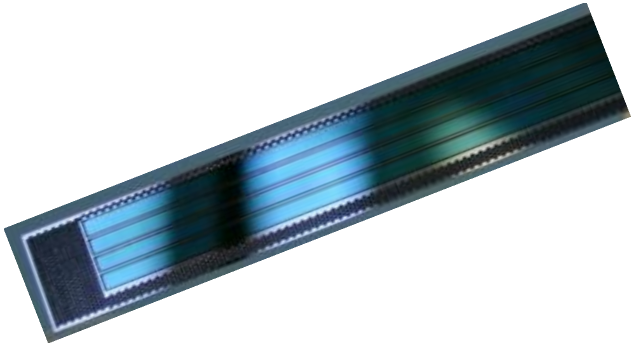


DEPFETs for Belle 2

- PXD (DEPFET matrix) suffers from ionizing radiation, estimated 1…2 Mrad/yr (10…20 kGy/yr)





DEPFET WORKING PRINCIPLE

Working principle of a DEPFET

What is a DEPFET?

Working principle of a DEPFET

What is a DEPFET?

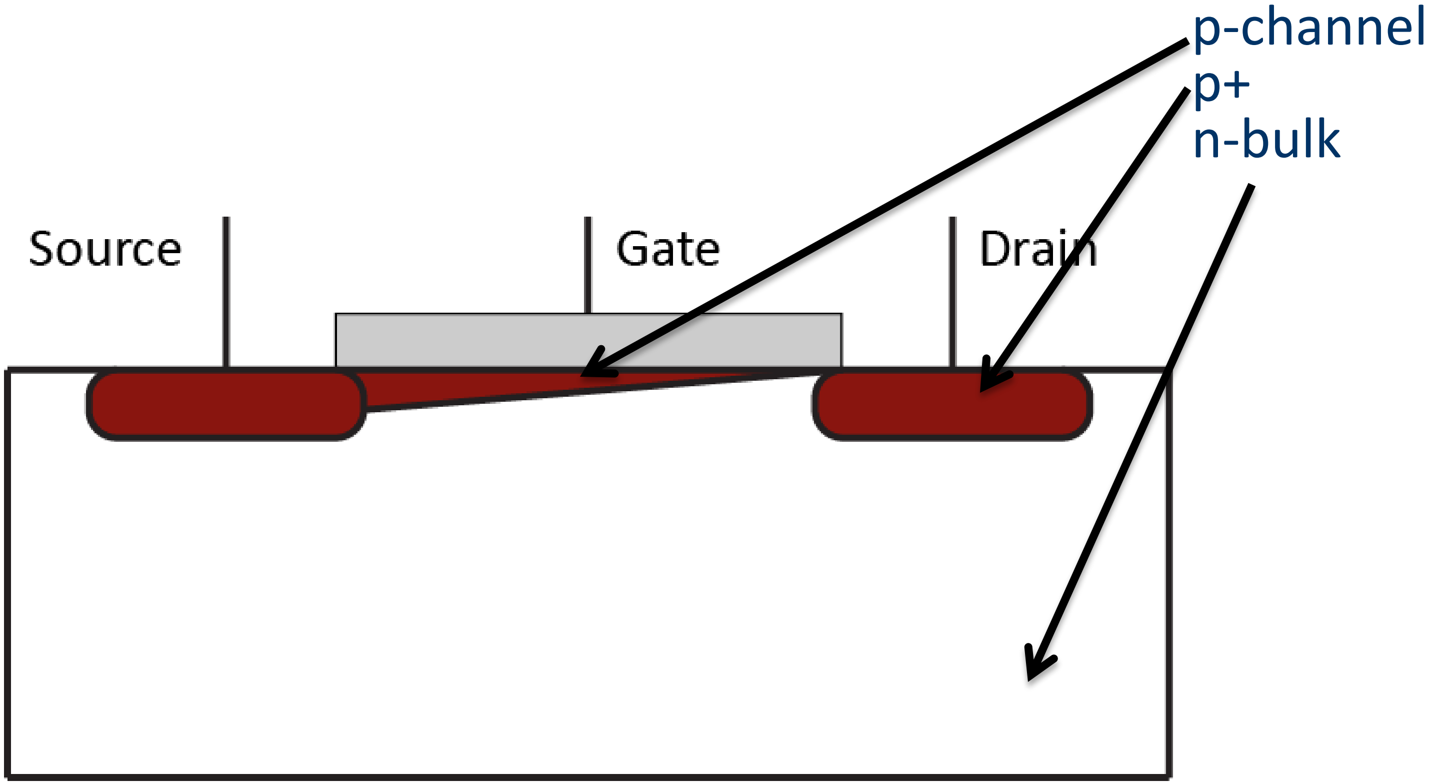
-It‘s a MOSFET!

Working principle of a DEPFET

1. DEPFET = Depleted Field Effect Transistor

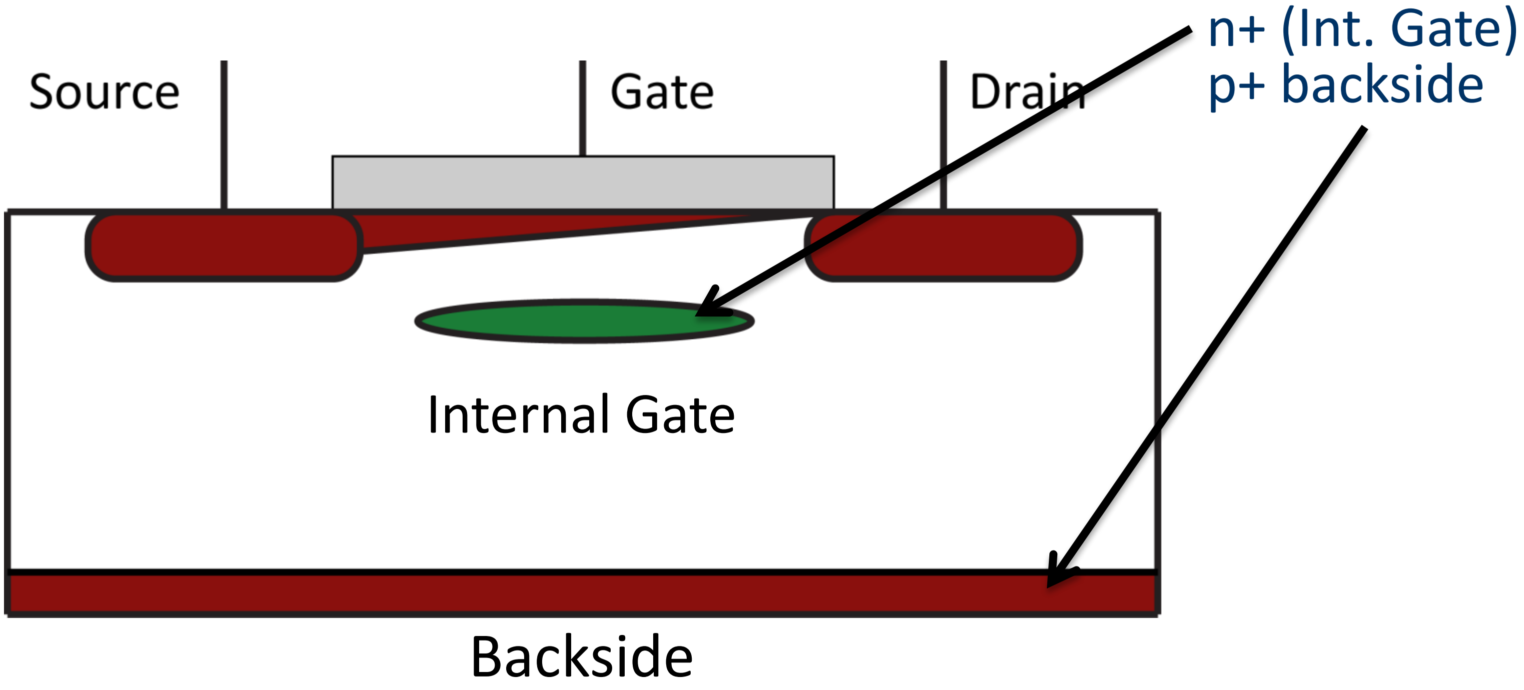
Working principle of a DEPFET

1. DEPFET = Depleted Field Effect Transistor
2. Consider a normal MOSFET…



Working principle of a DEPFET

1. DEPFET = Depleted Field Effect Transistor
2. Consider a normal MOSFET…
   …now add some DEPFET specifics.



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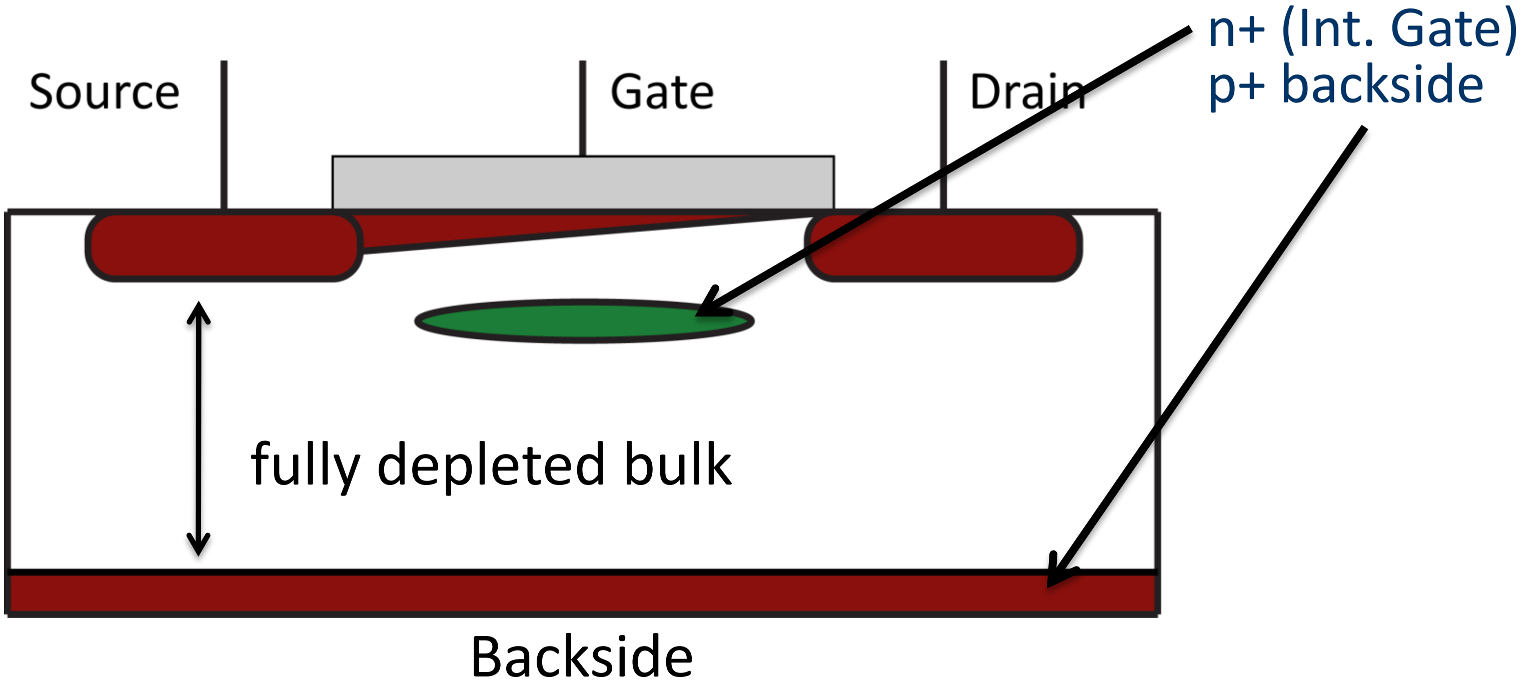
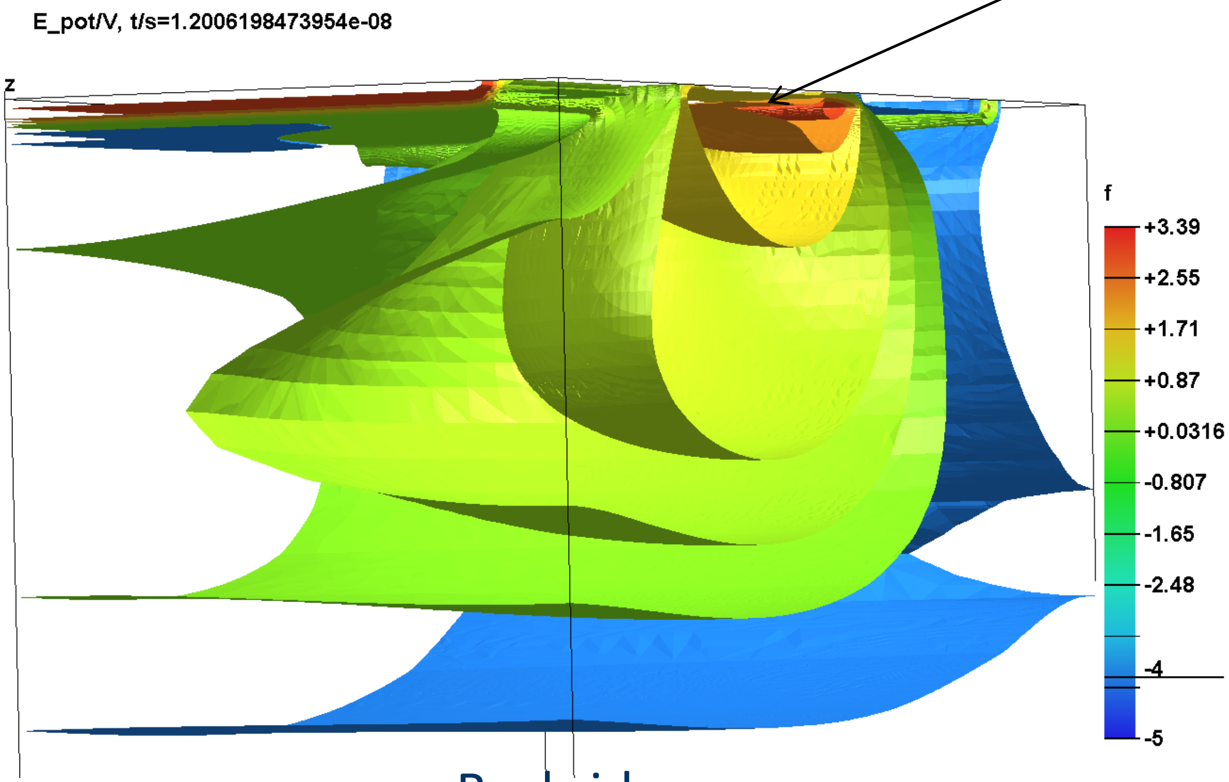


Working principle of a DEPFET

1. DEPFET = Depleted Field Effect Transistor
2. Consider a normal MOSFET…
3. Sidewards depletion – Equipotential planes



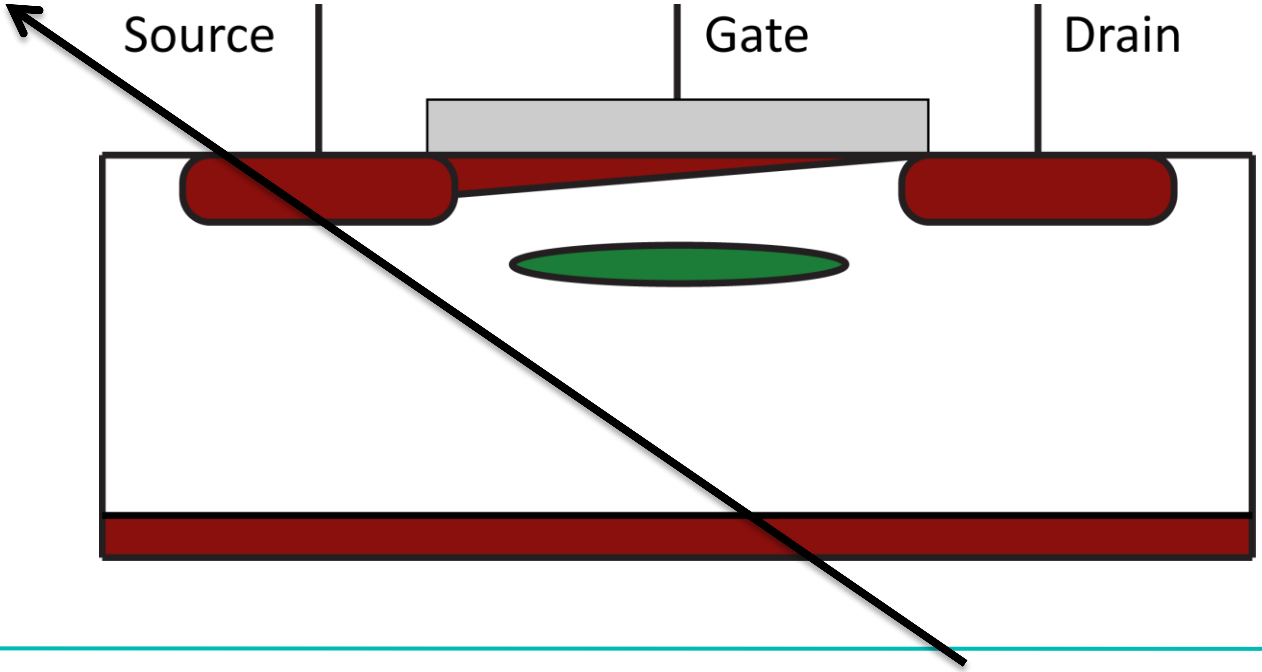
Internal Gate

Backside

Performed by
K. Gärtner
WIAS Berlin

Working principle of a DEPFET

1. DEPFET = Depleted Field Effect Transistor
2. Consider a normal MOSFET…
3. Sidewards depletion
4. Charge creation and collecting



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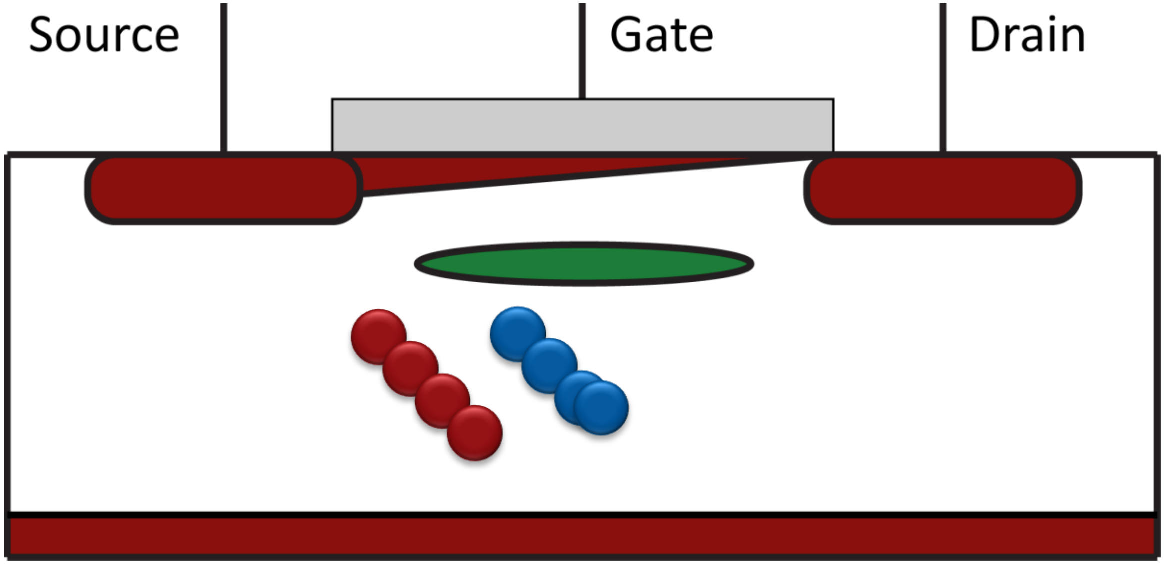

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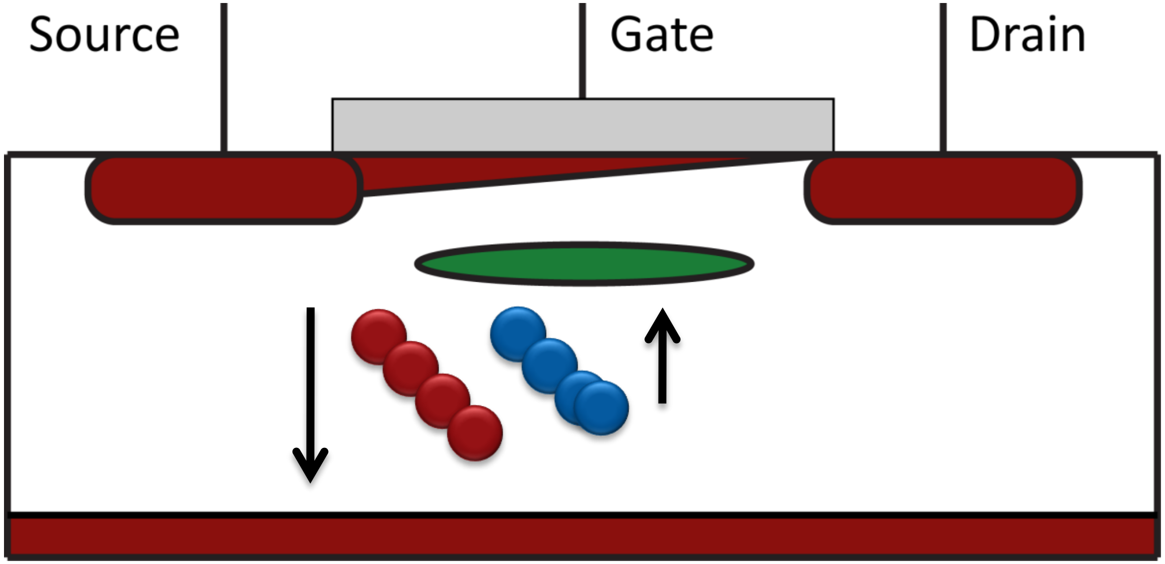

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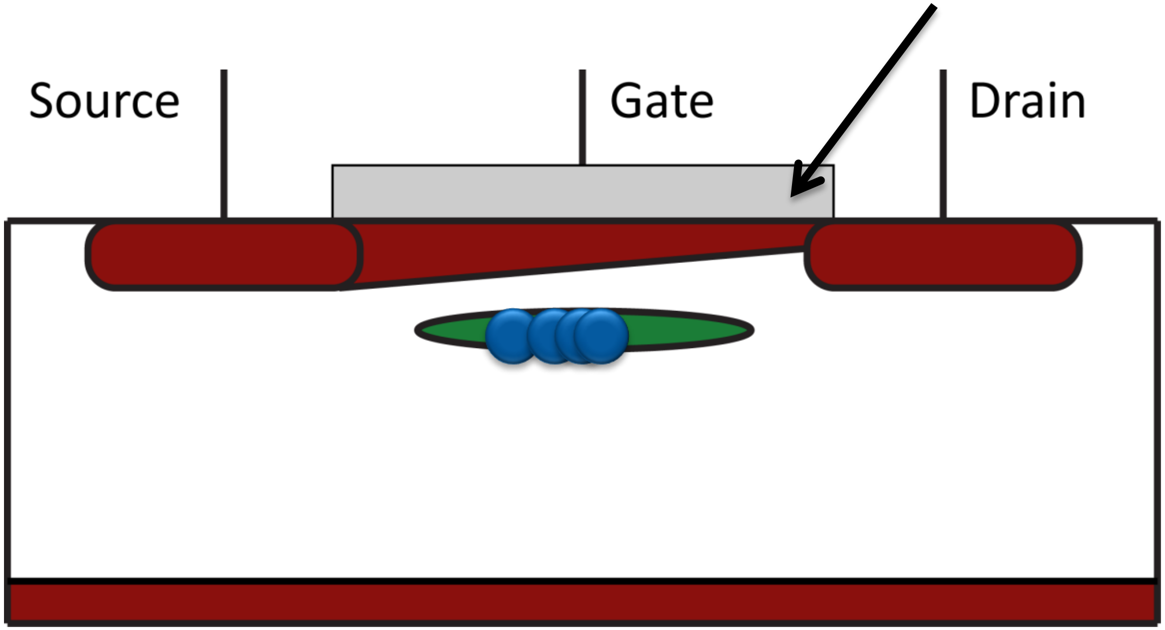

higher current via mirror charges

Working principle of a DEPFET

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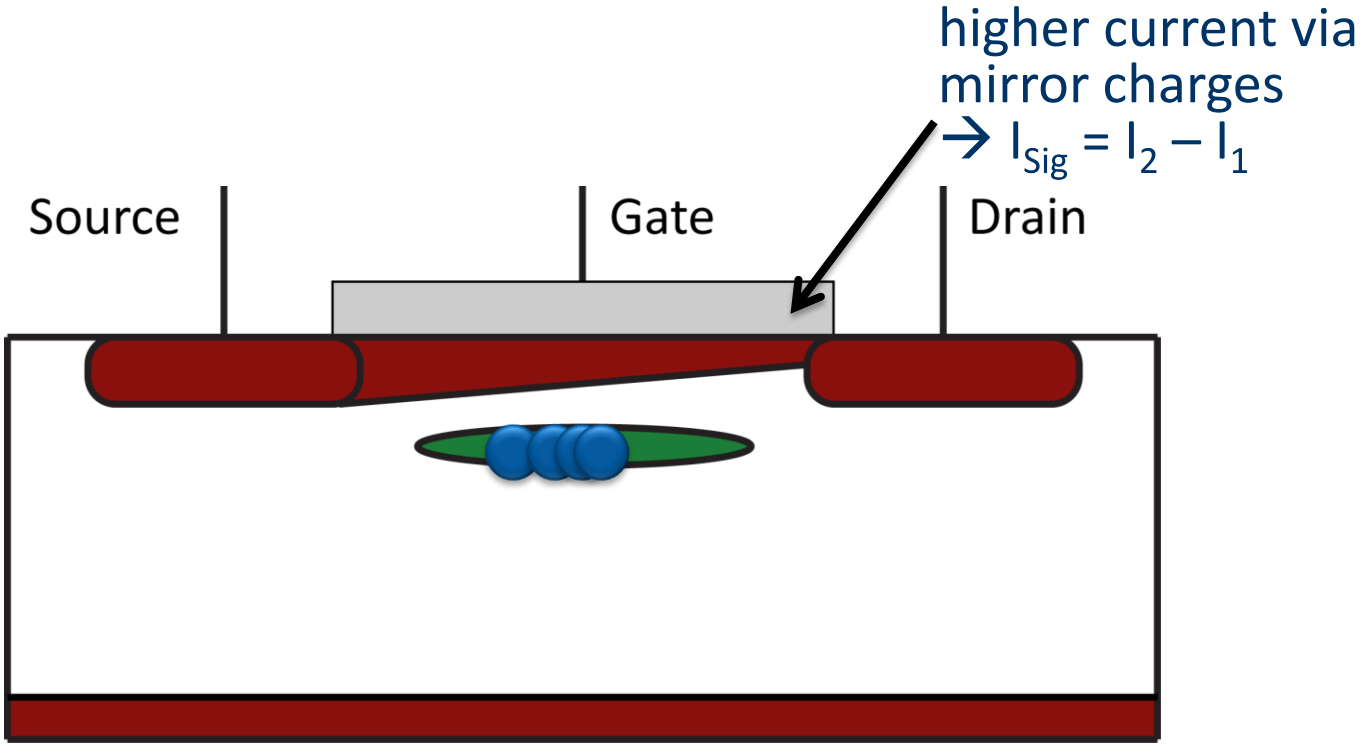
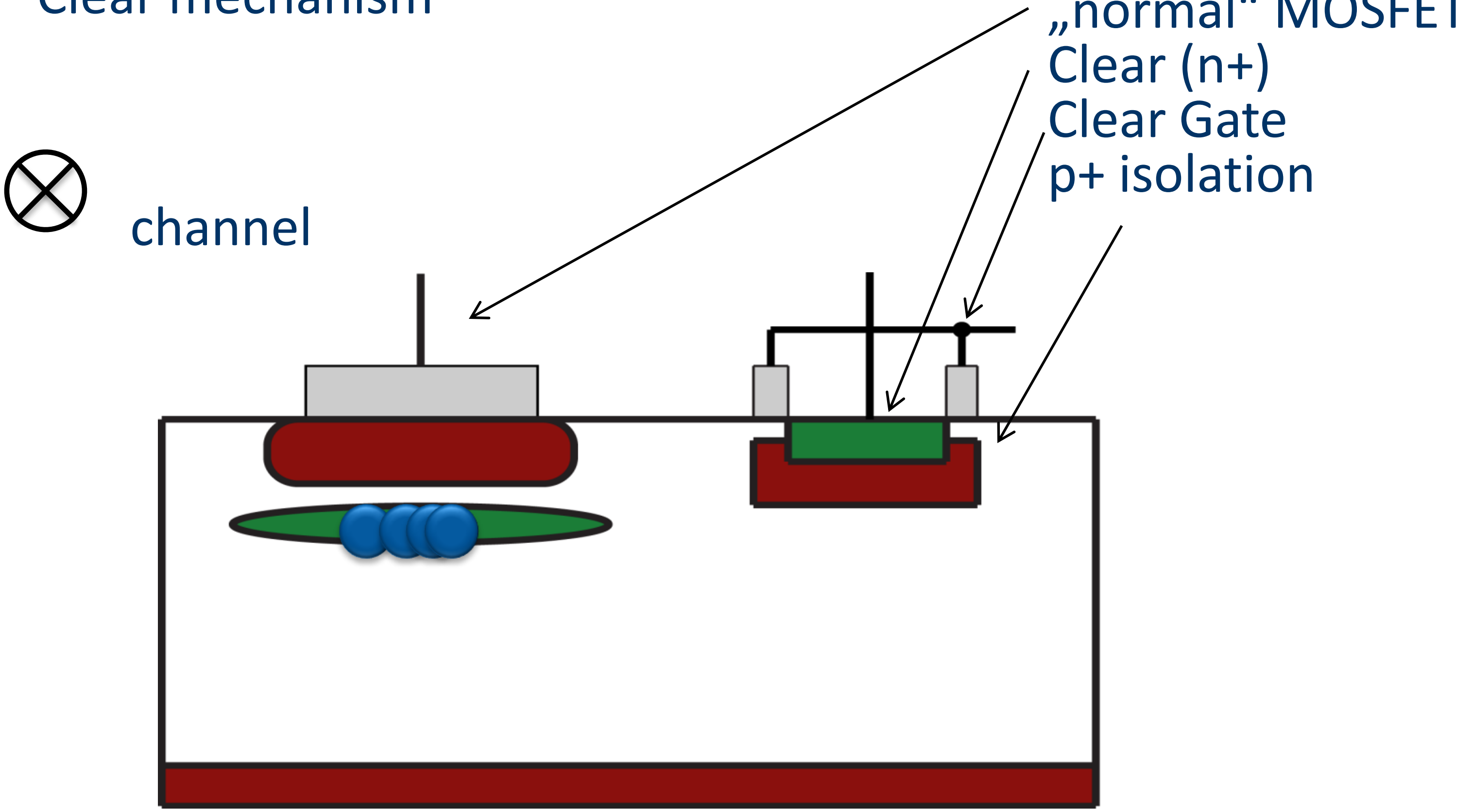


higher current via mirror charges

→ $I_{Sig} = I_2 - I_1$

Working principle of a DEPFET

1. DEPFET = Depleted Field Effect Transistor
2. Consider a normal MOSFET…
3. Sidewards depletion
4. Charge creation and collecting
5. Clear mechanism



Picture from side (90°rotated)

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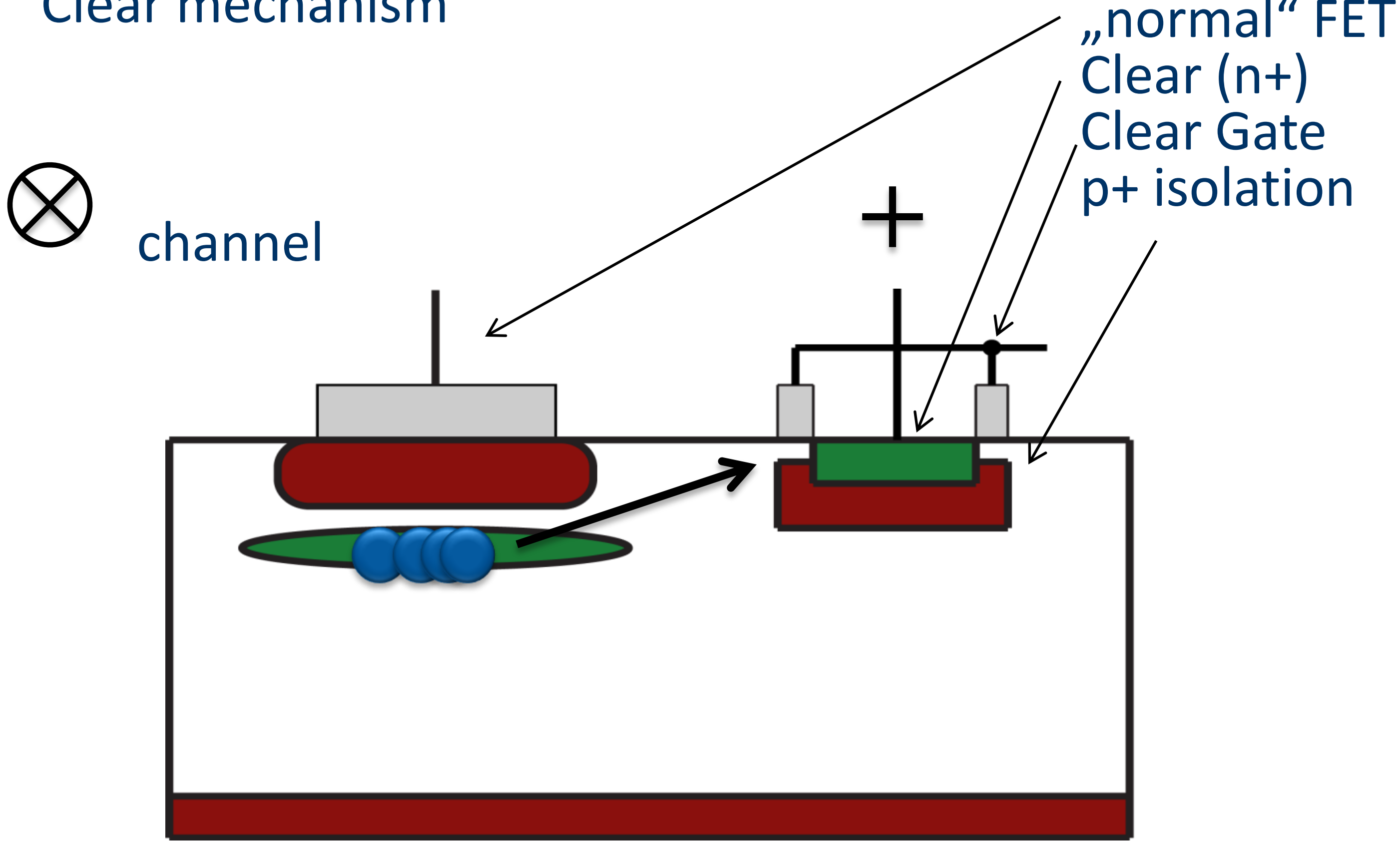

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Working principle of a DEPFET

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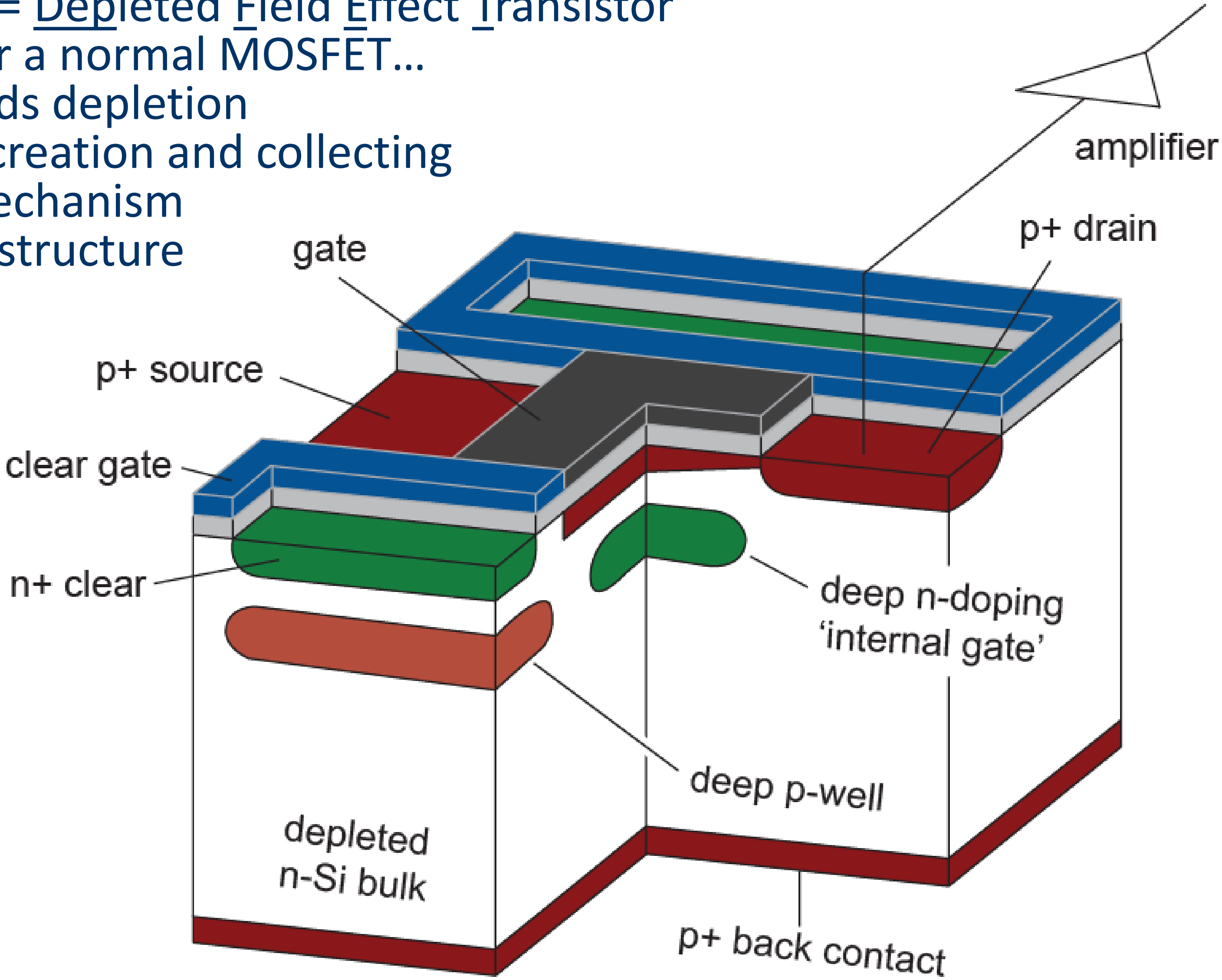
4. Charge creation and collecting
5. Clear mechanism
6. DEPFET structure



IONIZING RADIATION AND SIO_2

Ionizing radiation damage

Two types of damage:

1. Trapped oxide charges

   → Changes MOSFET operating point

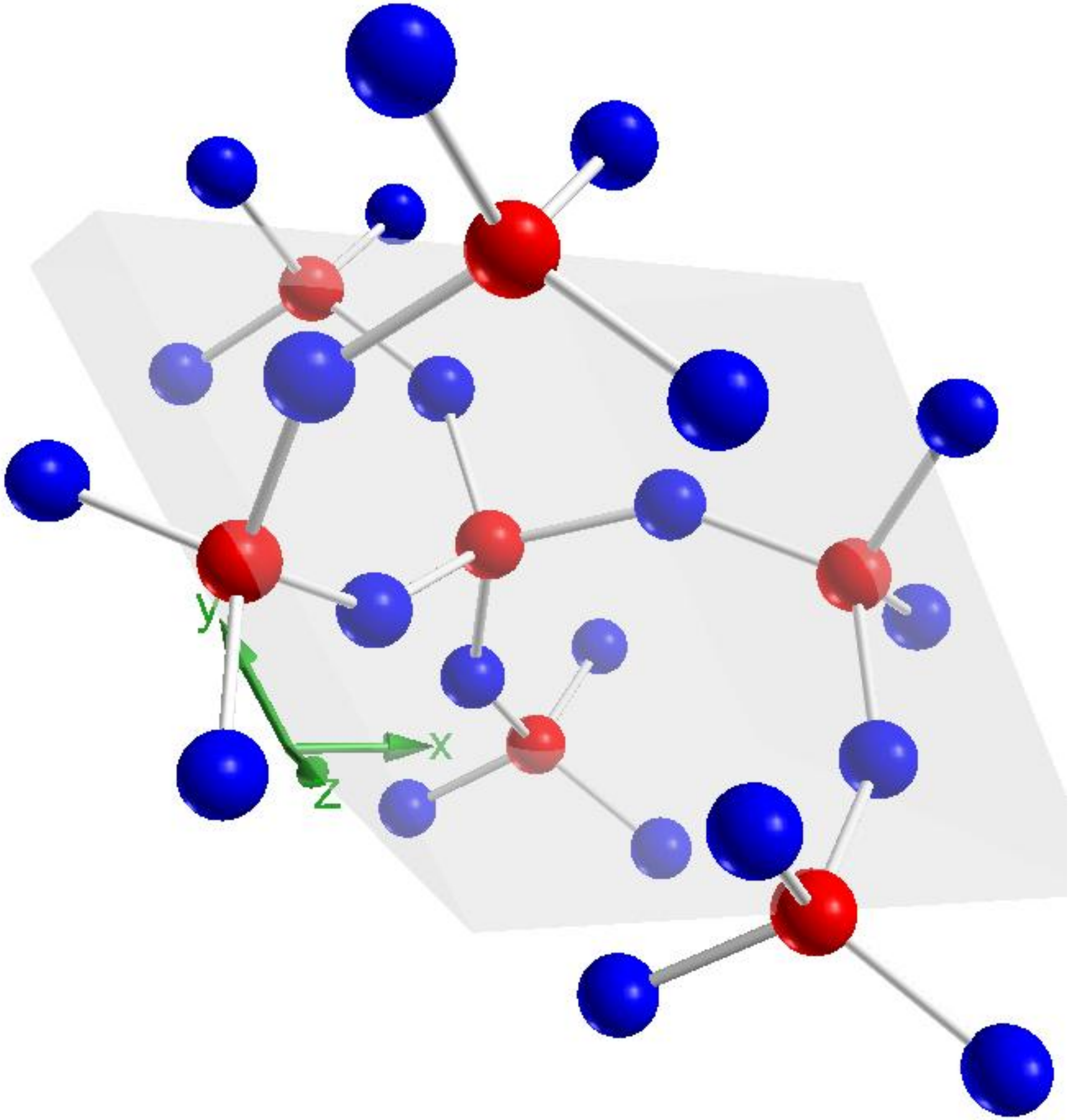
2. Interface traps

   → Creates 1/f noise

   → **not** covered in this talk

Defects – Creation of Oxide Charge (I)

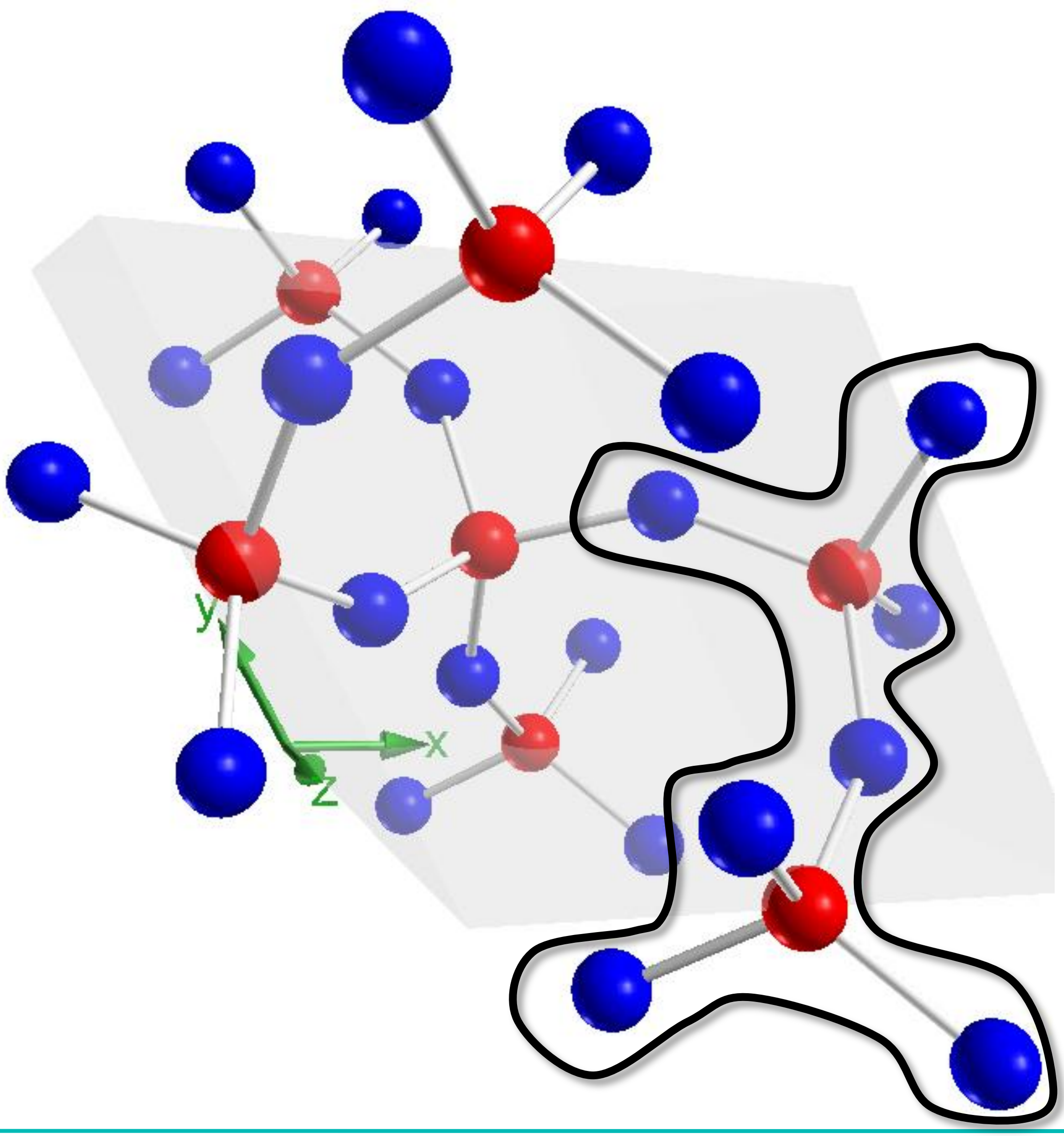
SiO_2 Crystal structure



Defects – Creation of Oxide Charge (I)

SiO_2 Crystal structure

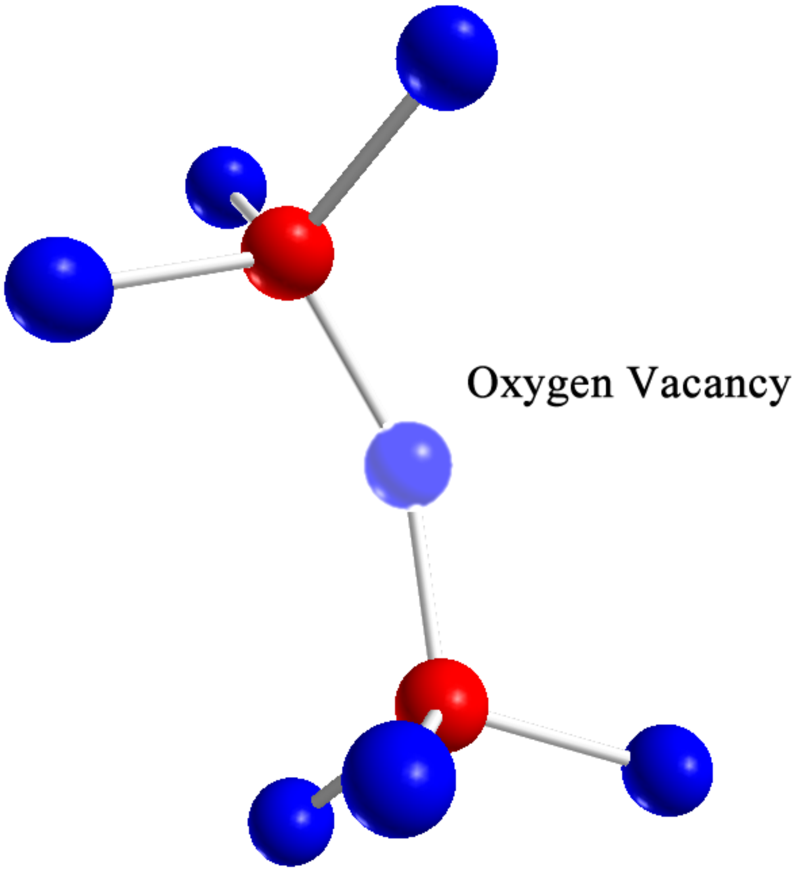
Interface between Si and SiO_2: “*Lattice*” mismatch



Defects – Creation of Oxide Charge (I)

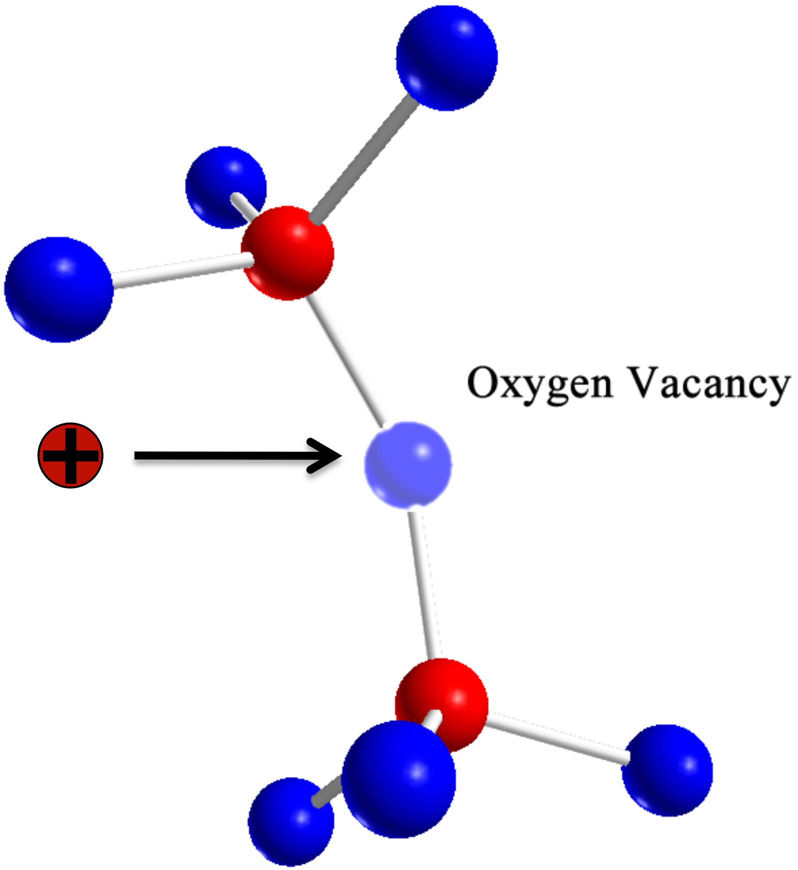
SiO_2 Crystal structure

Interface between Si and
  SiO_2: “*Lattice*” mismatch
  → Bond from Si to Si



Defects – Creation of Oxide Charge (I)

- SiO_2 Crystal structure
- Interface between Si and SiO_2: “*Lattice*” mismatch → Bond from Si to Si
- Strained Bond can be broken by holes in the oxide (coming from ionizing radiation)



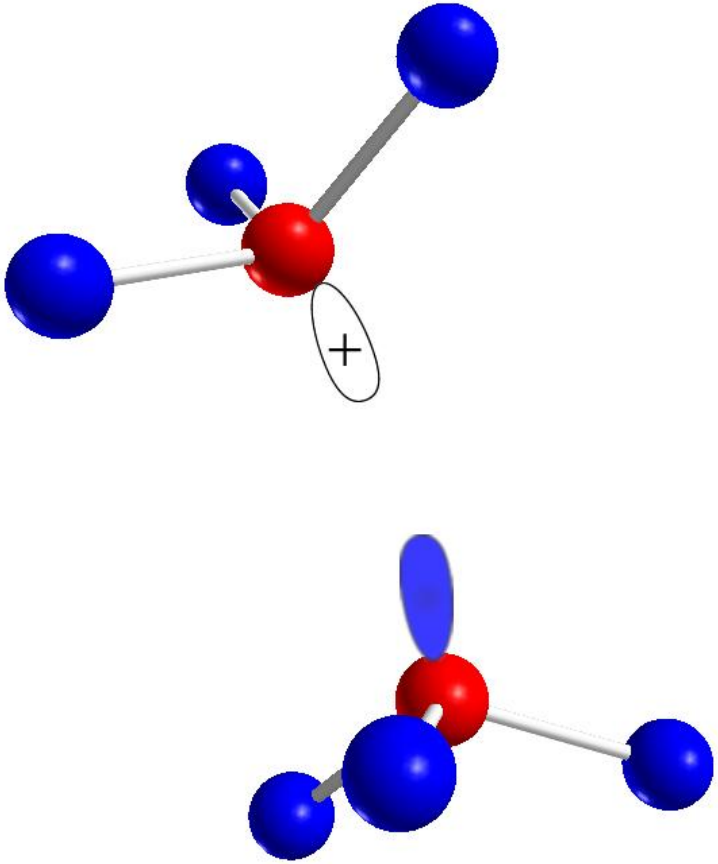
Defects – Creation of Oxide Charge (I)

SiO_2 Crystal structure

Interface between Si and SiO_2: “*Lattice*” mismatch
→ Bond from Si to Si

Strained Bond can be broken by holes in the oxide (coming from ionizing radiation)

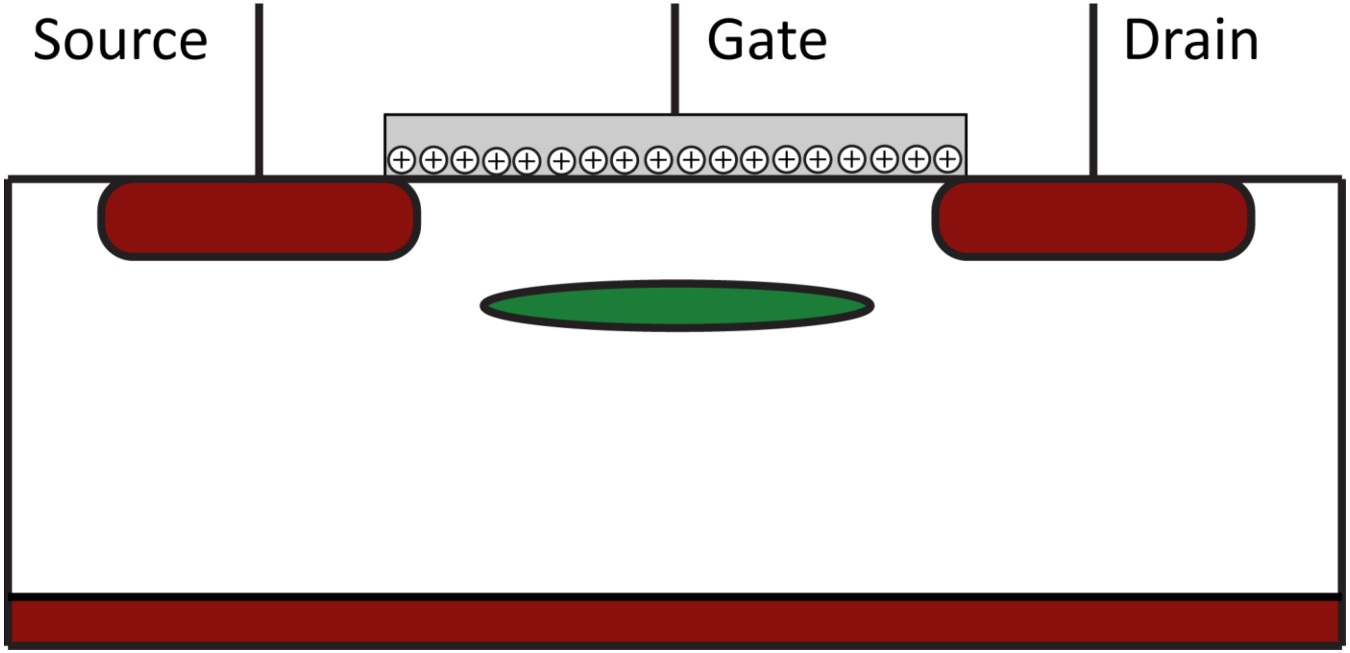
Positive charge remains…



Impact of Oxide Charge on the DEPFET

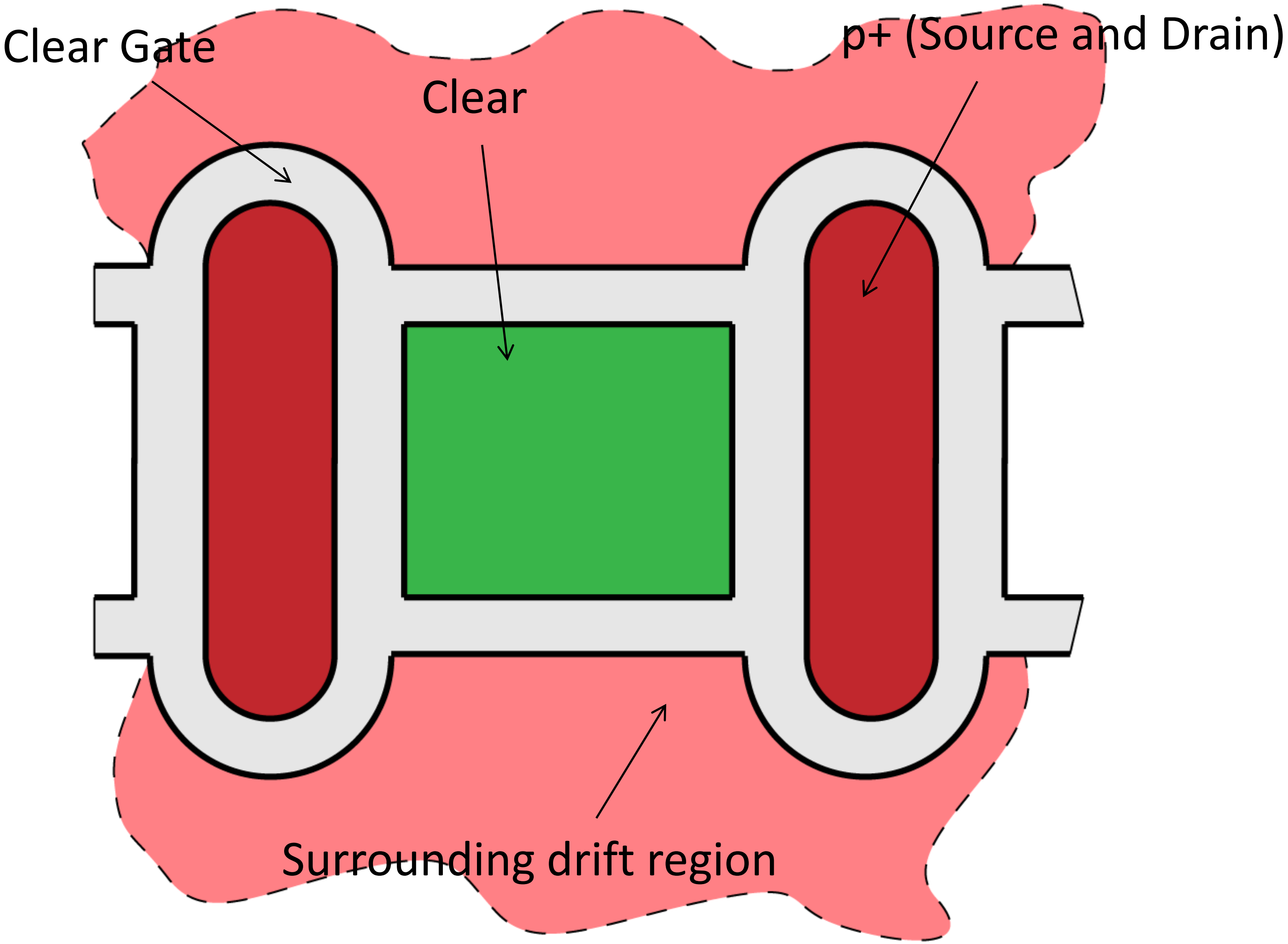
Oxide charges are trapped holes in the oxide

Change threshold voltage and may create parasitic channels

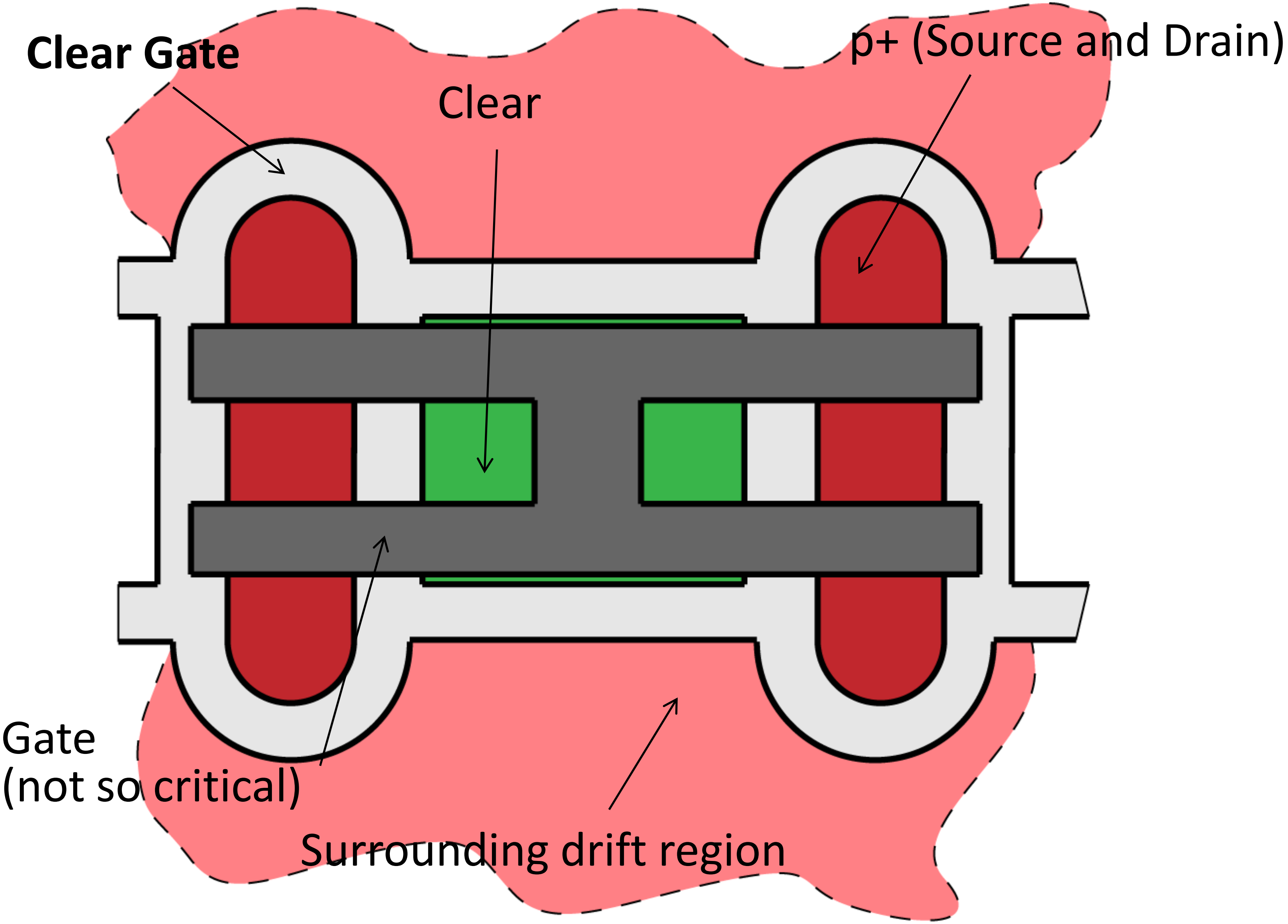


PIXEL LAYOUT AND VOLTAGE DEPENDANCIES

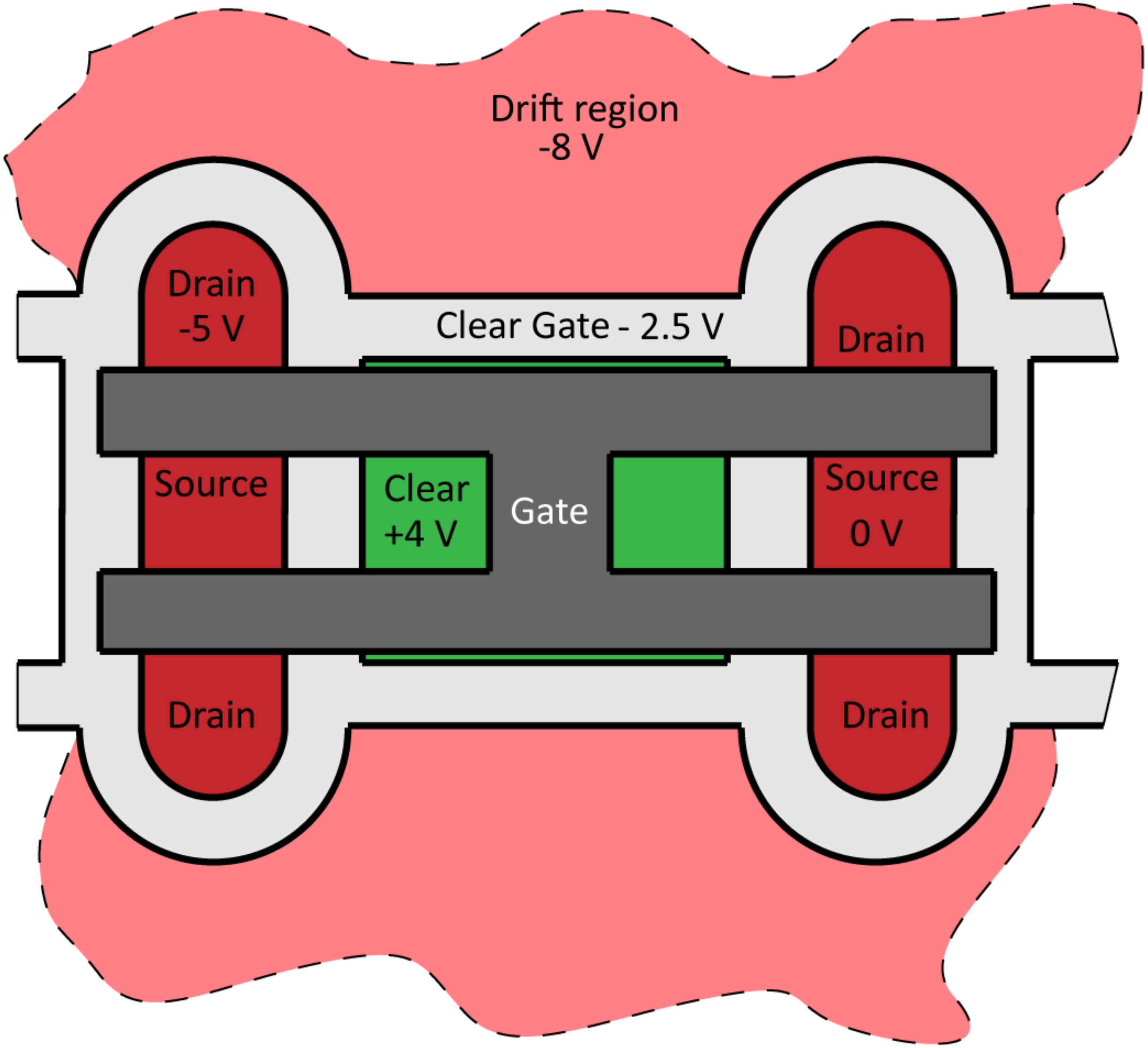
Motivation - Possible Pixel Layout



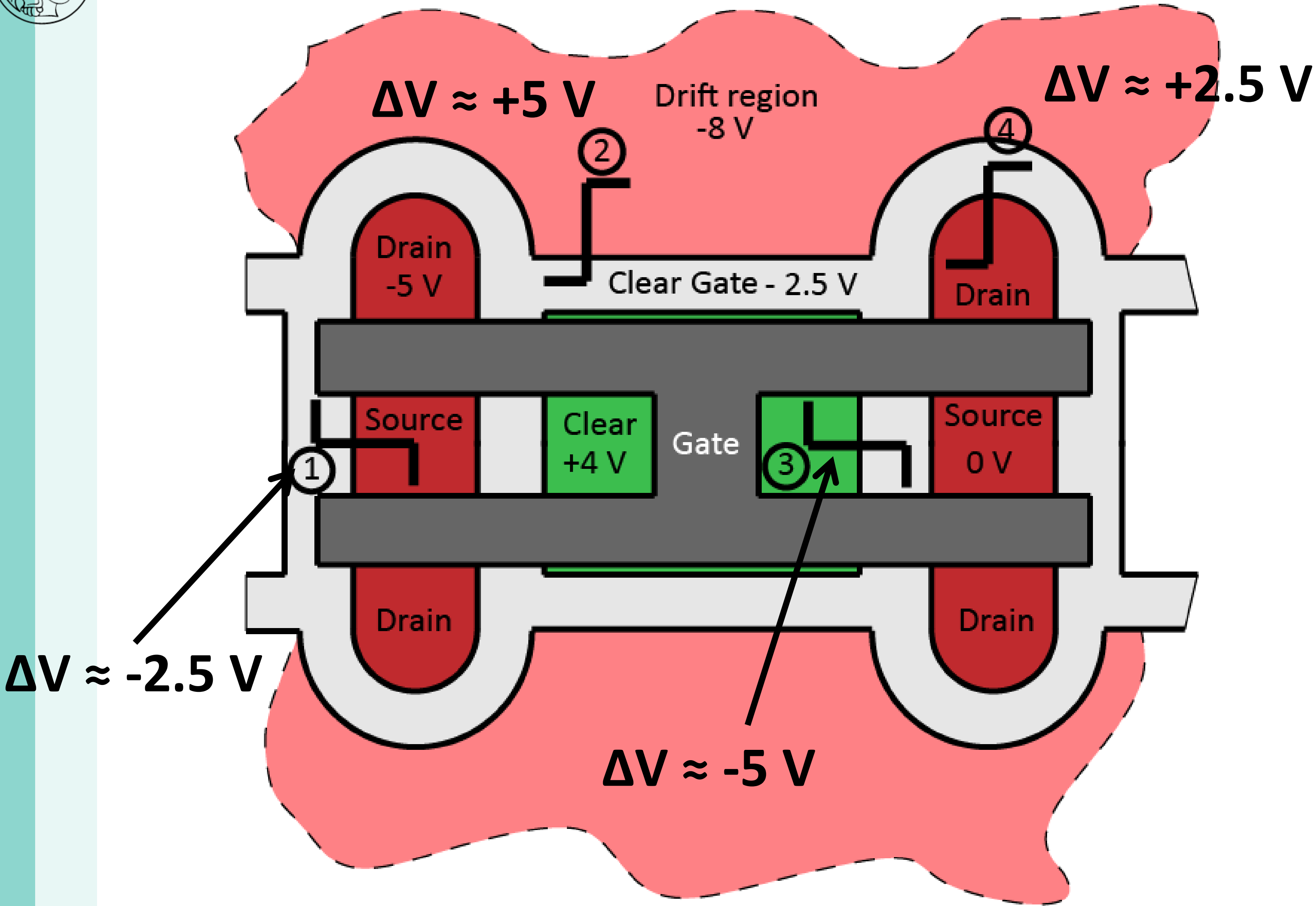
Motivation (II)- Possible Pixel Layout



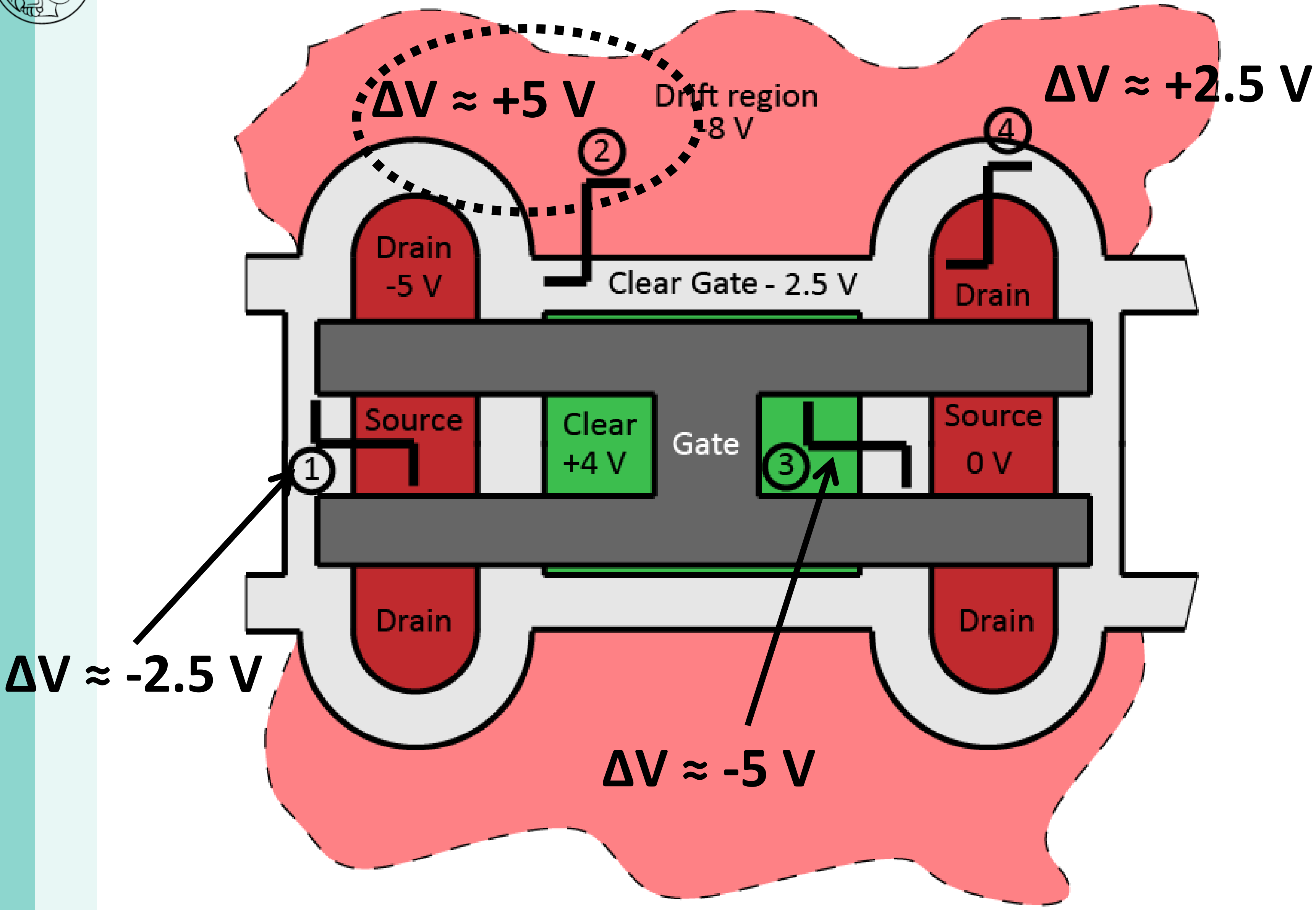
Motivation (III)- Possible Pixel Layout and Potentials



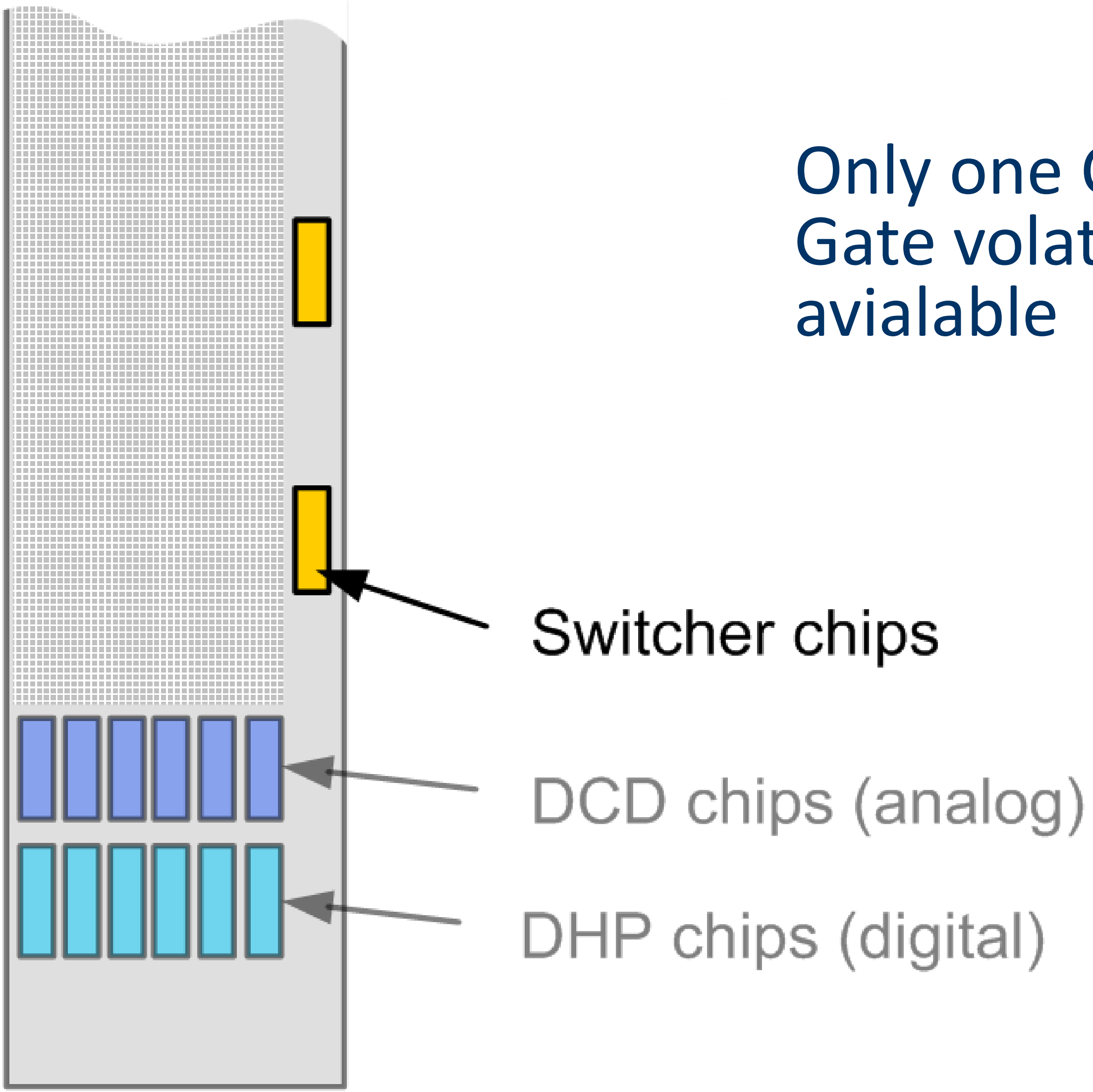
Motivation (IV)- Possible Pixel Layout and relevant cross sections



Motivation (IV)- Possible Pixel Layout and relevant cross sections

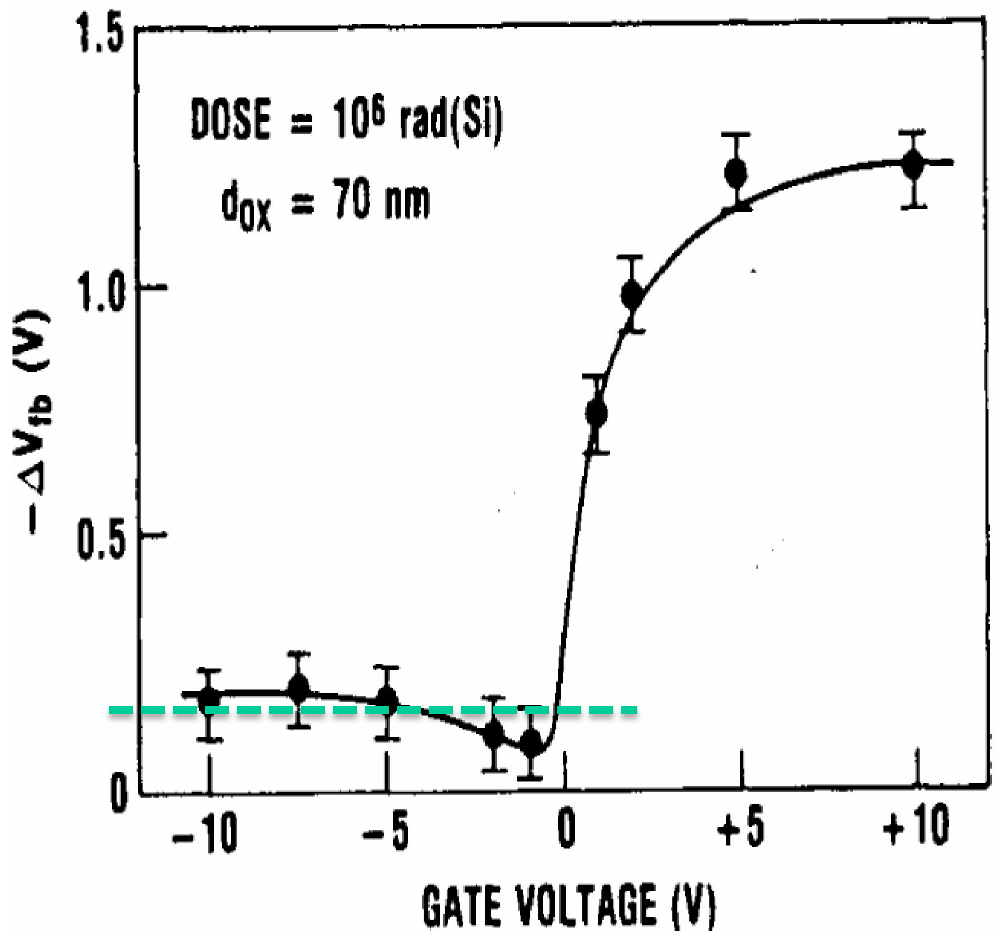


Change in threshold voltage shift due to certain Gate voltages



Only one Clear Gate volatge avialable

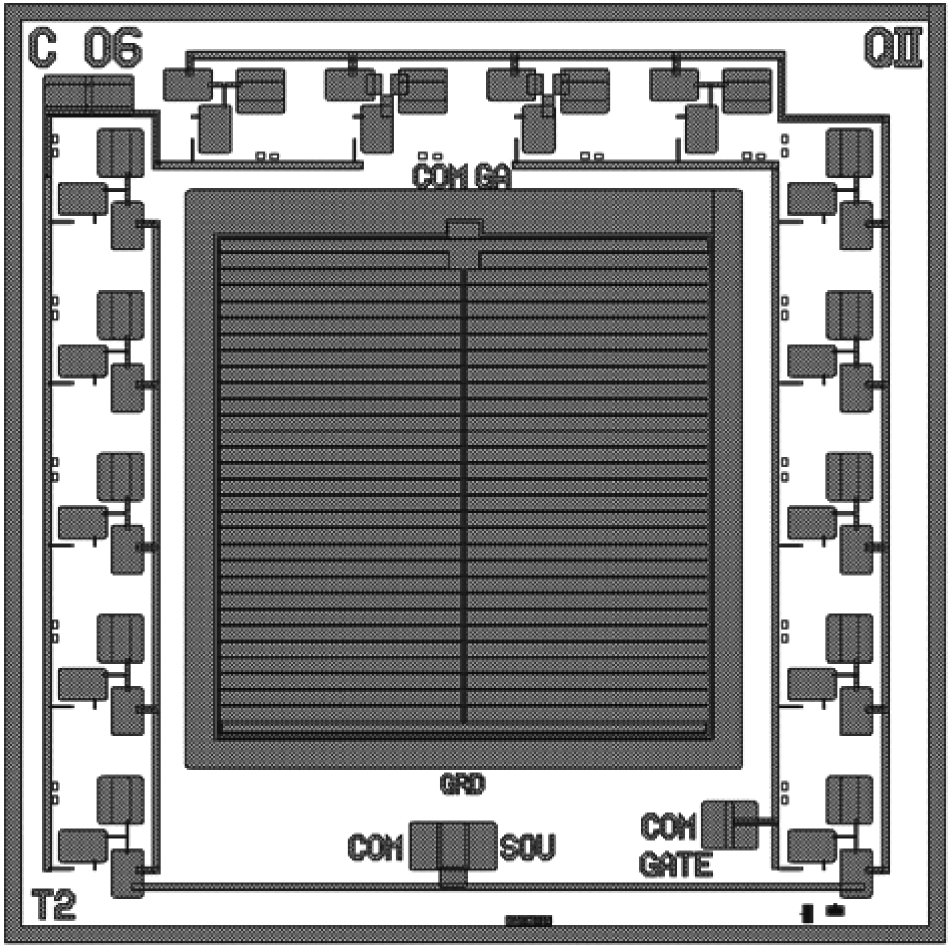
Change in threshold voltage shift due to certain Gate voltages



Ma/Dressendorfer

Only one Clear Gate volatge avialable → **flat** region is favoured

Layout of thin oxide devices



Characteristics of thin oxide structures:

- thin and thick Si_3N_4

- SiO_2 thickness is the same for all

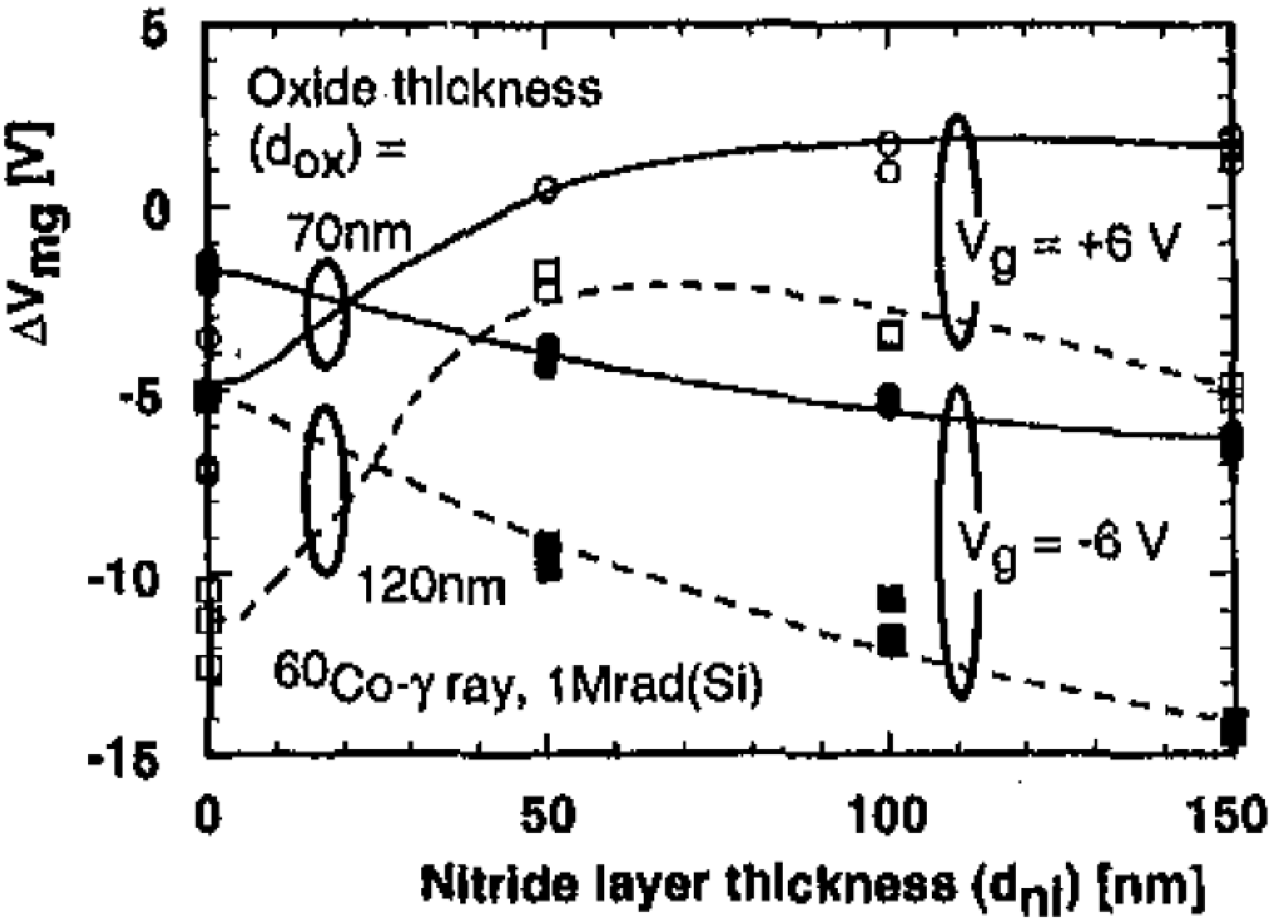
- Central device: Gate Controlled Diode

- 14 Transistor (=2x7), with diff. Gate length and width

- Doping profiles similar to Clear Gate

Thick nitride and Gate voltages

Thicker nitride could be a solution to the problem at hand.



Radiation-Induced Trapped Charge in
Metal-Nitride-Oxide-Semiconductor Structure; Takahashi et. al.
IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL 46, NO 6, DECEMBER 1999

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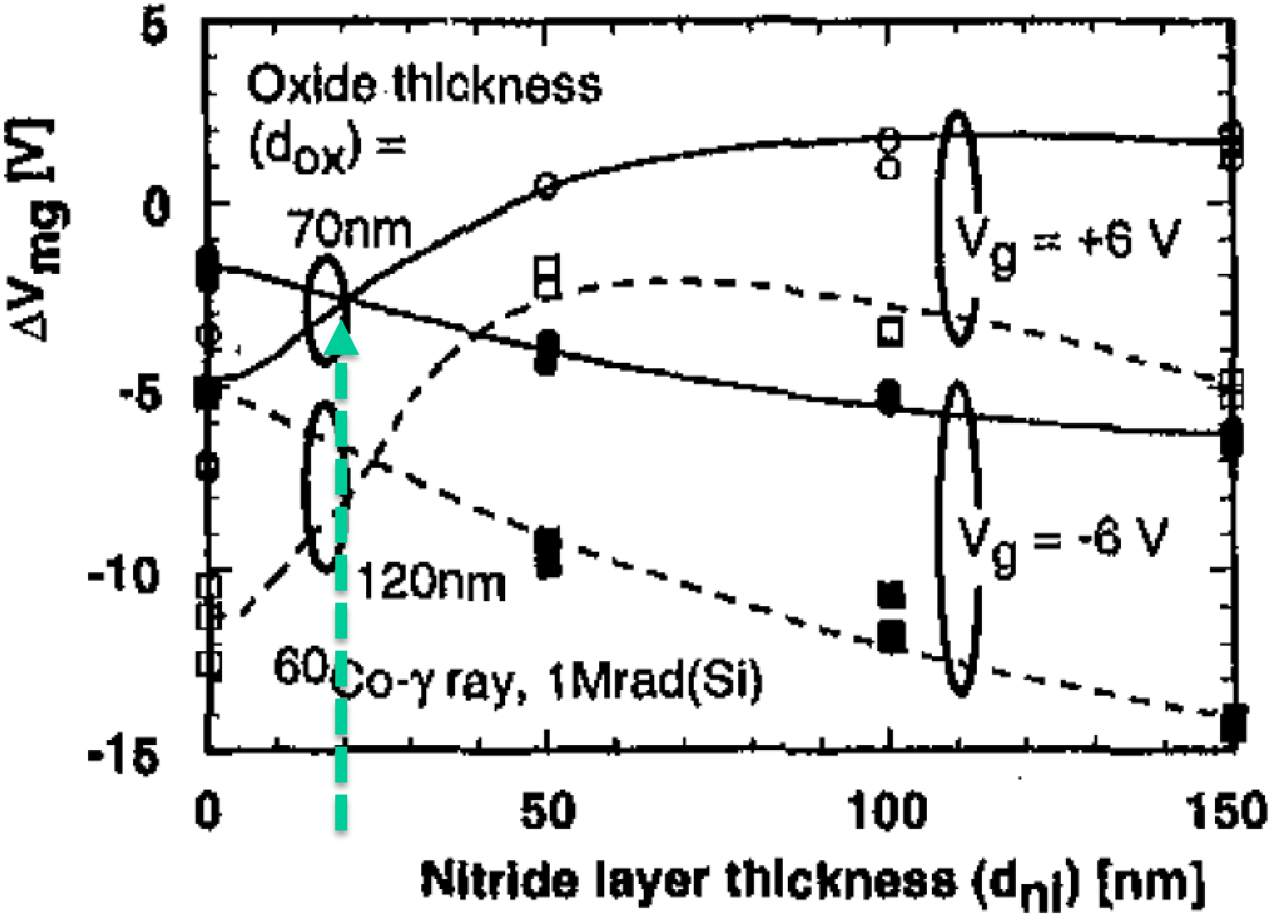

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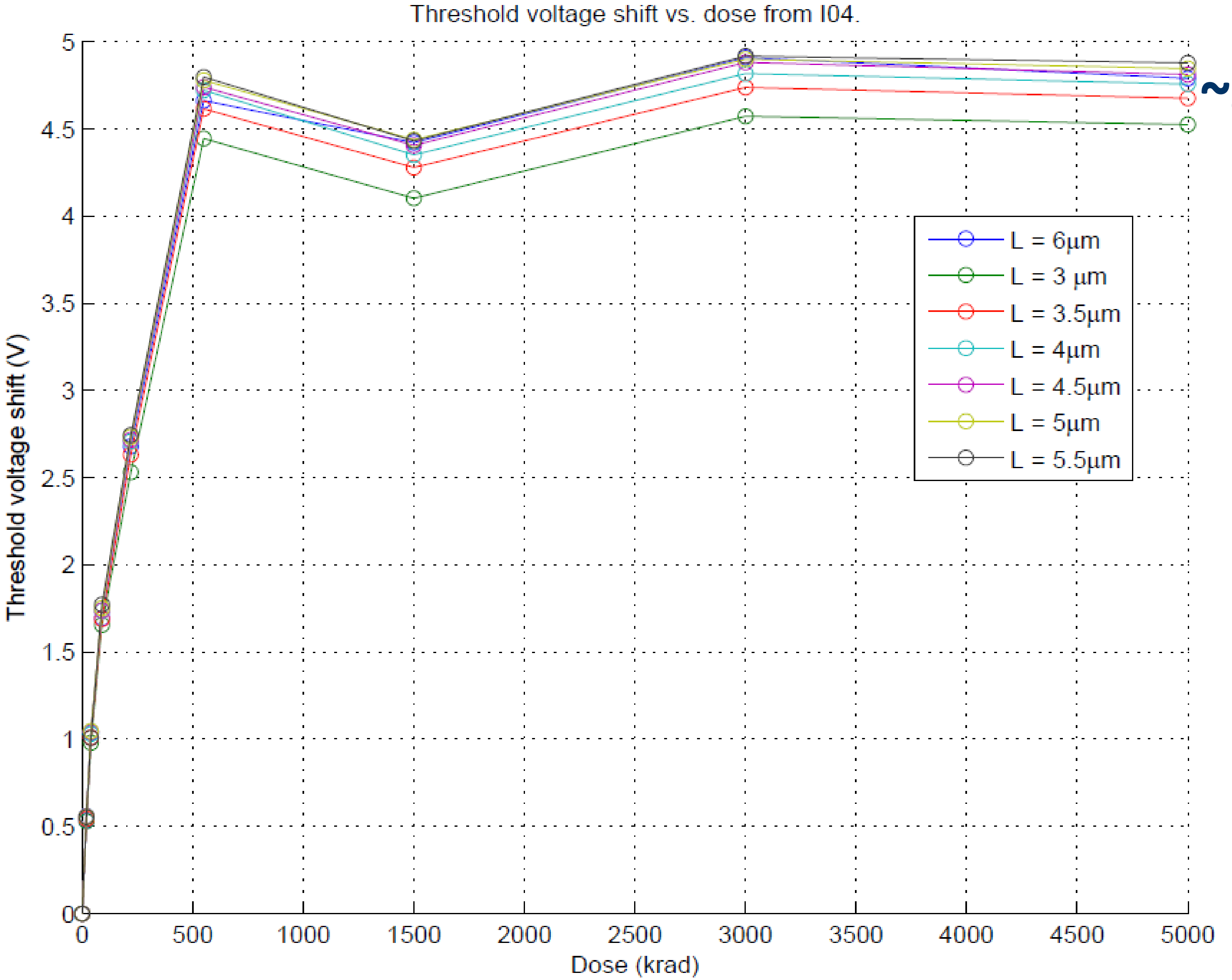
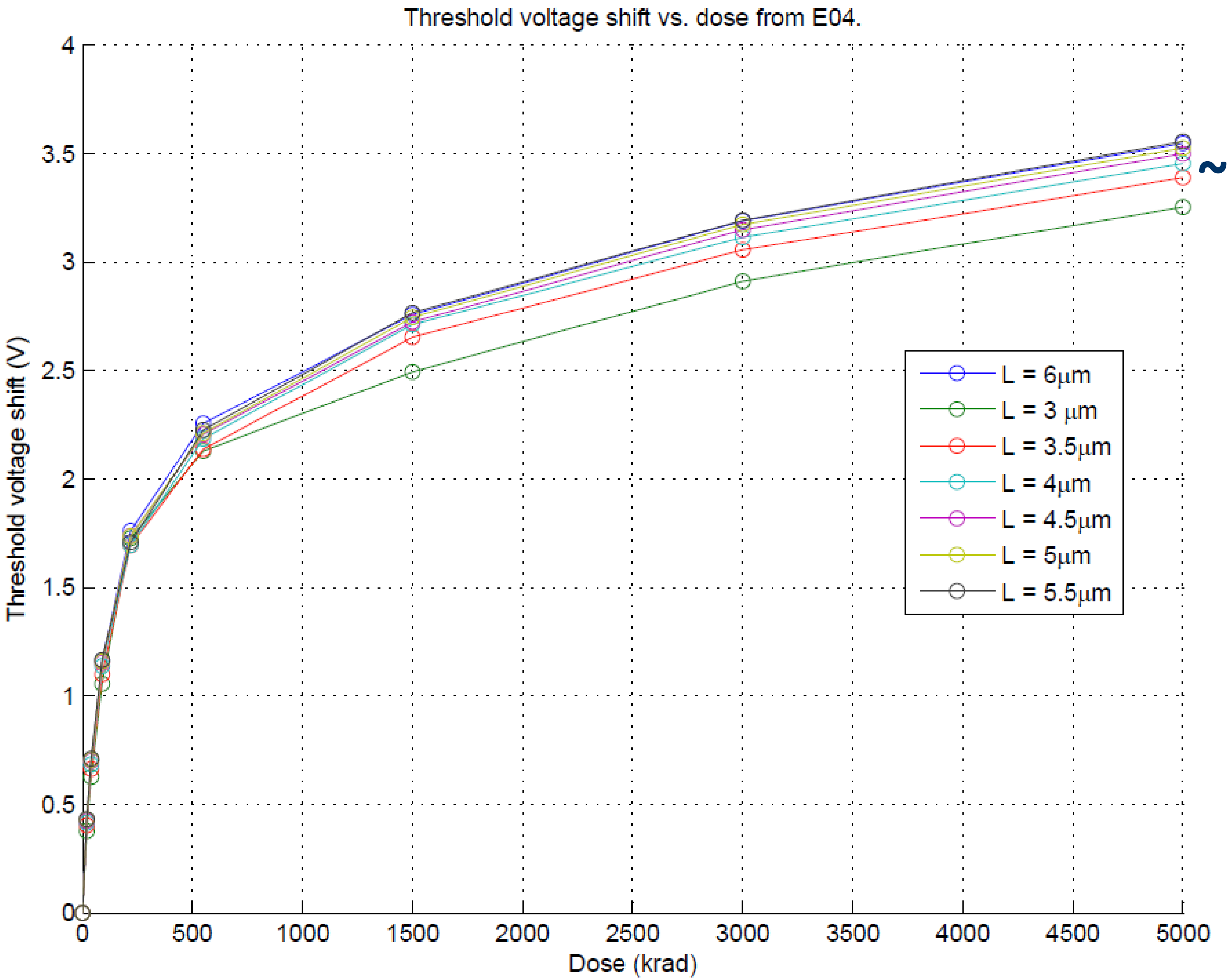
Clear Gate Results, **-5 V** during Irradiation



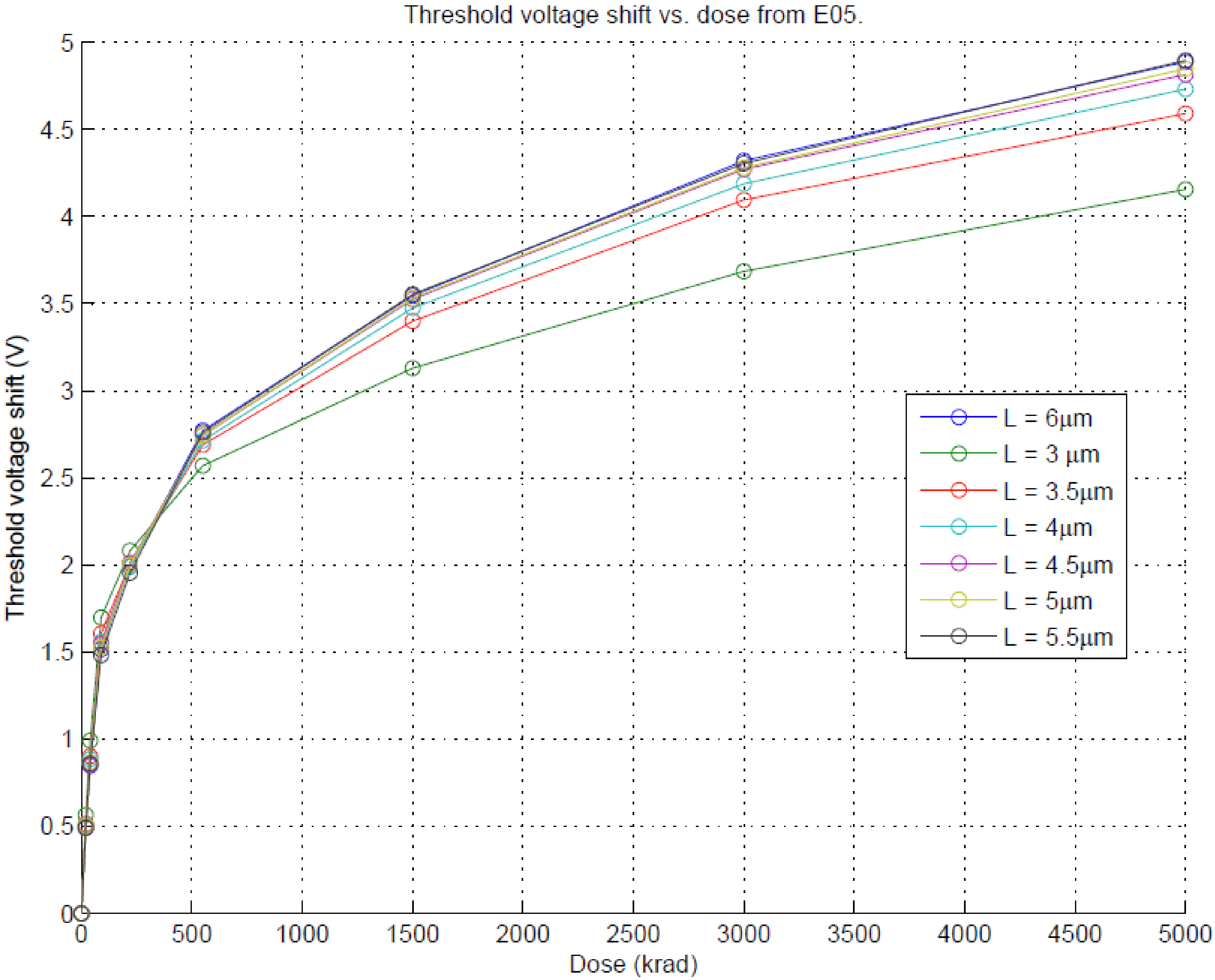
~4.7 V

Clear Gate Results, **0 V** during Irradiation



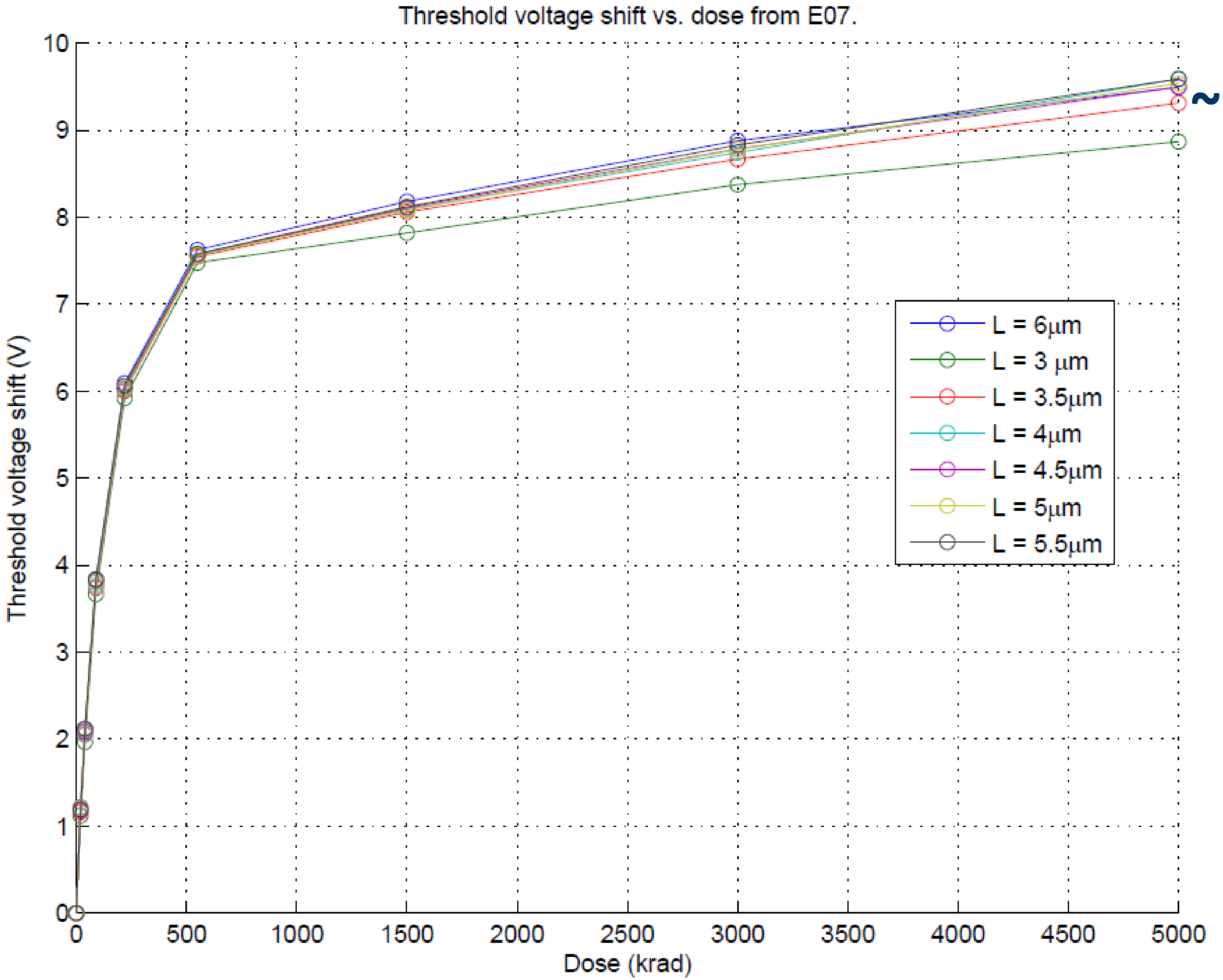
~3.4 V

Clear Gate Results, **+2.5 V** during Irradiation



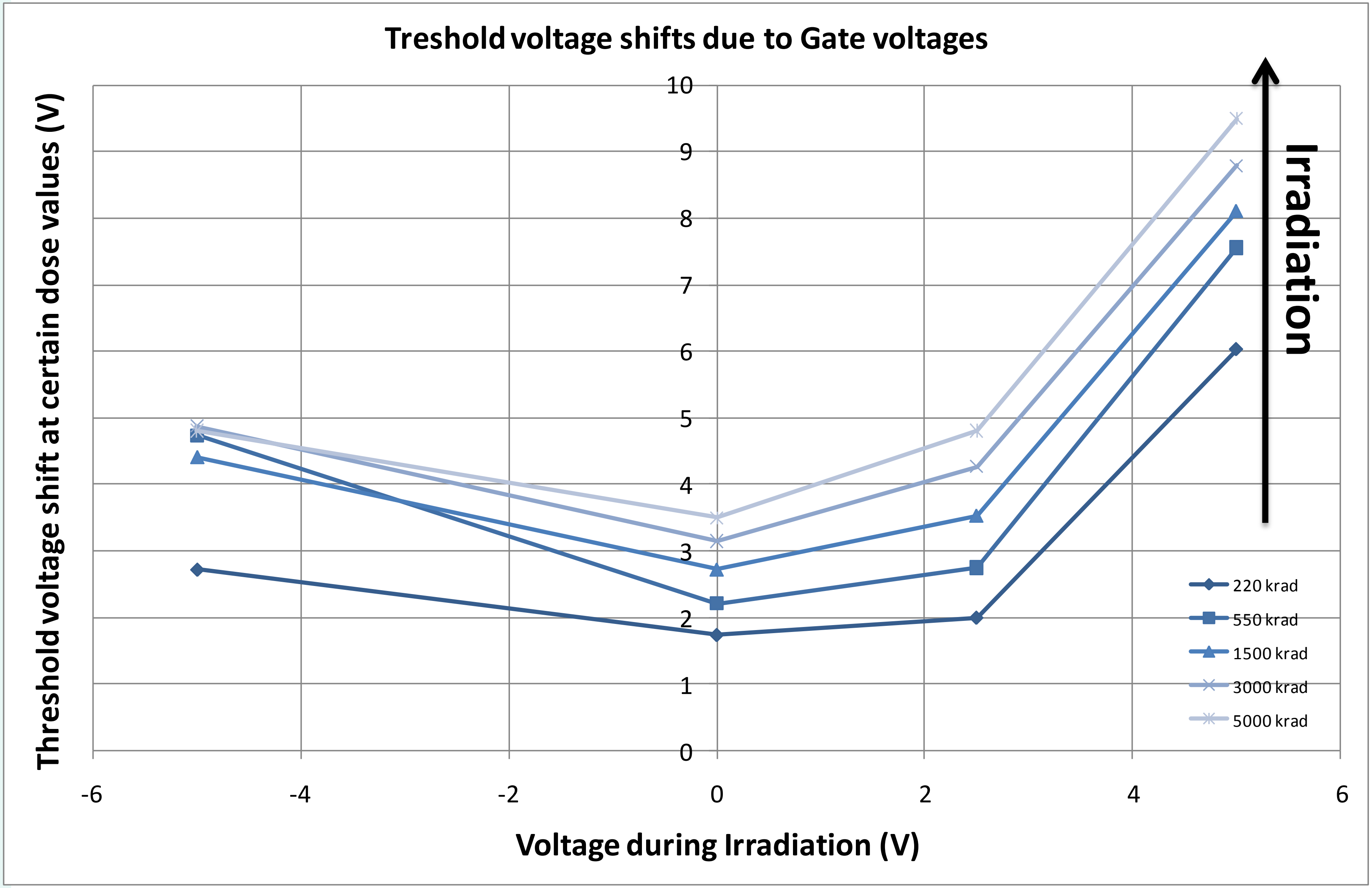
~4.7 V

Clear Gate Results, **+5 V** during Irradiation



~9.4 V

Change in threshold voltage shift due to certain Gate voltages (thick nitride)



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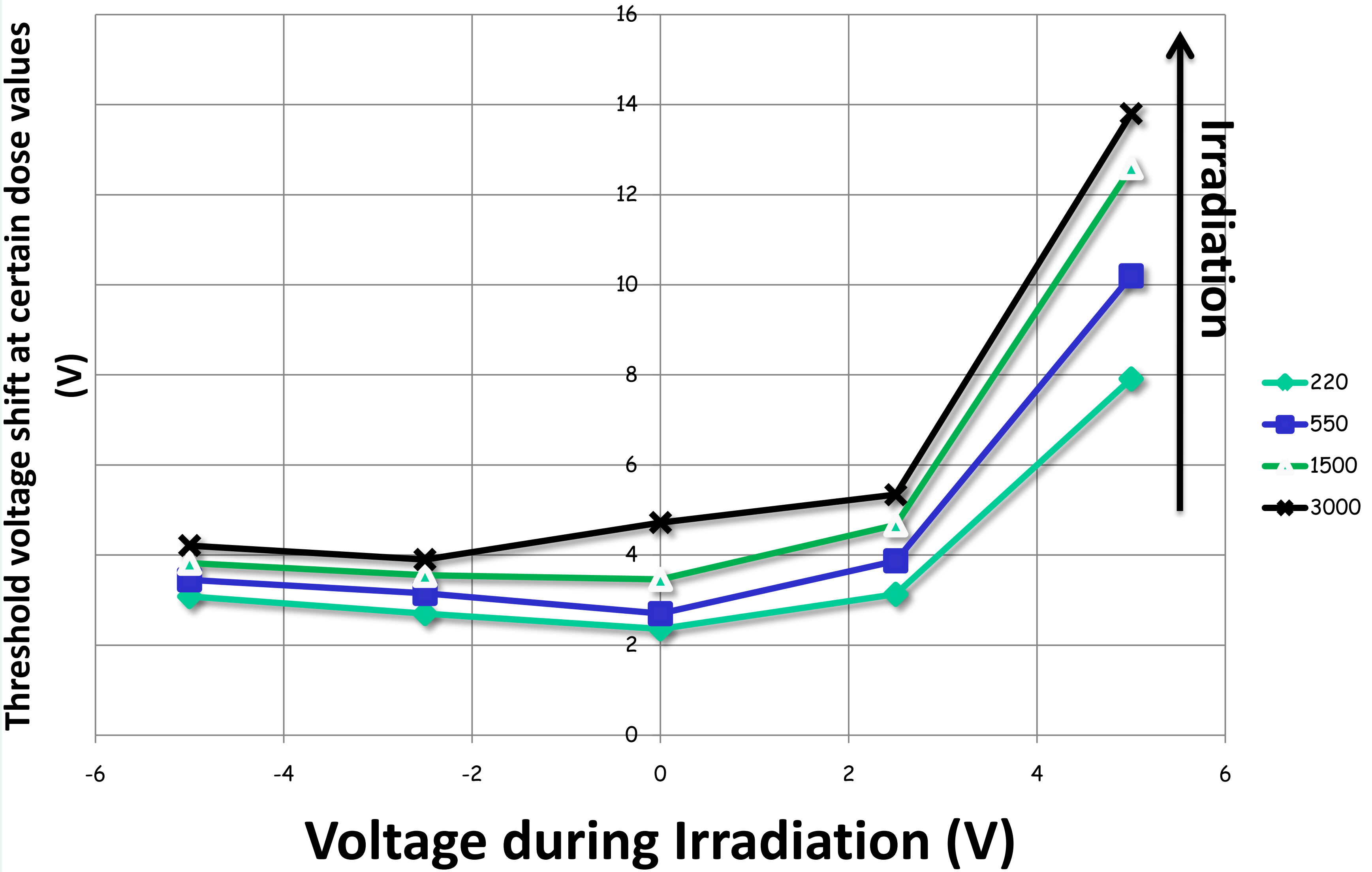


Summary and Outlook

Summary

- DEPFET is a MOSFET
- Ionizing radiation damages gate oxides → trapped positive charge
- Trapped oxide charge alters operating point
- Intra pixel variations → no good!

Outlook

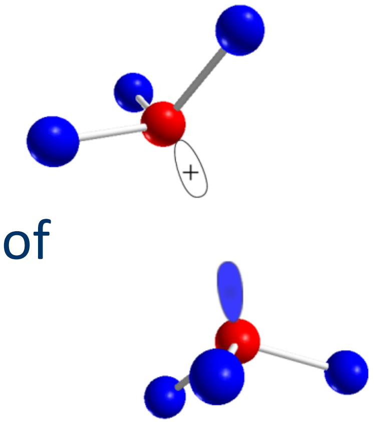
- Additional radiation campaigns with diff. nitride layer thickness will be conducted

Thank you

Backup

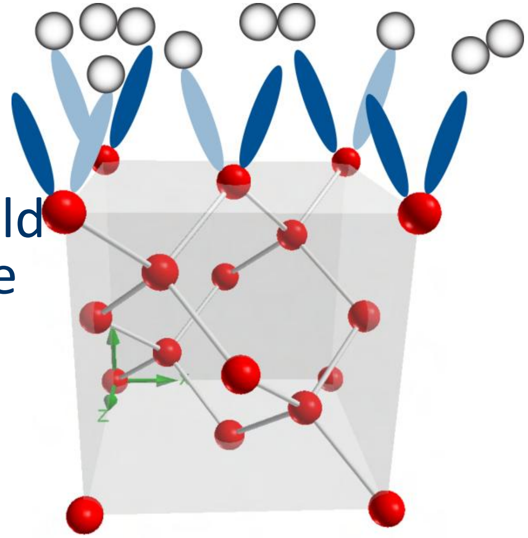
Influence of ionizing radiation

Surface defects – Defects in silicon dioxide

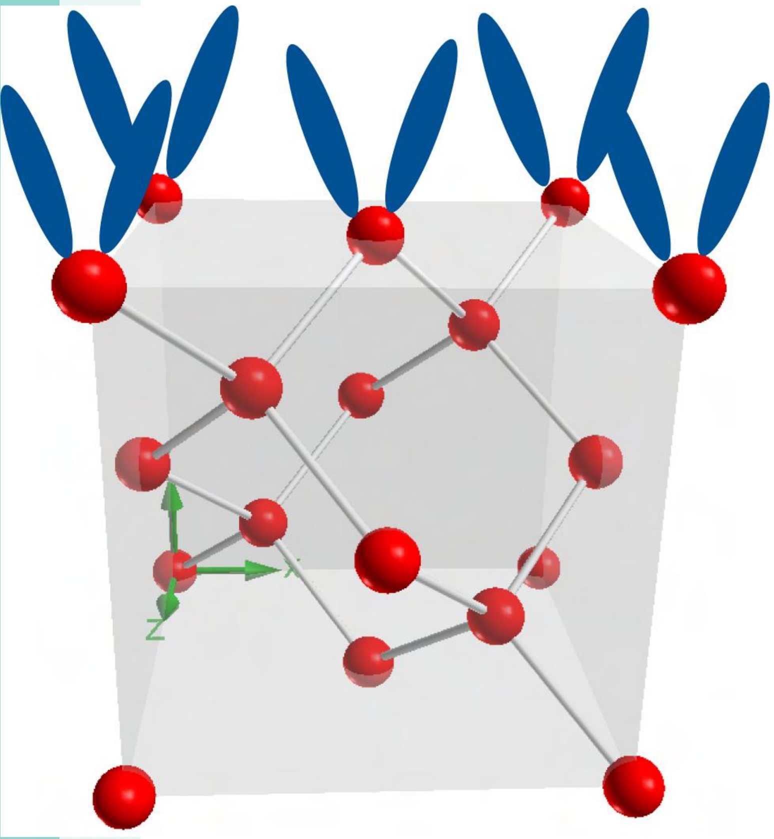


1. Trapped oxide charge
   a) e^-/h^+ pairs created
   b) Electrons have high mobility, swept out of the oxide, holes get trapped
      i. E‘ center → change in $V_{threshold}$

2. Dangling bonds
   a) Hydrogen is used to saturate open bindings (dangling bonds) during production
   b) Ionizing radiation frees protons
   c) Protons travel to defects (near Si-SiO_2 interface)
   d) Creation of H_2 and dangling bonds
      i. Increase in noise(1/f), and subthreshold swing S. Decrease in transconductance g_m



At the Interface between Si and SiO_2…

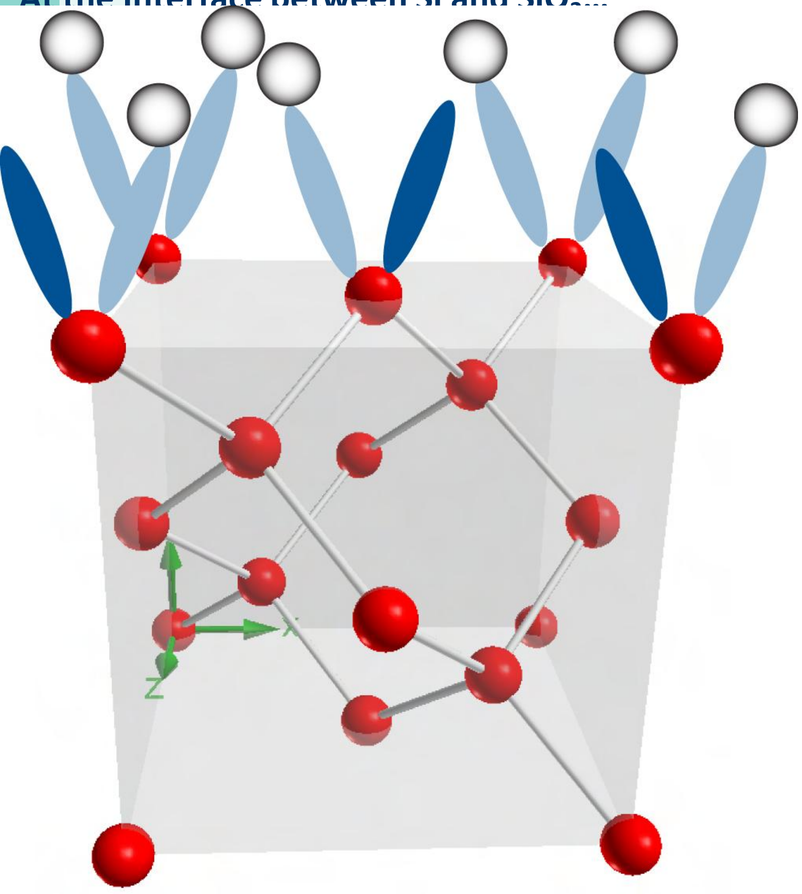


Lattice constants of Si and SiO_2 do not match

open bindings

highly electrically active

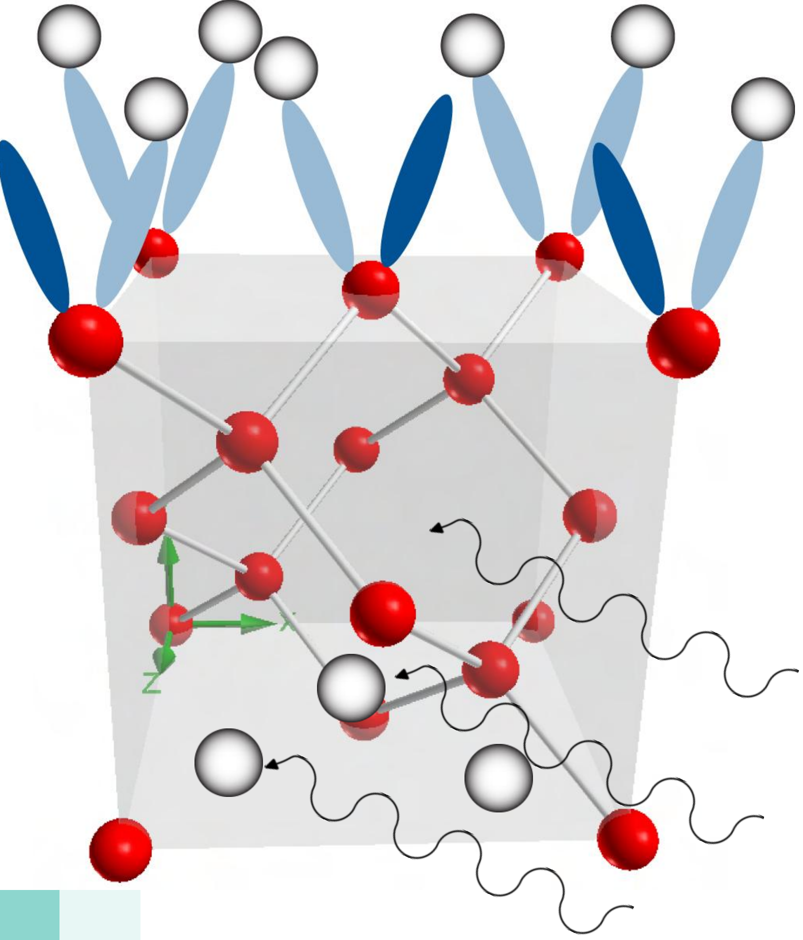
At the Interface between Si and SiO$_2$...



Use Hydrogen (Forming Gas) to get rid of Interface Traps

→ Passivation

At the Interface between Si and SiO_2...



Ionizing radiation creates/frees protons somewhere in the device. Via diffusion and drift Hydrogen nuclei get to the interface.

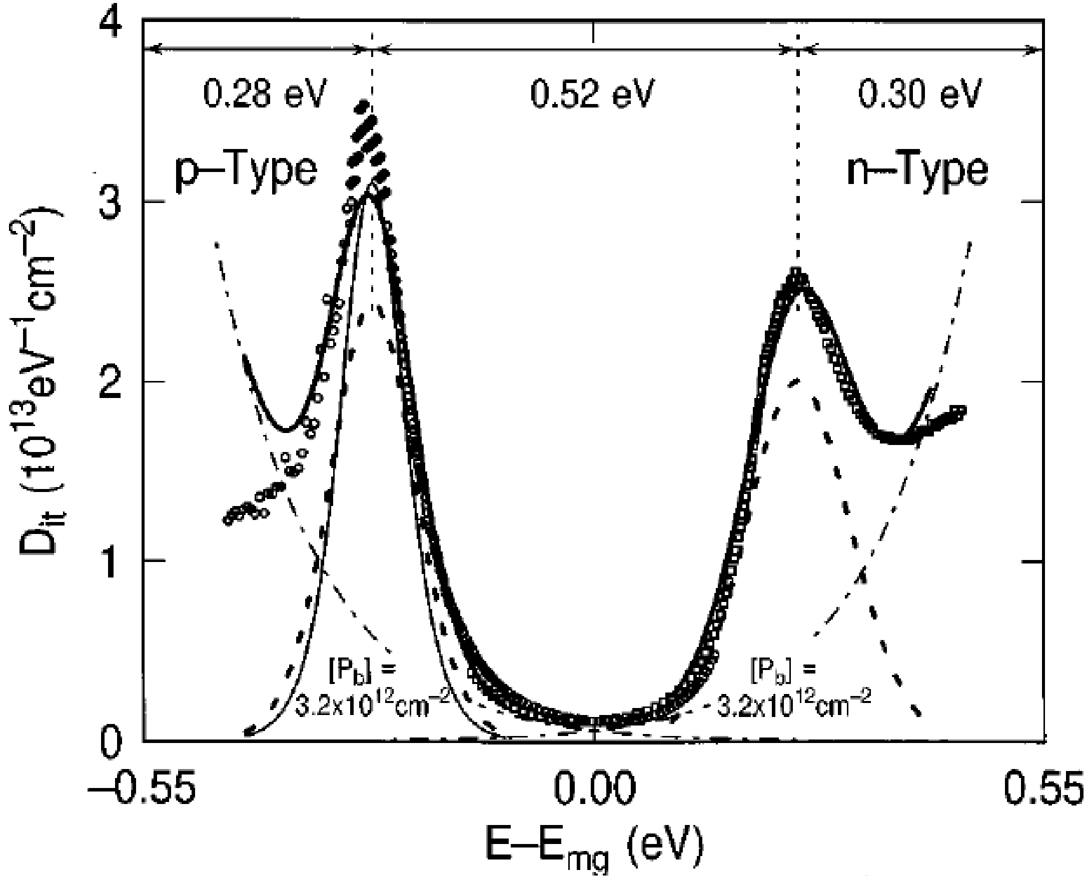
$H^+ + Si\text{-}H \rightarrow Si^+ + H_2$

At the Interface between Si and SiO$_2$…

The most common interface trap is called Pb.

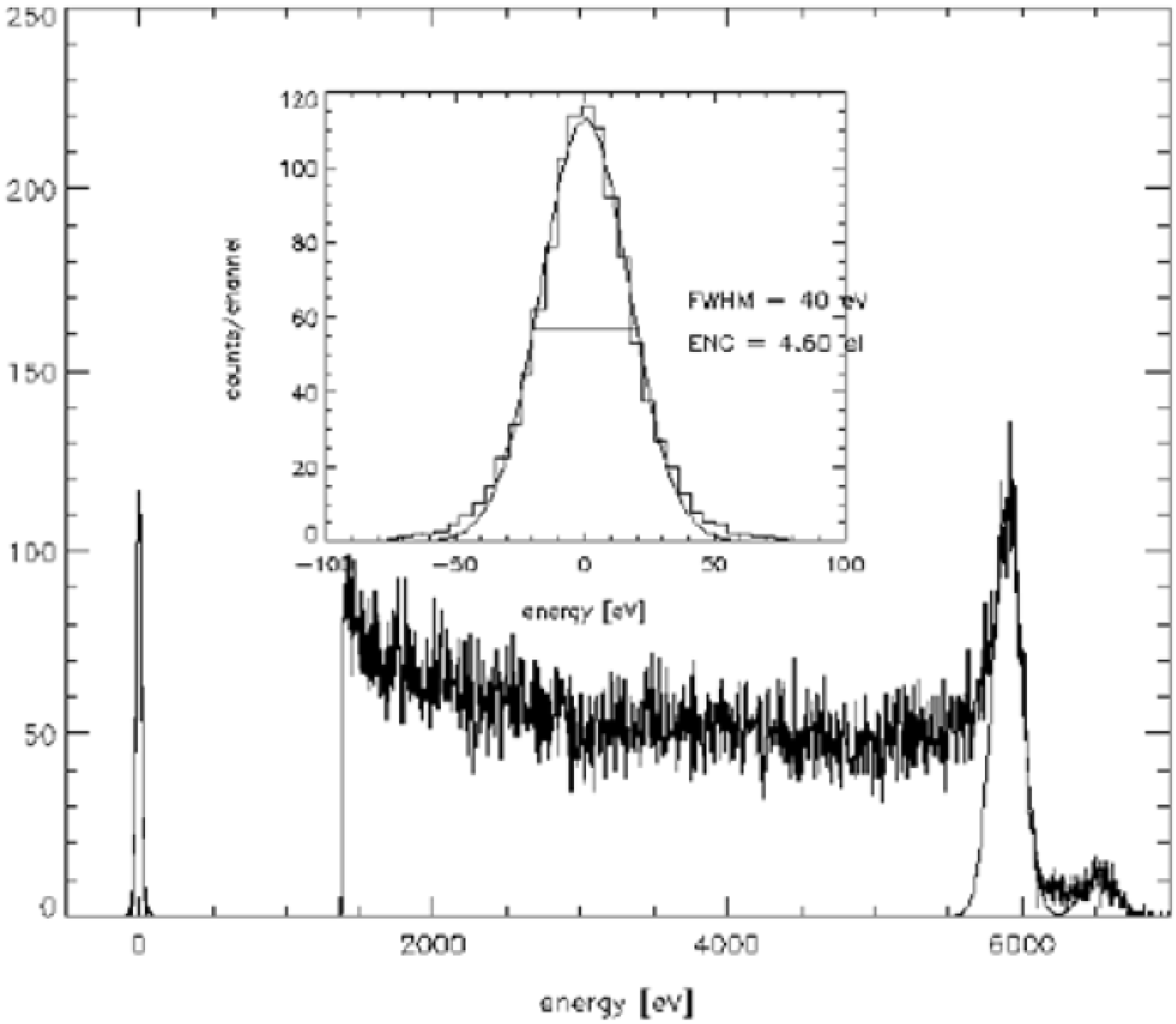
Interface trap is amphoteric = act as Donor or as Acceptor.

In lower Half Band Gap mostly acceptor type, in the upper half donor-type.



Hot-electron induced passivation of silicon dangling bonds at the Si(111)/SiO$_2$ interface
E. Cartier and J. H. Stathis from
Appl. Phys. Lett., Vol. 69, No. 1, 1 July 1996

Noise after Irradiation



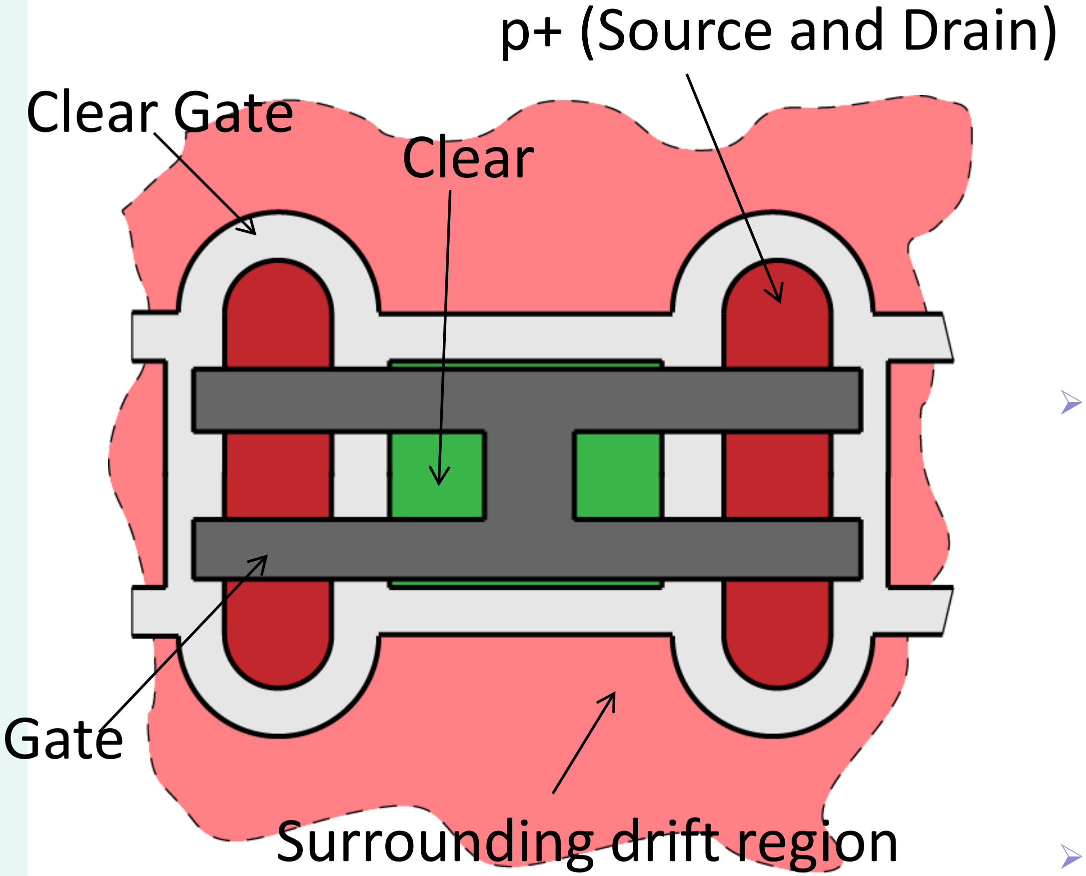
(b) Fe^{55} spectra after 8MRad

4.6 e^- ENC after 8 Mrad (^{55}Fe), PXD5

SNR=27 @ ^{109}Cd (22keV)

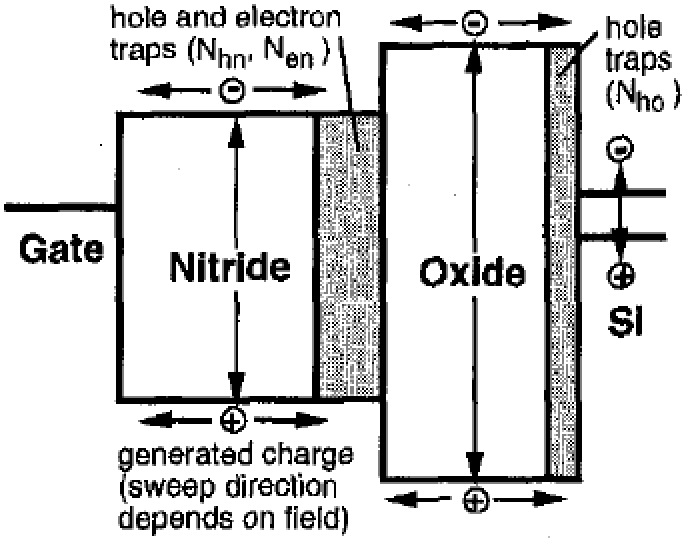
S. Rummel

Ionizing radiation in gate region



- Gate region exhibits a more homogeneous voltage region than the clear gate (very thick oxide in between)
  → common shift adjustable
- Problem: inhomogeneous irradiation along z in the detector
  → Solution: segmentation of module
- Irradiations with diff. Nitride thicknesses show good results for thinnest layer.

Trapping in insulator layer



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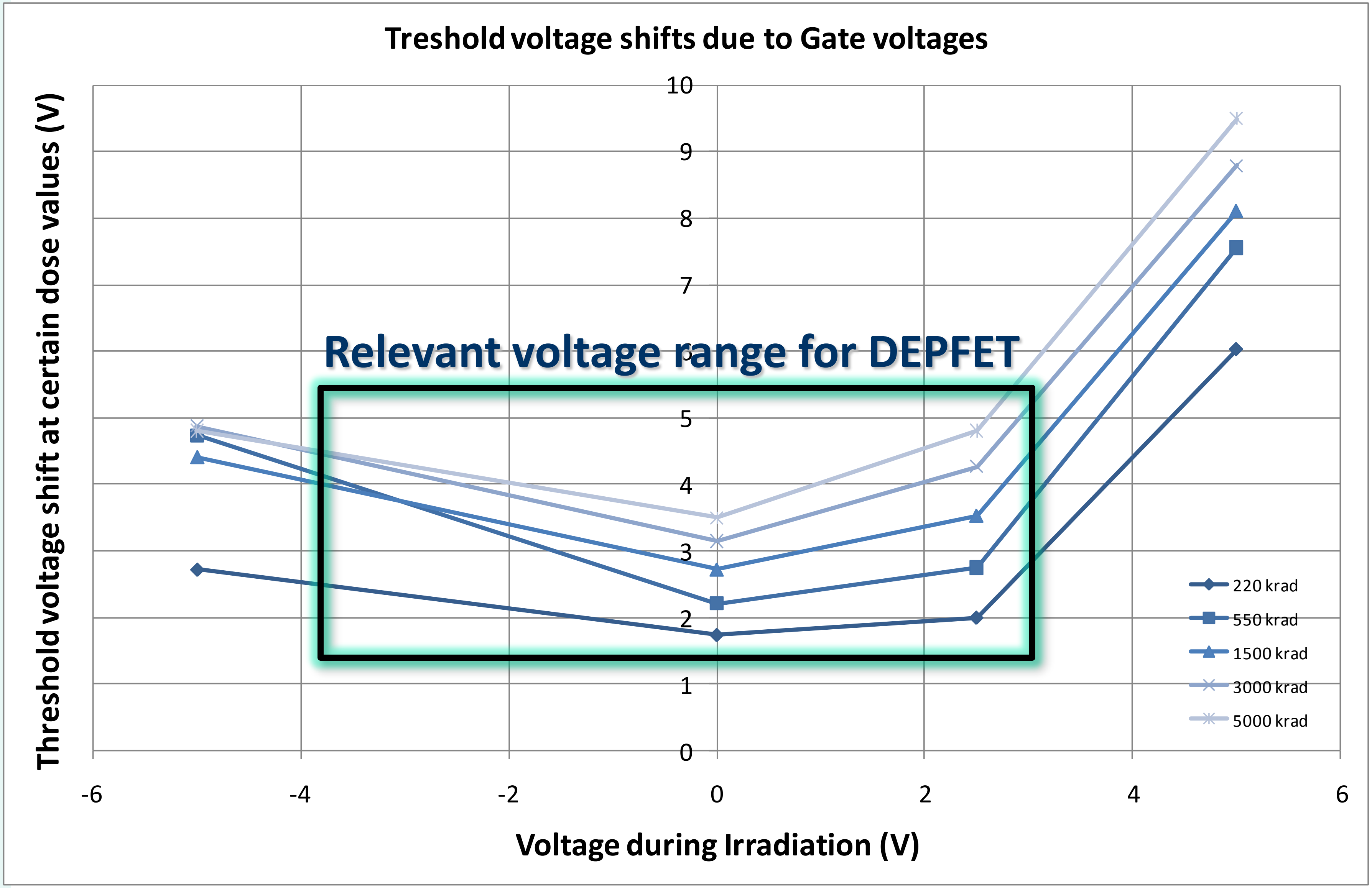
+V_G

1. Holes in oxide to Si-SiO_2 interface
2. Holes in Si_3N_4 and electrons from SiO_2 to N-O interface
3. Recombination rate in Si_3N_4 lower than in SiO_2 (+trap density precursors)
   → more e^- trapped at N-O
4. Build-up of e^- reduces field in oxide → saturation

-V_G
Field always present

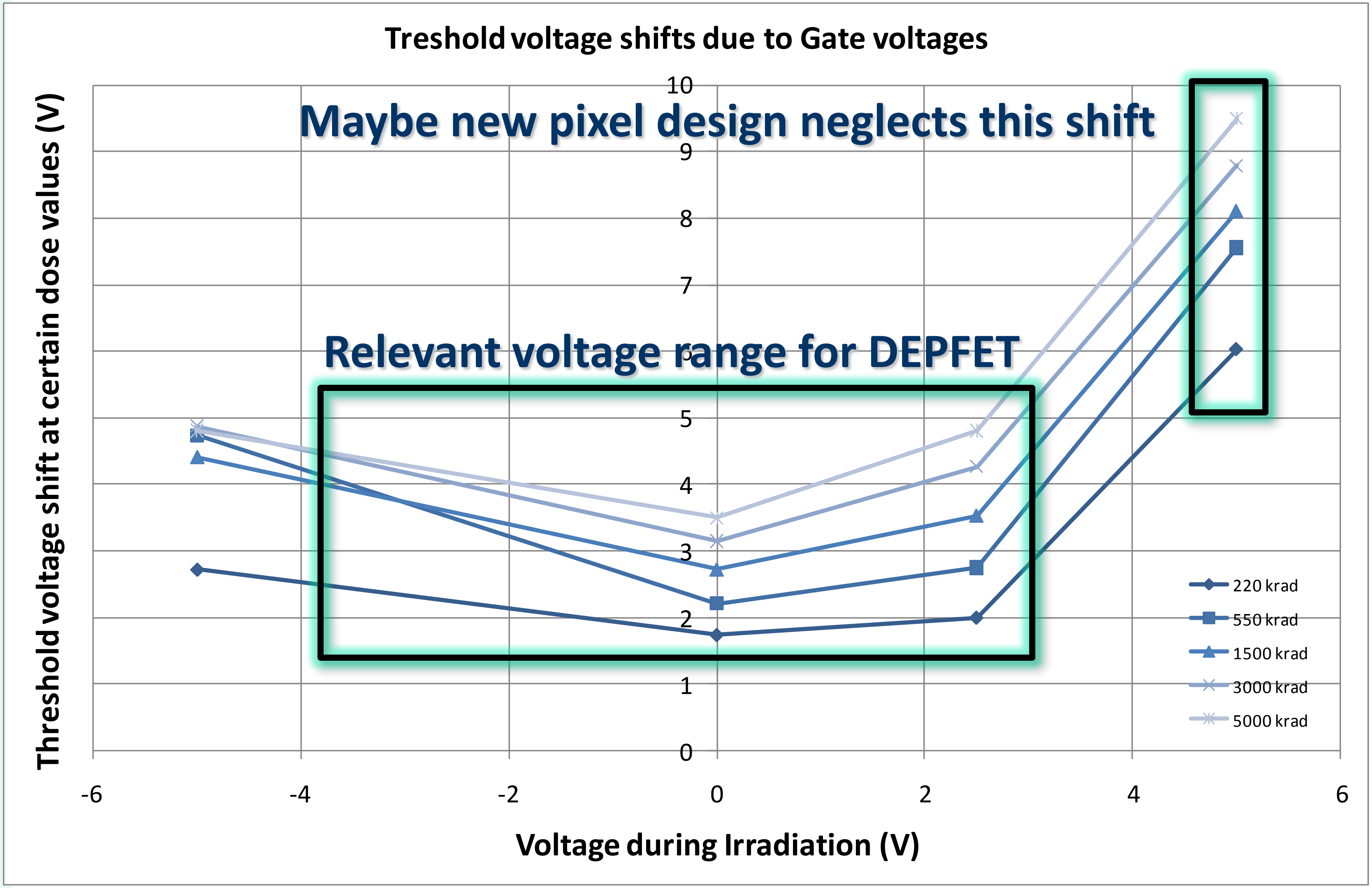
Thick Si_3N_4
→ Reduces field in ox (capacitance voltage divider) → saturation

Threshold voltage shifts due to Gate voltages



Relevant voltage range for DEPFET

Threshold voltage shifts due to Gate voltages



Maybe new pixel design neglects this shift

Relevant voltage range for DEPFET