SiPMs with bulk integrated resistors
– Future perspectives –

- Concept of SiPMs with Bulk Integrated Quench Resistors – SiPMl concept
- First results from the prototype production
- Future perspectives

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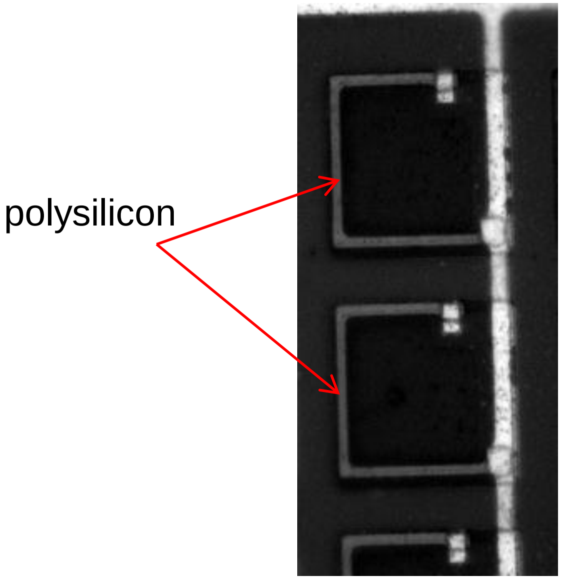
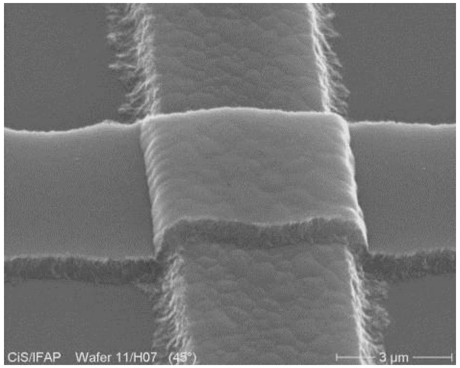
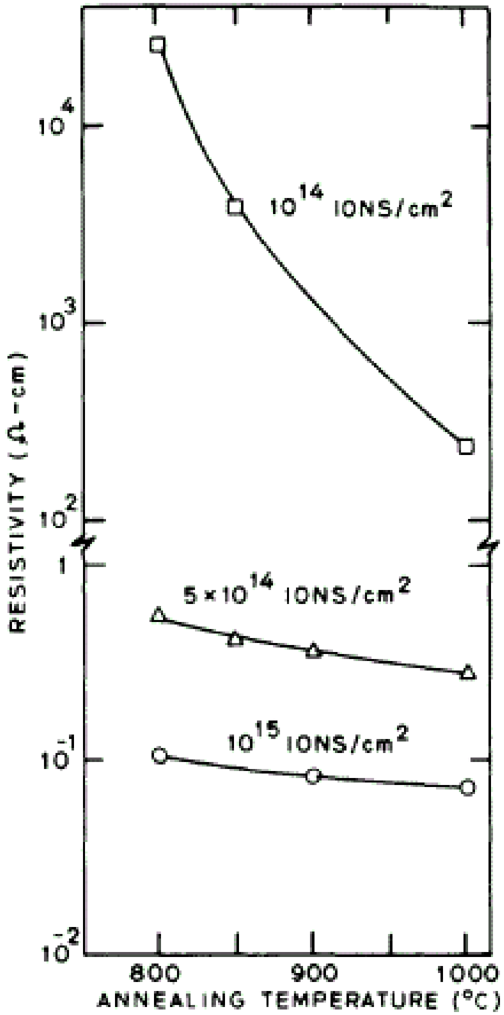
Polysilicon Quench Resistors







M. Mohammad et al.

‘Dopant segragation in polycrystalline silicon‘,

J. Appl. Physics, Nov.,1980

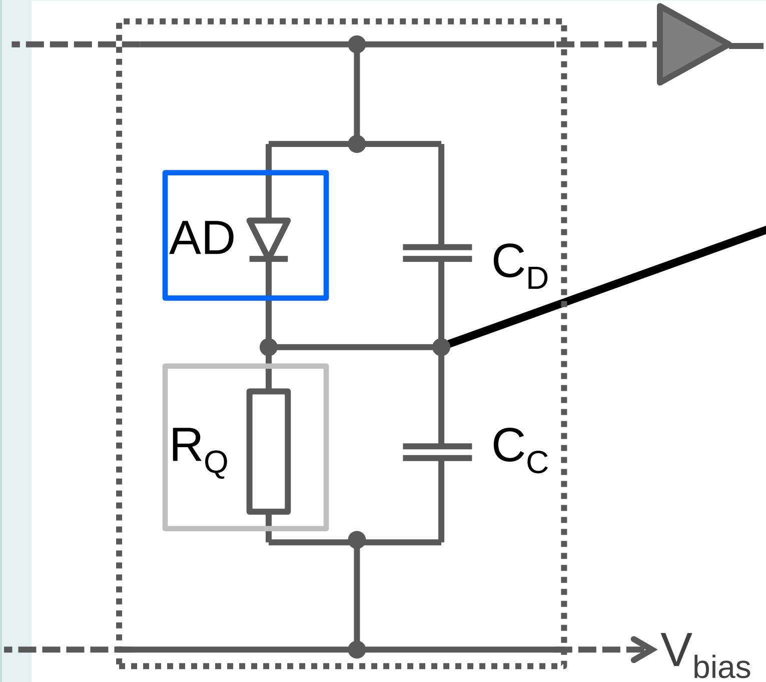
Complex production step

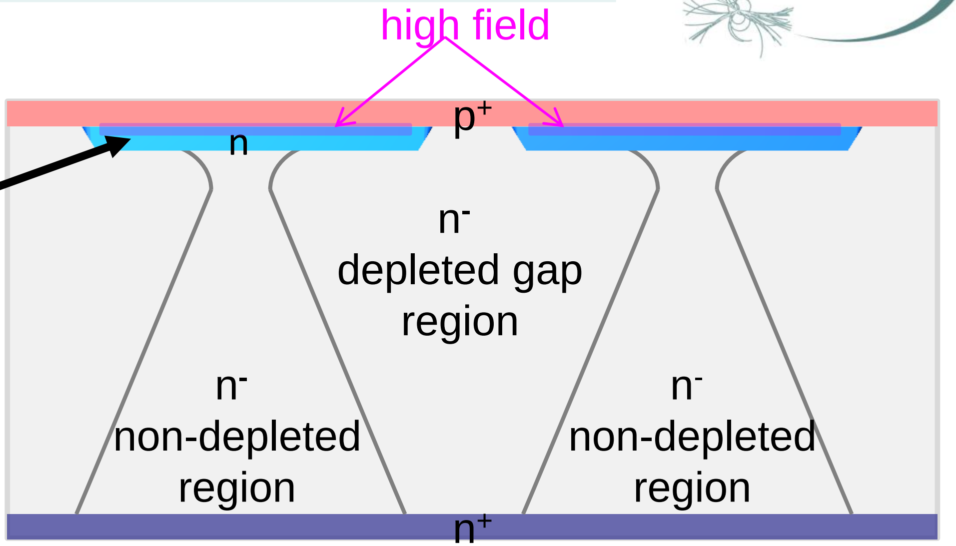
Critical resistance range

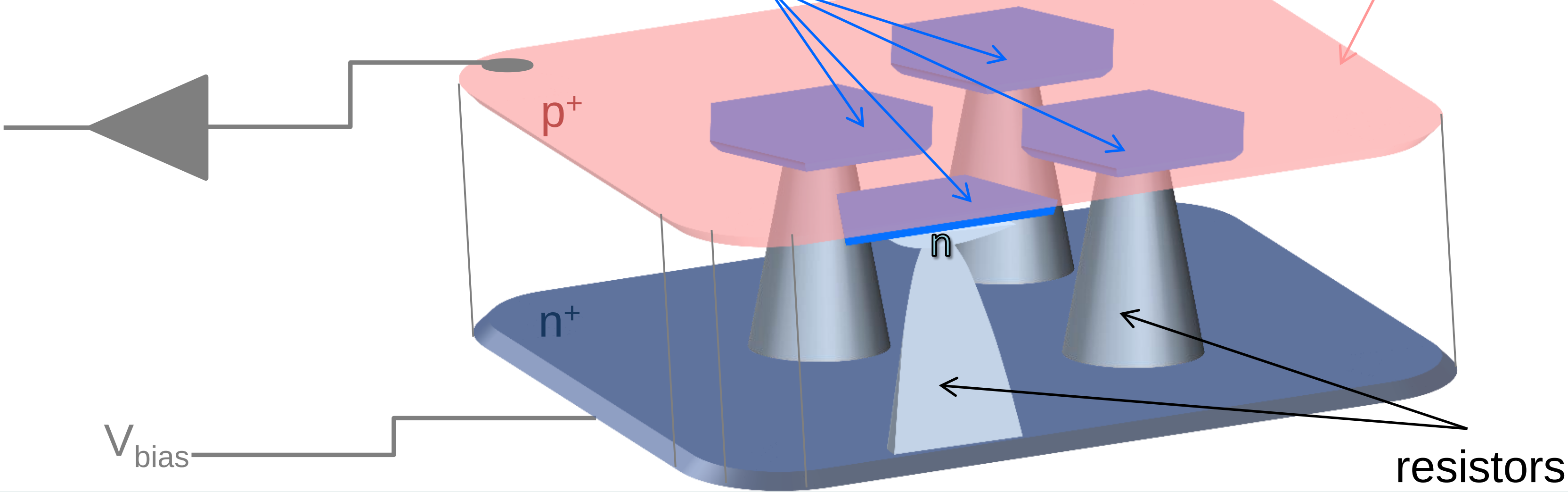
influenced by: grain size, dopant segregation in grain boundaries, carrier trapping, barrier height

Rather unreliable process step and an absorber for light

SiPM cell components → SiMPI approach

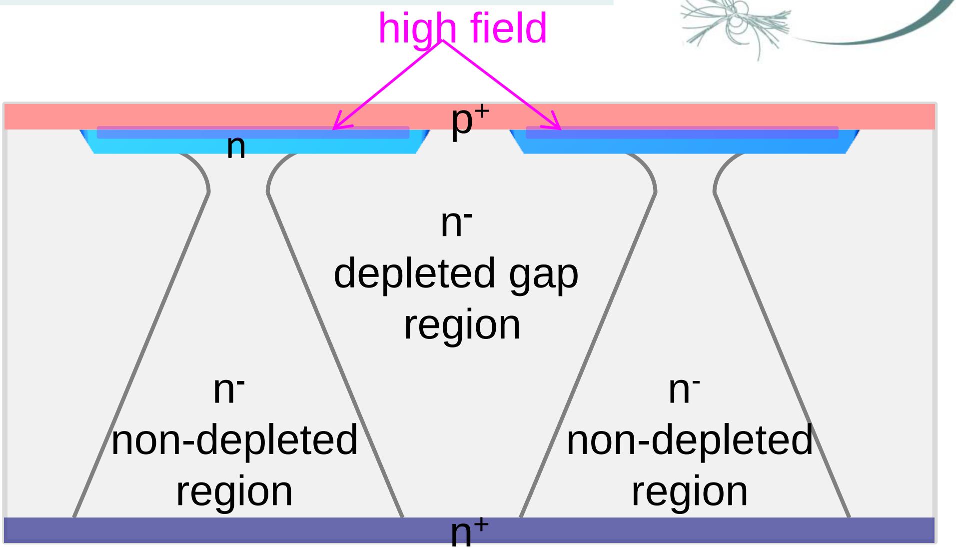


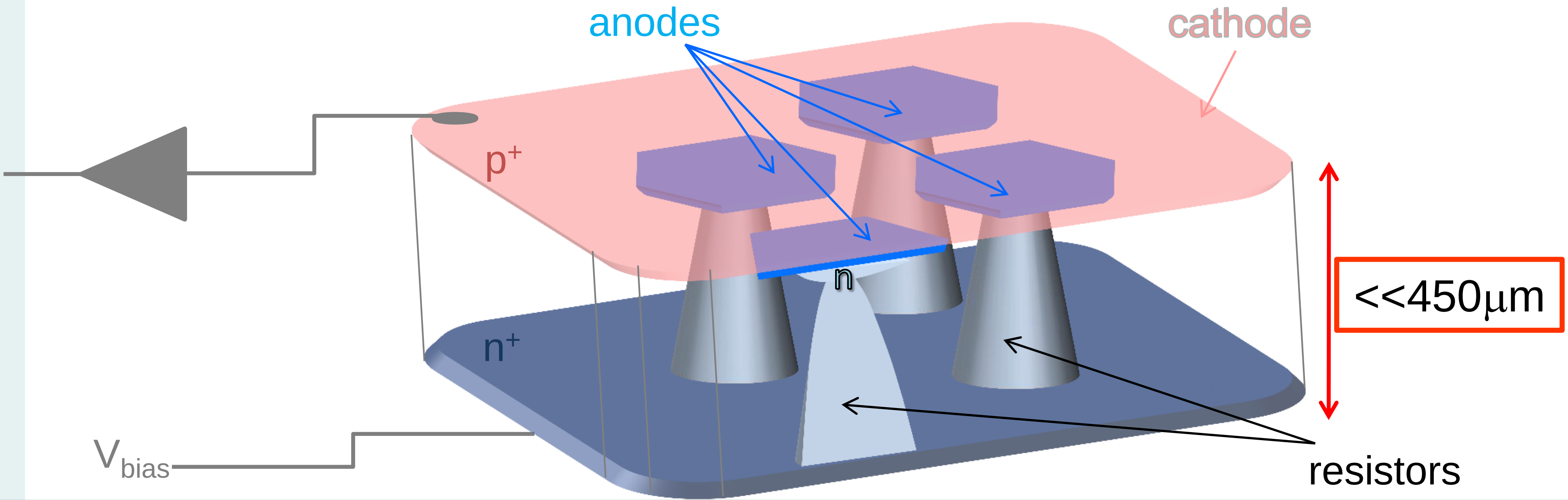




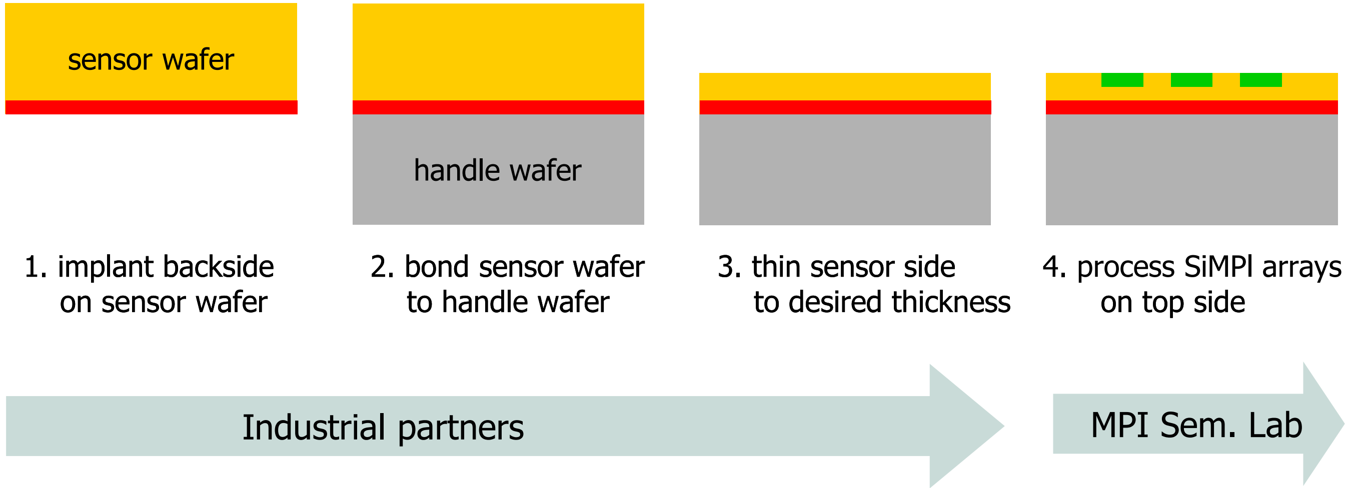
SiPM cell components → SiMPI approach

Resistor matching requires thin wafers !





SOI wafers



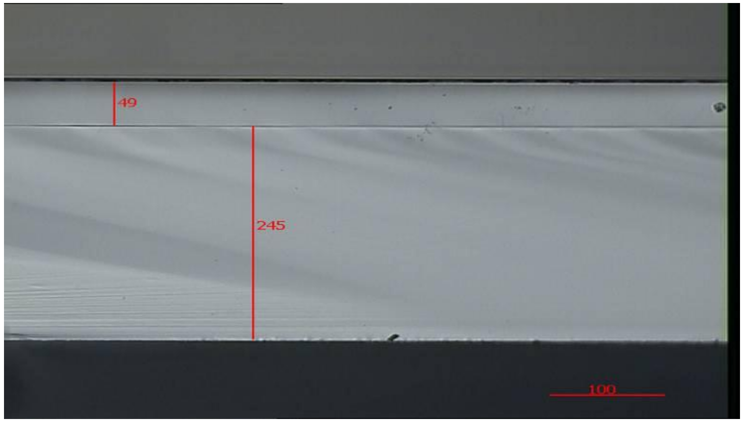
sensor wafer

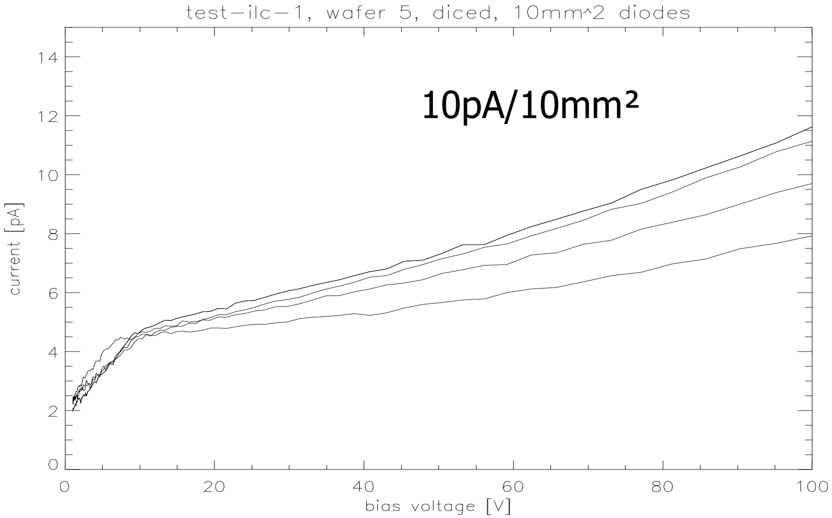
handle wafer

1. implant backside on sensor wafer
2. bond sensor wafer to handle wafer
3. thin sensor side to desired thickness
4. process SiMPl arrays on top side

Industrial partners

MPI Sem. Lab





10pA/10mm²

Simulations

Not a simple resistor problem

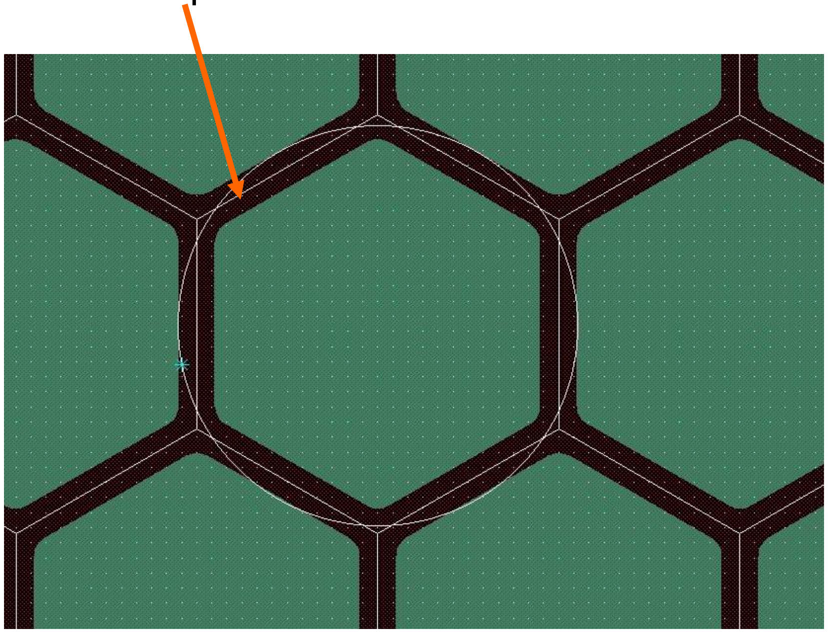
- bulk resistivity
- sensor thickness
- pitch size
- gap size

Influence

- carrier diffusion from top and bottom layer into the resistor bulk
- sideward depletion

➔Extended device simulations performed and showed promising results for both small (25μm) and big (100μm) cells.

cylindrical approximation of hexagons for quasi 3d simulation



Ninkovic et al., NIM A, 610, Issue 1

Advantages and Disadvantages

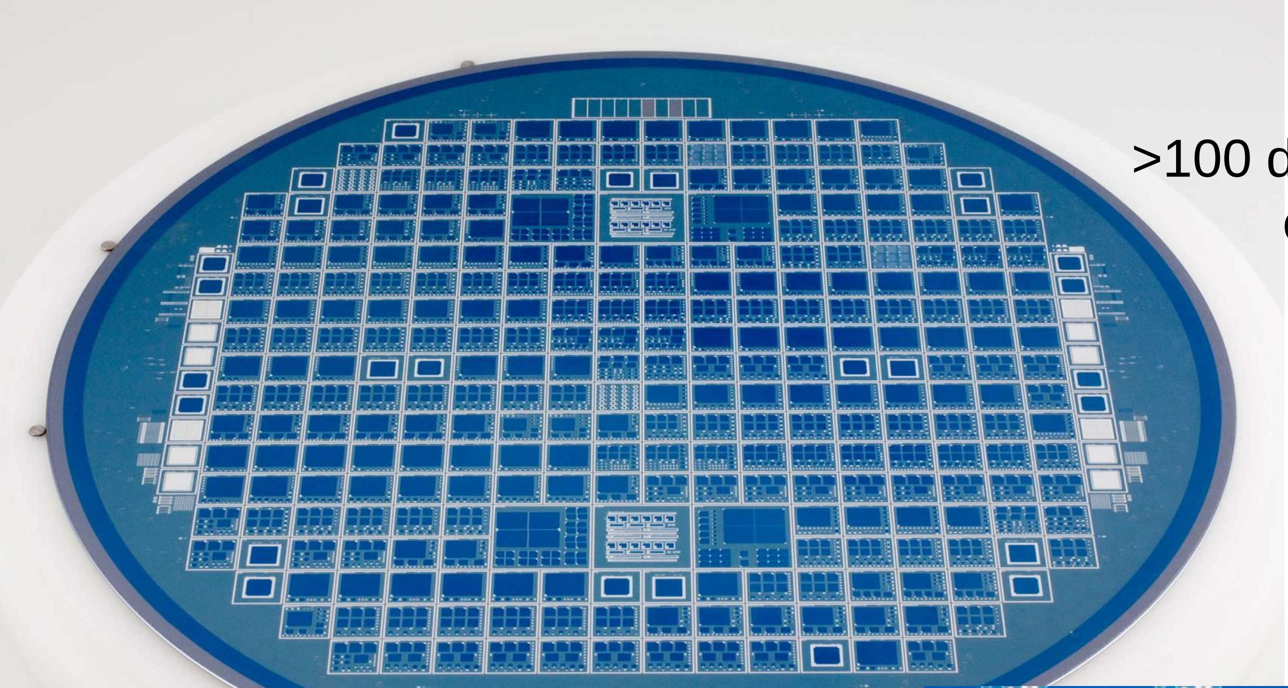
Advantages:

- no need of polysilicon
- free entrance window for light, no metal necessary within the array
- coarse lithographic level
- simple technology
- inherent diffusion barrier against minorities in the bulk -> less optical cross talk

Drawbacks:

- required depth for vertical resistors does not match wafer thickness
- wafer bonding is necessary for big pixel sizes
- significant changes of cell size requires change of the material
- vertical ‘resistor‘ is a JFET -> parabolic IV -> longer recovery times

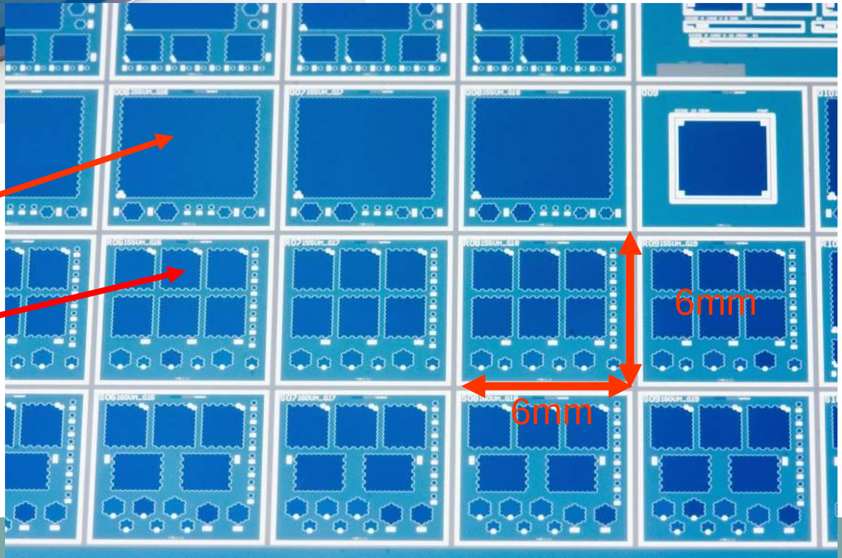
Prototype production



>100 different geometrical combinations

30x30 arrays

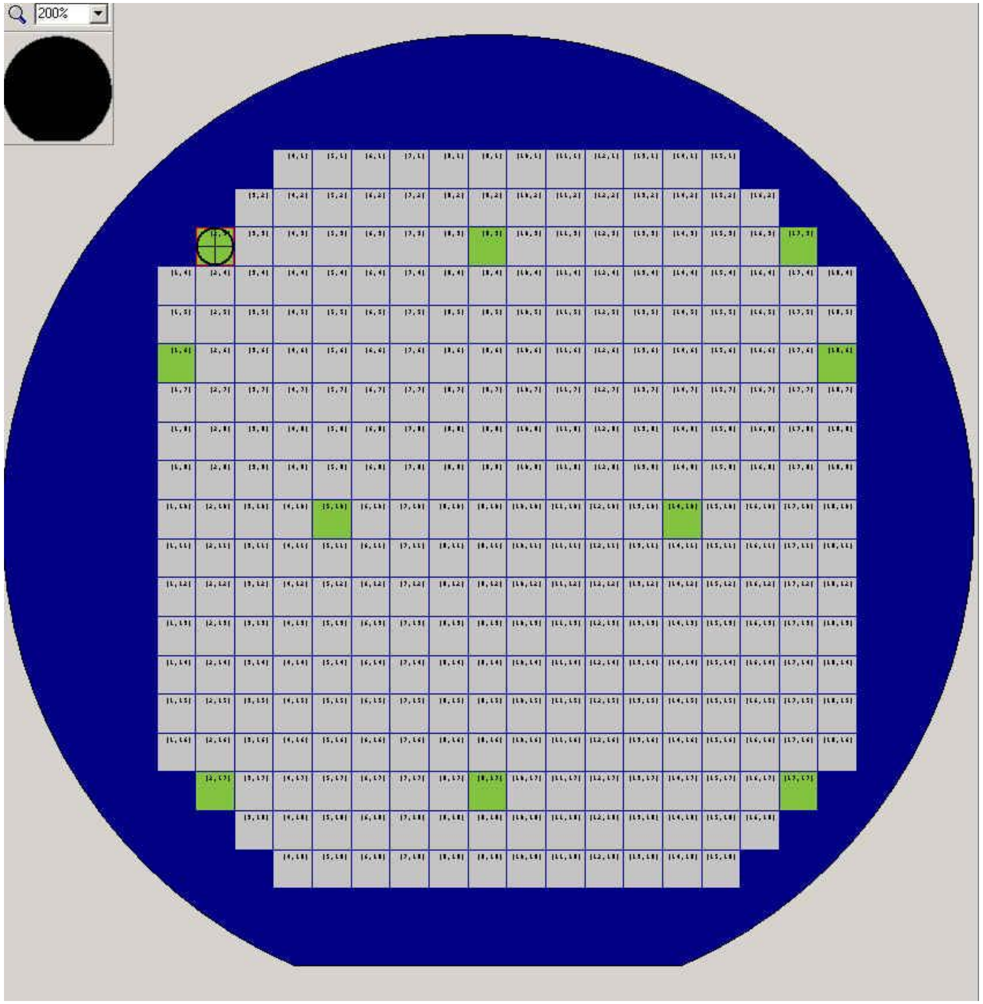
10x10 arrays



Bulk doping

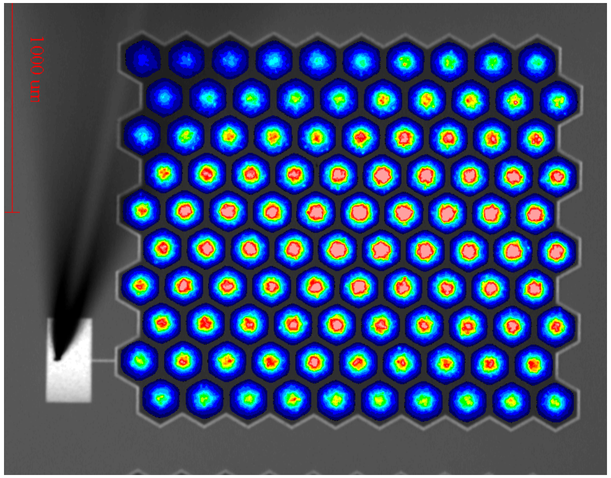
- Critical parameter
- Bulk doping variation of the top wafers measured on 10 diodes*/wafer (CV)

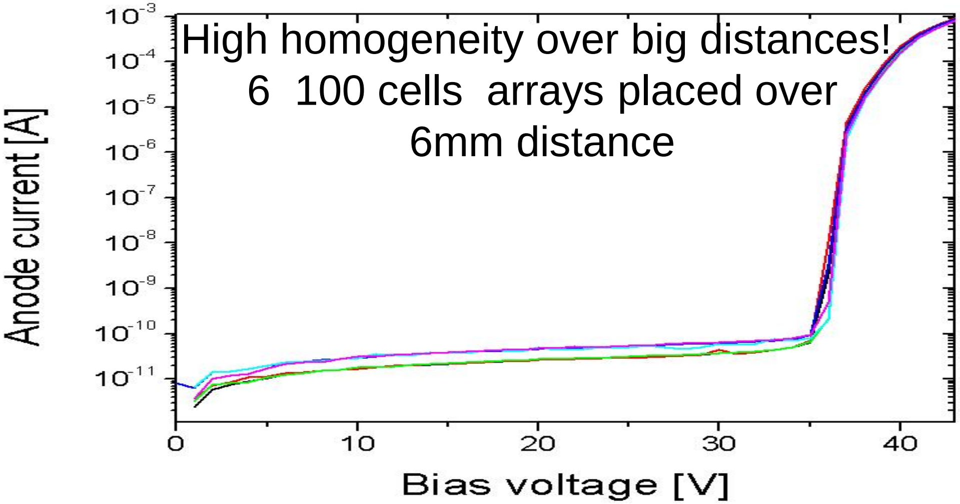
  (*test diodes without high energy implantation)



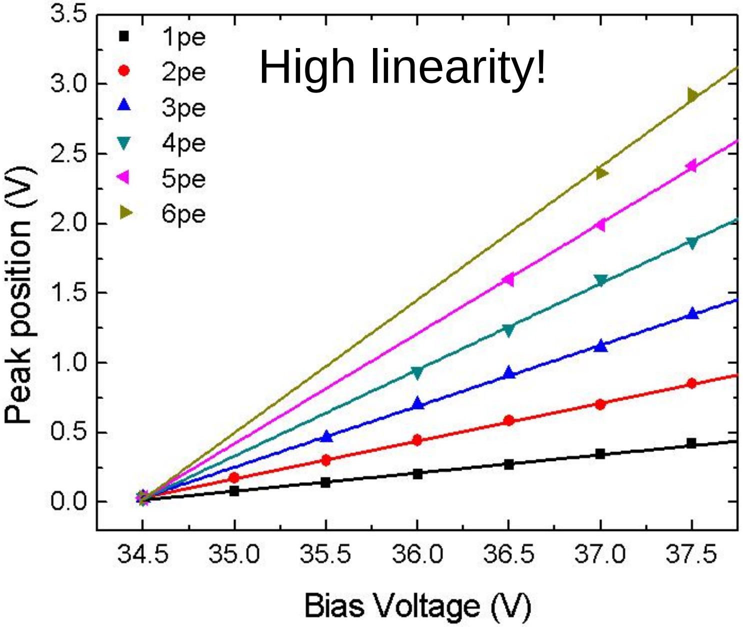
Standard deviation
1—2% of the mean value
over the wafer

Prototype production

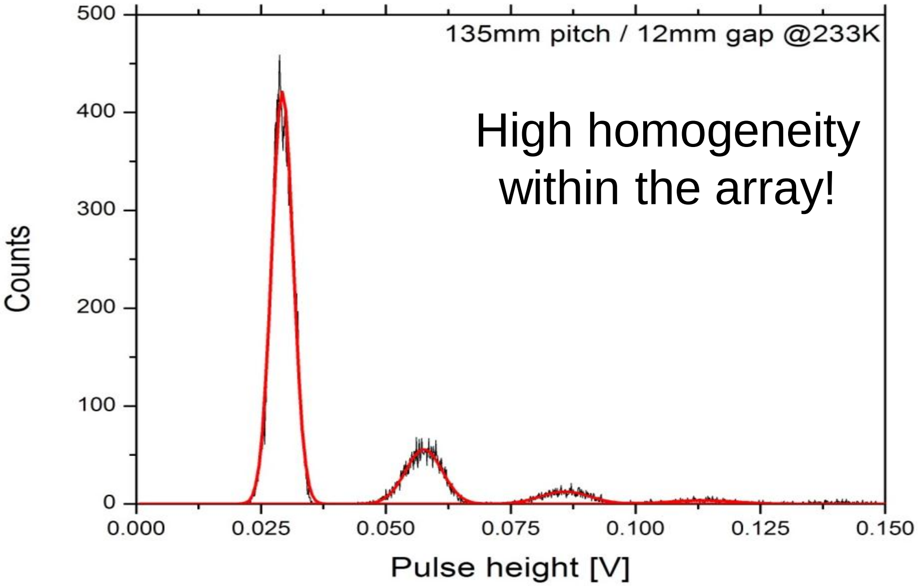




High homogeneity over big distances!
6 100 cells arrays placed over
6mm distance



High linearity!



High homogeneity
within the array!

Fill factor & Cross Talk & Photon Detection Efficiency

Produced SiMPI devices have the world record in the fill factors!

Pitch / Gap	Fill factor	Cross talk meas. (ΔV=2V)	PDE calc. (ΔV=2V)	PDE calc. (ΔV=5V)
130μm / 10μm	85.2%	29%	39%	61%
130μm / 11μm	83.8%	27%	38%	60%
130μm / 12μm	82.4%	25%	37%	59%
130μm / 20μm	71.6%	15%	32%	52%

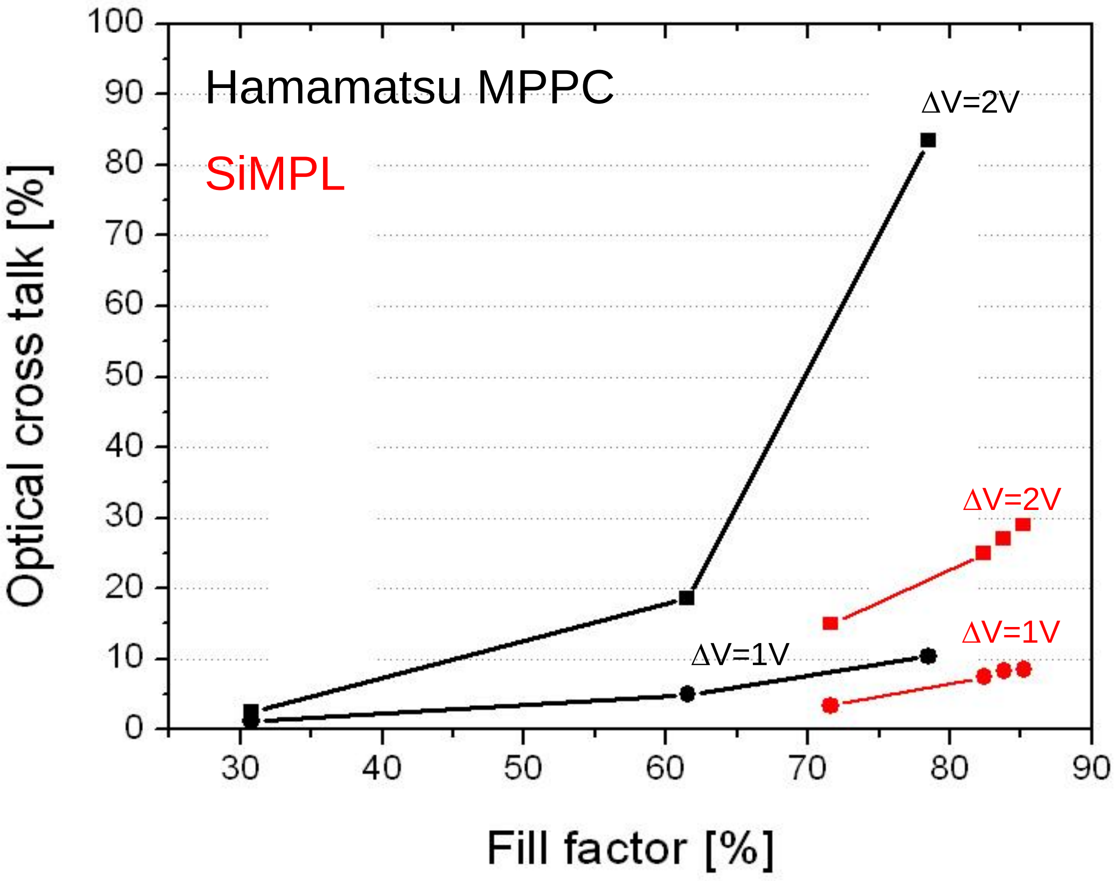
PDE estimate:

- Optical entrance window: 90% @400nm
- Geiger efficiency : 50% @ 2V overbias 80% @5V overbias

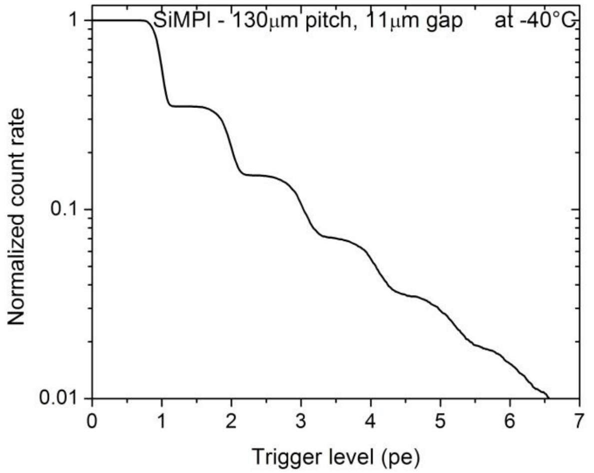
Fill factor & Cross Talk

Produced SiMPl devices have the world record in the fill factors and still lower cross talk!

No special cross talk suppression technology applied
just intrinsic property of SiMPl devices



Quenching ability



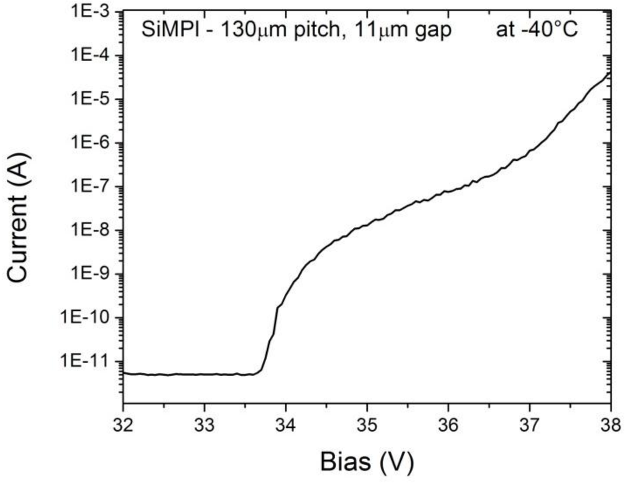
In an ideal device the dark current through a diode is given by:

$$I = DC \cdot G \cdot e$$

with *DC* dark count rate, *G* internal gain and elementary charge *e*.

Contribution of optical crosstalk (OCT) has to be taken into account

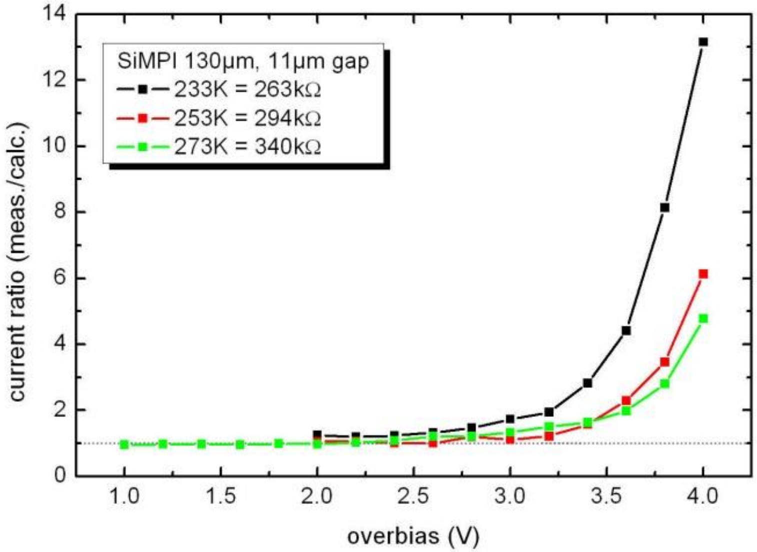
Dark counts and gain → a theoretical current



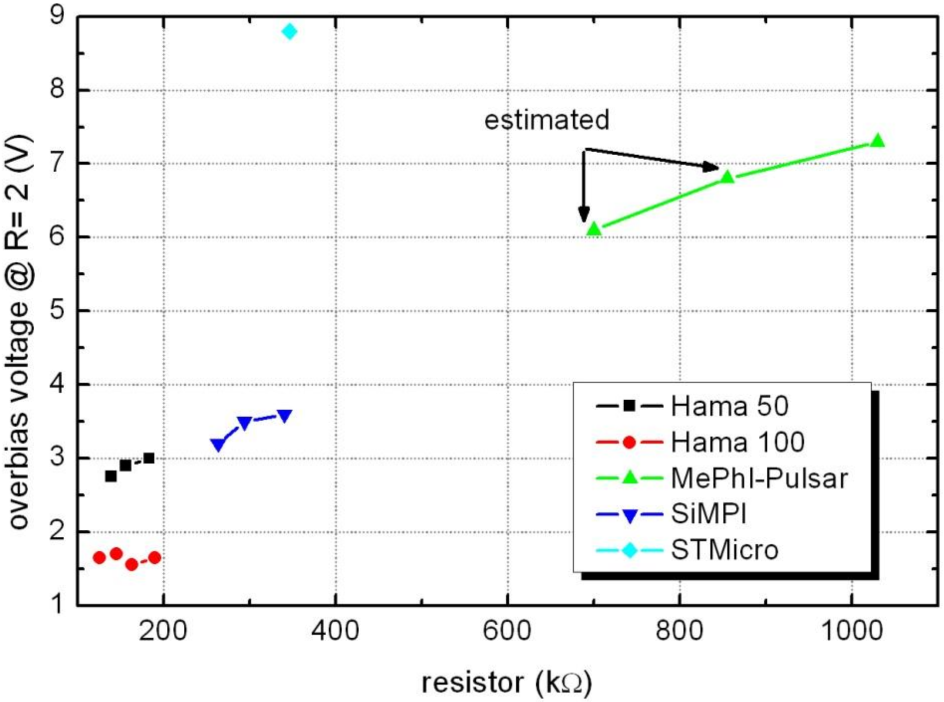
Static IV → measured Dark current

The current ratio as a function of overbias at different temperatures was studied.

Quenching ability



Current ration vs. overbias for SiMPl device



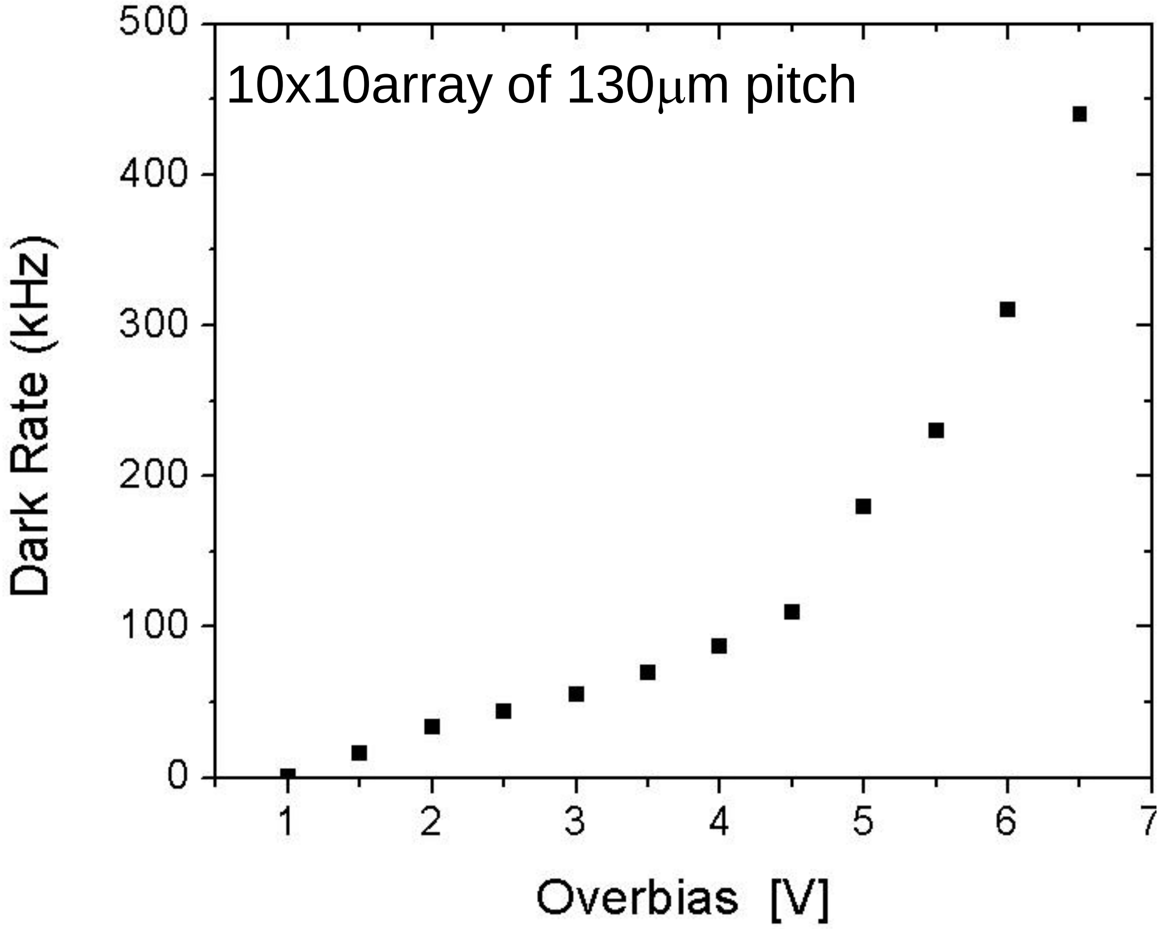
Overbias voltage vs. resistor
for a ratio of R = 2.

More details:

C. Jendrisyk et al.
DOI: 10.1016/j.nima.2011.10.007
accepted for publication

Dark rate

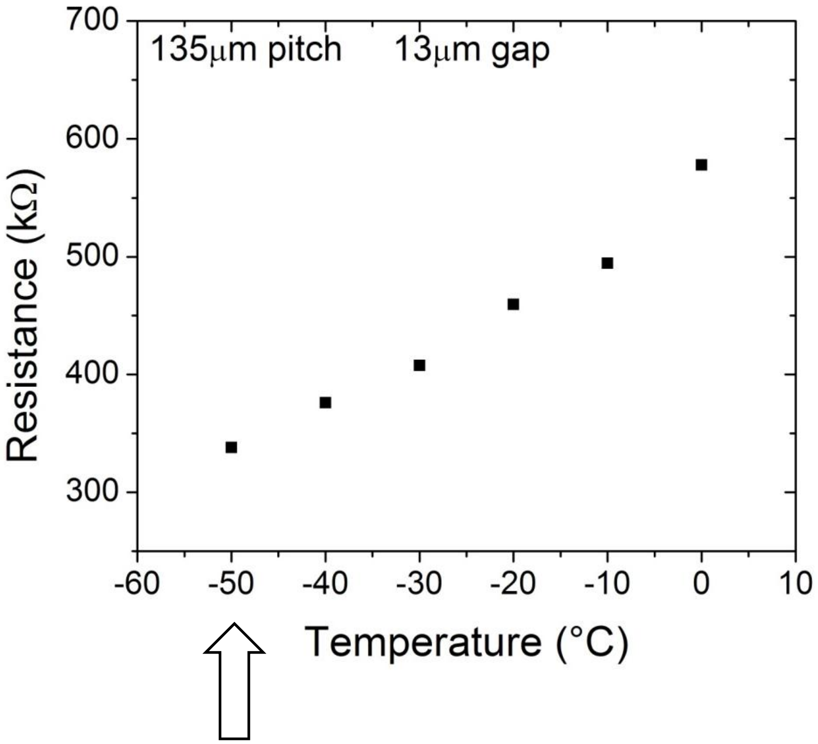
Due to the non optimal process sequence of the high field processing ~10MHz @300K for 4V overbias



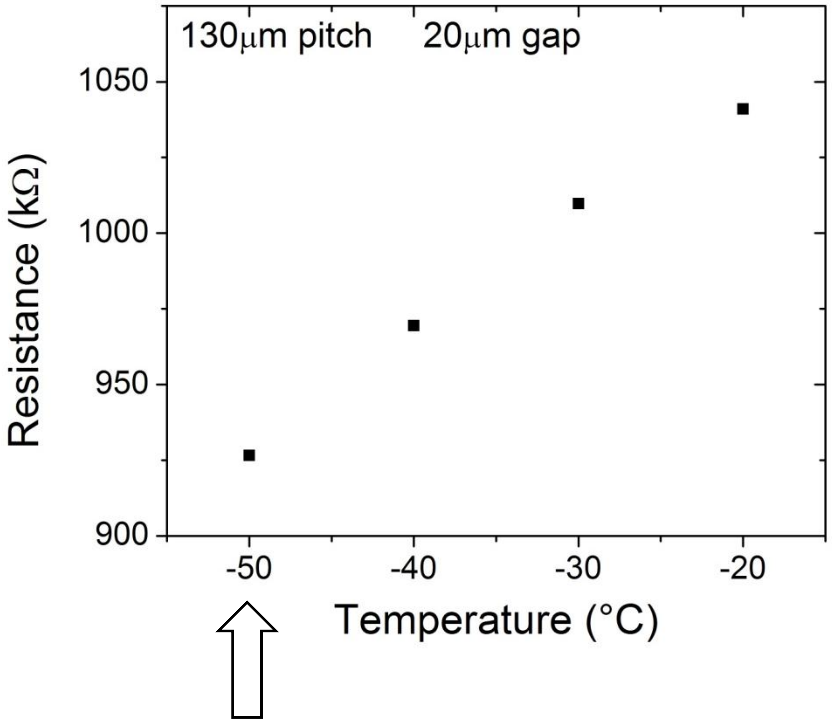
Normal operation up to 4.5V overbias @227K

Resistor behavior

Resistor value designed for the room temperature operation



350kΩ @ -50°C

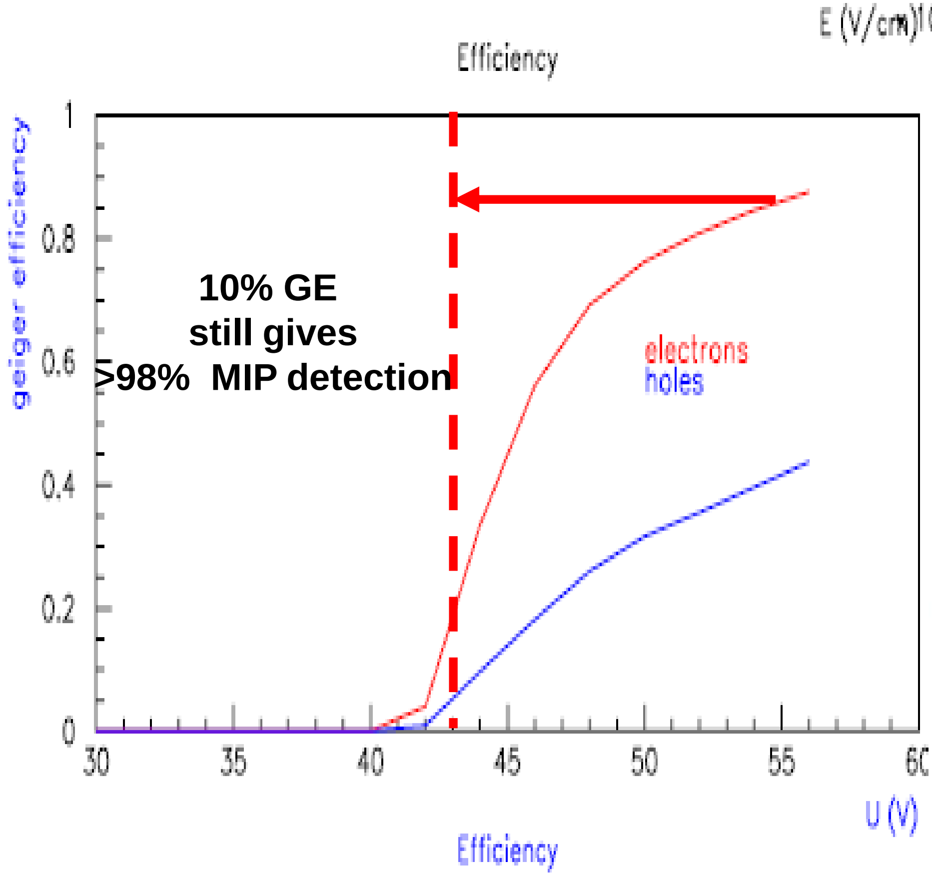


920kΩ @ -50°C

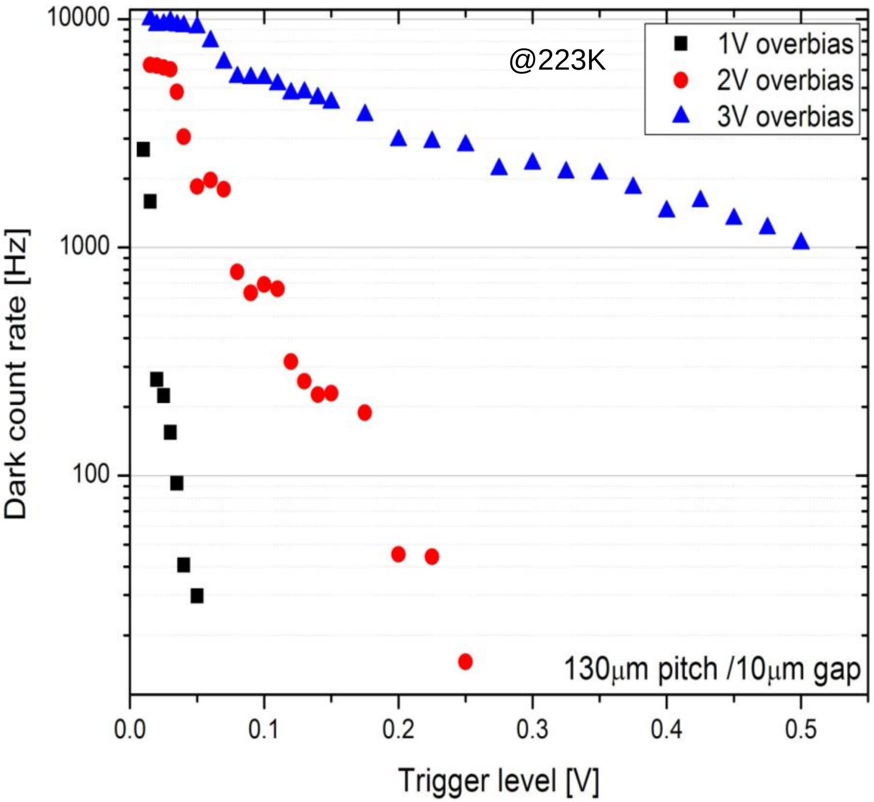
Detection of particles

Excellent time stamping due to the fast avalanche process (<1ns)

MIP gives about 80pairs/μm → huge signal in SiPM→ allows operation at small ΔV



10% GE still gives >98% MIP detection



Reduction of dark rate and cross talk by order of magnitude

Detection of particles

Dark rate: 1 MHz/mm^2 = 1 $hit/\mu m^2/s$ = O(Belle II)

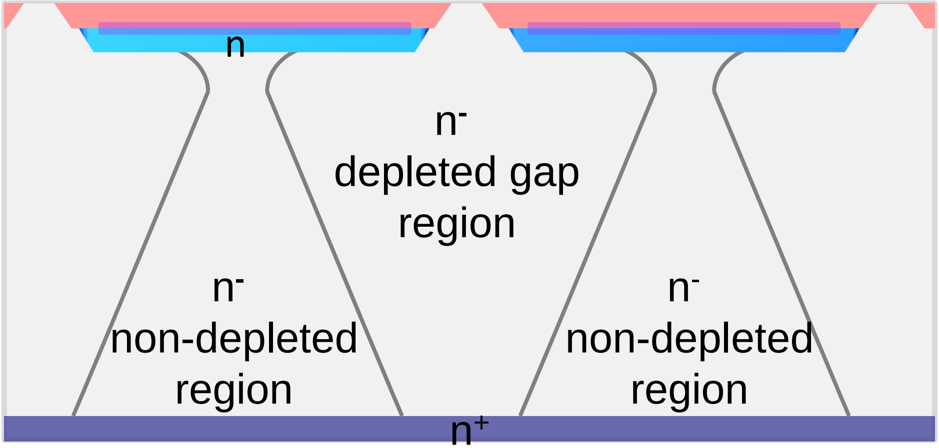
With 20 µm pitch and 12 ns time stamp: occupancy: 2.5×10^{-6}

Power (analogue): ~ 5 $\mu W/cm^2$
Dominated by dark rate

Possible problems:

- Radiation hardness (dark rate increases due to bulk damage)
- Cross talk – low with low overbias
- Efficiency (fill factor)
- Digital power

Next generation SiMPl devices



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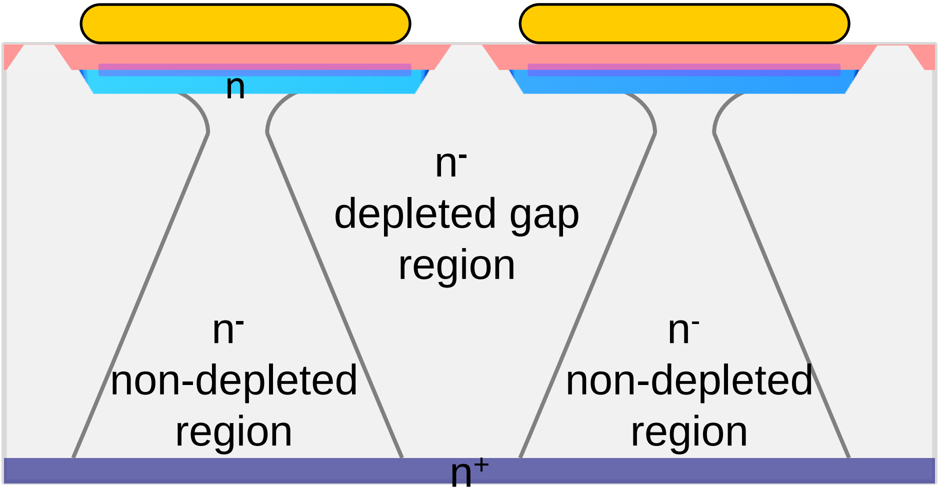

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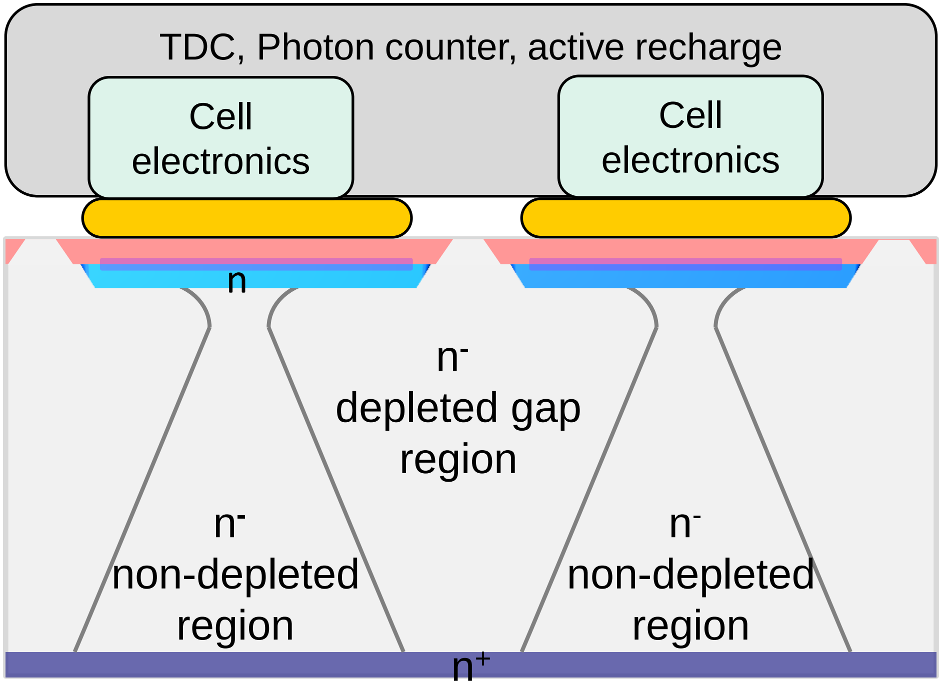


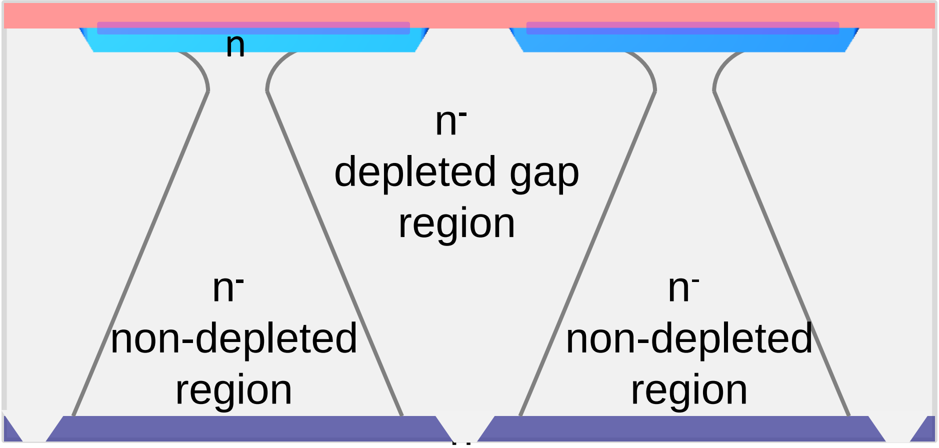
Topologically flat surface

High fill factor

Adjustable resistor value

Pitch limited by the bump bonding

Next generation SiMPl devices

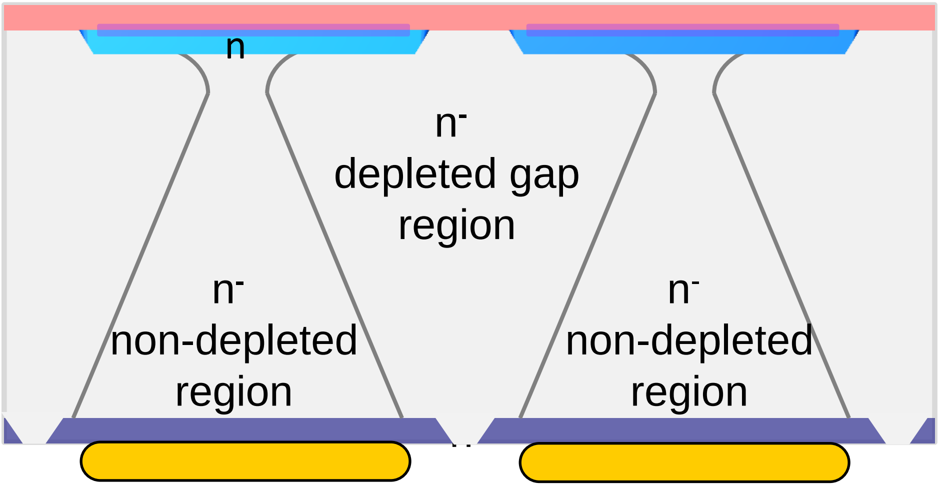


Topologically flat and free surface

High fill factor

Sensitive to light

Next generation SiMPl devices



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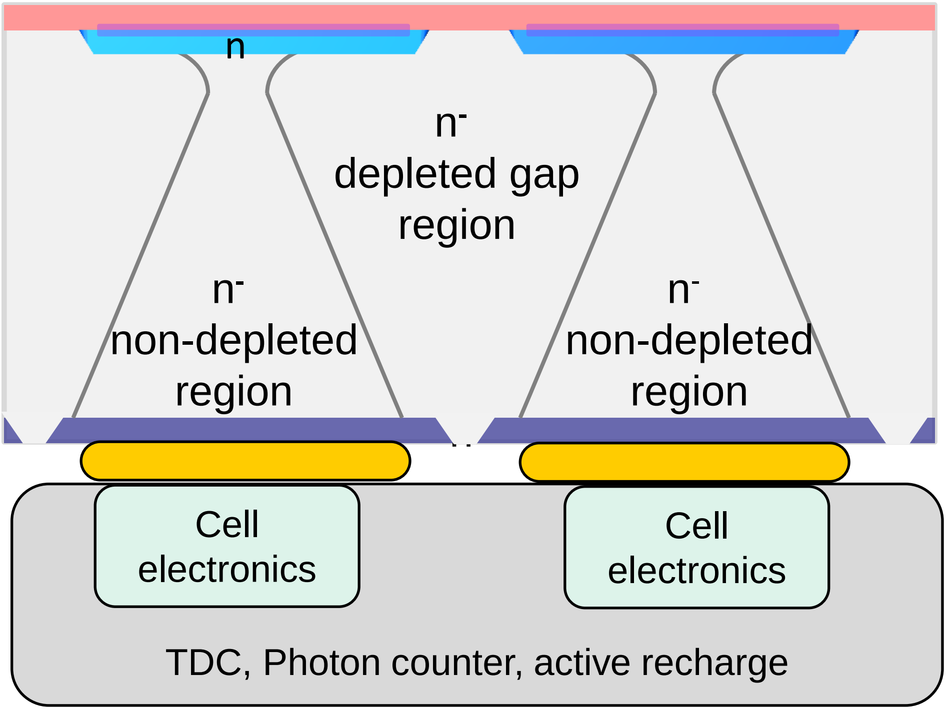

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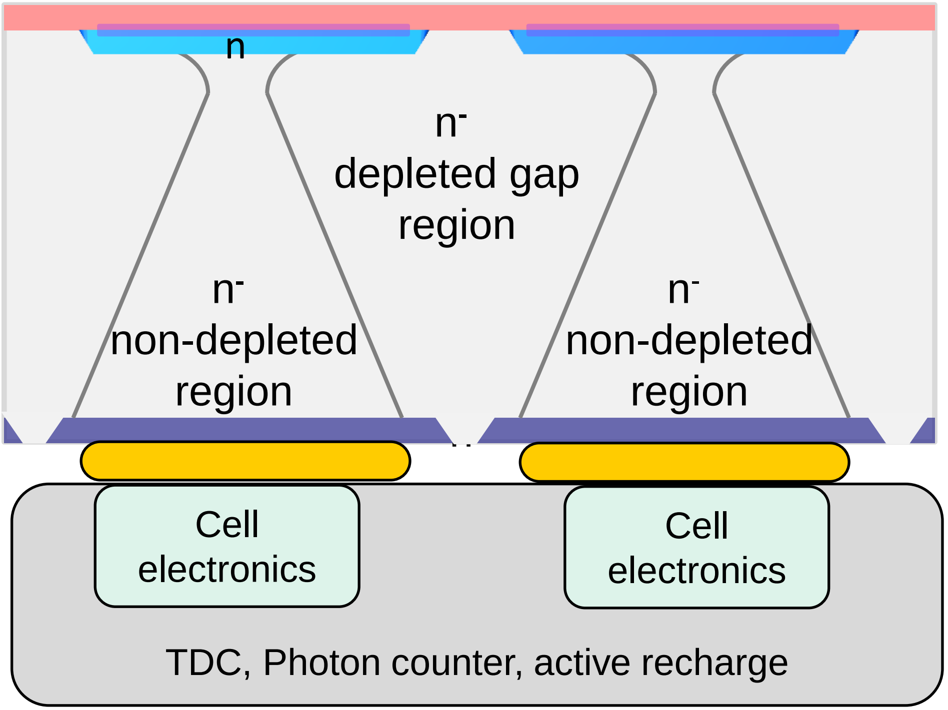


n

n^-
depleted gap
region

n^-
non-depleted
region

n^-
non-depleted
region

Cell
electronics

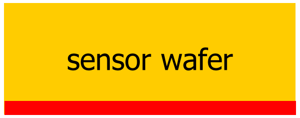
Cell
electronics

TDC, Photon counter, active recharge

Topologically flat and free surface

High fill factor

Sensitive to light



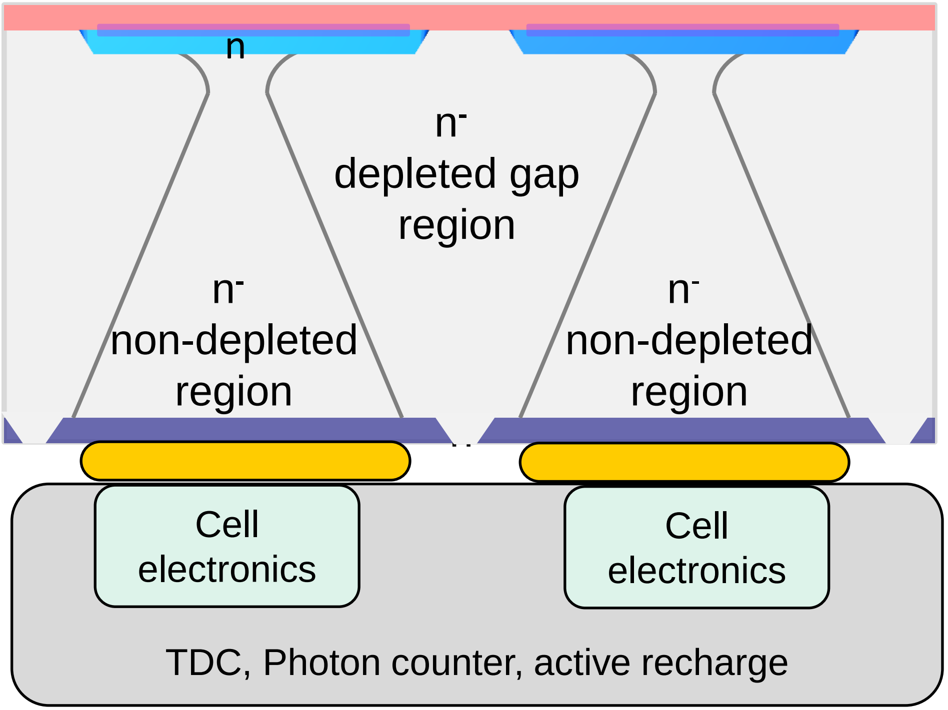
1. Structured implant on backside on sensor wafer

2. bond sensor wafer to handle wafer

3. thin sensor side to desired thickness

4. process SiMPl arrays on top side

Next generation SiMPl devices



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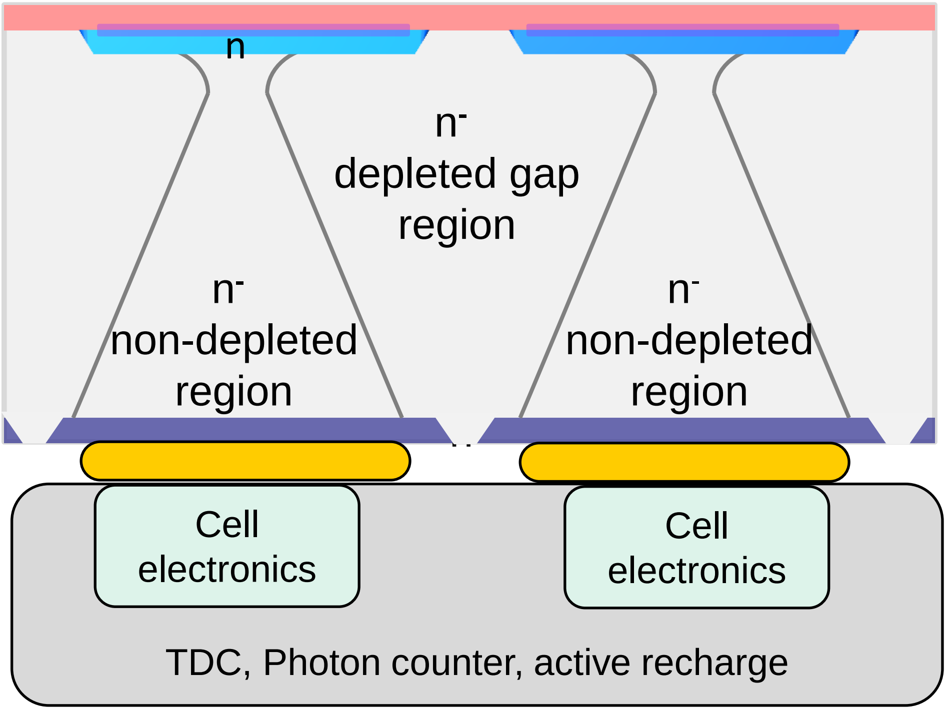

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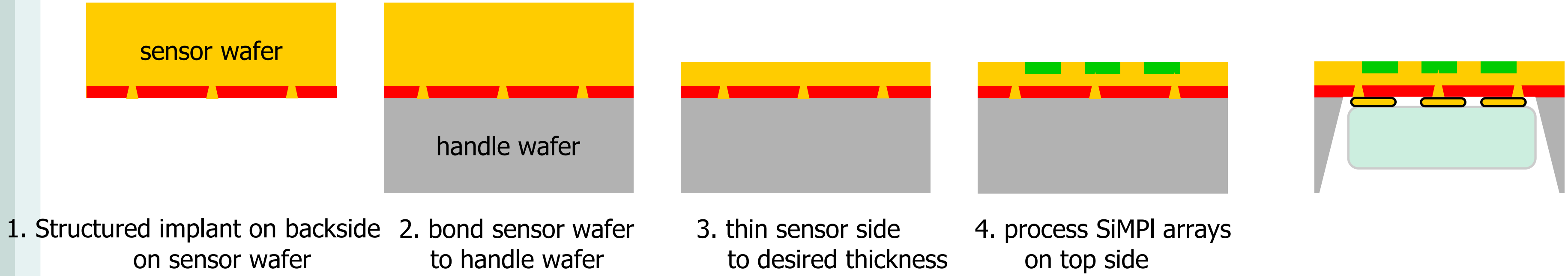

Summary

Silicon photomultiplier array with individual quench resistors, integrated into the silicon bulk - SiMPl detector

- Required flexibility for quench resistor adjustment comes with wafer bonding technique (for small pixels an epitaxial layer is also suitable)
- No polysilicon resistors, contacts and metal necessary at the entrance window
- Geometrical fill factor is given by the need of cross talk suppression only
- Very simple process, relaxed lithography requirements

Prototype production finished – quenching works , first measurements very promising, functional devices with very high fill factor and low cross talk

Next generation SiMPl devices with electronics interconnected

- on front side can be used for trackers at future colliders
- on back side → high sensitivity, high fill factor digital SiPM

Thank you for your attention!