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Activities of MPP/HLL in particle physics

Future HEP Projects:

ATLAS

-> sLHC upgrade -> complete replacement of inner detector

Time Scale: 2016

ILC

-> Vertex Detector

-> SiPM Readout of Calorimeter

Time Scale: 2016 +

MAGIC/CTA/EUSO

-> SiPM Camera

GERDA (Germanium.....)

Muon Collider: SDD

Activities without MPP participation: Fair (CBM, Panda), Star, Belle.....

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ATLAS at sLHC: The Challenge

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Expected conditions at LHC and sLHC

LHC:

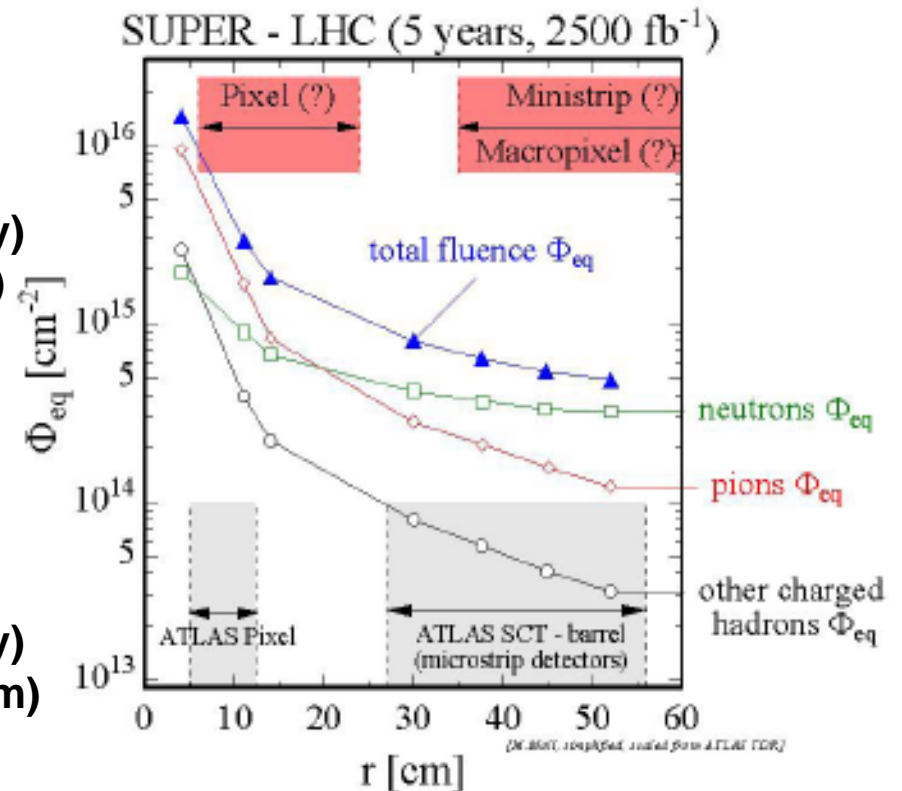
- Start 2008
- $L = 10^{34} \text{cm}^{-2} \text{s}^{-1}$
- Integrated Luminosity: 500fb^{-1} (10y)
- Fluence: $3 \times 10^{15} \text{cm}^{-2}$ (1 MeV n, 4cm)
- Multiplicity: 0.5-1 k tracks/event

sLHC:

- Start 2016
- $L = 10^{35} \text{cm}^{-2} \text{s}^{-1}$
- Integrated Luminosity: 2500fb^{-1} (5y)
- Fluence: $1.6 \times 10^{16} \text{cm}^{-2}$ (1 MeV n, 4cm)
- Multiplicity: 5-10 k tracks/event

New detector concepts needed

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The ATLAS Pixel Detector

Present Layout:

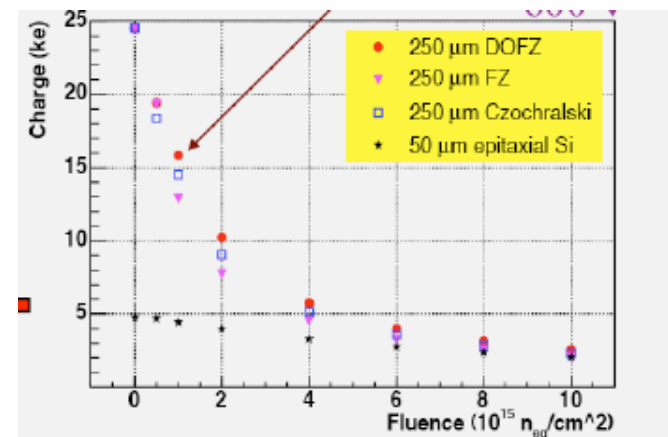
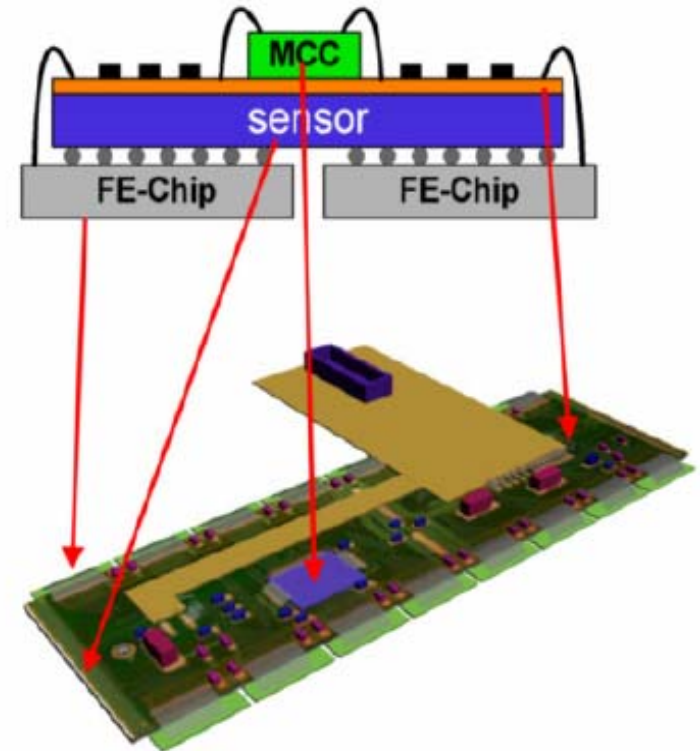
- 250 μm n-in-n pixel sensor
- 50 x 400 μm^2 pixels
- 0.25 μm rad hard ASIC
- rad hard till 10^{15} n/cm²

- Live fraction ~71%
- Cantilever for readout
- Sensor width 2x chip size: 16 mm
- Large material overhead

At sLHC:

- $V_{\text{dep}} \sim 4200\text{V}$
- Charge collection: ~15%
(at 10^{16} n/cm²)
- High occupancy

Main cost driver: Bump bonding !





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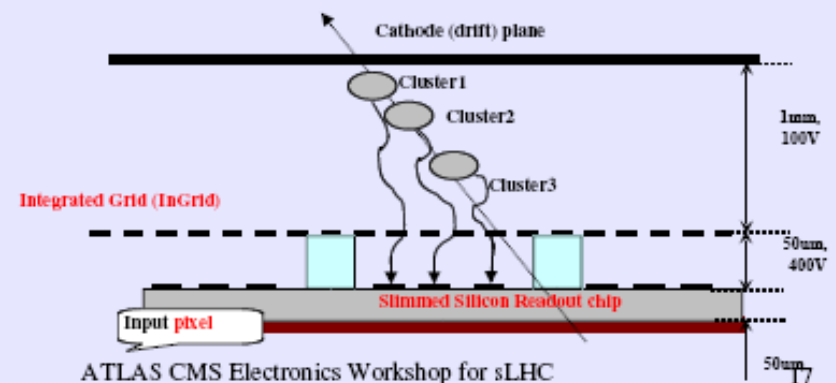
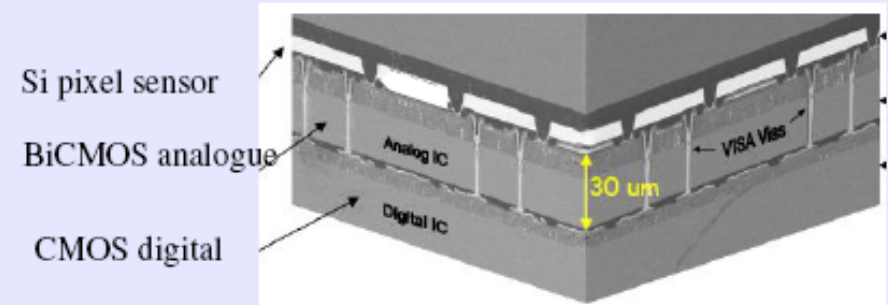
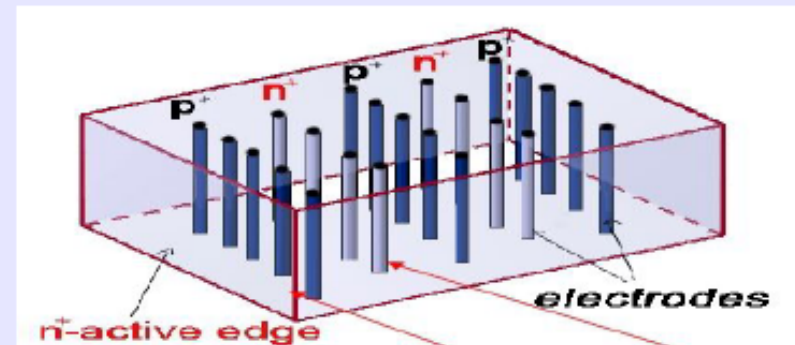
ATLAS sLHC Upgrade R&D

B-layer: Highest radiation damage, look for new technology

- 3D-Silicon (Sherwood Parker, Cinzia Davia, et al):
 - Test-beam results available; R&D proposal under review (currently being improved)

- Thin-silicon combined with 3D-interconnect technologies (Richard Nisius/MPI-Munich et al):
 - Vias through si layers + replace bump bonding with solid-liquid diffusion
 - Low bias V; low C + low signal -> still good S/N

- Gossip (Harry van de Graaf/NIKHEF et al)
 - Gas detector on slimmed silicon pixel chip
 - PO will set up a group to exploit common items, keep together, look at risk etc.





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R&D for a novel pixel detector for SLHC

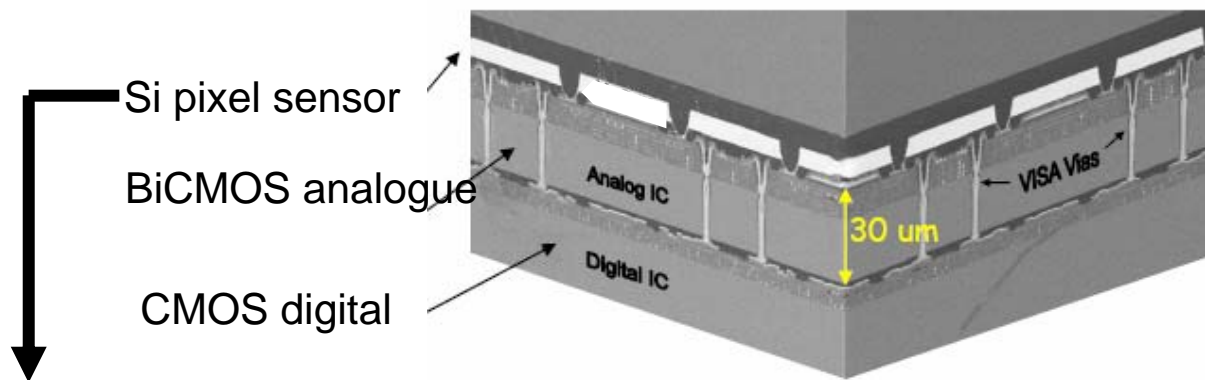
3D interconnection (sensor – electronics; electronics – electronics):

Alternative to bump bonding (fine pitch, potentially low cost?).

New possibilities for ASIC architecture (multilayer, size reduction).

Optimization of rad. hardness, speed, power.

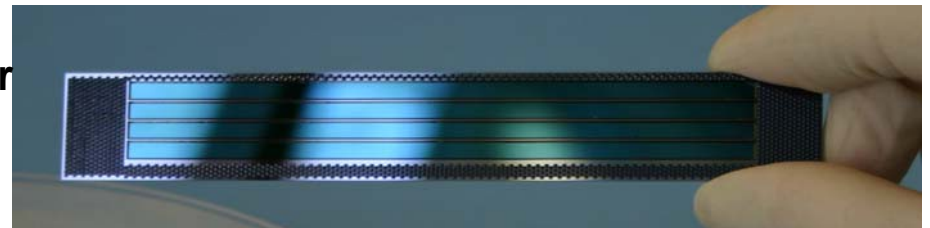
Impact on module design (ultra thin ASICs, top contact, 4-side abutable).



R&D on thin ($O(50\mu\text{m})$) FZ silicon detectors:

Based on well known pixel sensor technology.

Can be operated at 10^{16} n/cm^2
(V_{dep} , I_{leak} , CCE).



Can lead to an advanced module design: rad hard with low material budget



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Motivation for Thin Detectors

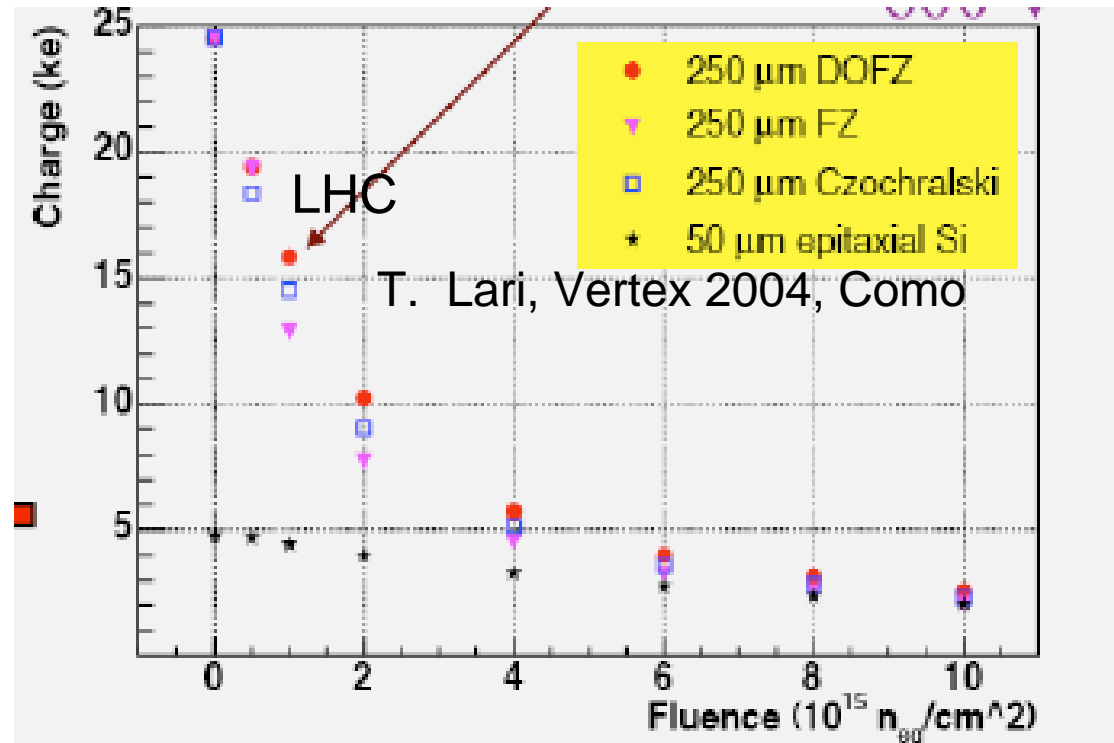
After 10^{16} n/cm²:

$V_{\text{dep}} > 4000\text{V}$ (250 μm) \rightarrow operate partially depleted.

Large leakage currents.

Charge loss due to trapping (mean free path ~ 25 μm).

$I_e > I_h$ (need n-in-n or n-in-p) to collect electrons.

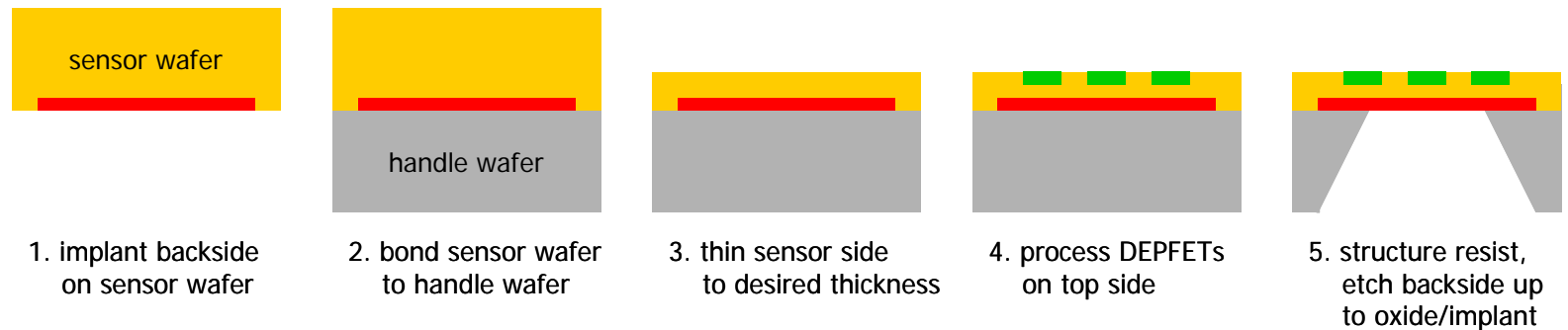


No advantage of thick detectors \rightarrow thin detectors: low V_{dep} , I_{leak} (and X_0)
However: small signal size is a challenge for the readout electronics



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Thinning Technology

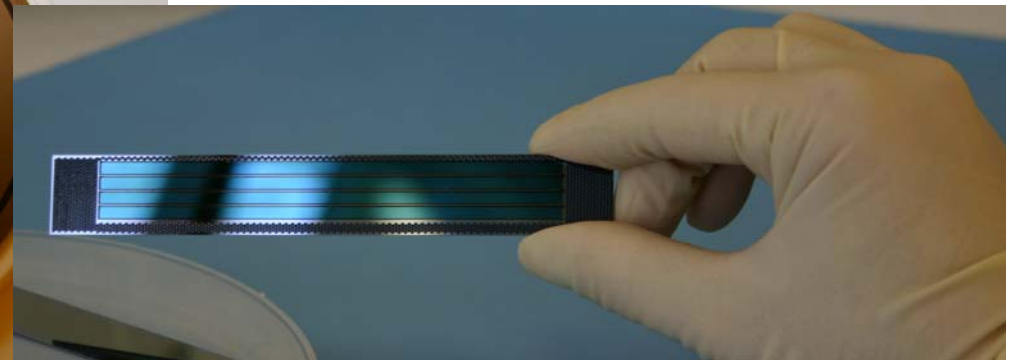
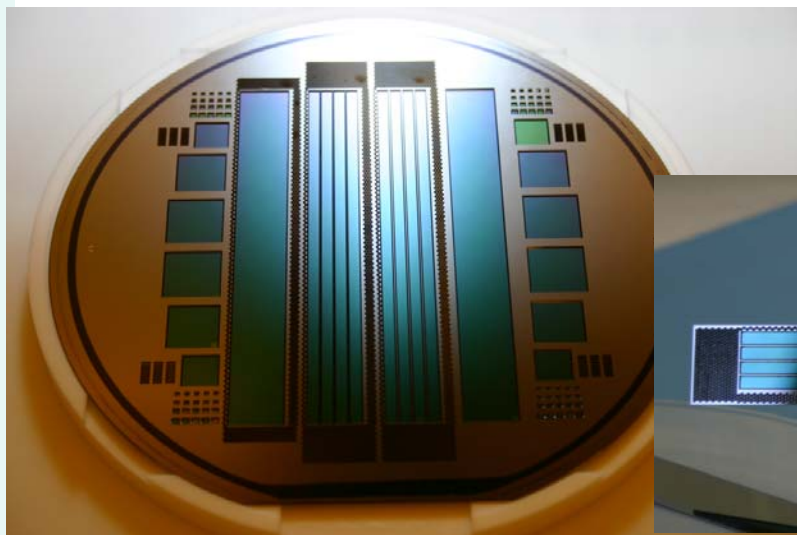


- Sensor wafer: high resistivity $d=150\text{mm}$ FZ wafer.
- Bonded on low resistivity “handle” wafer”.
- (almost) any thickness possible

Thin ($50\ \mu\text{m}$) silicon successfully produced at MPI.

- MOS diodes.
- Small strip detectors.
- Mechanical dummies.

-No deterioration of detector properties, keep $I_{\text{leak}} < 100\text{pA}/\text{cm}^2$



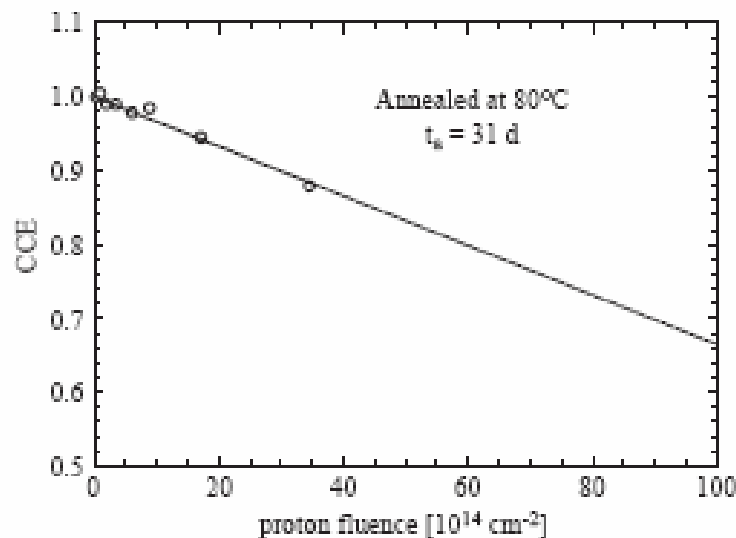
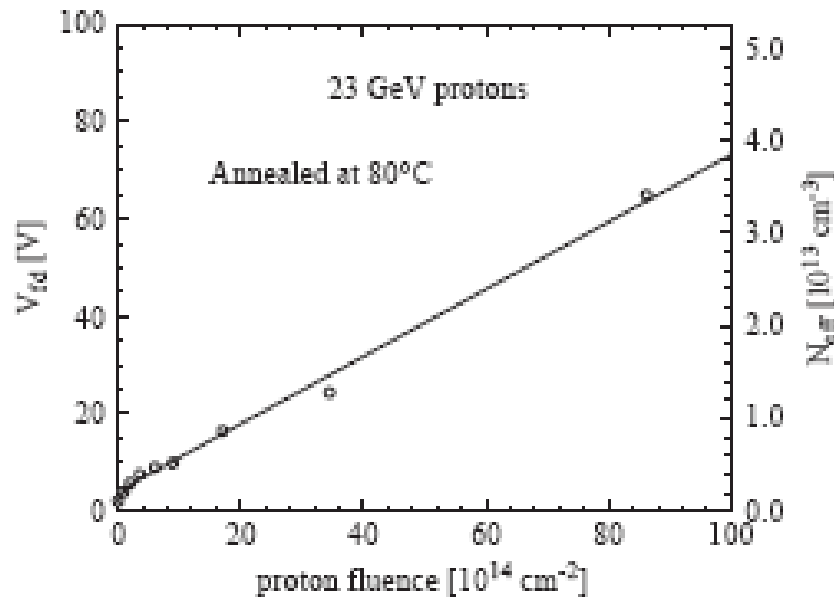
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Measurements (V_{dep} , I_{leak} , CCE)



Fretwurst et al. NIM A 552 (2005):
After short term annealing:

$V_{\text{dep}} < 100 \text{ V}$ at 10^{16} 1/cm^2 .

However, detectors need to be
kept cold (reverse annealing!).

Leakage currents:

$\alpha(80^\circ\text{C}, 8 \text{ min}) = 2.4 \times 10^{-17} \text{ A/cm}$.

Fretwurst et al. NIM A 552
(2005): MPI diodes, $50 \mu\text{m}$:

$\text{CCE} \sim 66\% @ 10^{16} \text{ p/cm}^2$
(extrapolated).



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Summary: Thin Pixel Detectors

Cannot beat trapping (with planar detectors)! Challenge: small signal!
Small pixel size (low capacitance) helps. Electronics R&D.

- Keep V_{dep} low.
- Keep I_{leak} low.
- Reduce X_0^* .

- First results on radiation hardness and CCE encouraging.
- Can be produced with standard FZ material.
- Large scale industrial production possible.
- Thickness can be adapted to radius (fluence) -> parameter!

R&D topics:

- Make real pixel detectors.
- Irradiations, measurement of CCE.
- Optimize thickness, n-in-n or n-in-p ?
- Charge sharing.
- Optimize production process, industrial fabrication.
- Electronics development: operate at ~1000 e- threshold (50 μm)

*) if this is not an issue: backside etching not necessary, simpler fabrication.

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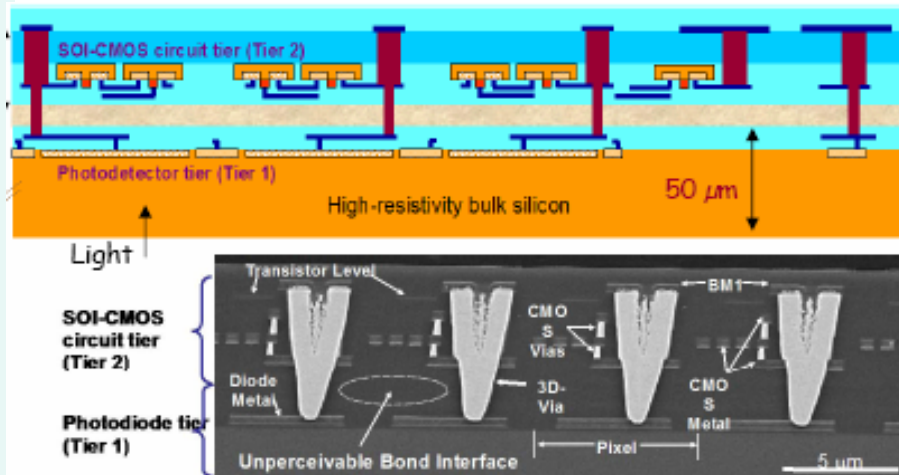
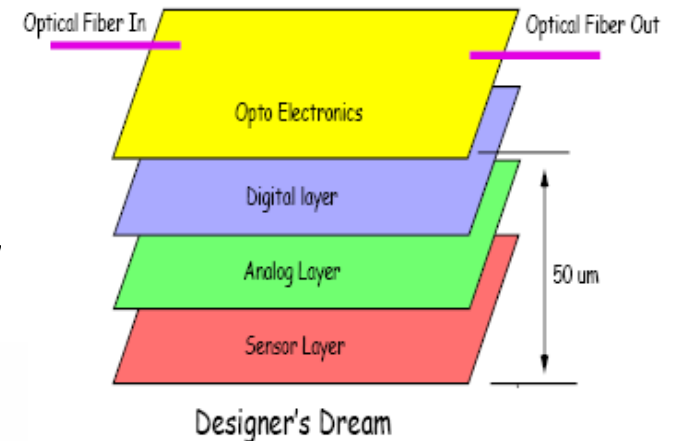


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3D Interconnection (see presentation by Laci)

Two or more layers (=“tiers”) of thinned semiconductor devices interconnected to form a “monolithic” circuit.

- Different layers can be made in different technology (BiCMOS, deep sub- μ CMOS, SiGe,.....).
- 3D is driven by industry:
 - Reduces R,L and C.
 - Improves speed.
 - Reduces interconnect power, x-talk.
 - Reduces chip size.
 - Each layer can be optimized individually



Drawing and SEM Cross section

For HEP: sensor layer: fully depleted Si
Example: 2-Tier CMOS Sensor,
1024 x 1024 pixel, pitch 8 μ m
by MIT-Lincoln Lab

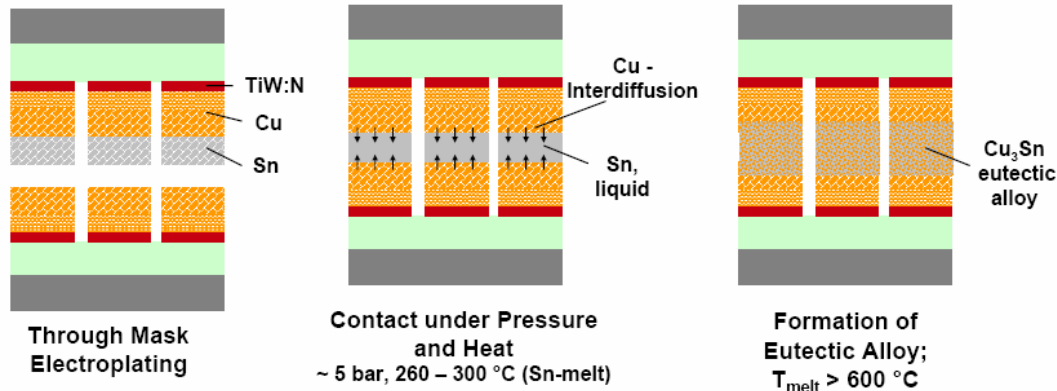
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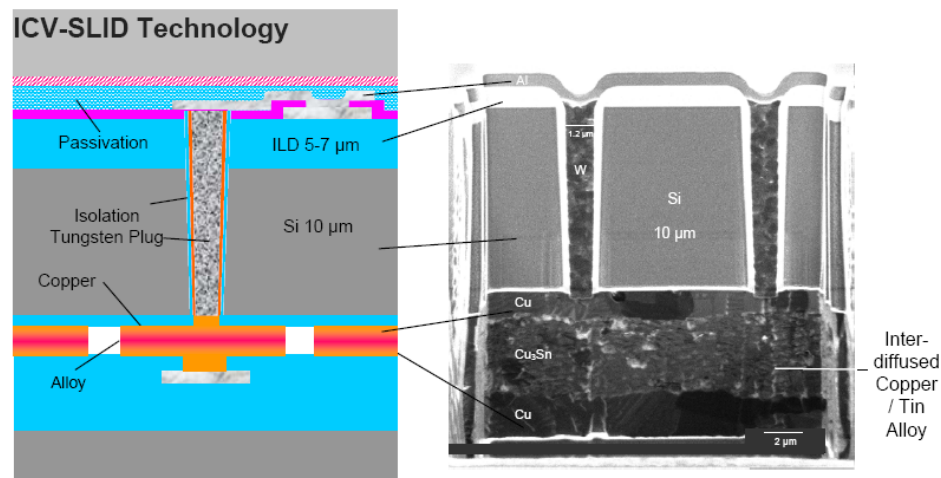
IZM SLID and ICV Process

Metallization SLID (Solid Liquid Interdiffusion)



IZM
Fraunhofer
Institut
Zuverlässigkeit und
Mikrointegration

- Alternative to bump bonding (less process steps “low cost” (IZM)).
- Small pitch possible ($\ll 20 \mu\text{m}$, depending on pick & place precision).
- Stacking possible (next bonding process does not affect previous bond).
- Wafer to wafer and chip to wafer possible.



- Hole etching and chip thinning
- Via formation with W-plugs.
- Face to face or die up connections.
- 2.5 Ohm/per via (including SLID).
- No significant impact on chip performance (MOS transistors).

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Advantages of 3D

Multilayer electronics:

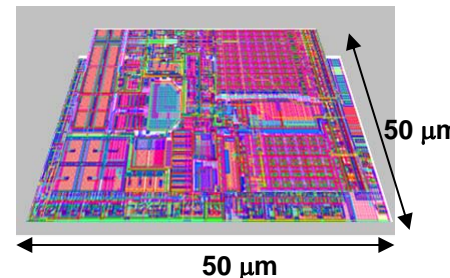
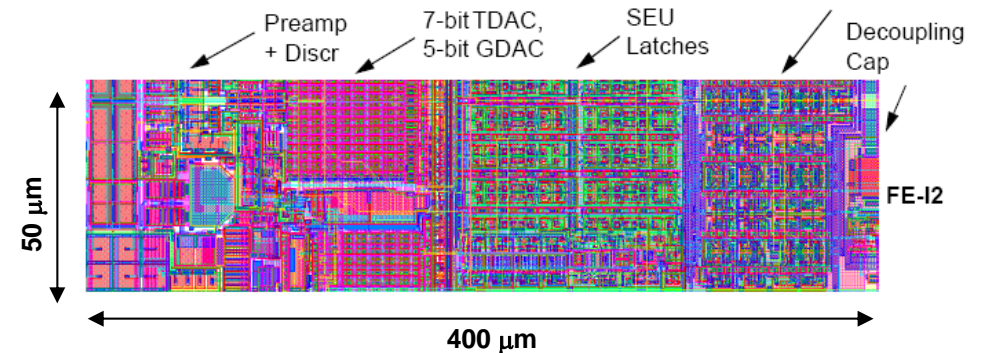
Split analogue and digital part
Use different, individually
optimized technologies:

- > gain in performance, power, speed, rad-hardness, complexity.
- > smaller area (reduce pixel size or more functionality).

4-side abutable devices:

- > no dead space.
- > simpler module layout.
- > larger modules.

(reduce complexity and material)



$50 \times 400 \mu\text{m}^2$
($0.25 \mu\text{m}$)
May shrink to
 $\sim 50 \times 50 \mu\text{m}^2$
(130 nm)



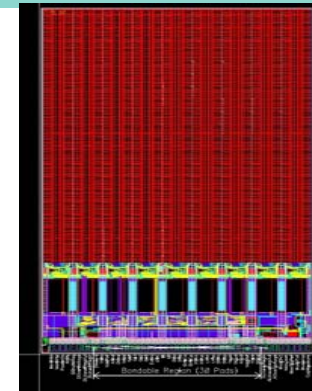
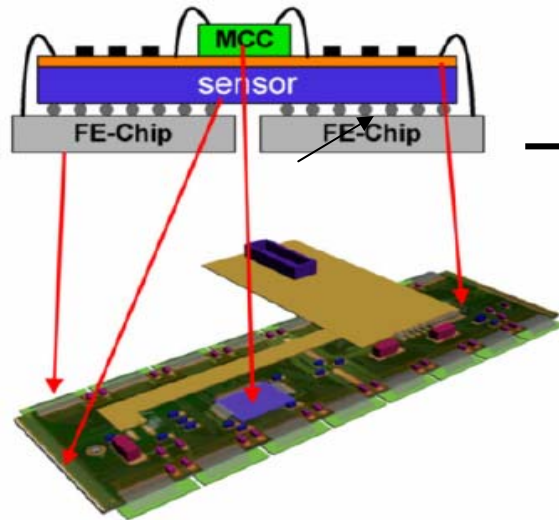
Conventional CMOS sensor
(optical, similar: MAPS)

3D Pixel Layout⁹



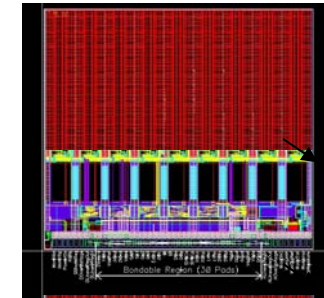
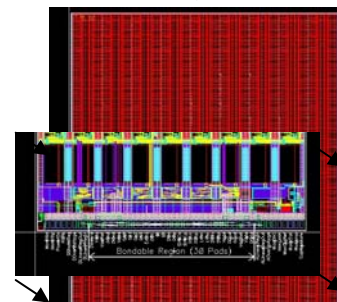
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Advantages for Module Design



Pixel area
(facing sensor)

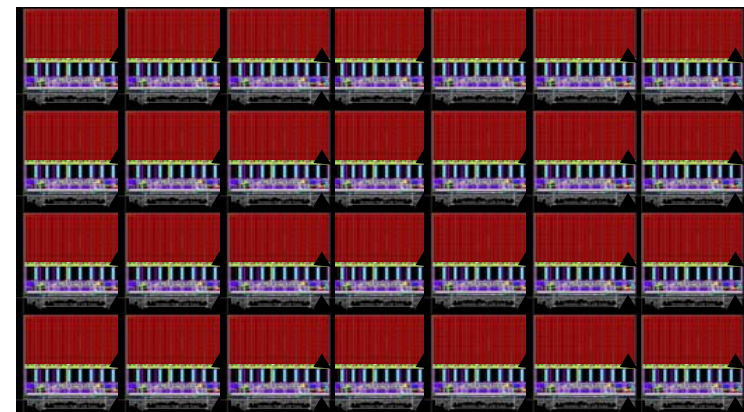
Periphery
Pipeline and control
Bond pads
(cantilever)



Control on top of pixel area.
External contact from top.
Contact pixels through vias:
-> 4-side buttable.
-> No “cantilever” needed.

Larger module with minimal dead space.

Less support structures & services.
Substantial material savings.



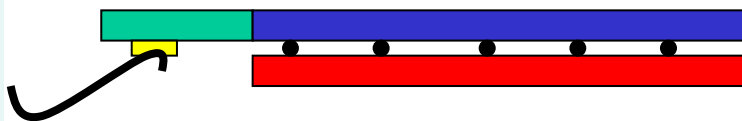
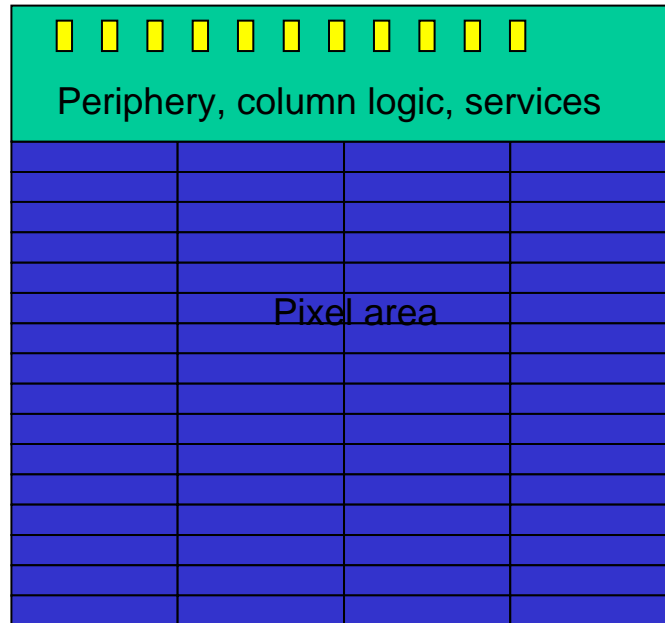
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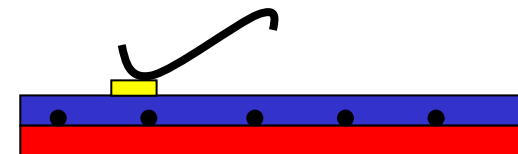
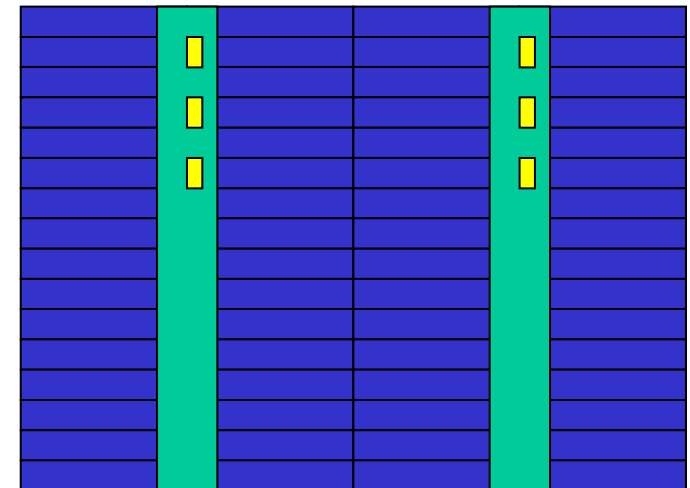
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Advantages even for single layer

Conventional Layout



3D Layout



Make use of smaller feature size (gain space)

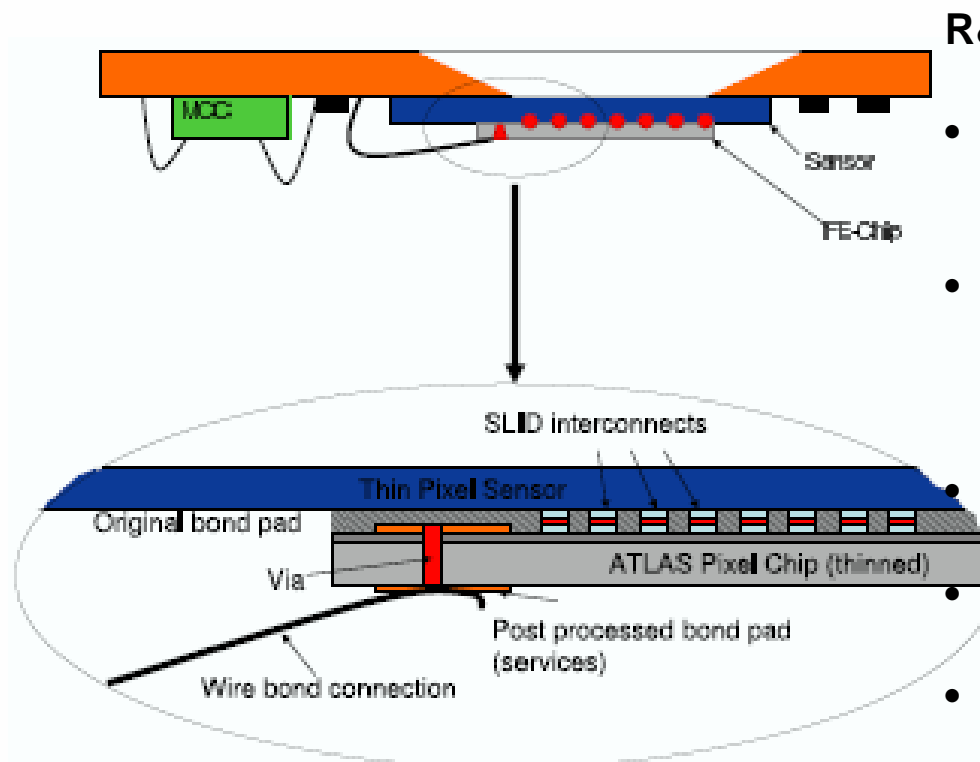
- > move periphery in between pixels (can keep double column logic)
- > backside contacts with vias possible
- > no cantilever needed, 4-side abutable



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Proposed R&D Program

- a) Test interconnection process with diode test structures
- b) Build demonstrator using ATLAS pixel chip and pixel sensors made by MPI



R&D Issues:

- Technology: compatible with sensors, ASICs?
- Interconnection quality: e.g. capacitance (face-to-face or die up?).
- Yield & Costs.
- Production in industry.
- Reduce material (copper layer).



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Time Scale

Technology tests with IZM: ongoing

**Production of thin test structures (for demonstrator): Summer
2007**

-> important preparation for thinning of ILC DEPFETs and SiPMs!

Detector/ASIC: interconnection: 2008

Full 3D demonstrator (SLID, vias, thinning): 2009

Needed: ASIC R&D (low threshold & 3D layout)

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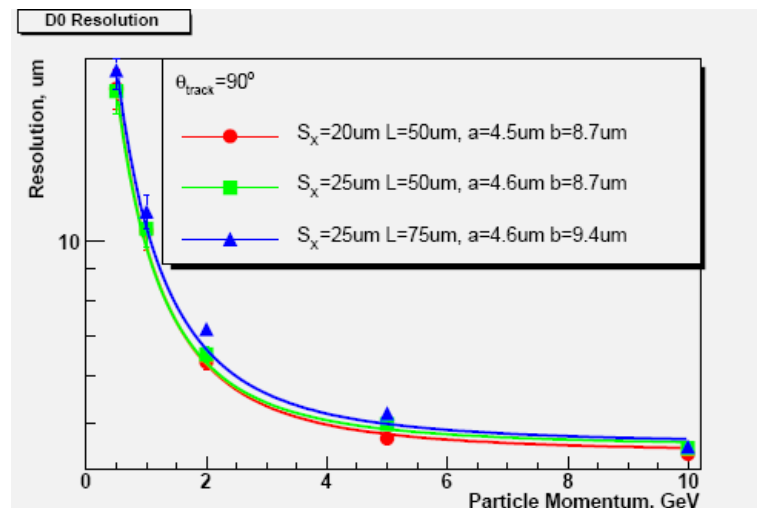
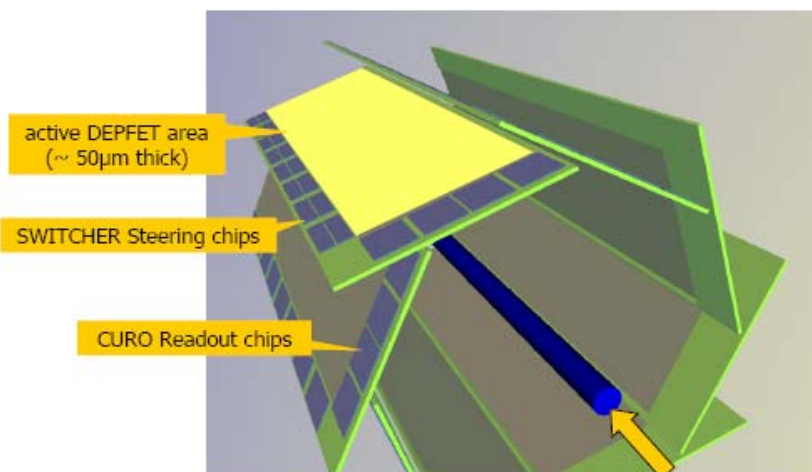
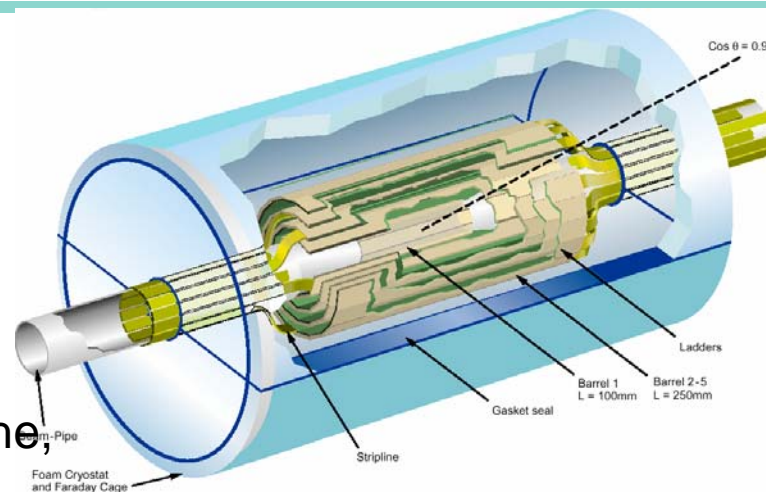


ILC: Pixel Detector

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Propose: DEPFET

Well focused R&D program
MPP Project (A. Frey)
DEPFET Collaboration
(Bonn, Mannheim, Aachen, Karlsruhe,
Valencia, Prague)



**Simulation (A. Raspereiza):
ILC specs fulfilled**

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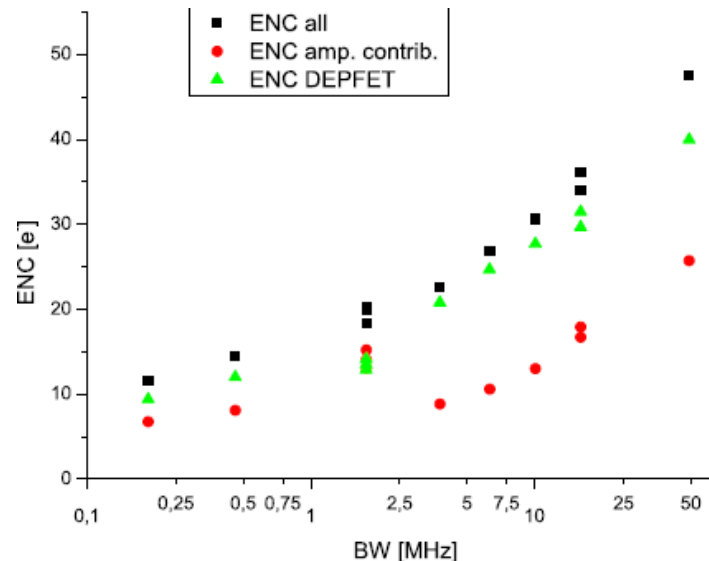
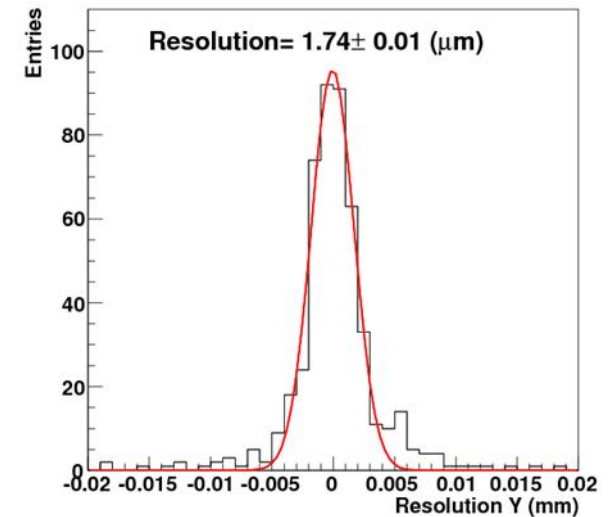
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Recent Results

Testbeam at CERN (180 GeV/c π)

5 plane DEPFET telescope
(extrapolation error < 1 μm)

DEPFET resolution: 1.74 (μm)
(22 μm pitch, 450 μm thick)



Intrinsic DEPFET noise at
ILC bandwidth < 40 e- ENC

However, noise and speed of
CURO disappointing
ENC ~ 250 e- (want 100 e-)
Line rate: 4 MHz (want 20 MHz)

New chip developed



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Present Activities

PXD5 production (till June)

- > large matrices
- > smaller pixels
- > optimized gain and clear

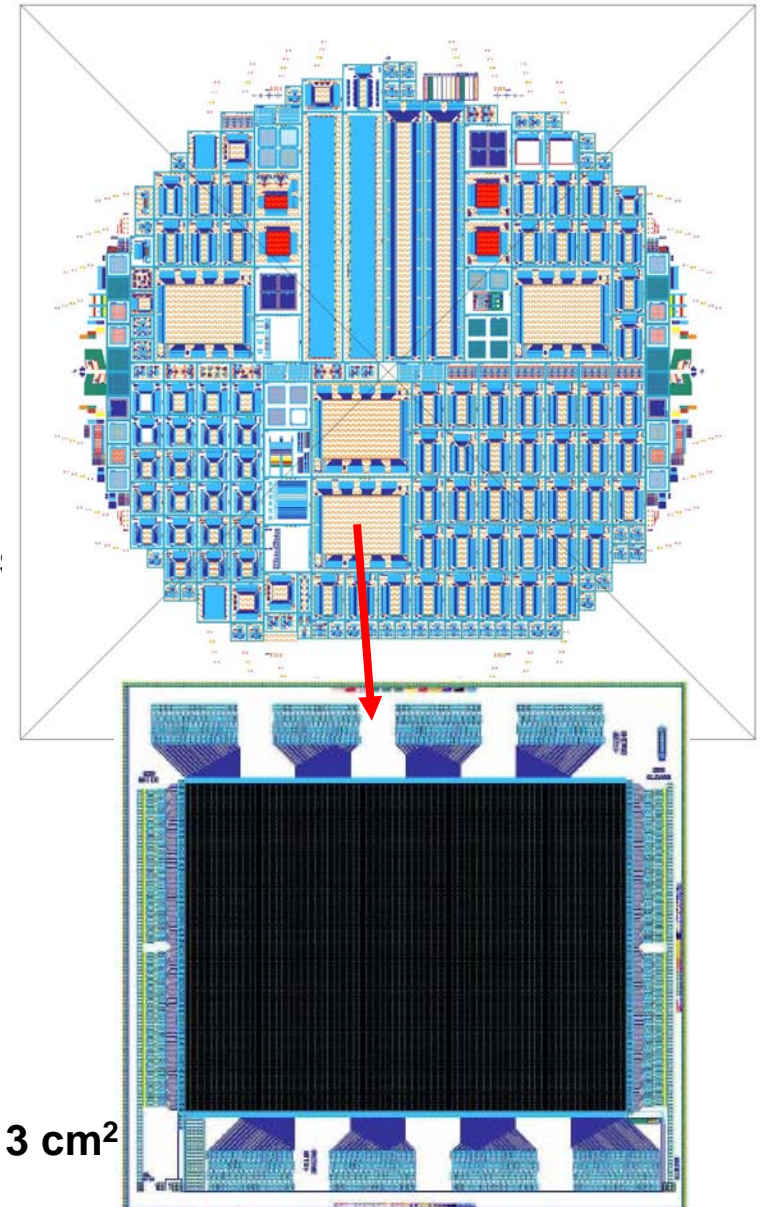
EUDET Testbeam (EU FP6)

**New readout (DCD1) and Switcher chip
submitted**

(address noise and speed)

Next important step:

Thin DEPFETS (2008?)



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512 x 512 pixel array, 2 x 3 cm²



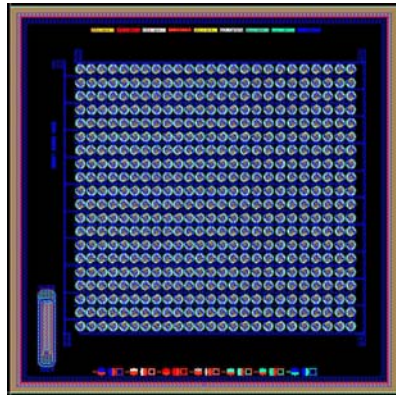
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SiPMs for Cerenkov Telescopes

Test structures work!

Excellent resolution

Good dark rates



Next Step:

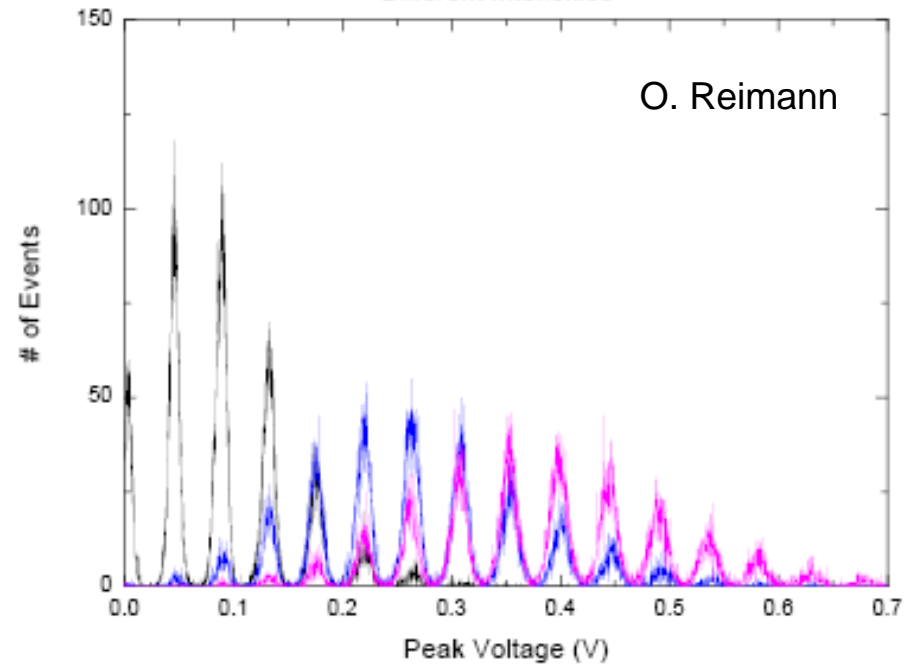
Production of devices with backside illumination

(Started, finished: End of 2007)

Possible problems -> X-talk

**New tools: 2 photon source for QE measurements
 Hamamatsu Phemos 1000 emission microscope**

HLL-SiPM @ 41.4 V and 850nm
Different Intensities



Analysis Tools

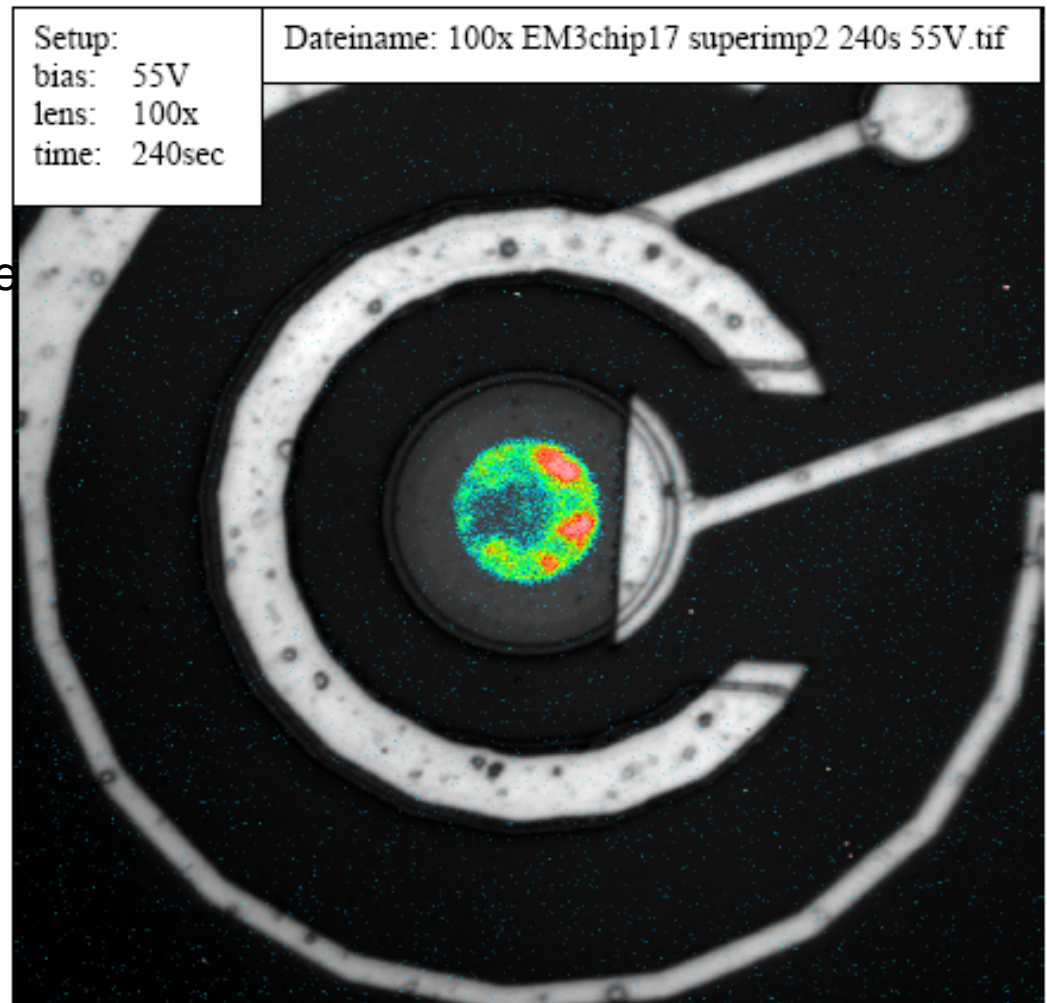


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Phemos 2000 picture
(C. Freuerbaum)

Photon emission of hot
Carriers in an avalanche

Excellent tool to study
SiPMs



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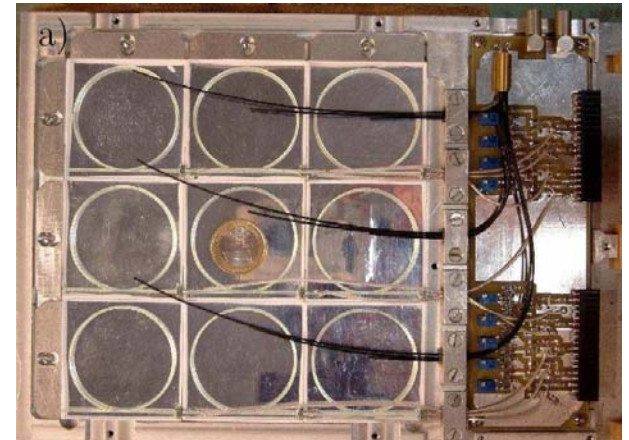
Other Applications of SiPMs

MAGIC: optimized for highest QE (100%) in near UV and blue
price to pay: time resolution, dark rate, cross talk

Other Projects (Scintillator readout, CALICE, PET): different optimization required -> backside illumination not really necessary

Our devices may still excel in dark rate, resolution, QE, blue sensitivity,...

Problem: cheap mass production needed
(CALICE: 6M SiPMs!)



Future

use 3D interconnection technique to combine SiPM array with ASIC ?

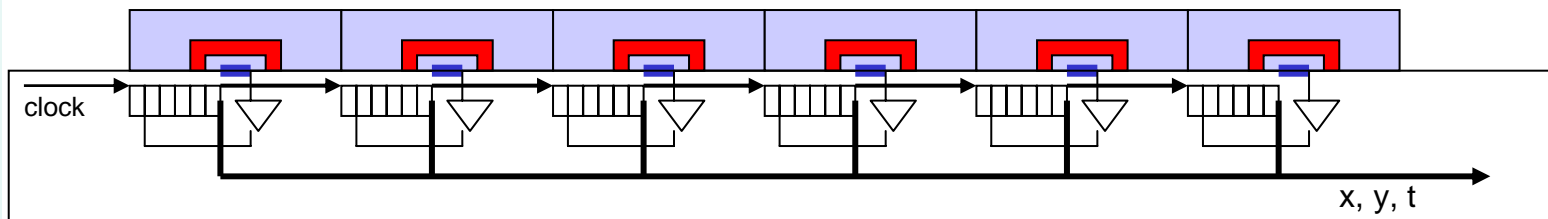
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SiPM with 3D interconnection

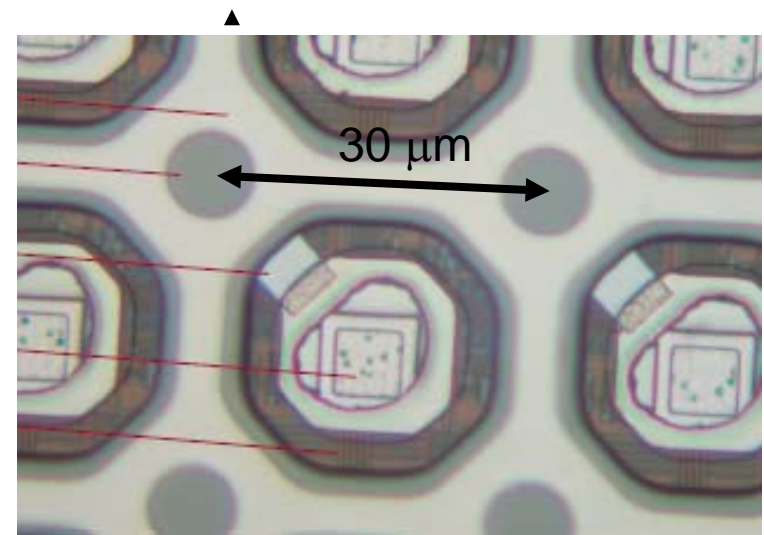
- active quenching of single pixel
- low threshold, low gain, low QE
- excellent timing and rate
- single pixel position resolution
- ultra thin (low dark rate, low x-talk)
- 4-side abutable devices (-> large area sensors)



Similar device made by MIT Lincoln
Lab (Laser Radar -> timing!)

SiPM rather primitive:

frontside illuminated
modest fill factor



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General Remarks

Challenges of future HE experiments (tracking detectors)

- radiation damage (10^{16} n/cm²)
- resolution (-> S/N, low mass)
- speed
- data rates (>10 Gbit/sec)

Some issues:

- Smaller structure sizes (-> smaller pixels, short channel length..)
- Thin oxides (Rad. hard)
- Electronics integration will become a key issue (3D)
- ASIC design competence (analogue) needed!
- Thinning technology becomes more and more important
(our SOI approach looks extremely promising! Keep on!)

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