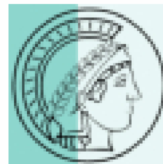
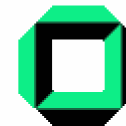
DEPFET Active Pixel Sensors for the ILC

Laci Andricek

for the DEPFET Collaboration
(www.depfet.org)





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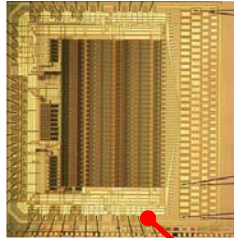
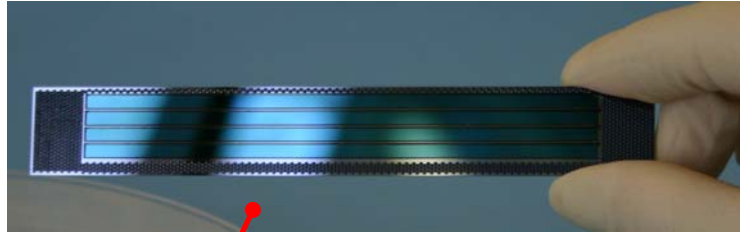
RHEINISCHE FRIEDRICH-WILHELMS-UNIVERSITÄT

The DEPFET ILC VTX Project

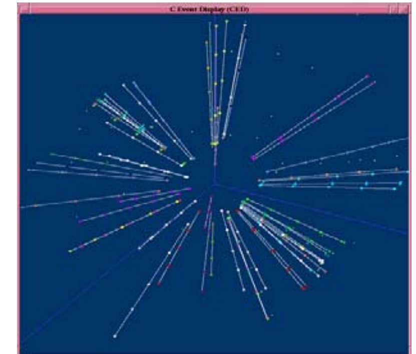
✓ steering chips Switcher



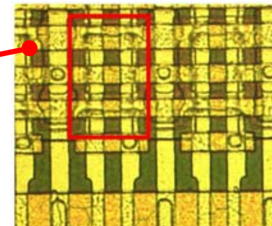
✓ thinning technology



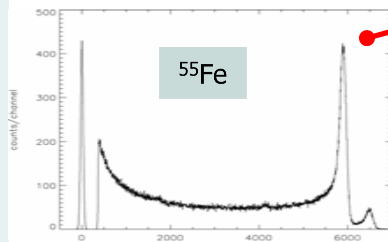
✓ Simulation

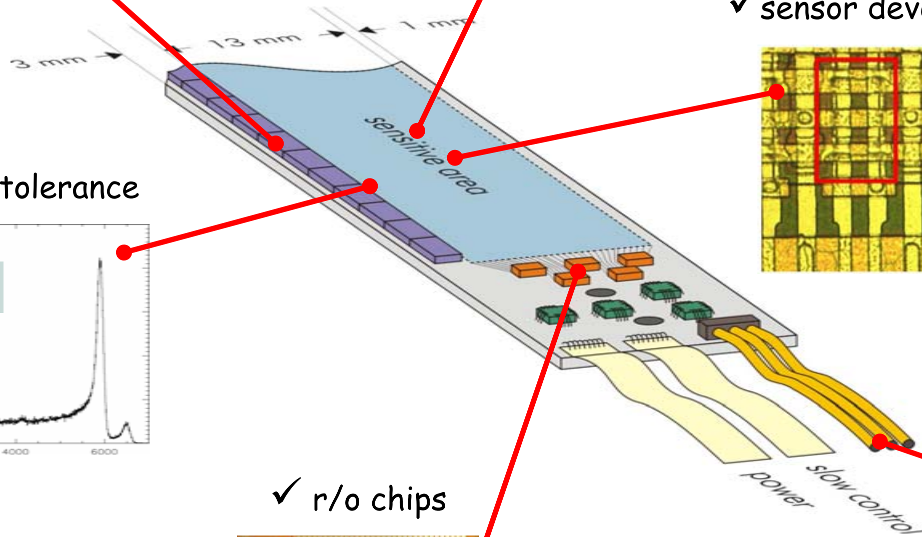


✓ sensor development

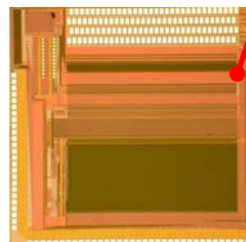


✓ radiation tolerance

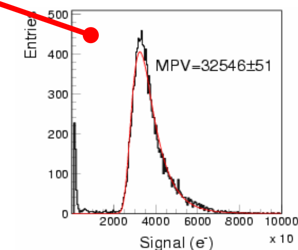




✓ r/o chips

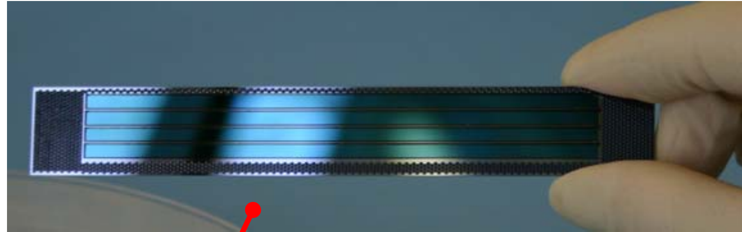


✓ beam test

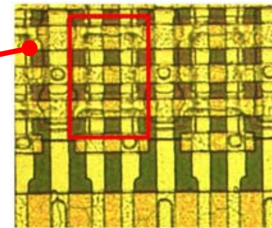


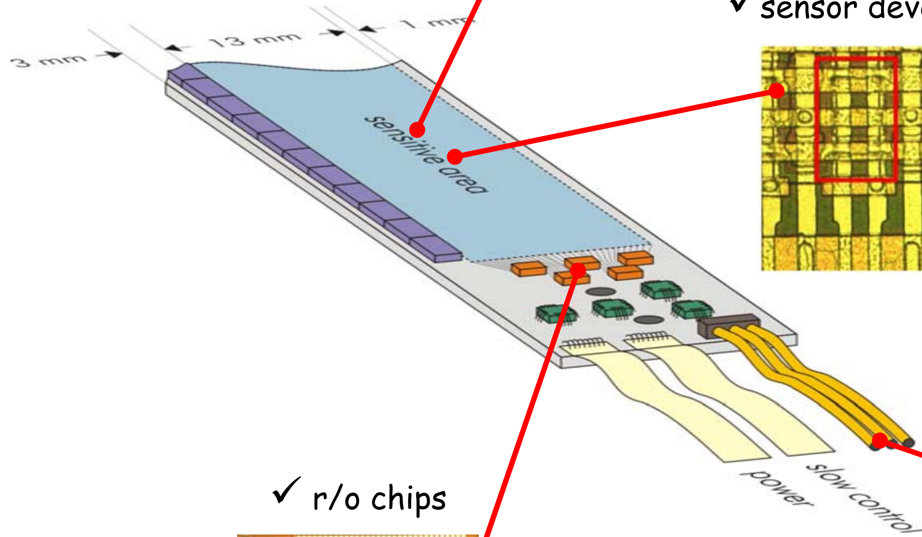
The DEPFET ILC VTX Project

✓ thinning technology

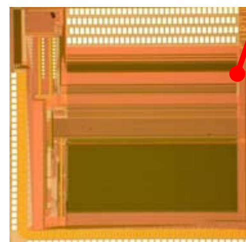


✓ sensor development

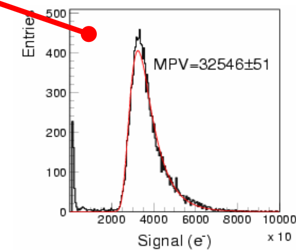




✓ r/o chips



✓ beam test

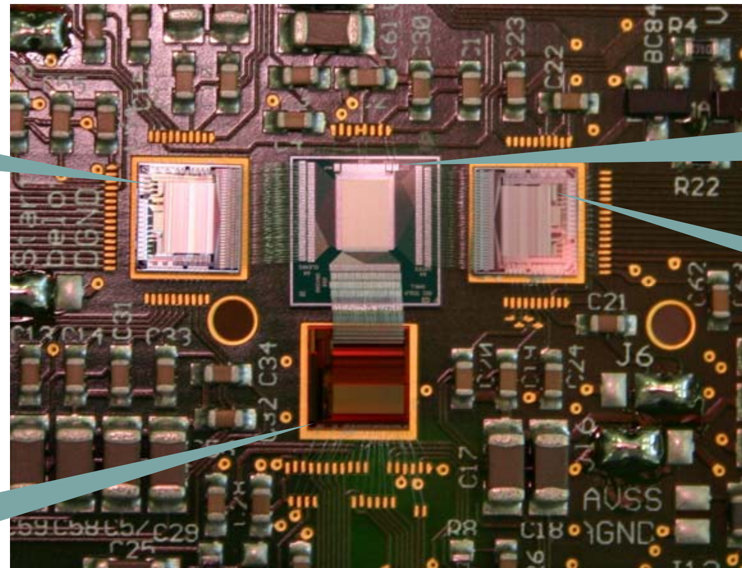


ILC Prototype System

mpi halbleiterlabor

Gate Switcher

DEPFET Matrix
64x128 pixels, 33 x 23.75µm²



Clear Switcher

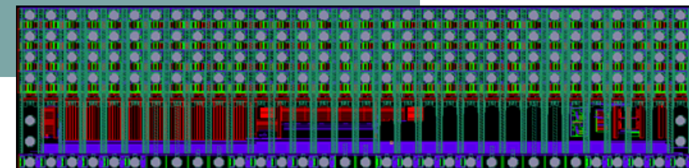
- 2 analog MUX outputs with
- 64 channels each
- Can switch up to 25 V
- 0.8µm AMS HV technology

Current Readout CUROII

- current based 128 channel readout chip
- 50 MHz band width in the f/e
- On-chip pedestal subtraction by switched current technique (CDS)
- Real time hit finding and zero suppression
- 0.25µm CMOS technology (radhard design)

new SWITCHER 3 available now:

- 0.35 µm technology
- rad. hard technology
- 128 channels with up to 10V swing
- bump bond pads



Test Beam(s)

:- 5 test beam periods have been done in the past

3 x @ DESY (1-6 GeV e^-) – spatial resolution limited by multiple scattering to ~6µm for us.

2 x @ CERN (120 GeV π) – August and October 2006. Analysis still not finished...

:- Reference system

a. the 4 layer Silicon strip telescope (Bonn), double sided strip detectors, 50 µm pitch

b. high precision telescope, 4 reference planes of DEPFETs at CERN test beam

:- Sensors are

450µm thick (mip = 36ke)

min. pixel size = **33x23.75µm²**

various DEPFET variations have been studied

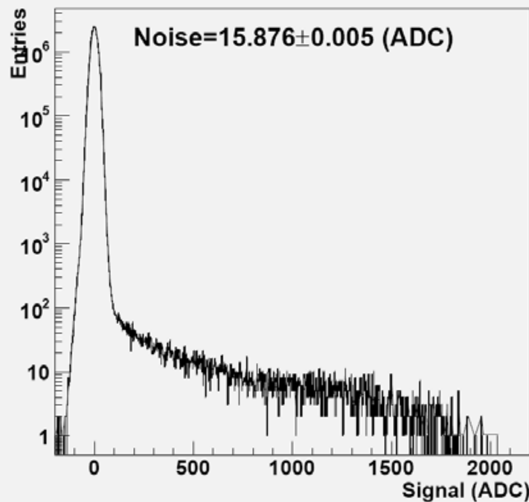
:- Speed:

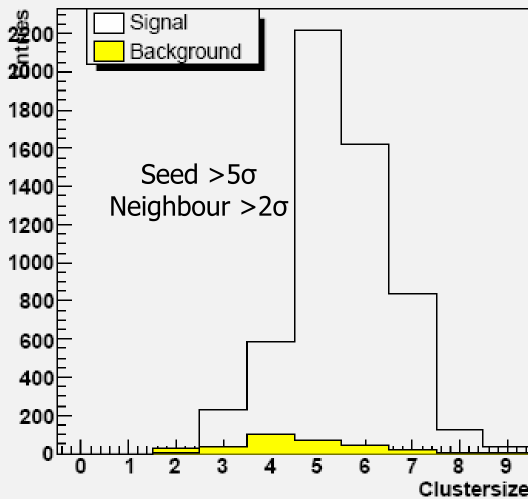
Clearing in 20ns

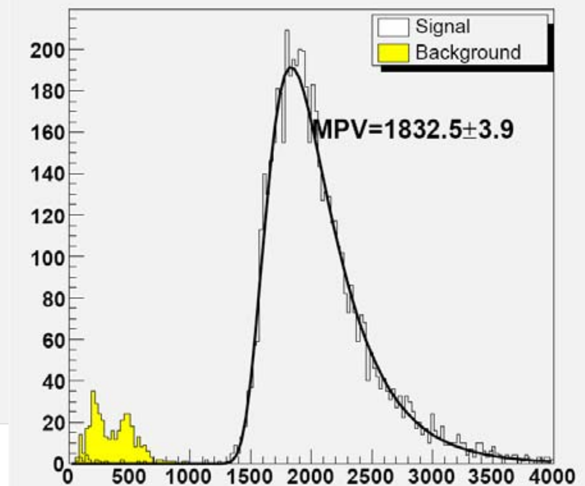
Sample-clear-sample in CURO: ~ 240 ns (This would give a 4 MHz row rate)

Non-zero suppressed readout (mostly)~ 800 µs/frame (128 rows) → ~ 6 µs/row

Test Beam at DESY, Jan. '06







(Jaap Velthuis)

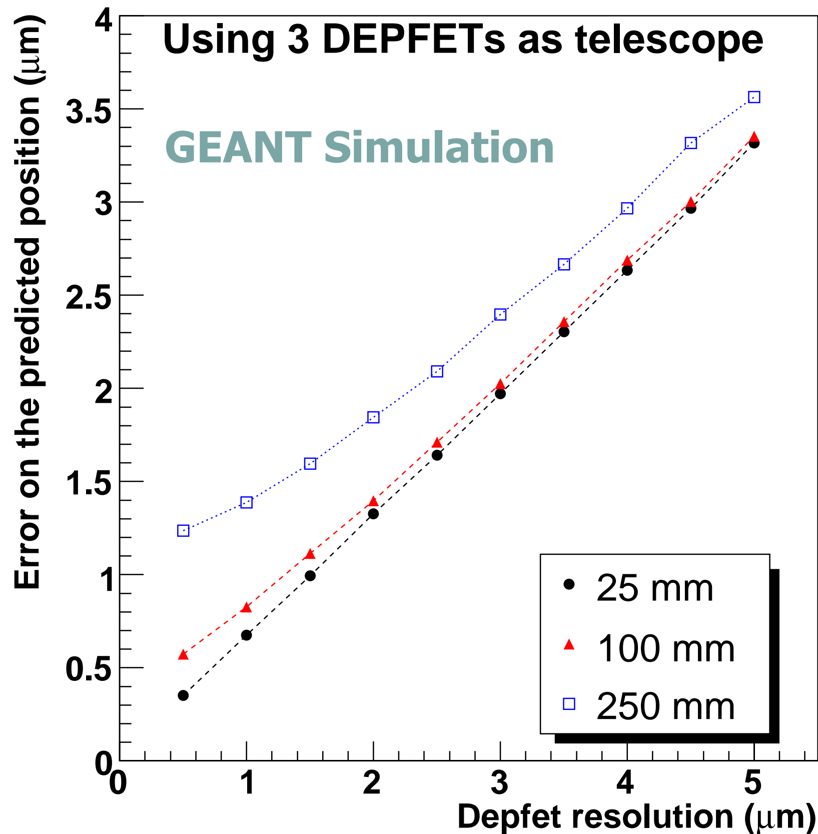
- Noise is determined from pedestal variations
- Seed pixel has signal >5 σ in central area
- Add neighbors if signal ≥2σ
- charge mostly confined in 3x3 cluster

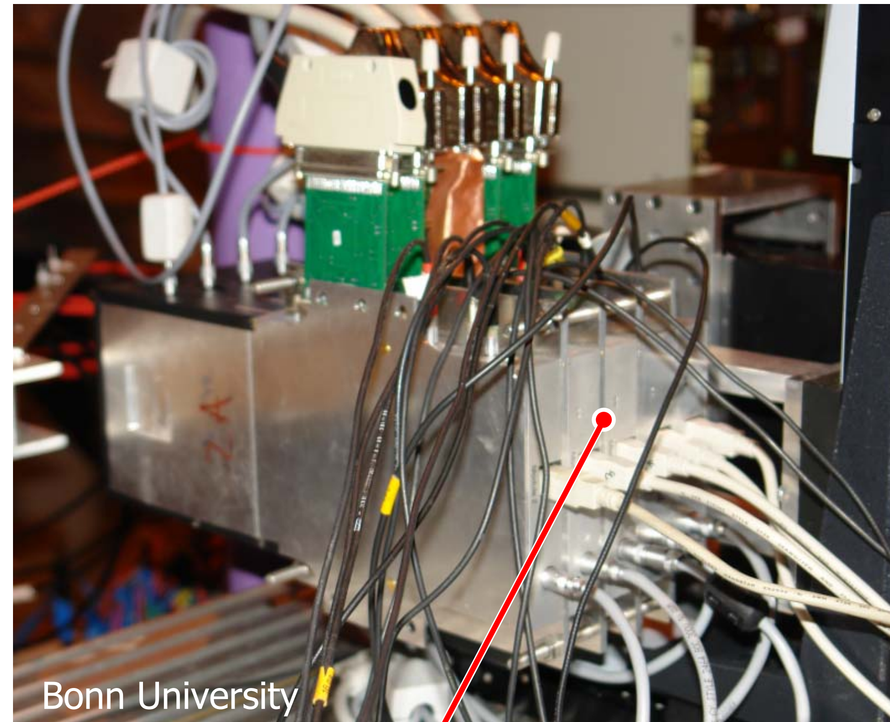
- S/N ≈ 110..120 (for 450 µm sensor!)
- Noise about 300 e- ENC

most of the noise is attributed to the CURO II chip (internal cross talk, noisy f/e, noisy current storage cells..)

Test Beam Setup (at CERN)

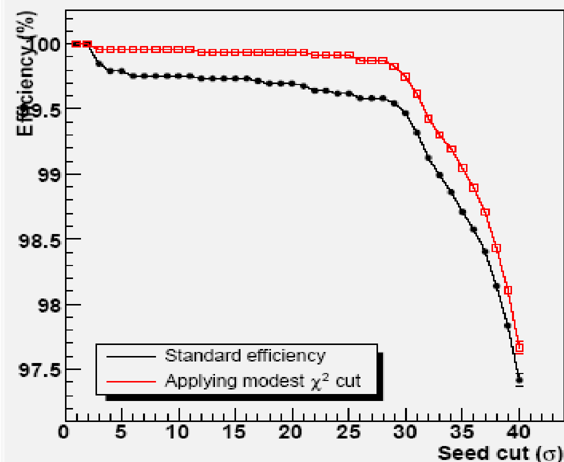
The high precision DEPFET telescope
→ <1 µm track resolution in the DUT plane





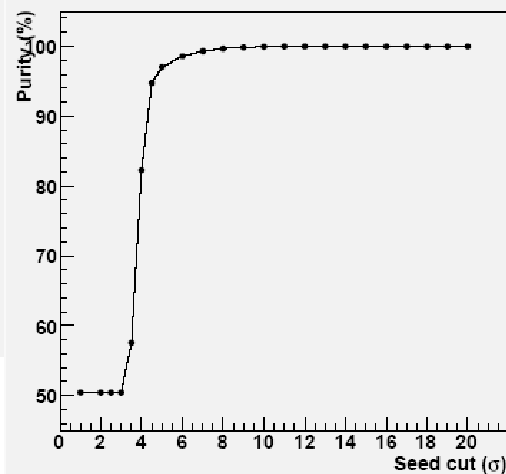
5 (!) DEPFET planes, Δx=25mm

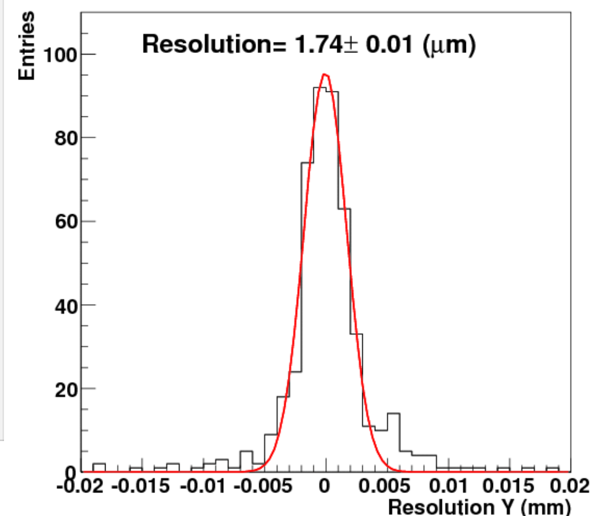
Efficiency & Position resolution



$$\text{Efficiency} = \frac{\text{Number of tracks with cluster}}{\text{Total number of tracks}}$$

$$\text{Purity} = \frac{\text{Number of clusters with tracks}}{\text{Total number of clusters}}$$





(Jaap Velthuis)

For 5 σ seed cut

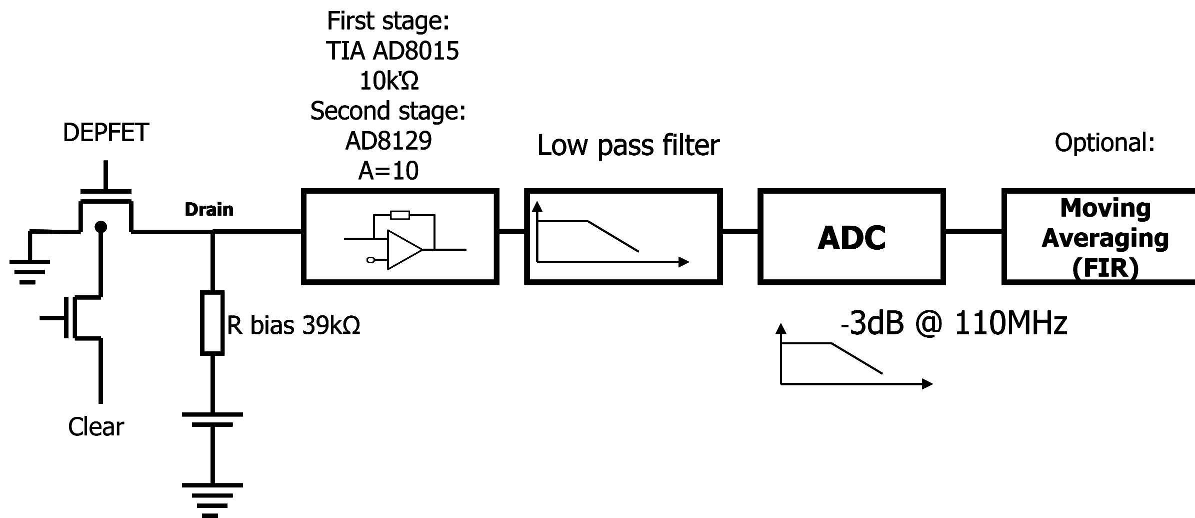
- Efficiency ≈ 99.96%
- Purity ≈ 99.6 %

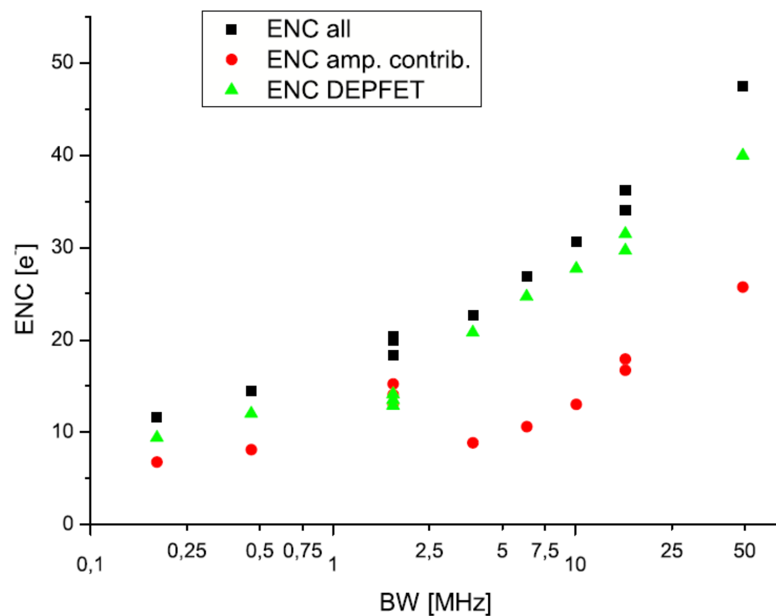
First results from CERN test beam now available:

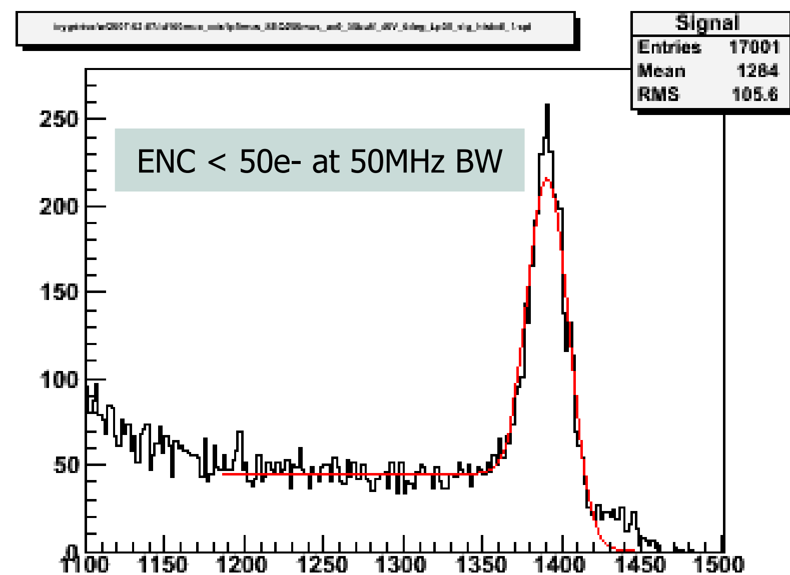
120 GeV π, 33x23.75 μm² pixels

single point resolution ≈ 1.7 μm

DEPFET noise at high BW



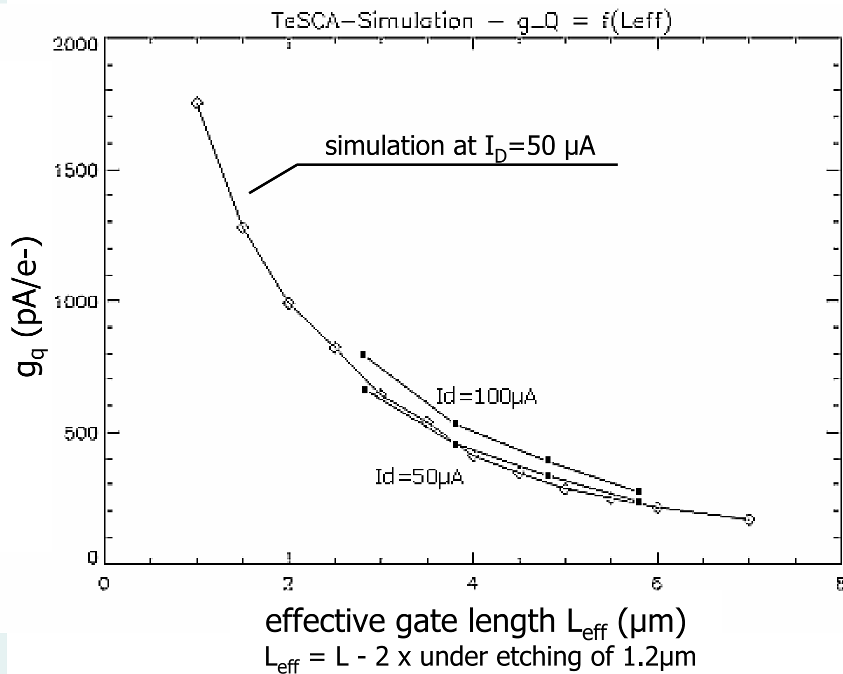




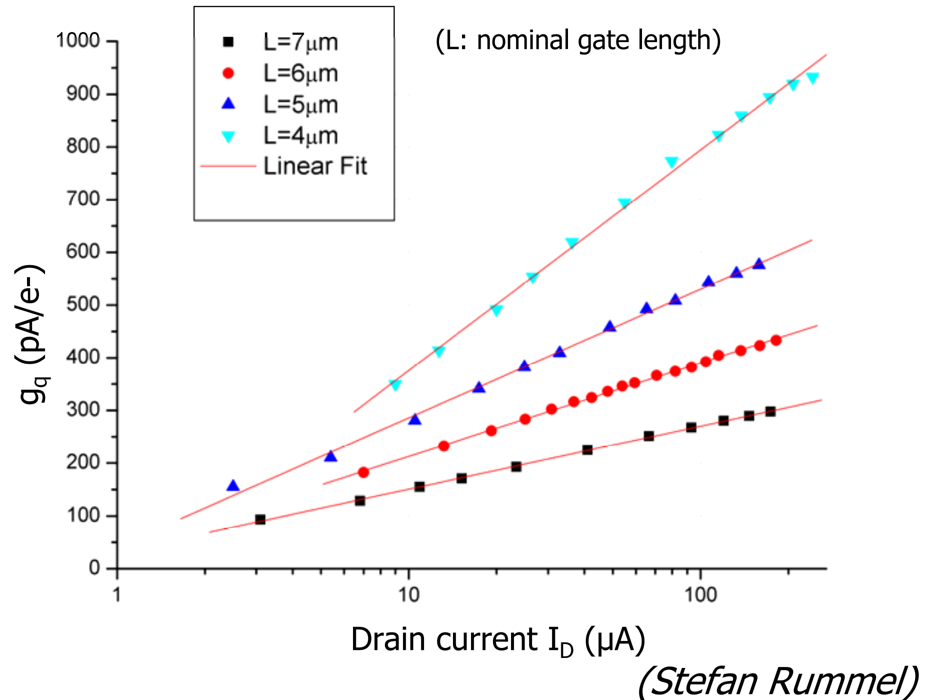
(Stefan Rummel)

Internal amplification g_q

$$g_q = \frac{dI_D}{dQ} = -\frac{\mu_p}{L^2}(V_{GS} - V_{th})$$ (neglecting short channel effects)



L_{eff} = L - 2 x under etching of 1.2µm



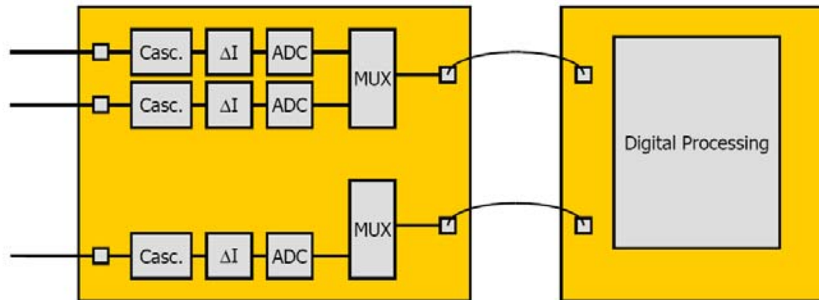
(Stefan Rummel)

As long as noise is dominated by r/o chip → S/N linear with g_q

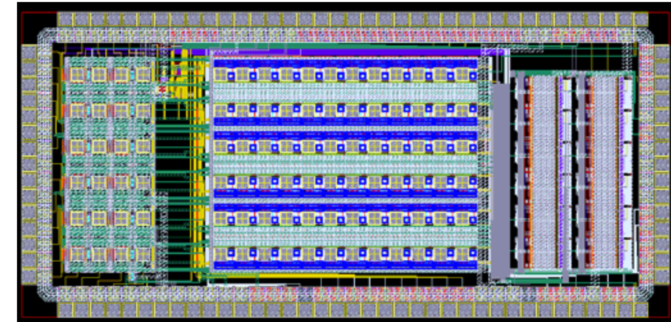
PXD4 has L=6µm, some matrices in PXD5 have now L=4µm → expect factor 2 better S/N

A new r/o chip - DCD1

DCD: **D**rain **C**urrent **D**igitizer



Test chip: 6X12 channels (pixels)



submitted (UMC 0.18), April 2007

what is new?

-: improved input cascode (regulated) and current memory cells

-: designed for 40 pF load at the input (1st layer ILC VTX)

-: f/e noise: 34nA@40pF, 17nA@10pF, add 37nA for memory cells→ **50nA@40pF**
→ at 40pF with g_q=500pA/e → **100 e- ENC in total**

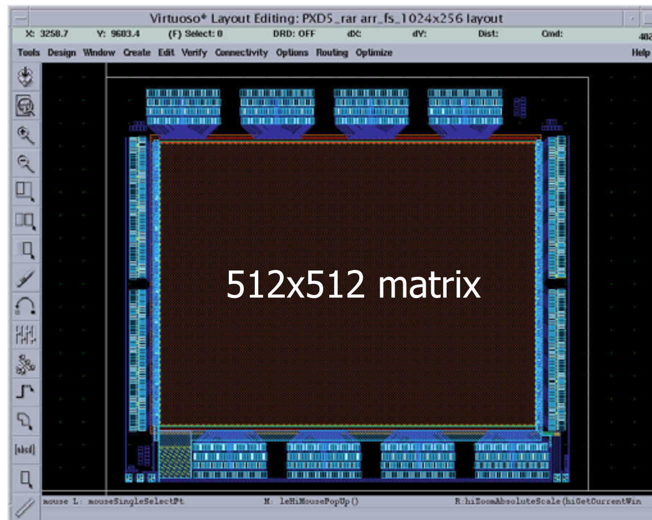
-: 2 current based ADCs per pixel, 6 bit

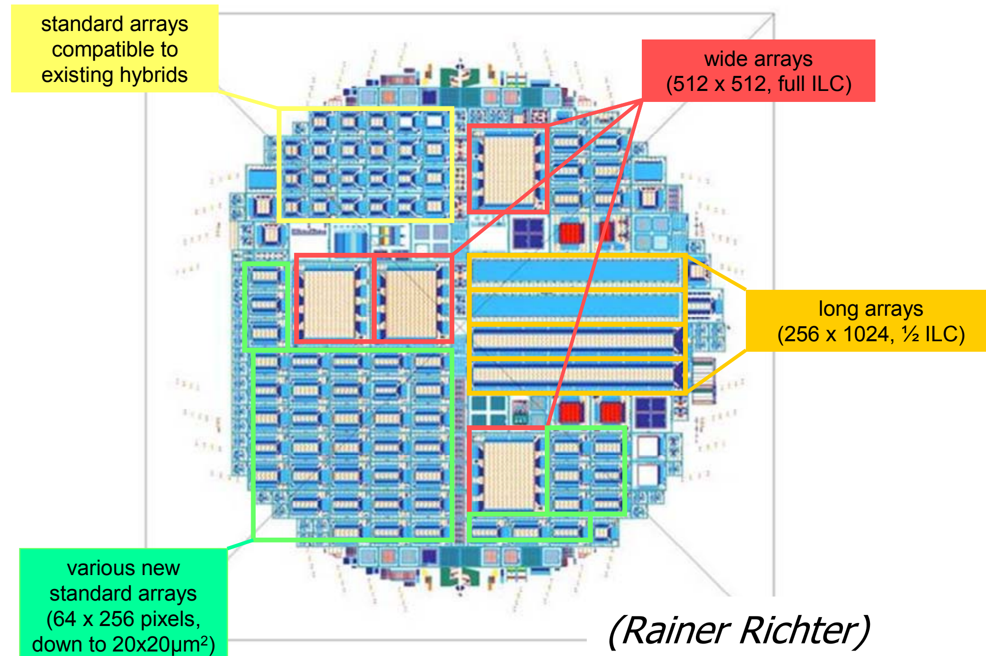
-: layout for bump bonding

(Ivan Peric/Peter Fischer)

New DEPFET Generation 'PXD5'

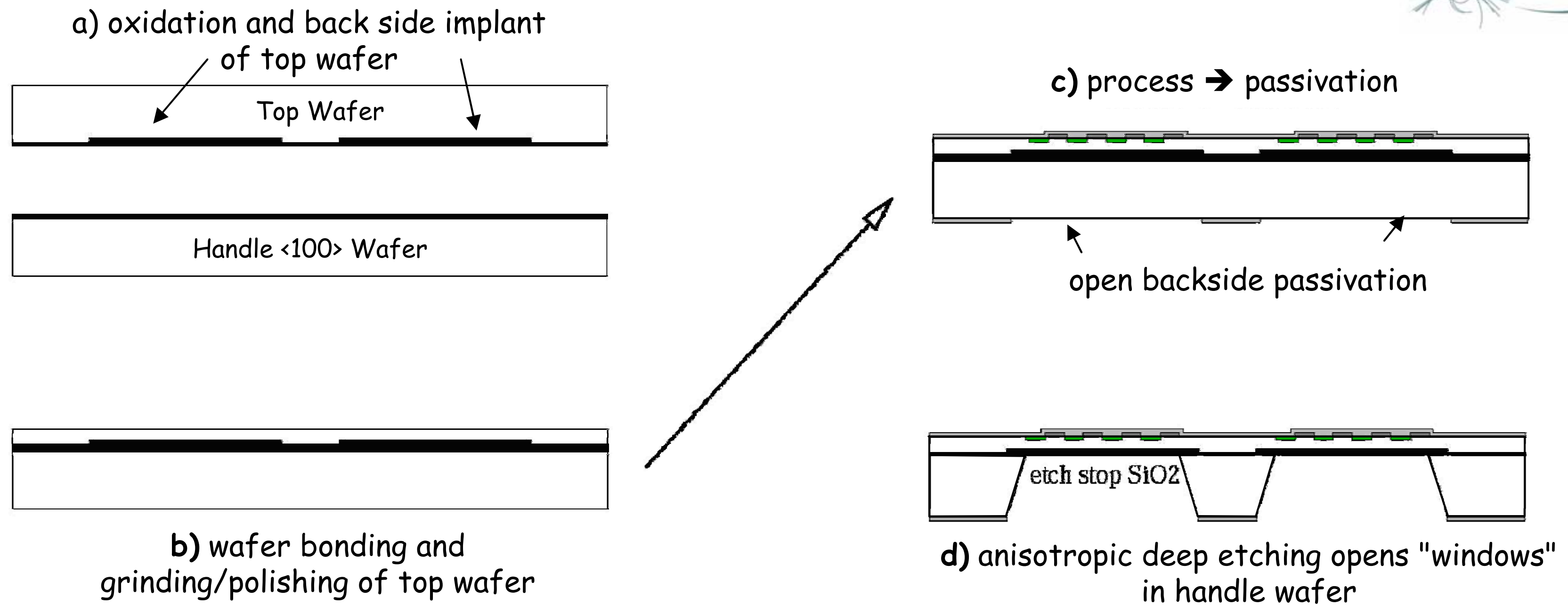
- Mostly use 'baseline' linear DEPFET geometry
- Build **larger matrices**
  - Long matrices (full ILC drain length)
  - Wide matrices (full Load for Switcher Gate / Clear chips)
- Try new DEPFET variants:
  - reduce **clear voltages** (modified implantations, modified geometry)
  - Very **small** pixels (20µm x 20µm)
  - Increase internal **amplification** (g_q)
- Add some bump bonding test structures





(Rainer Richter)

Thinning Technology

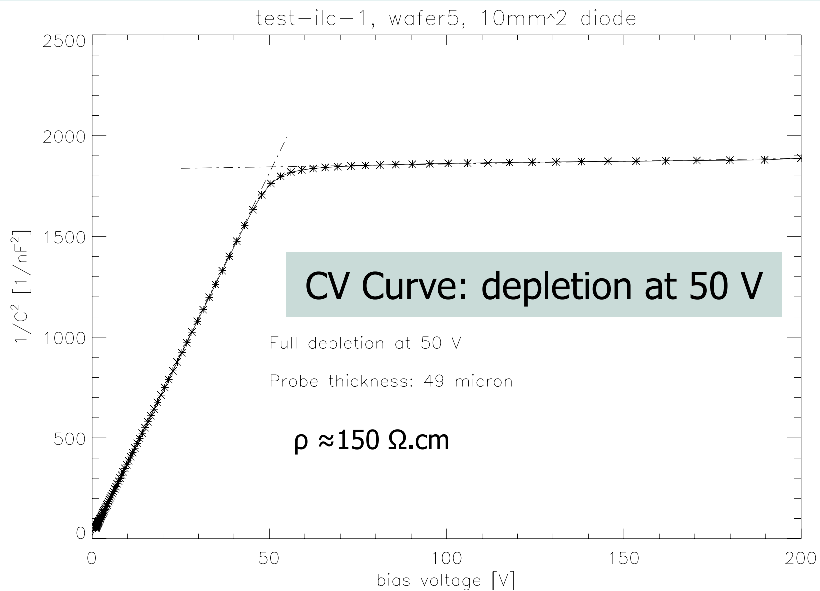


New: **150mm** Ø wafers!
New: Wafer bonding and thinning in **industry**
New: Compatibility with the main production line tested

Still in R&D phase:
1: processing test structures on SOI wafers
2: mechanical samples

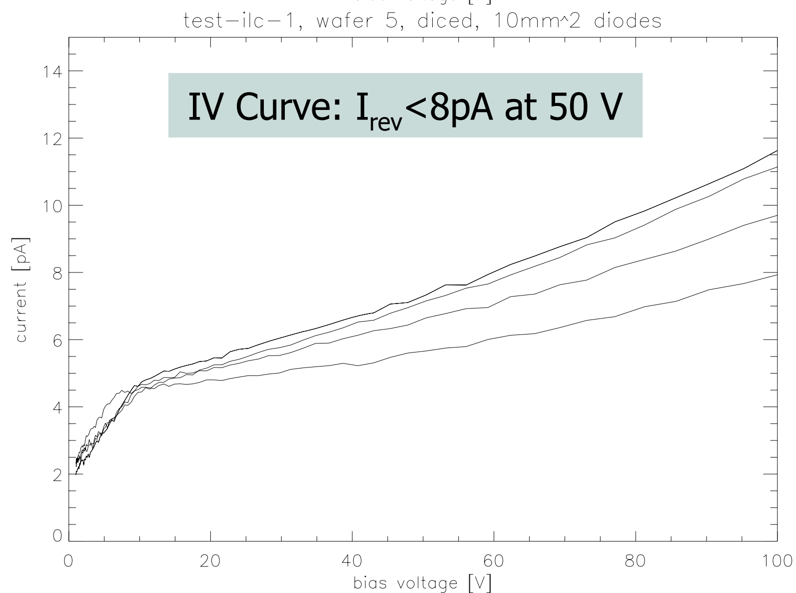
PiN Diodes on thin Silicon

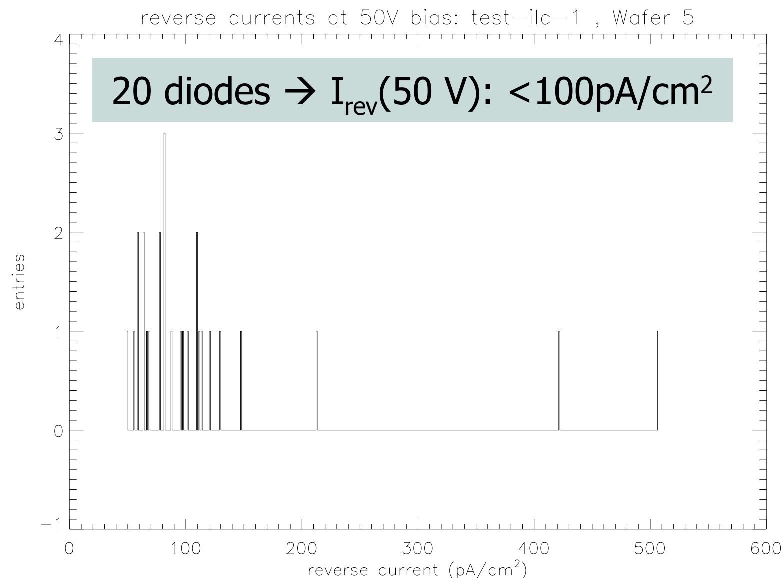
mpi halbleiterlabor



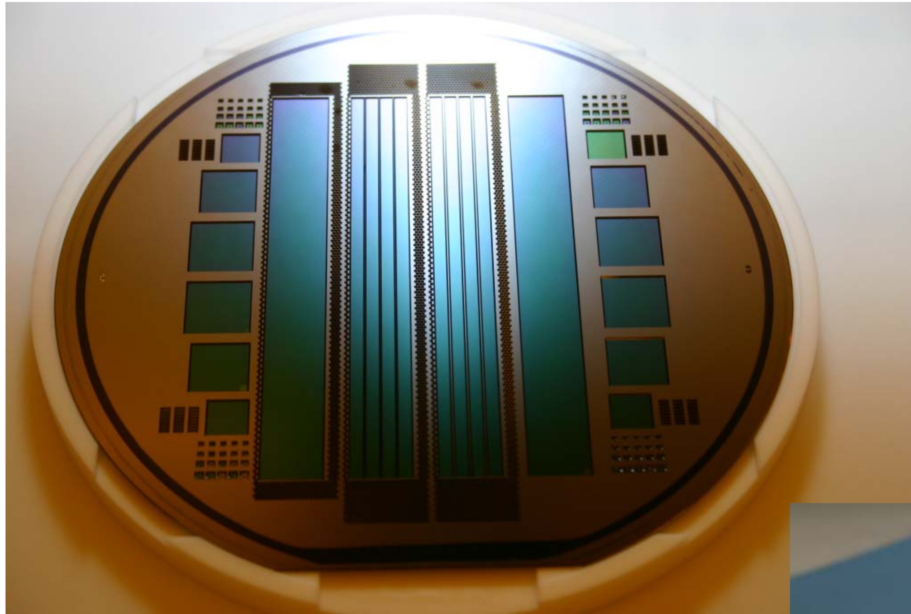
Thin diodes have **excellent** leakage currents.

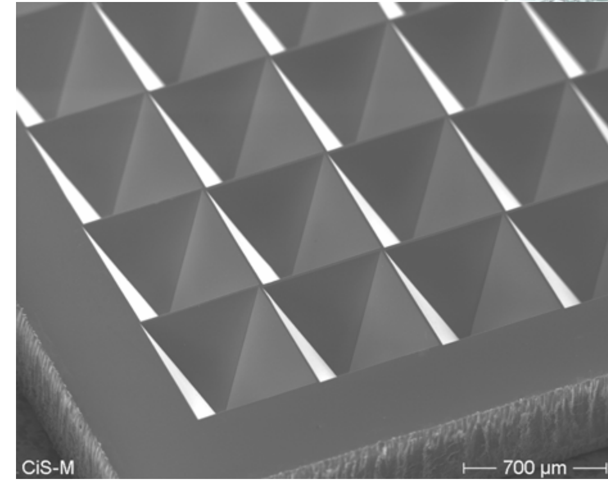
Processing of the SOI wafers and removal of handle wafer
does not degrade devices!

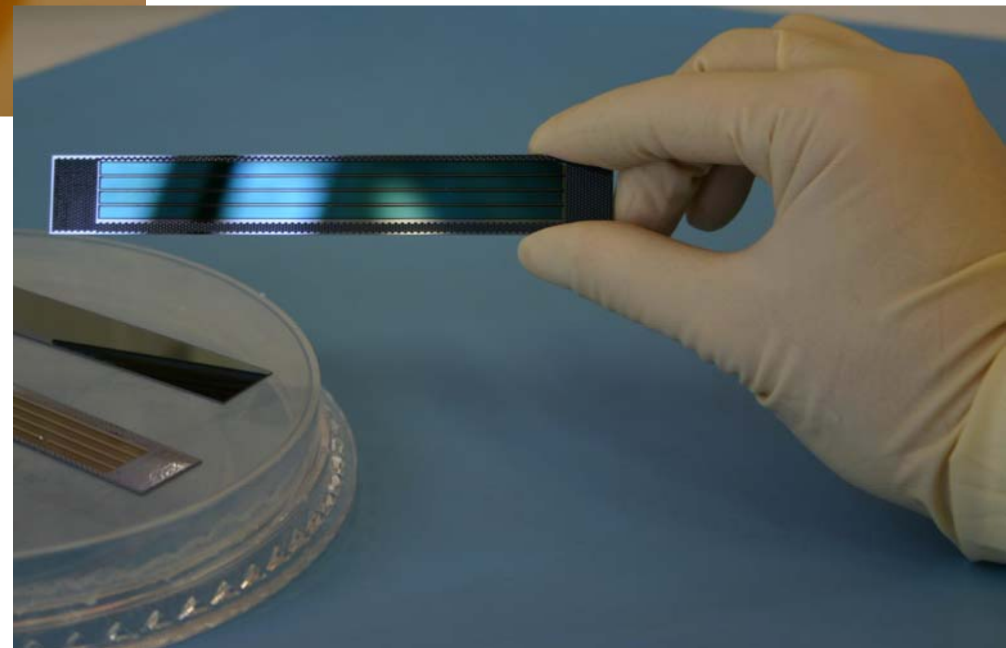


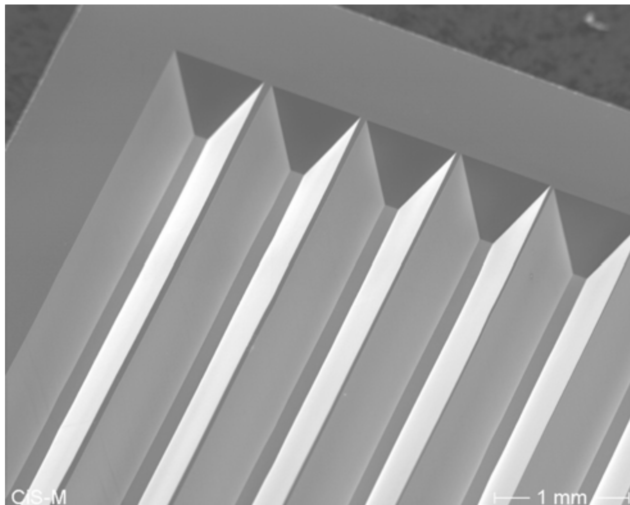


Thinning : mechanical samples









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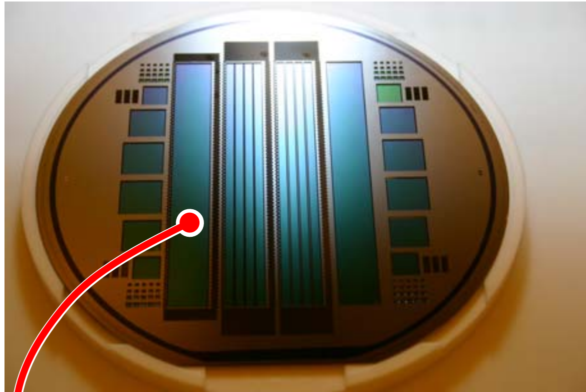
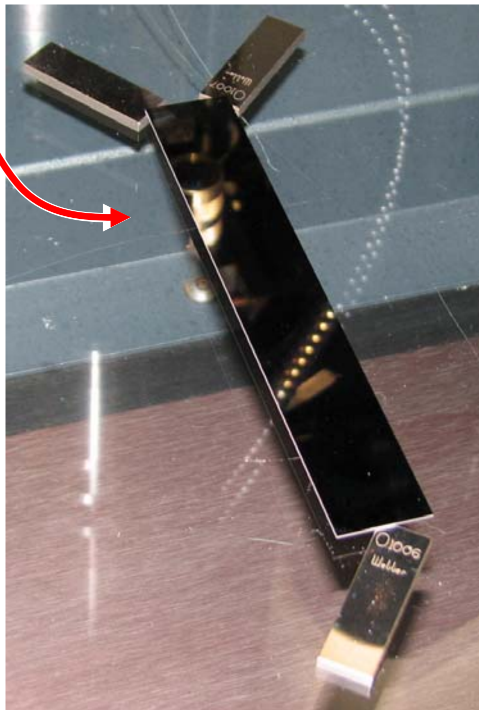
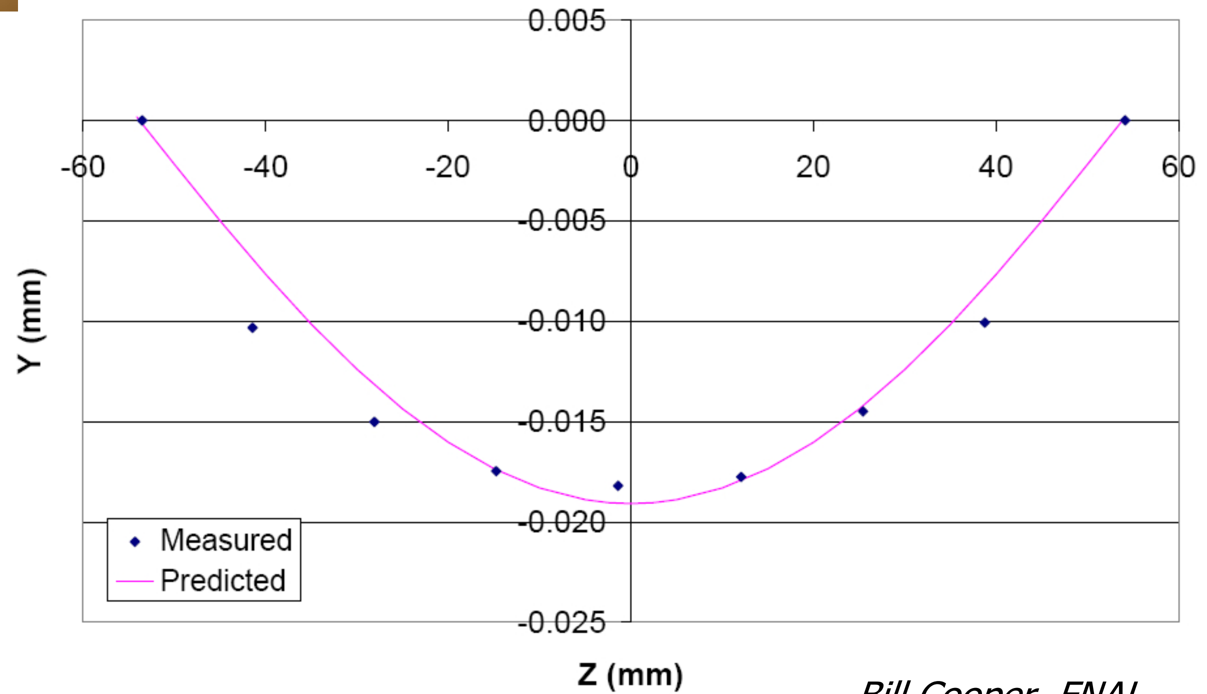




full size 1st layer module:

100x13 mm² sensitive area, 50 µm thin, 400 µm frame, no support bars

→ 20 µm deflection due to gravity



Bill Cooper, FNAL

~~Roadmap~~ Subway map towards a thin demonstrator

	2006	2007	2008	2009	2010
DEPFET **incl. rad. tolerance**	PXD5		PXD6		
Thinning					
chips/system development	CURO3 SWITCHER3	DCD1			full size demonstrator
thin Me./El. Samples					
interconnections on & off module					
Engineering module/barrels/ discs…					

Summary

- ✓ Matrices operated ‘routinely’ in test beams at DESY and CERN including a 5 layer **DEPFET telescope with sub-micron precision.**
- ✓ **New sensor production** with larger devices and improved DEPFET pixel cells **almost finished**.
- ✓ **Reducing the channel length** of the DEPFET translates directly into a **higher S/N** in the experiment! **Dry etching** would make it possible to exploit the potential of the DEPFET and is therefore **highly desirable**!
- ✓ **Thinning** technology at the door step to migrate to the production line. Excellent results using a commercial supplier for the engineered SOI wafers.

We are on schedule for the construction of a full size thin demonstrator by 2010!