

A New High-Speed, Single Photon Imaging CCD for the Optical

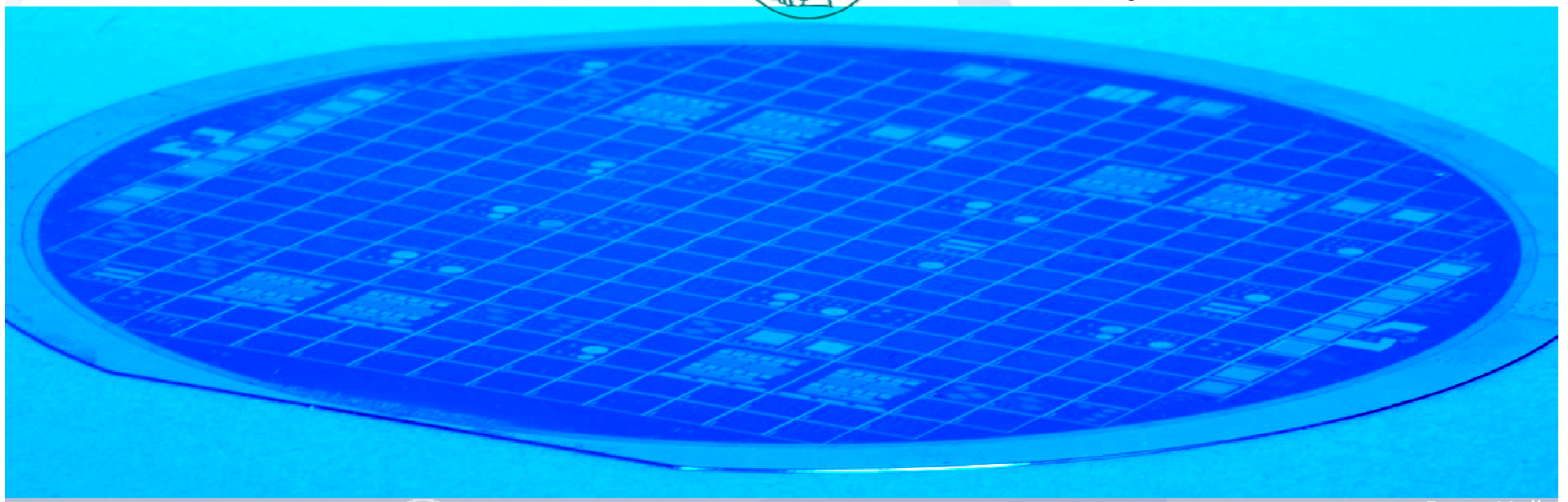
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Outline

- Introduction:
 - Motivation
 - Principle of a Single Photon Imaging CCD
- Approach / Components
 - New low noise pnCCD
 - Entrance window for optical light
 - Back illuminated avalanche diodes
 - Avalanche readout test circuit
- Project Status, Summary and Outlook

Motivations

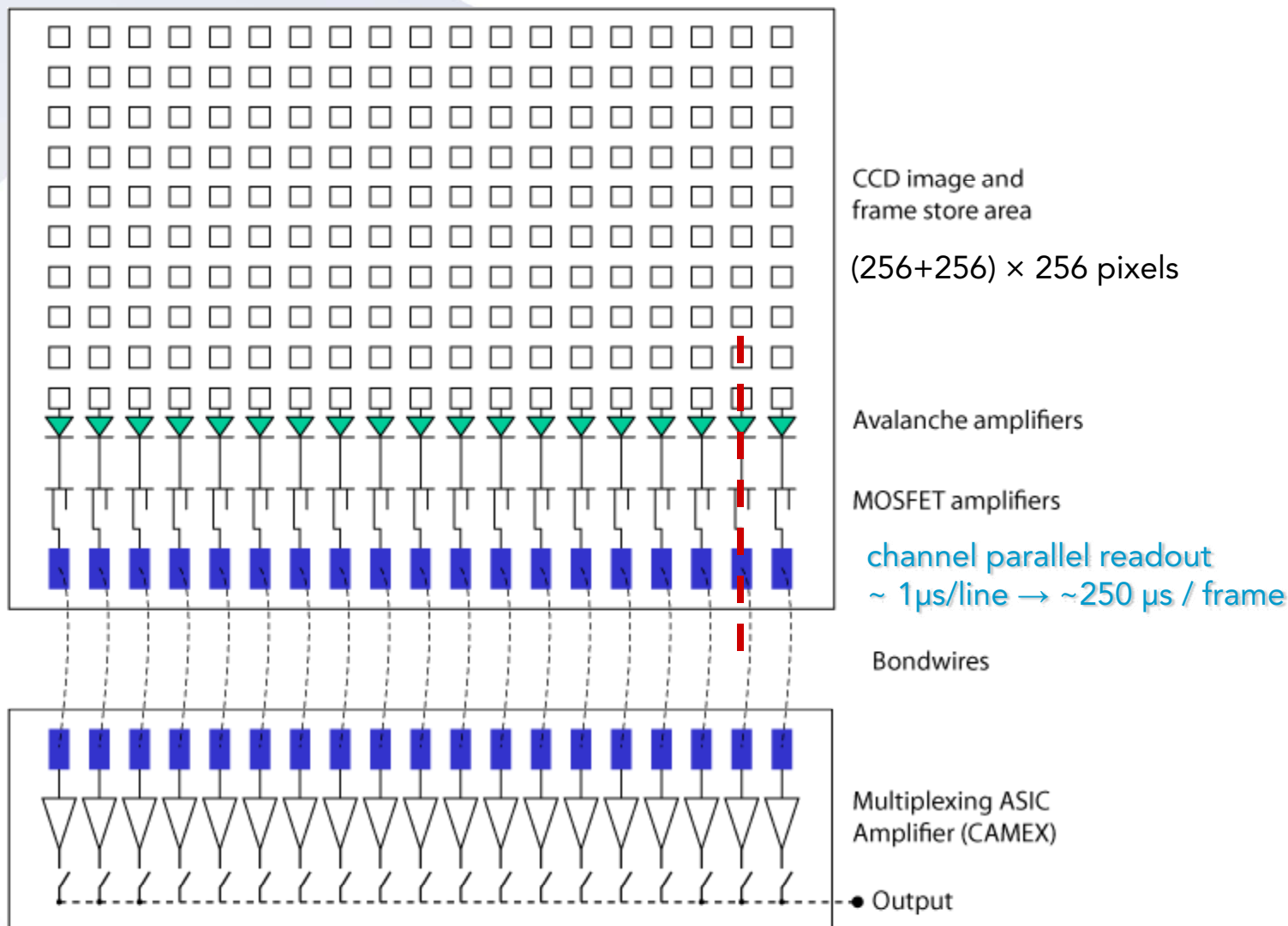
Applications:

- High Time Resolution Astrophysics (HTRA)
(Funding from OPTICON JRA3)
- General Low Light Level Imaging

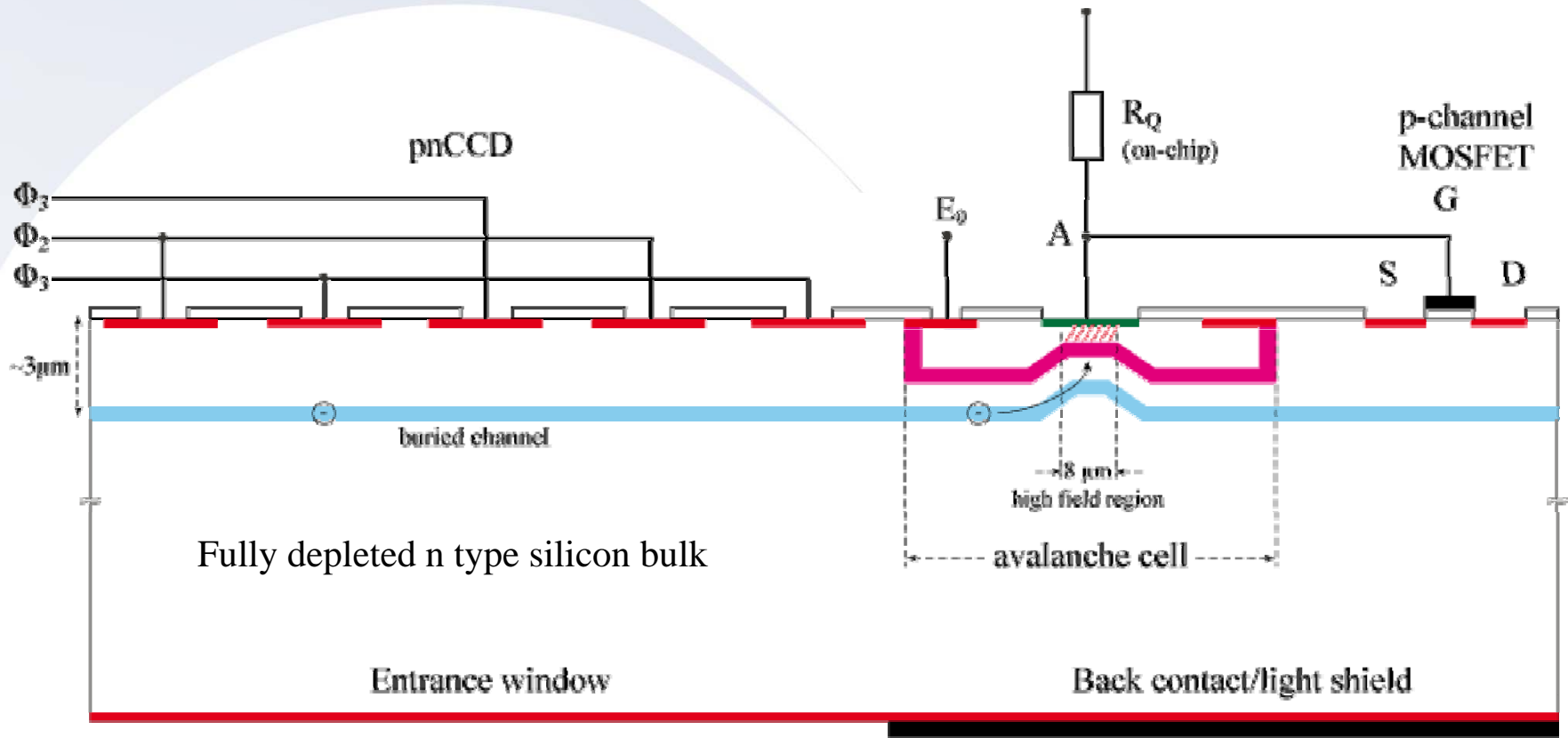
Performance:

- Superior to Existing Devices (L3CCDs and EMCCDs)
- Higher Frame Rate (up to 2,000 Frames per Second)
- Better Photon Detection Efficiency (up to 80 %)
- Better Linearity by Photon Counting

Introduction: Avalanche CCD Principle



Introduction: Avalanche CCD Schematic Cross Section

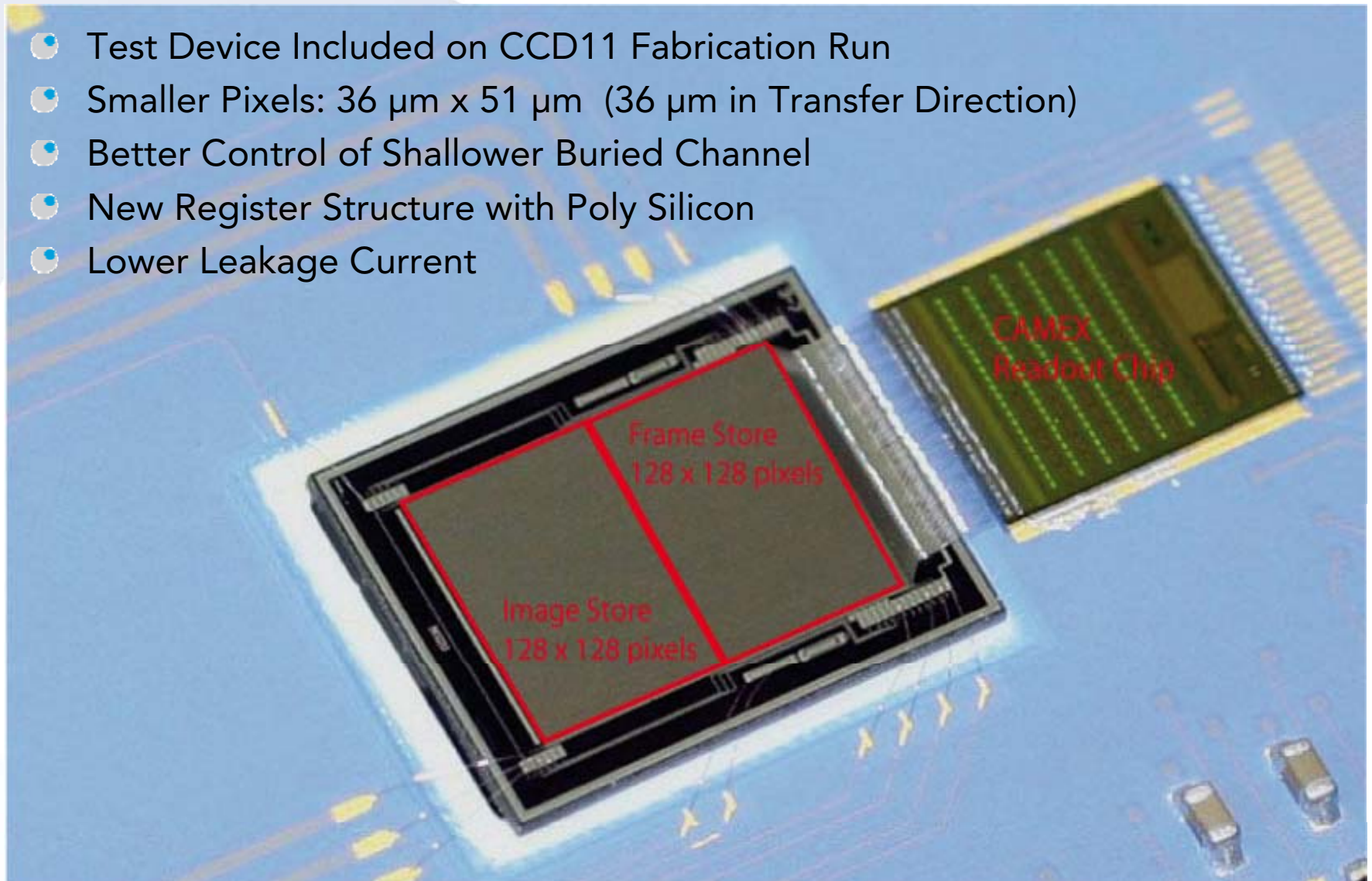


Approach to a New Device: Ingredients

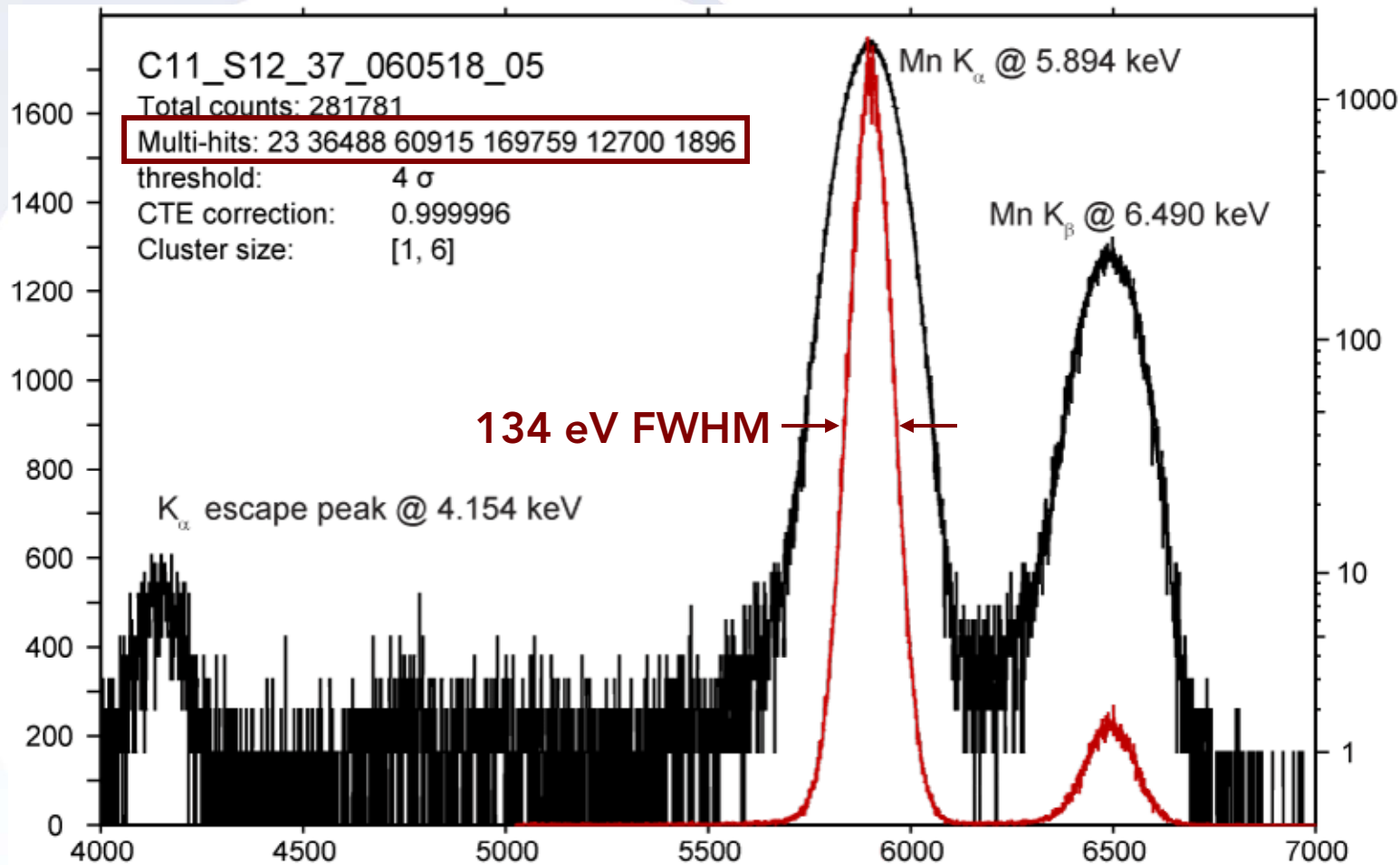
- CCD Region
 - Entrance window well established – can be adapted
 - Low Noise pnCCD, new register topology – to minimize dark rate
 - Similar design **successfully tested** (experimental device on CCD11)
 - Advanced design in current fabrication (CCD14 for SCLS)
 - Additional structures to suppress optical crosstalk (designed, AVA-ET)
- Avalanche Readout
 - Avalanche diode, feasibility **tested successfully** (AVA-QT)
 - n-Channel MOS-FET Readout **tested successfully** (AVA-QT)
 - Compatibility to CCD (designed for AVA-ET)

Novel Low Noise pnCCD: Overview

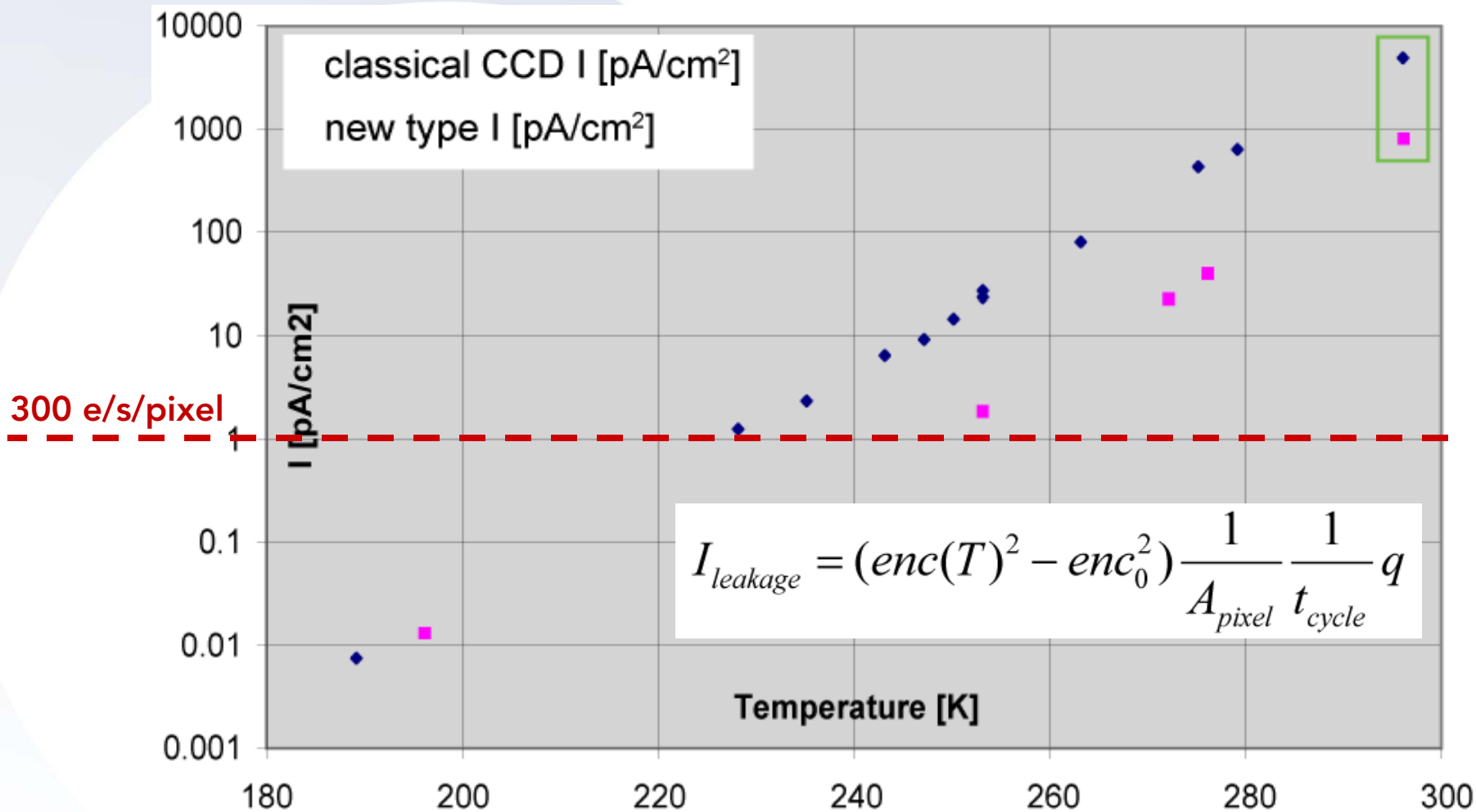
- Test Device Included on CCD11 Fabrication Run
- Smaller Pixels: $36\ \mu\text{m} \times 51\ \mu\text{m}$ ($36\ \mu\text{m}$ in Transfer Direction)
- Better Control of Shallower Buried Channel
- New Register Structure with Poly Silicon
- Lower Leakage Current



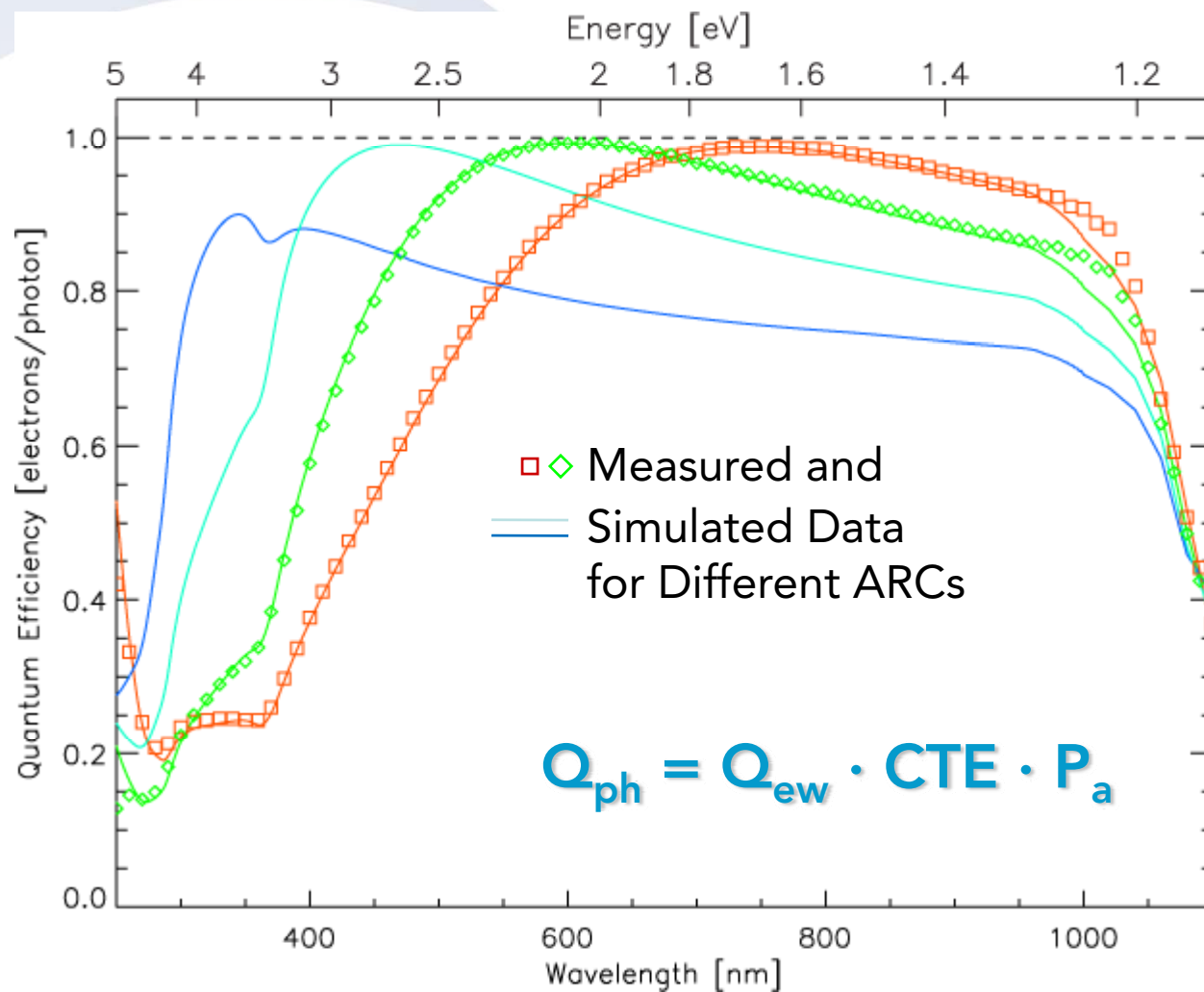
Novel pnCCD: ^{55}Fe X-Ray Spectrum



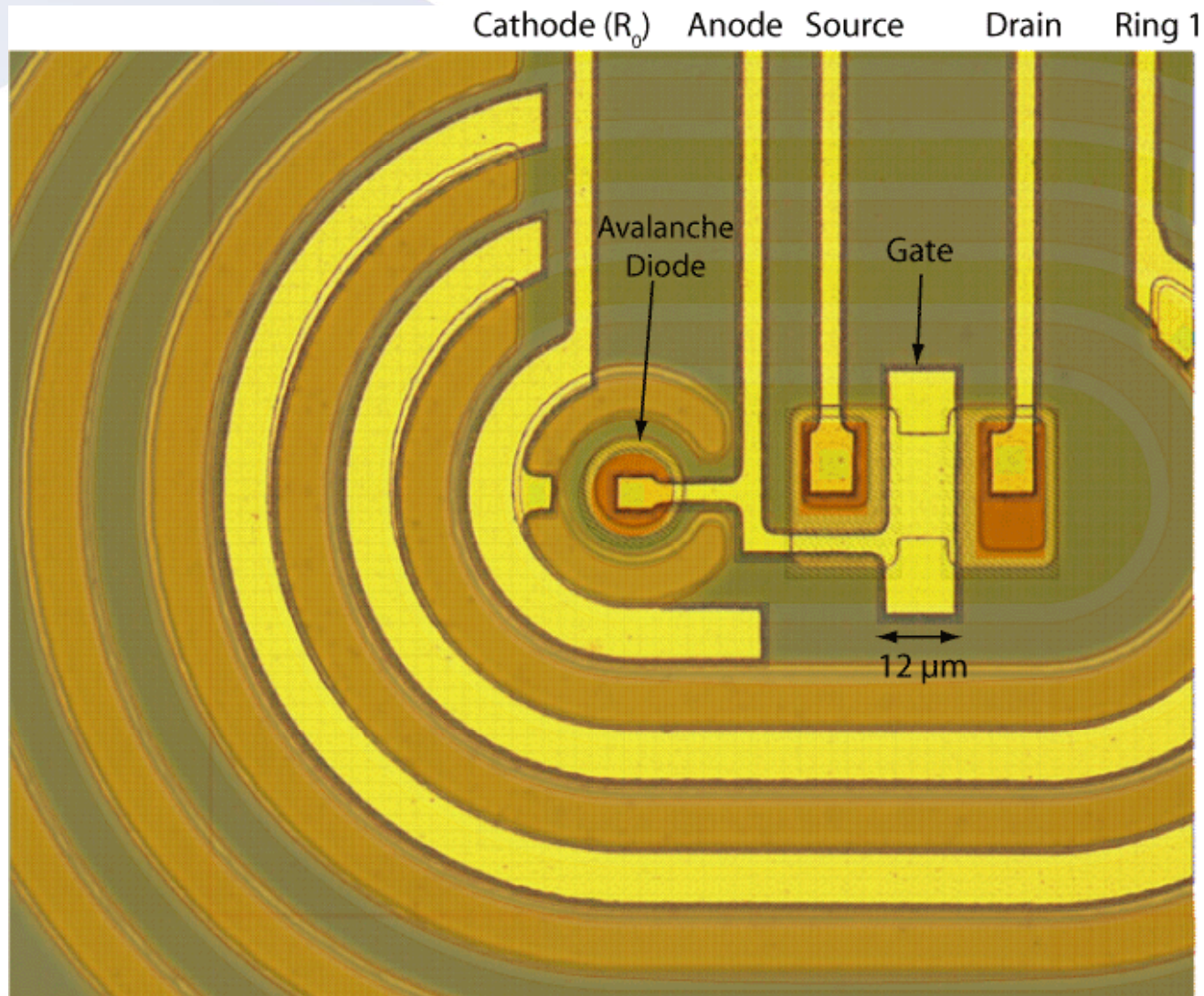
Novel pnCCD: Leakage Current Comparison



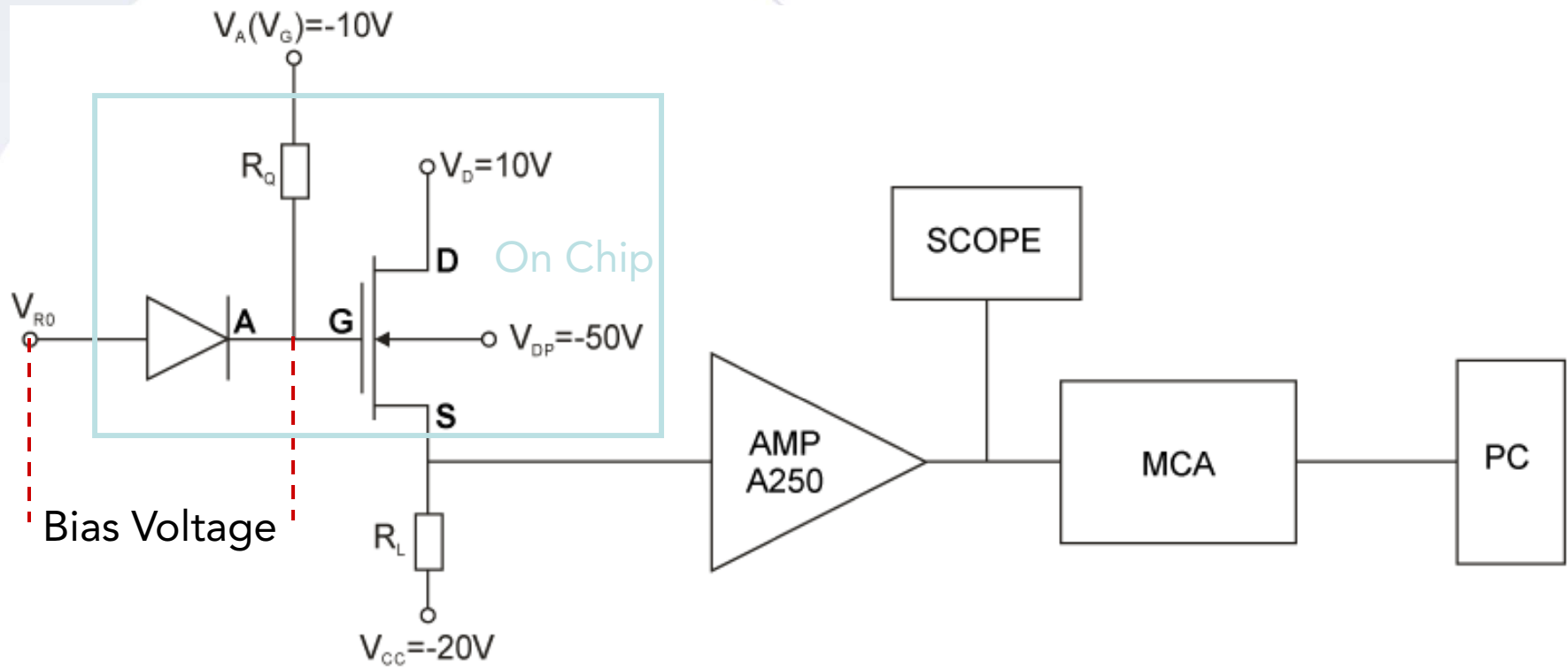
Entrance Window of Back Illuminated Devices



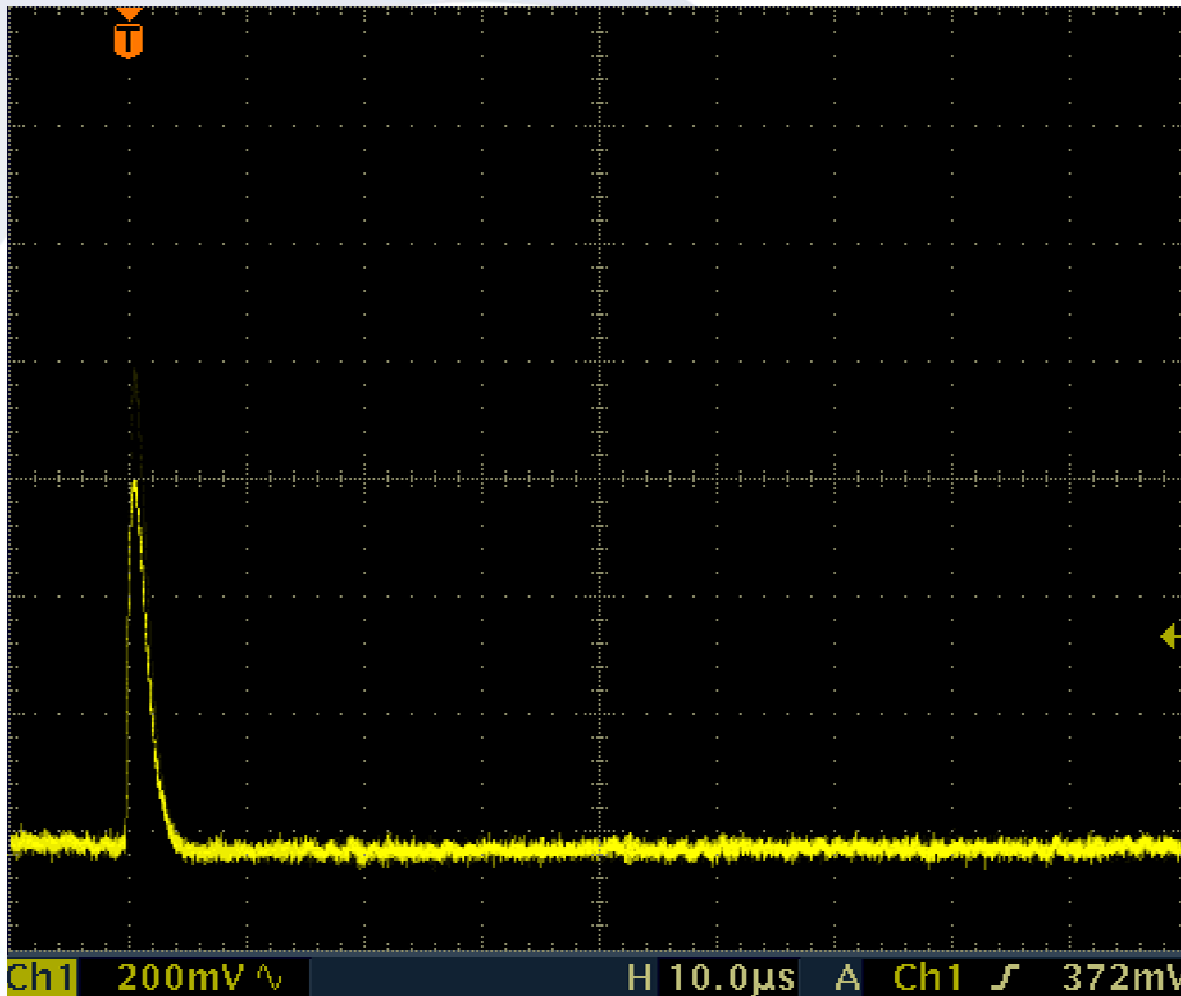
Avalanche Diode with NMOSFET Readout



Circuitry for Avalanche-NMOSFET Readout



Avalanche Diode: Single Electron Signal

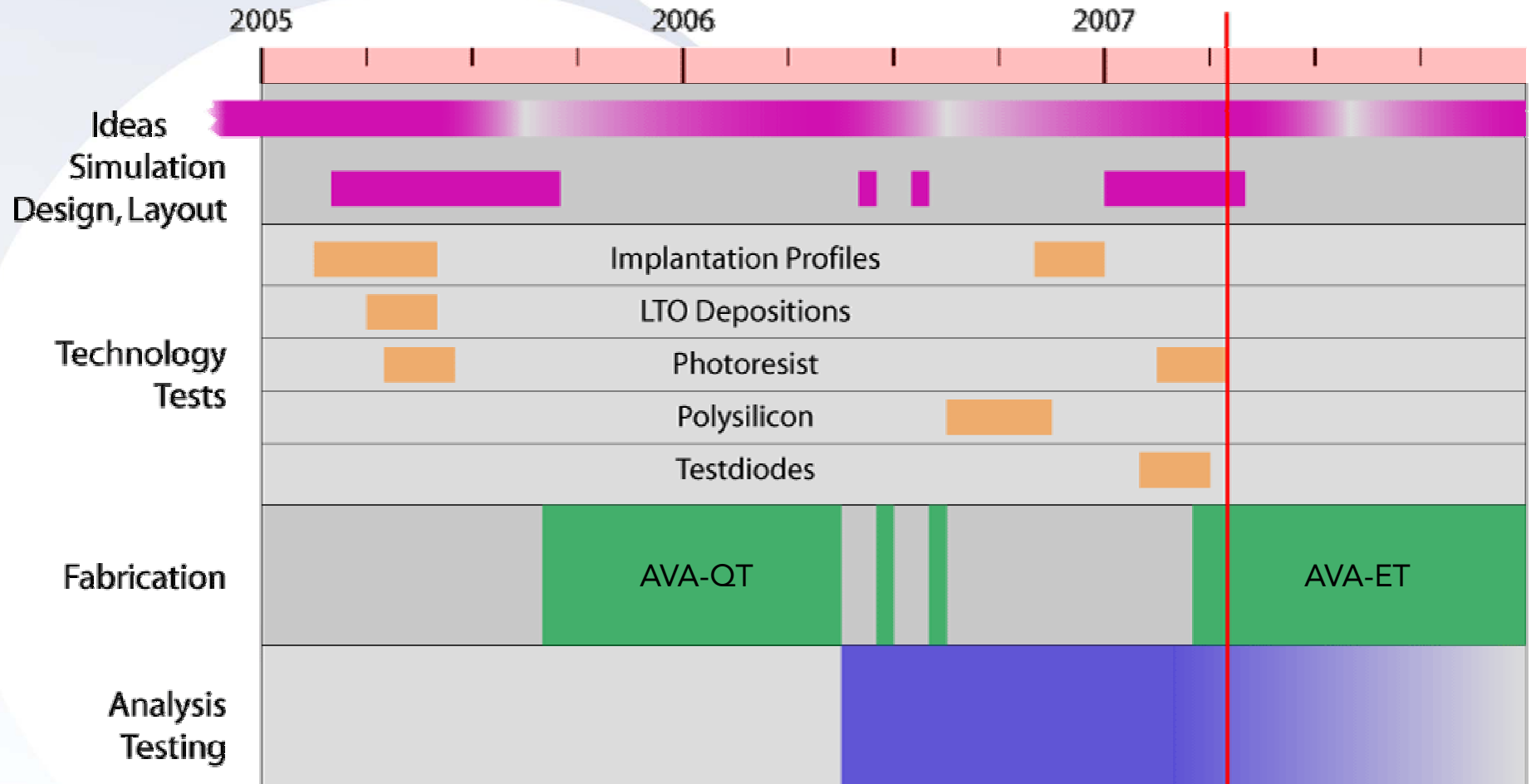


Rise Time: 400 ns

Fall Time: 2.5 μs

Multiplication ~10000

Status: Where Are We?



Further Steps (April 2007)

Fabrication related:

- Layout completion (prelim.) *imminent*
- Production *ongoing*
- Further, More Detailed Simulations *ongoing*
- Evaluation of Inline Measurements *~ 1 month*
- Finetuning of Layout and Fabrication *ongoing*

Measurements

- Additional Tests of 36 μm CDD from *starting May*
different Wafer Types (Temperature Scans)
- Preparation of Independent CCD Test Setup *planning phase*
- Concept for Operation (High Offset of *planning phase*
Clock-Voltages)
- Design and Fabrication of Mounting Modules *end of 2007*

CCD Variants

Pixel Size 51 μm x 51 μm

264 x (256+256) Pixels

1x **Avalanche/nMOS-FET Readout**
30 Chip Units (18 x 30 mm²)

132 x (60+60) Pixels

3x **with(out) Avalanche Multiplication**
with(out) Crosstalk Reduction
2.25 Chip Units (9 x 9 mm²)

132 x 60 Pixels

4x **Layout Variations**
1.5 Chip Units (9 x 6 mm²)

Pixel Size 75 μm x 71 μm

128 x (60+60) Pixels

2x **Avalanche/nMOS-FET Readout**
Crosstalk Reduction
4 Chip Units (12 x 12 mm²)

128 x 40 Pixels

2x **Layout Variations**
1.5 Chip Units (9 x 6 mm²)

54 Chips Units (of 360) + Test Structures

Summary and Outlook

We Can Do It!

- All Key Components Successfully Tested!
 - Proof-of-Principle of Back Illuminated Avalanche Structure *Tested and Testing*
 - Low Leakage Current pnCCD *Measured*
 - High Q.E. Back Illuminated Entrance Window *Measured and Modeled*
 - High Speed Readout up to 2,000 Frames per Second *Tested*

We Will Do It!

- Production of CCDs with Further Improved Leakage Current *Started*
- Prototype Production with Double Sided Processing *Starting*
 - Will Include CCD with Avalanche Readout
 - Shall Show Overall Feasibility
 - Answers on Gain, Avalanche Probability, Optical Crosstalk
- Dedicated Production as Follow-Up to AVA-ET *Wanted!*