Interconnection Techniques

Sensor fabrication

-: high resistivity Silicon
-: Double sided processing
-: fully depleted bulk
-: at HLL mainly with integrated first amp. stage (JFET, DEPFET..)
-: "large" feature sizes
…
→ best possible sensor for a specific application

Microelectronics Industry

-: low resistivity Silicon
-: single sided processing
-: most of the bulk insensitve
-: lot of process steps not compatible with sensor fabrication
-: small (really!) feature sizes
-: technology ever changing and improving

→ dedicated readout chip

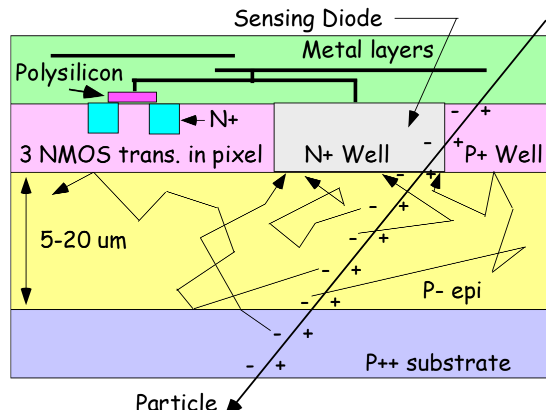
Interconnection

-: wire bonding (Danilo's talk…)
-: flip chip / bump bonding
-: 3D integration approach

→ Tailored detection system

Sensors made in CMOS Fabs

Sensors made in "CMOS" … compromises …

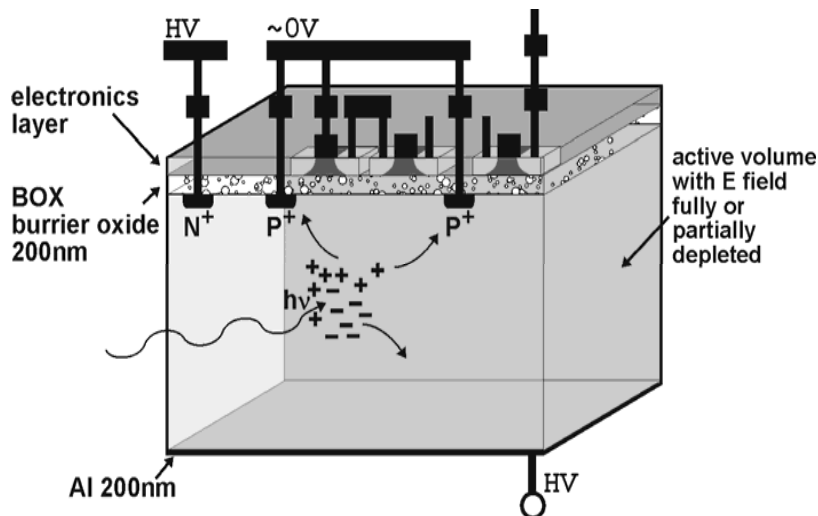


CMOS on epi material → MIMOSA, CAPS, FAPS..

(adoption of the CMOS Sensors for optical consumer cameras)

-: n-well as collecting Anode, collection by diffusion
-: restricted to epi Wafers (mainly AMS Opto Process)
-: can only use NMOS transistors in the p-well

→ mainly for the use as tracking detectors



CMOS on SOI wafers

major players: OKI, American Semiconductor, Hamamatsu (?)

-: use thin silicon layer on top for the r/o circuit
-: thick handle wafer (separated by the BOX) as detector
-: can use full CMOS in top layer
-: processing and handling of the back side still somewhat delicate for standard CMOS lines

→ in R&D phase, first results expected soon…

It is definitely not the "best of both worlds"! → try the modular approach…..

Flip Chip Bump Bonding → Hybrid Pixel Sensor

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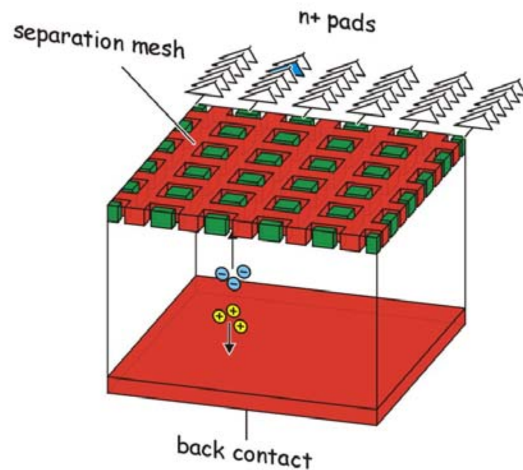
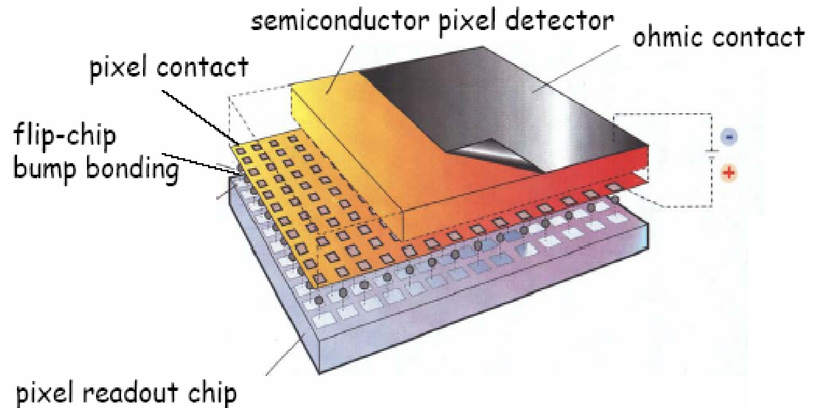
→ each pixel has its own amp, signal processor etc..





→ ATLAS and CMS Pixel Detectors (LHC)
→ PILATUS Detector (PSI) for Xray imaging

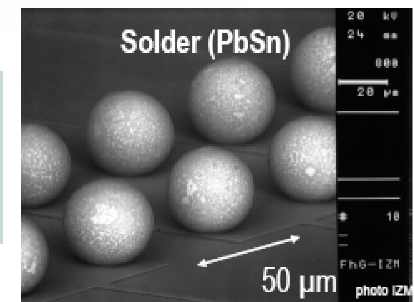
Works nice in the mean time → 99.9% yield (ATLAS)

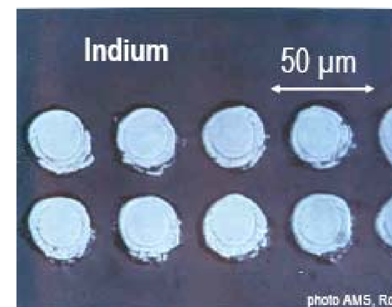
but……

-: minimal pitch is limited by technology
10 µm bump, 20 µm pitch is seen as ultimate limit
-: chip area per pixel is small, too small for
high rate/fine pitch applications like XFEL
-: amount of material (Si, high Z metals…) is too big
for applications in high precision vertex detectors (ILC)

for more details, ask Dr. Fipchip:
http://www.drflipchip.com/

-: electrodepostion of Cu, PbSn, Ni..
-: reflow..
-: flip chip…

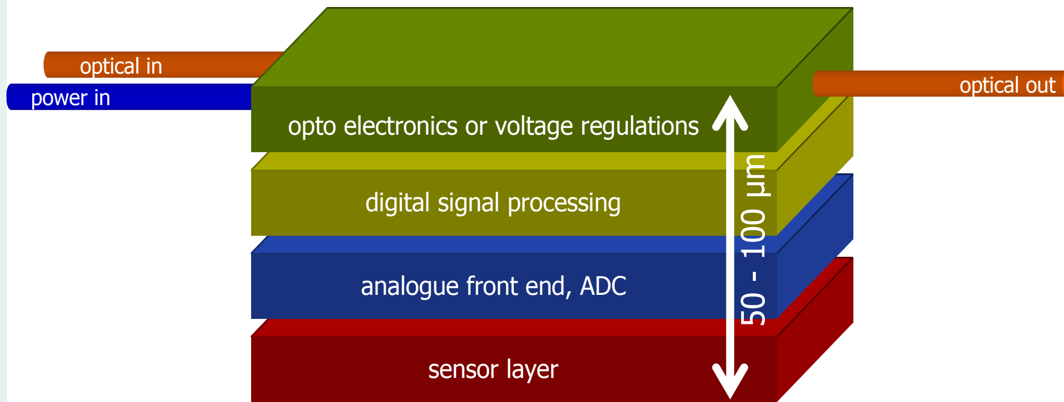


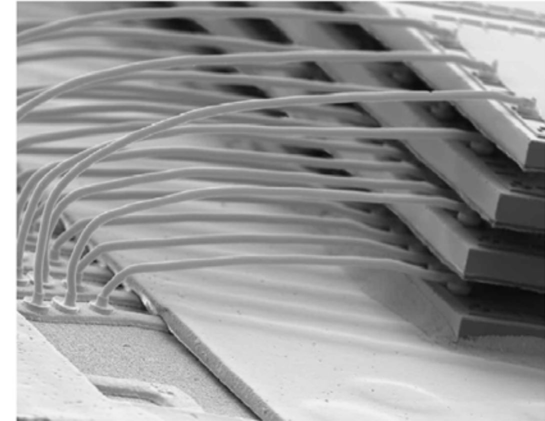


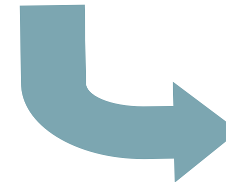
-: through mask evaporation of Indium
-: Wet lift off process
-: flip chip…

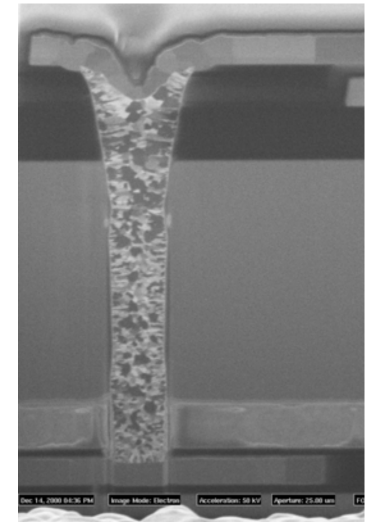
Vertical System Integration ("3D") - the Vision

the (HEP) detector physicist's dream
(for long and lonely nights or boring presentations ...)









In this way one could really combine the best of both (all!) worlds!

-: interconnection on a very fine pitch has to be done after processing of the individual layers

-: independent control of the process for all the substrates

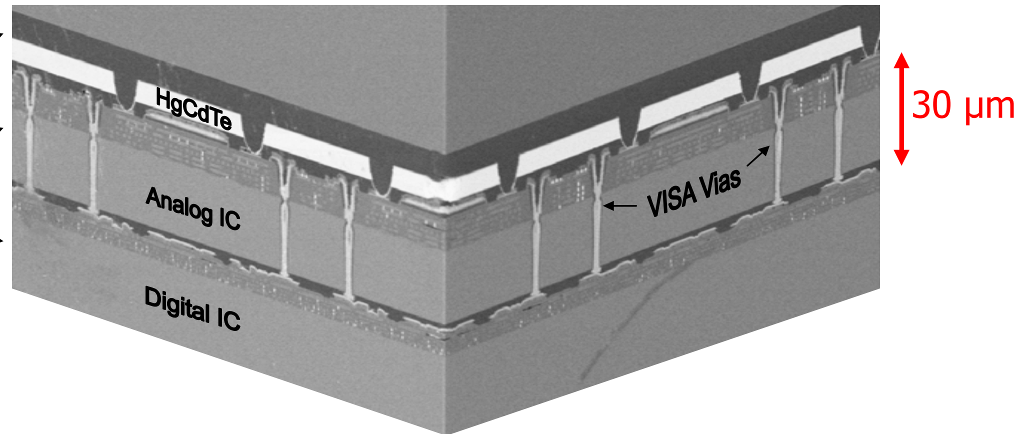
-: the sensor layer can be adapted to the specific application (DEPFETs, simple pad detectors, Avalanche Diodes..)

An example: IR Imager with three layers (RTI)

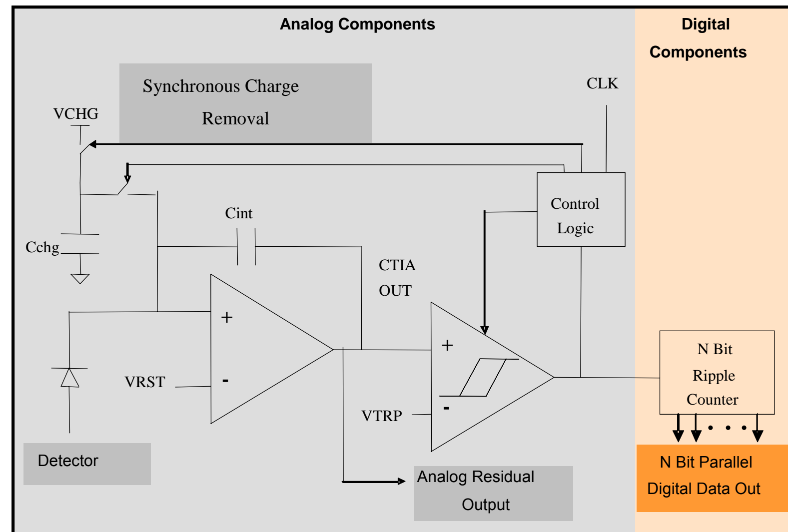
-: 30 μm pixels - 256 x 256

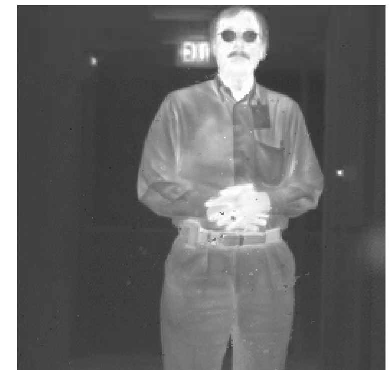
-: 3 layers
  HgCdTe (sensor)
  0.25 μm CMOS (analog)
  0.18 μm CMOS (digital)

-: Die to wafer stacking
-: Polymer adhesive bonding
-: 4 μm vias with insulated side walls
-: 99.98% good pixels



pixel schematics in three layers





IR Image

What is Industry doing??

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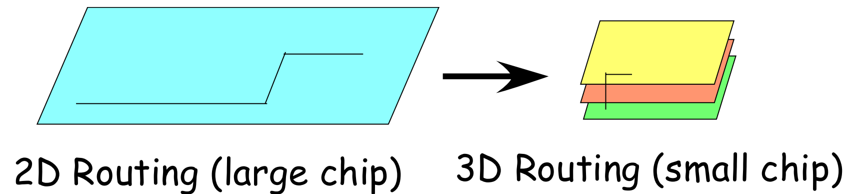
The advantages of vertical integration:

- -: faster: R, L, C are reduced
- -: number of chip I/O pads reduced
- -: due to smaller R: interconnect power reduced
- -: much higher functionality with the same foot print

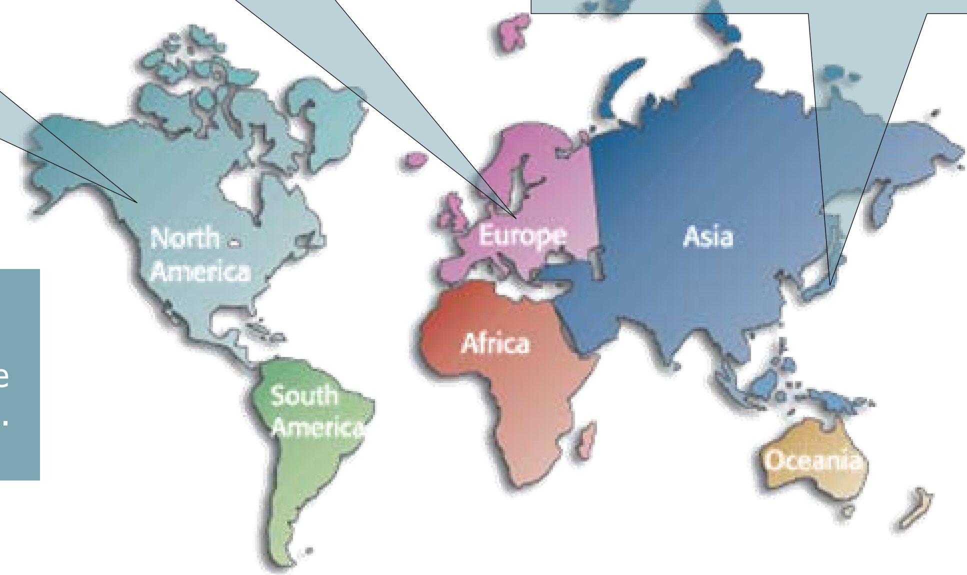
If real estate gets expensive, you start to build skyscrapers.



Irvine Sensors, DEPAC, IBM
Intel, Micron Technology
TI , Grumman Aerospace
Vertical Circuits, Raytheon E-systems
AT&T, Hughes, Lockheed, CTS,
Tessera Inc., Tru-Si Technologies
Rensselaer Institute

Thales, Alcatel Espace, NMRC
LETI, IMEC, EPFL, TU Berlin
Fraunhofer IZM, Infineon

ASET, NEC, Tohoku University
CREST, Fujitsu, Sanyo, Sony
Toshiba, Denso, Mitsubishi, Sharp
Hitachi, Matsushita, Samsung



IBM Press Release, April 2007:

IBM 3D technology with through silicon vias available for customers in 2nd half of 2007, in production 2008.
1st applications: wireless LAN and Cellular phones….

The Strategy

There are a lot of different 3D technologies on the market. And we cannot compete with the engineering power of the research departments of big companies like IBM, Intel etc.!

An advantageous strategy could be to develop (adopt) with partners (from industry) a technology, which allows the interconnection of diced 3D chips made in industry or conventional 2D ASICs in a sensor compatible way and to take advantage of the through silicon vias.

This technology should keep the way open to stack two or three conventional ASICs on a Sensor wafer without degrading its performance.

Technology: Chip-to-Wafer, ICV/SLID (Inter Chip Via/ Solid-Liquid InterDiffusion), developed by Fraunhofer IZM, Munich and Infineon

Partner: Fraunhofer IZM, Munich

"Chip to Wafer"

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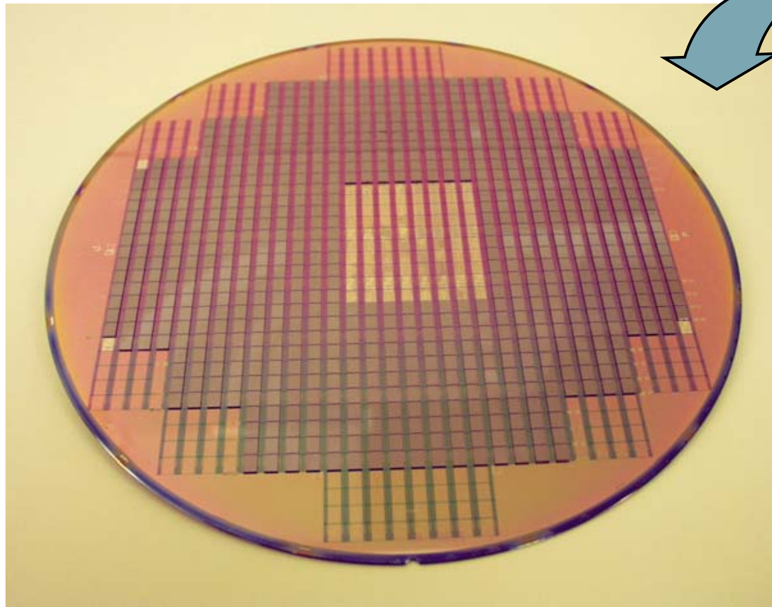
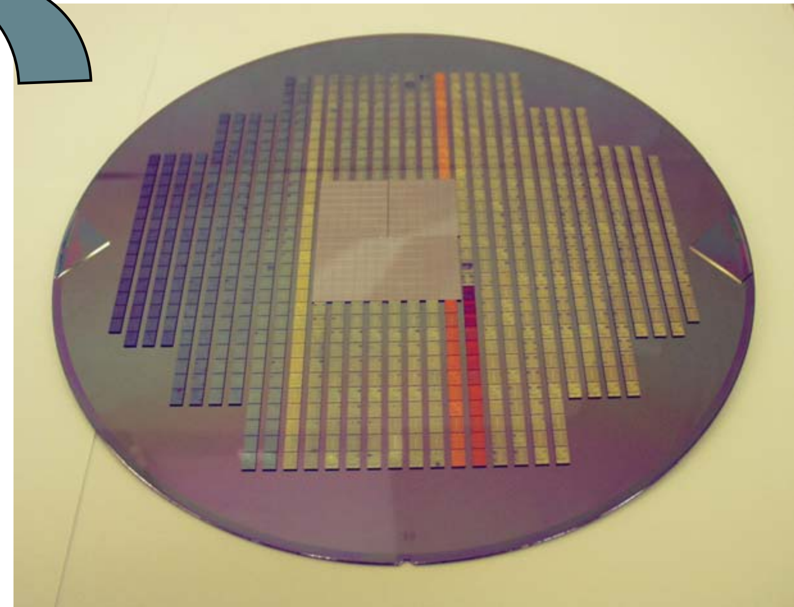
target wafer with placed chips
after removal of the handling substrate



chips on handling substrate

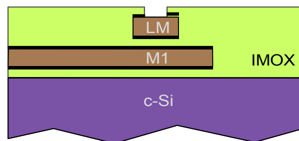


1. tested and diced chips are placed on a handling substrate with alignment marks
2. Handling substrate flipped and aligned to target wafer
3. SLID (temperature and pressure)
4. removal of handling substrate

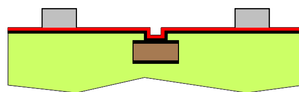
Eutectic Bonding

-: Developed at IZM Munich together with Infineon
-: vertical integration is an "add-on process"!! should be compatible with the major technologies

Wafer processes

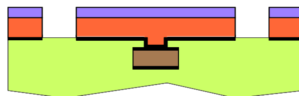


Initial state
Opened passivation
Vias Ø 2 µm, Al or Cu

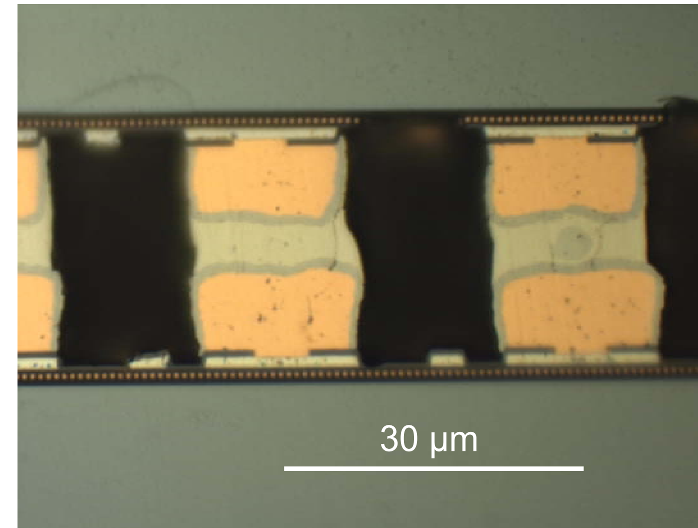


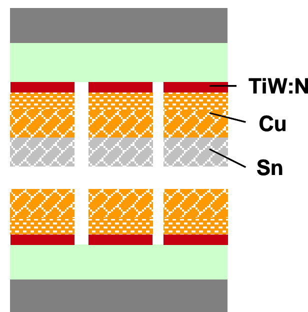
Sputtering
TiW barrier 50nm
Cu seedlayer 100nm

Litho
Insulation trenches

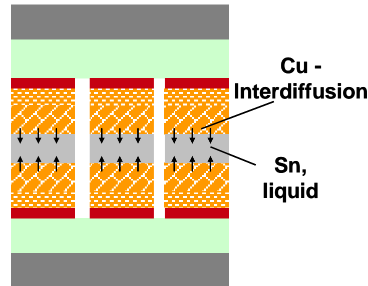


Plating module
Cu 5µm
Top wafer only: Sn 3µm
Resist strip
Wet etch seedlayer & barrier

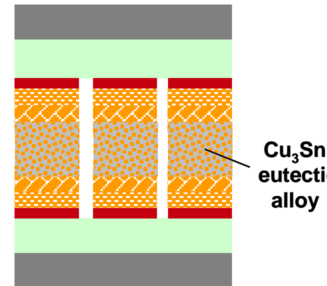




Through Mask Electroplating



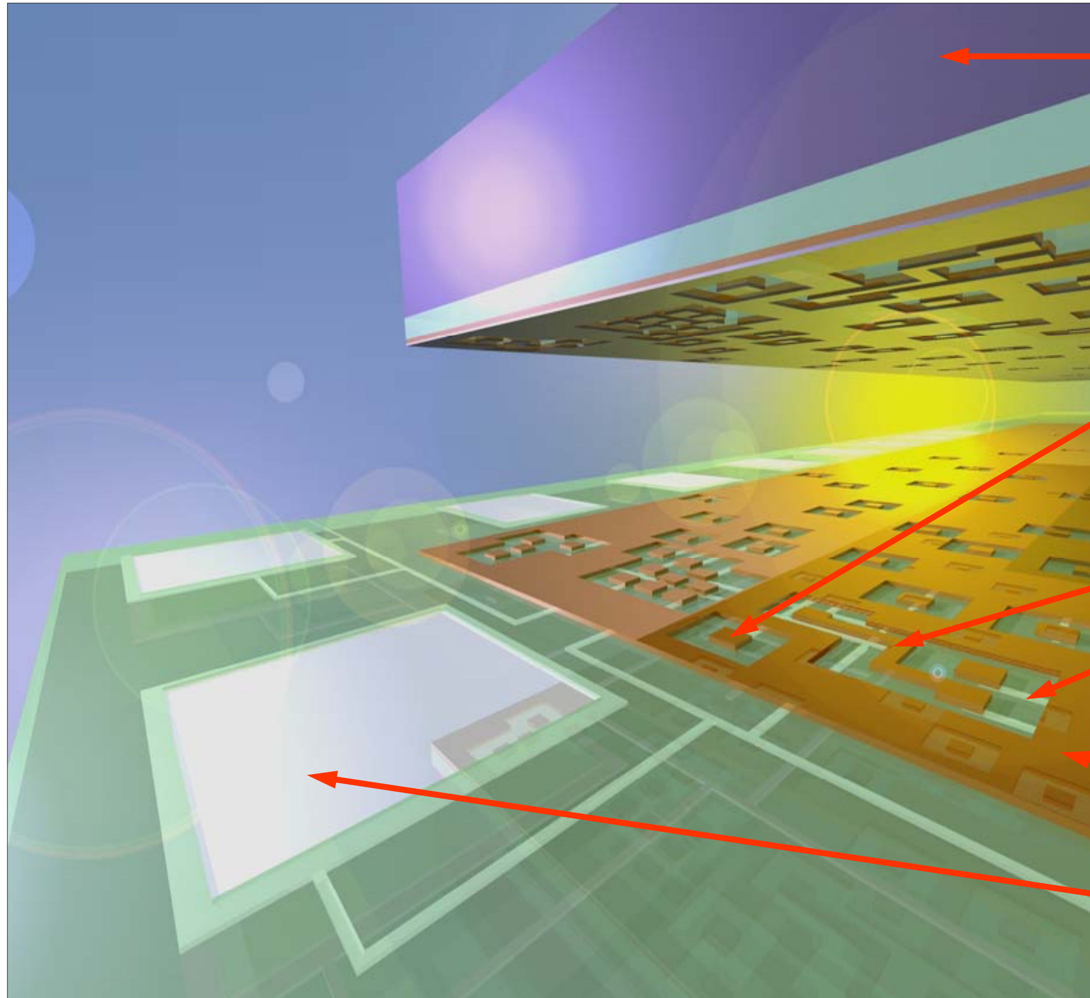
Contact under Pressure and Heat
~ 5 bar, 260 – 300 °C (Sn-melt)



Formation of Eutectic Alloy; T_{melt} > 600 °C

both, electrical and mechanical joint between chip and target wafer

Face-to-Face SOLID Process (IFX)



Top chip
Cu and Sn coating

Bottom chip
Cu coating, bond pads

No underfill

Inter chip vias
15 x 15 µm²
5 µm vias to LM

Redistribution

Insulation trenches
15 µm

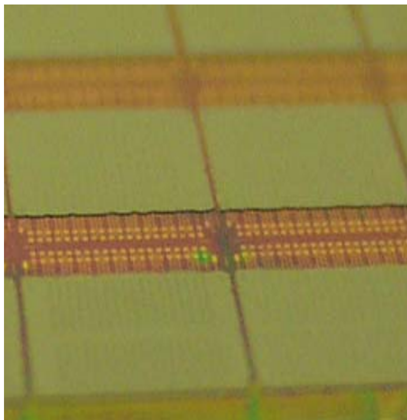
Passive area
heat spreader

External IOs
standard wire bonds

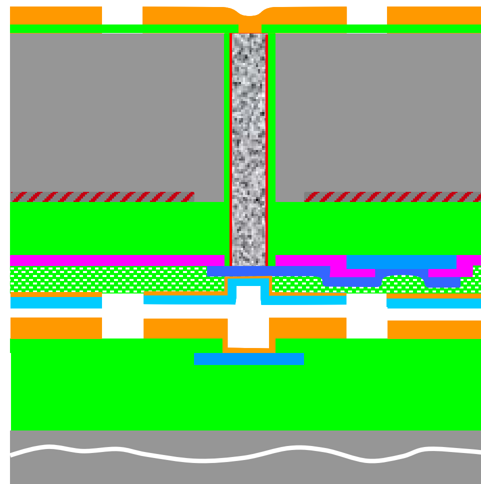
The 3rd Layer - InterChip Vias (ICV) → IZM, Munich

1. thin the attached chip and make a contact to the buried metal layer

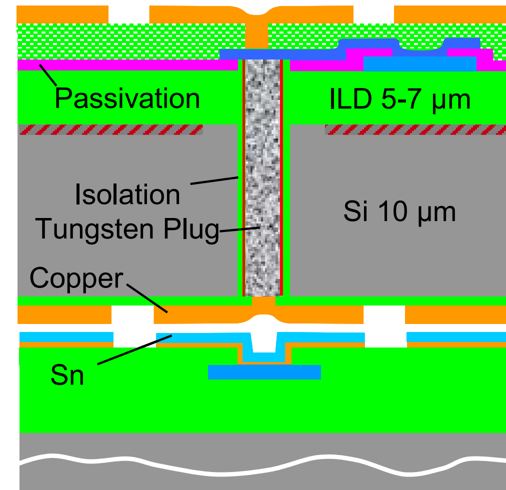
2. or….face up attachment of a thin chip to the target wafer →



After Thinning on Target Substrate
Chip Thickness 10 µm

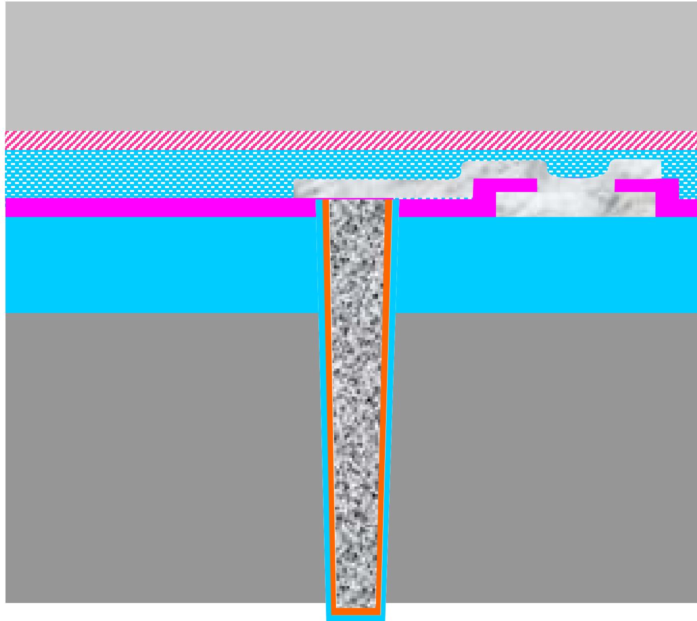


W-Plug / Cu / Sn

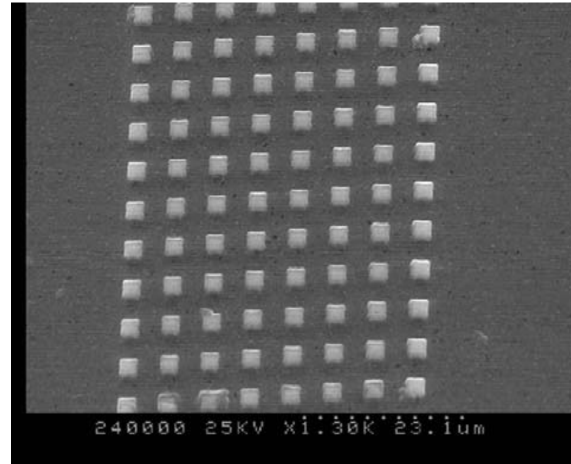


W-Plug / Cu / Sn

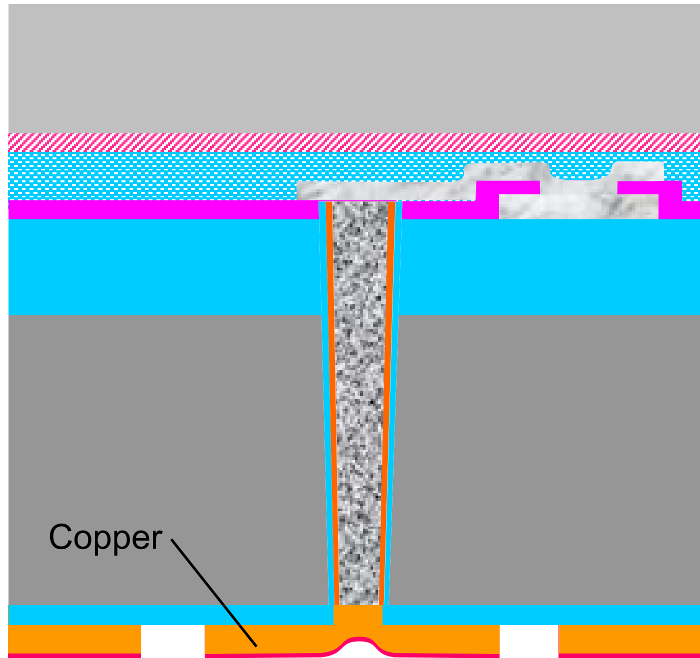
The 3rd Layer - InterChip Vias (ICV) → IZM, Munich

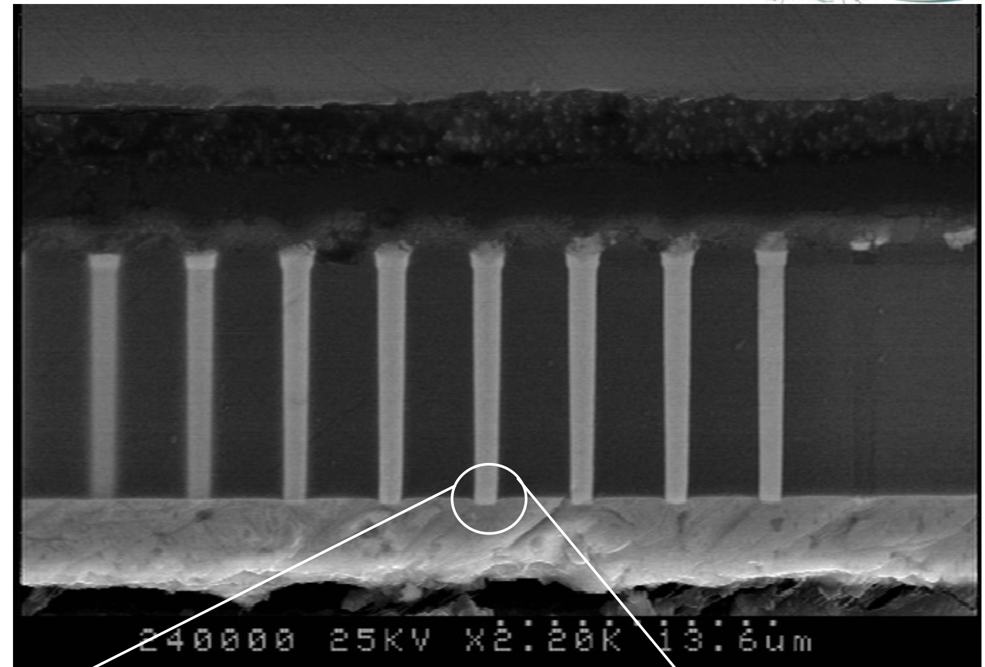


- Fabrication of Tungsten-filled InterChip Vias on Top Substrate
- Via Opening and Metallization
- Bonding to Handling Substrate
- Thinning

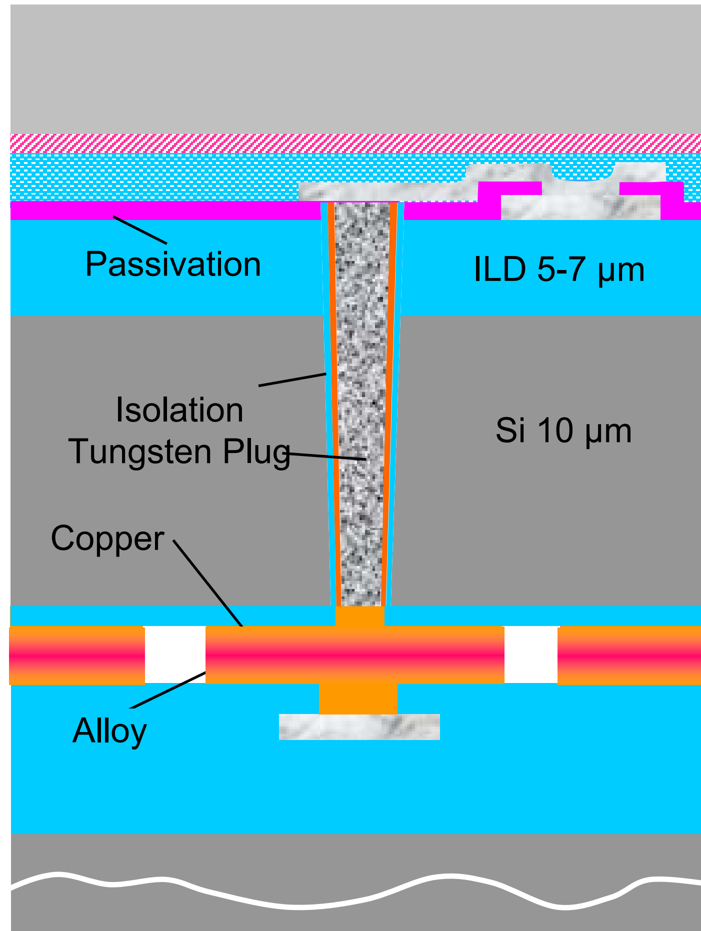


The 3rd Layer - InterChip Vias (ICV) → IZM, Munich



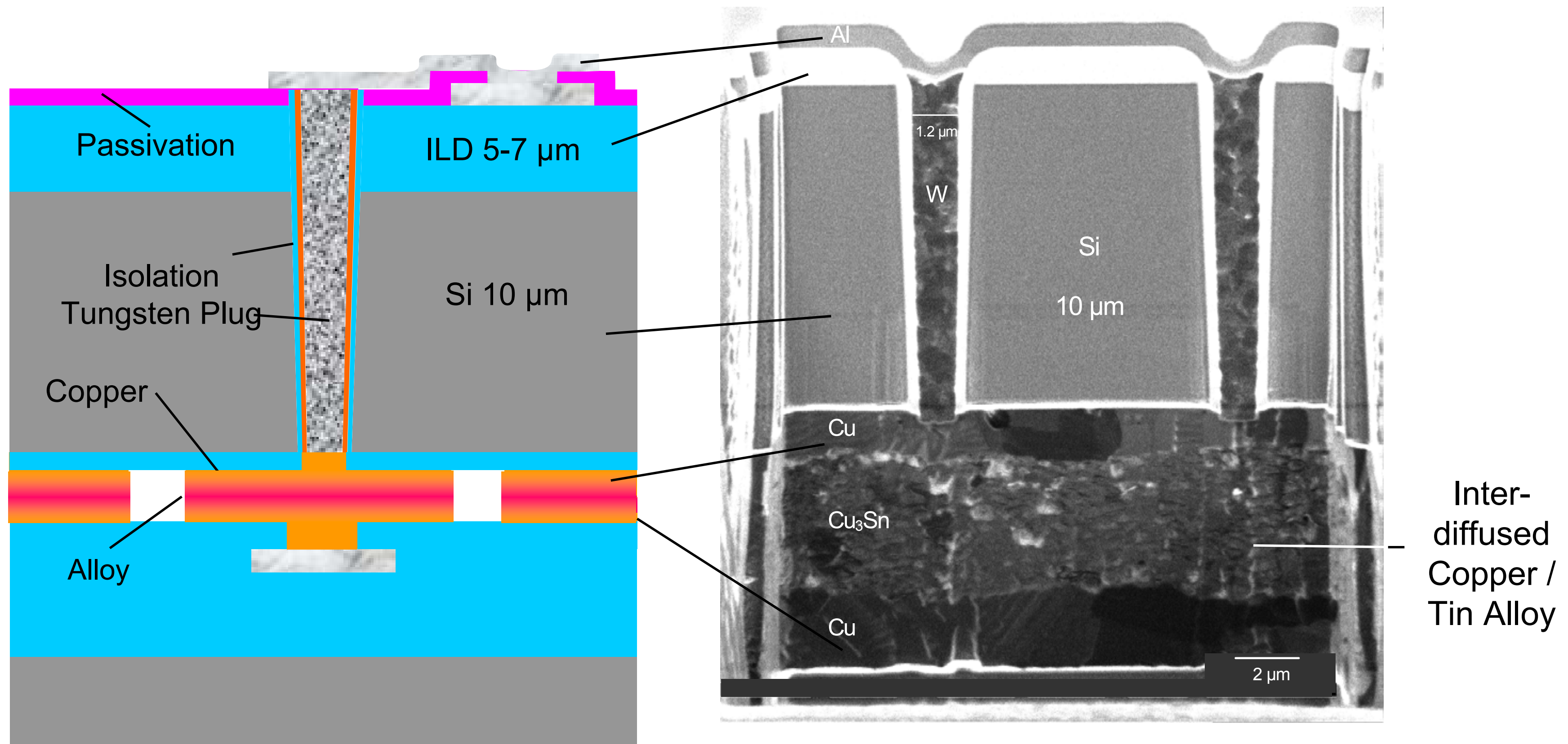


The 3rd Layer - InterChip Vias (ICV) → IZM, Munich



- Fabrication of Tungsten-filled InterChip Vias on Top Substrate
- Via Opening and Metallization
- Thinning
- Opening of Plugs
- Through Mask Electroplating
- Alignment and Soldering

The 3rd Layer - InterChip Vias (ICV) → IZM, Munich



So far so good…

Using this technology we could:

1. build two-layer systems (sensor and r/o chip), interconnected in very fine pitch. Due to the inter-chip vias, the (thin!) stack of sensor and electronics would be 4-side buttable.

2. and we would have a tool in our hands to go to "real" 3D integrated systems, if needed for certain applications.

For the time being, the driving projects are **sLHC** and to some extent **ILC** (because of the possibility to connect very thin ASICs to the sensor).

What do we have to do?

-: We certainly don't need to drill vias into the sensor wafer!

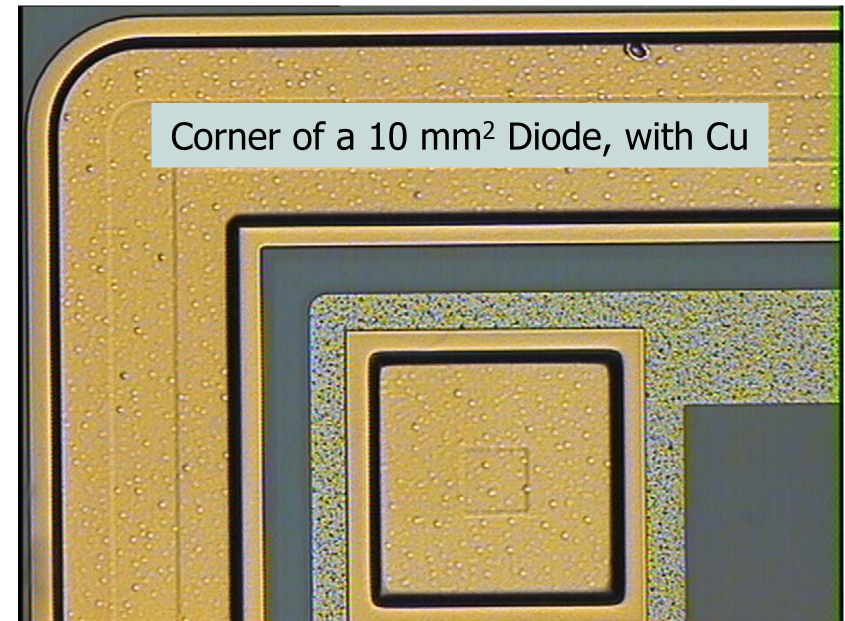
-: But we do have to make sure, that the preparation of the sensor wafers for SLID does not degrade the sensor. (TiW barrier layer, Cu and Sn elektroplating)

-: Check how the process (pressure and heat) of the "soldering" to a r/o chip affects the sensor.

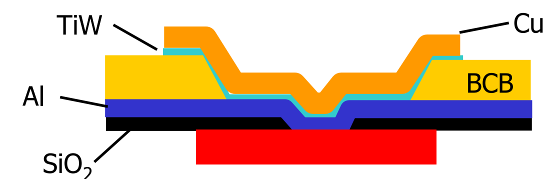
-: And, at the end of the day, build the first(!) detector system using SLID/ICV to show the feasibility of this approach!

First tests with IZM

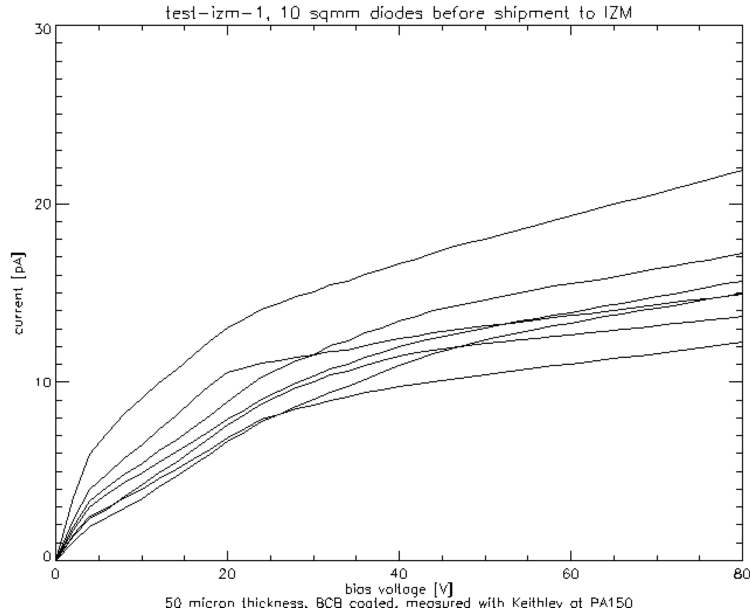
Diodes (our standard test vehicles) have been produced on SOI Wafers:
top layer: 50 µm thick, 150 Ω.cm

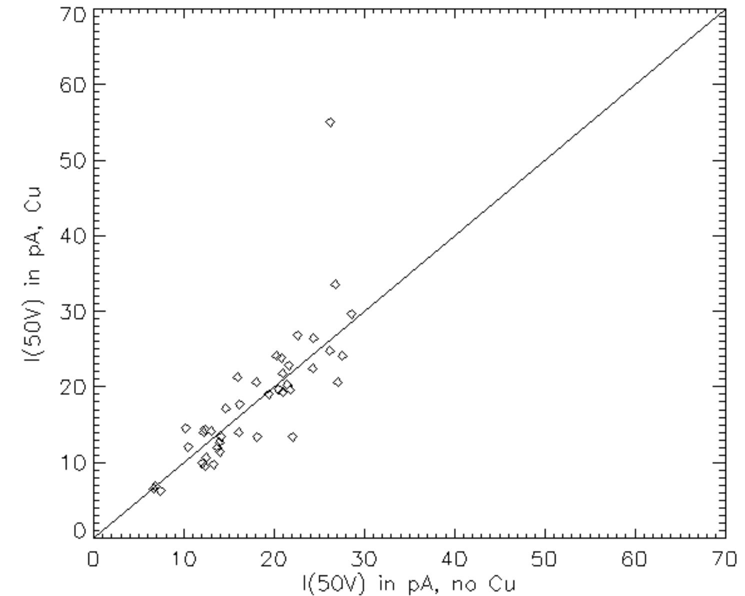


- -: contact mask modified → Oxide openings (blank silicon) minimized
- -: BCB layer with openings to define TiW/Cu/Sn System
- -: Handle wafer acts as back side protection layer during the IZM processing
- -: Metal system done at IZM:
  - 100 nm TiW, sputtered
  - 200 nm Cu, sputtered
  - 1 µm Cu, through mask electroplated



Characteristics





-: IV Curves before Cu metallization
-: measured at HLL, right before shipment to IZM
-: from CV curves → full depletion at 50 V

-: Correlation of the reverse current at full depletion (50 V) before and after Cu metallization.

-: max. Temp. so far 160 degC during sputtering

→ No significant effect of Cu metallization noticeable!

Wafers now with IZM for the simulation of the soldering process (few min, 270 degC)….let's see…

In Summary

Microelectronics Industry is moving into the 3rd dimension - vertical integration is becoming one of the major topics of semiconductor technology conferences and it is on the door step to be transferred to the production lines.

We have to keep up to date with our interconnection technology to be in the position to take advantage of this development.

The ICV/SLID technique offers the opportunity to connect highly granular pixel detectors with pre-tested and ultra-thin r/o chips and allows the construction of multi-layer detector stacks, if needed.

Even in the case of a "simple" two-layer stack of sensor and r/o, the use of inter-chip vias allows the construction of four-side buttable devices, reducing the dead region for large area pixel detectors.

Very first tests of the post-processing needed for SLID are promising but a much larger study has to follow in order to come to a conclusion on the feasibility of this approach.