

Radiation Damage on MOS-Structure

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Outline



- ◆ Motivation
- ◆ Radiation damage & effects on MOS-structure
- ◆ Experimental Conditions and Results
- ◆ Conclusion

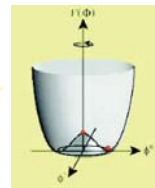
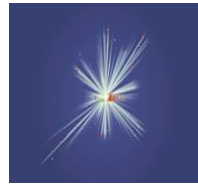
Motivation



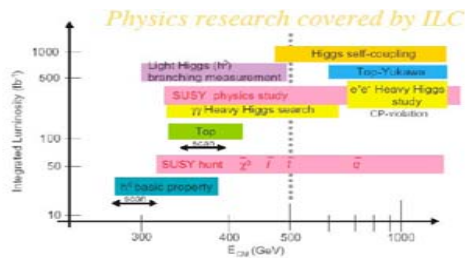
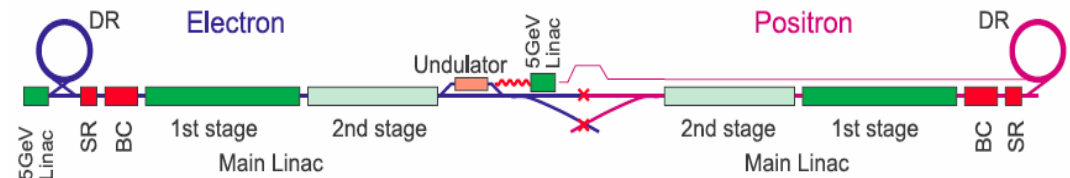
Physics topics

- Unexpected phenomena
- Mechanism of electroweak symmetry breaking
- New physics: SUSY; extra dimension; link to cosmology

Single production Higgs Extra-Dimension		ILC ~a few TeV $d\sigma/d\Omega > 10\%$	ILC ~1 TeV $\delta\sigma/\sigma \sim 1\%$ ($\delta\text{charm}(H) \sim 1\%$)
Pair production SUSY Heavy Higgs		~3 TeV (colored)	~0.5 TeV (any type) $\delta\sigma/\sigma \sim 1\%$ Energy scan, Beam pol
Intermediate state Extra-Dimension Strong EWSB Z', contact int.		~several TeV resonance	>10 TeV $\delta\sigma/\sigma \sim 1\%$ Energy scan, Beam pol Coupling, spin
Loop effect		ΔX	A few % level effect



International Linear Collider



precise vertex detector (DEPFET)

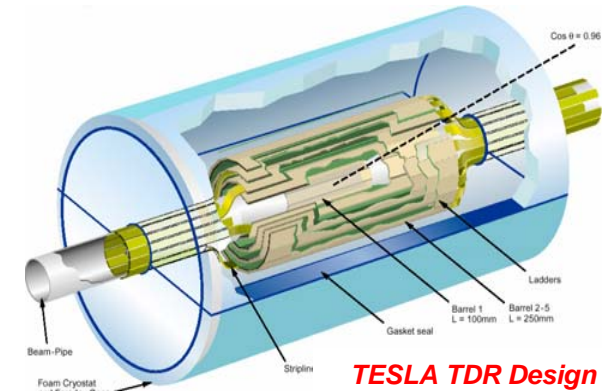
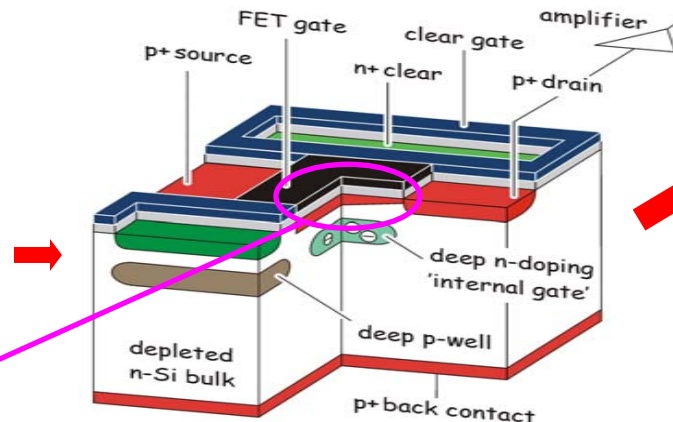
To do

Radiation on MOS-structure
(MOS-Capacitance & -DEPFET)

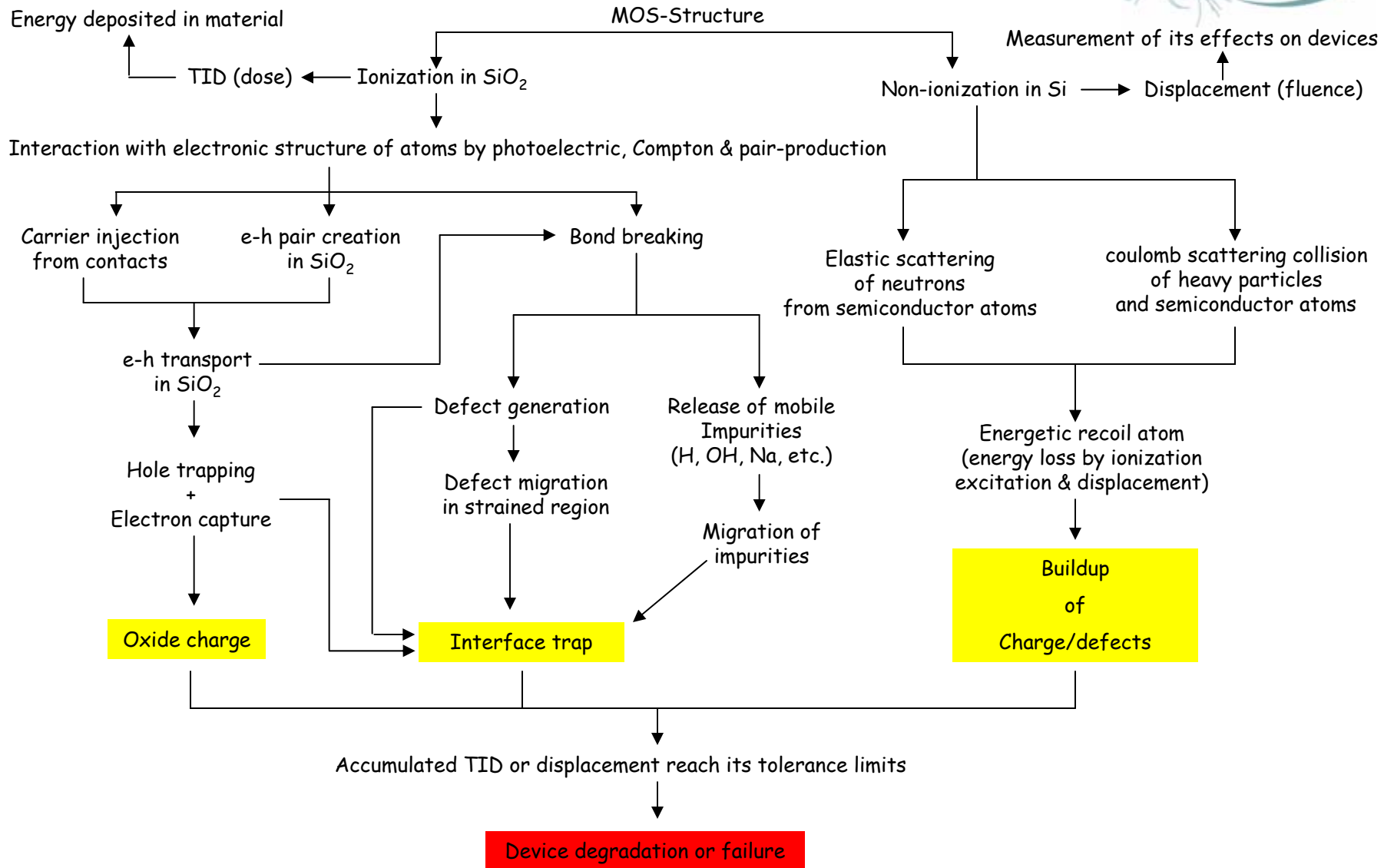
Research of radiation effect
(damage mechanism & model)

Radiation hardness structure

Depleted P-channel FET



Radiation Damage I



Radiation Damage II



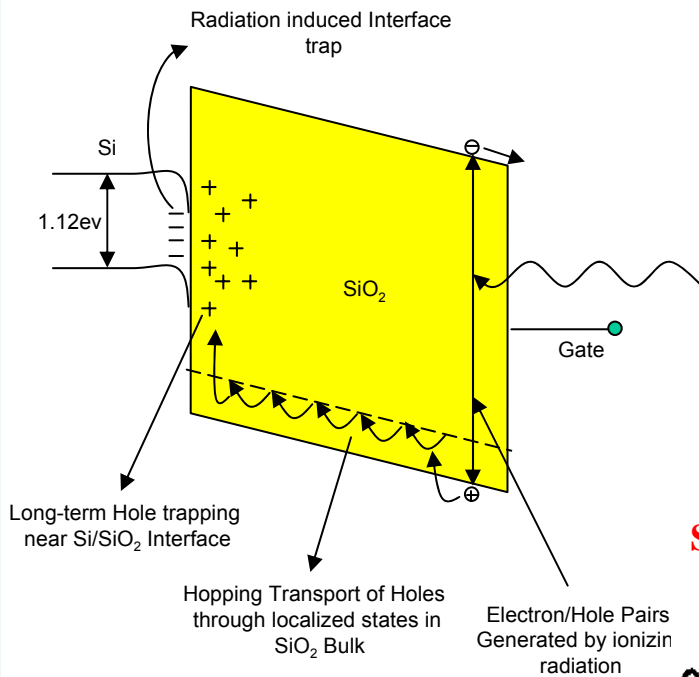
- ◆ Radiation damage in MOS-Structure:
 - ✦ Surface damage due to Ionizing Energy Loss (IEL)
 - ✦ accumulation of charge in the oxide (SiO_2) and Si/ SiO_2 interface
 - ✦ Oxide charge → shifts of flat band voltage, (depleted → enhancement)
 - annealing at RT
 - ✦ Interface traps → leakage current, degradation of transconduction,...
 - no annealing below 400 °C

- ◆ S/N Ratio deteriorated!

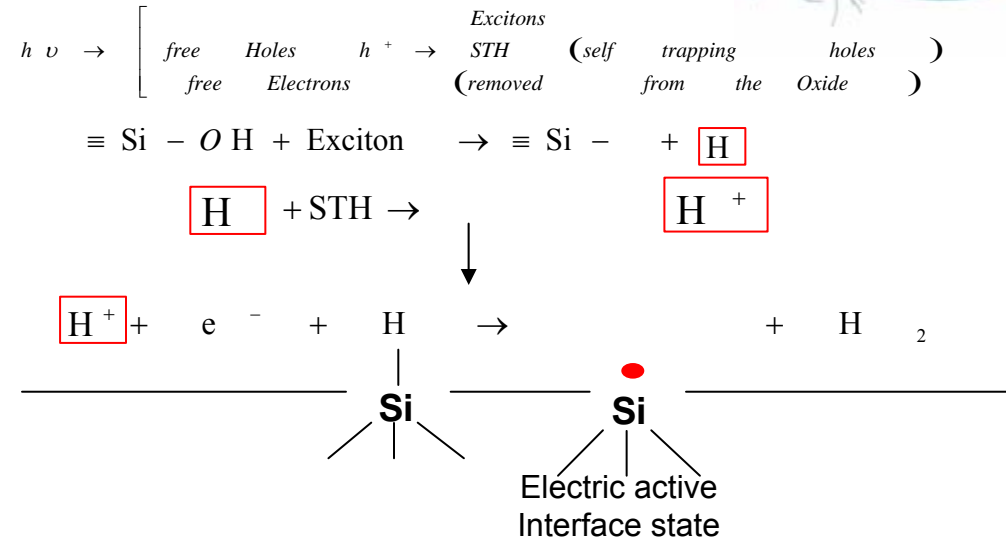
Damage mechanism (MOS)



Ionizing radiation:



Damage mechanisms:

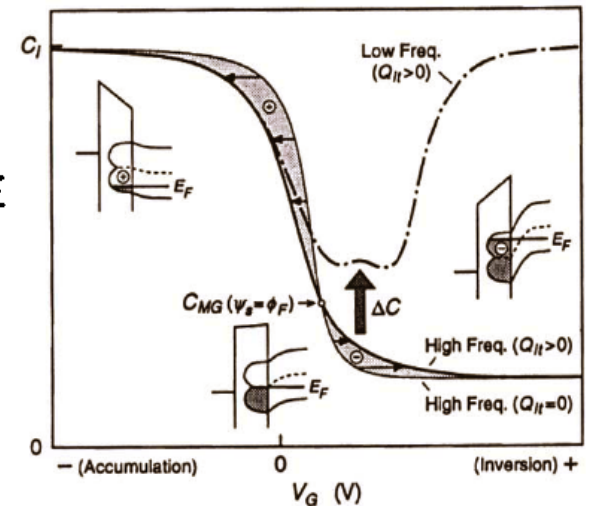
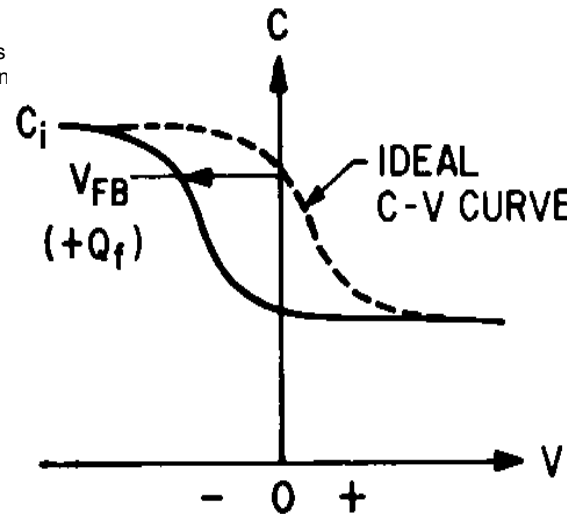


N_{ox} : positive oxide charge and positively charged oxide traps have to be compensated by a more negative gate voltage \rightarrow negative shift of the threshold voltage ($\sim t_{ox}^2$)

N_{it} : increased density of interface traps \rightarrow higher $1/f$ noise and reduced mobility (g_m)

Shifts of flat band voltage: $\sim N_{ox}$

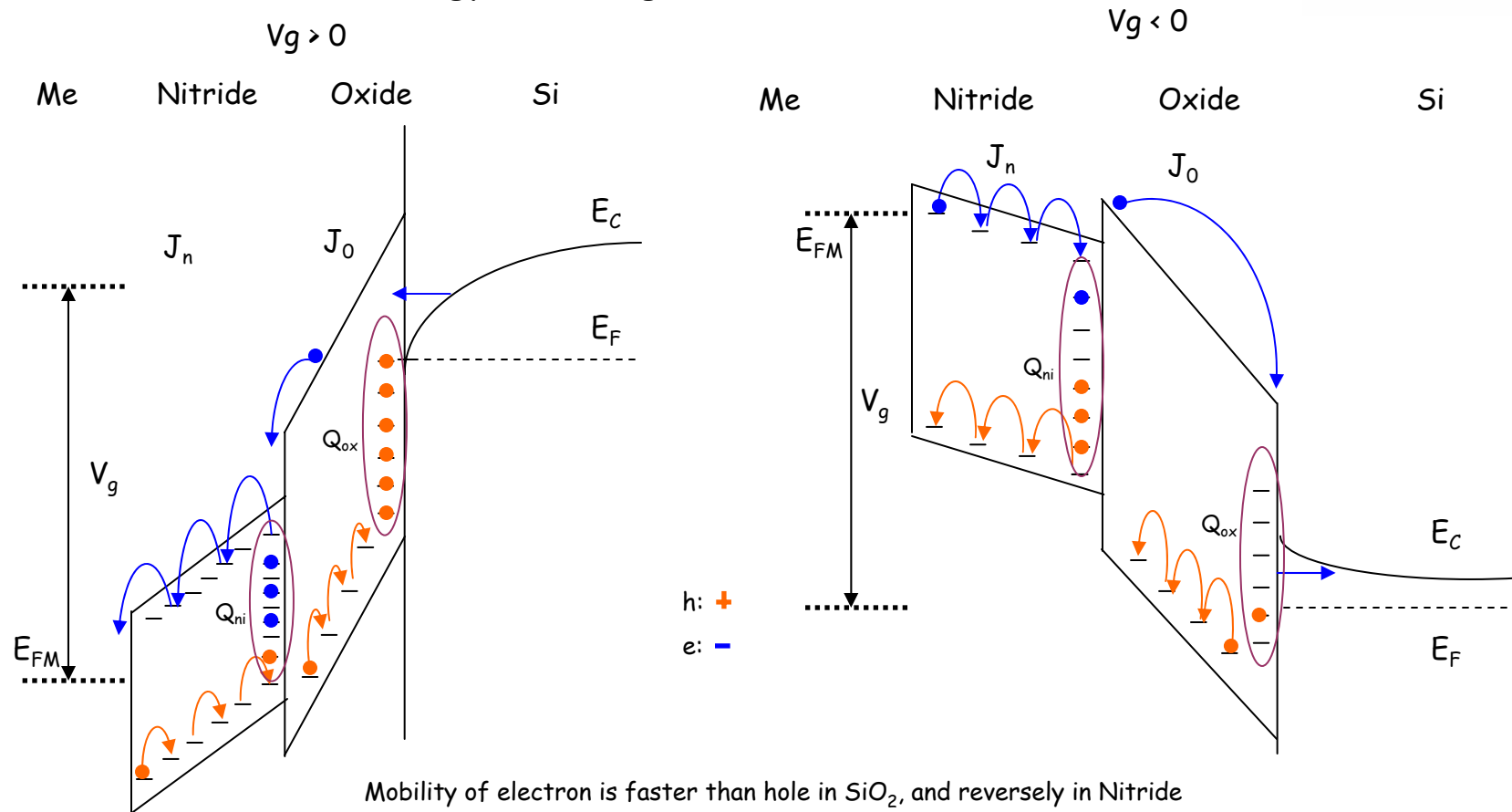
Stretch-out of CV curve: $\sim N_{it}$



Damage mechanism (MNOS) I

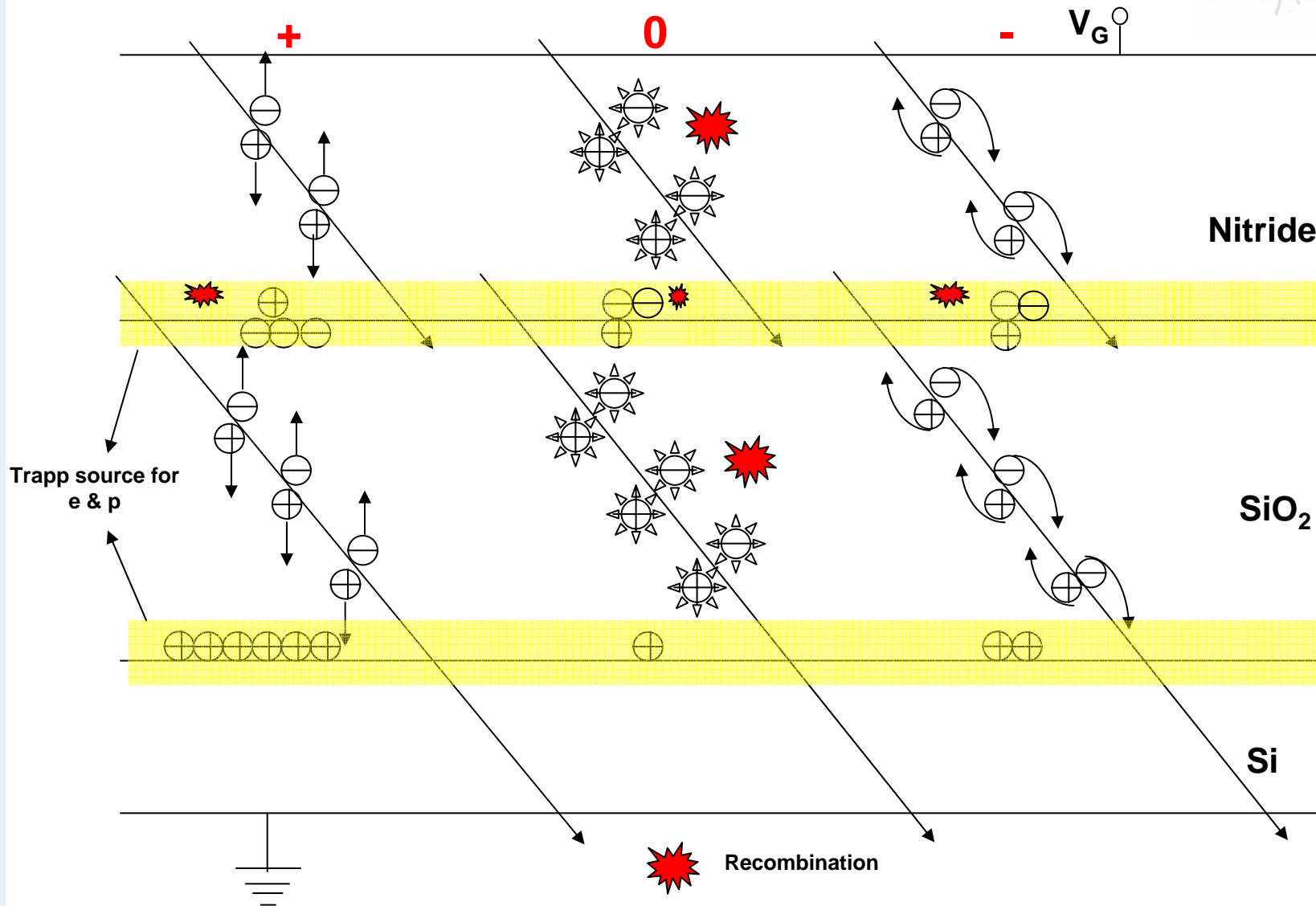


Energy band diagram of MNOS structure



Discontinuity of current density $J_n - J_0$ in short time lead to charge carriers accumulation & trapping in N/O strained interface
 field dependence of current density & thickness of the dielectrics plays an important role!
 charge in Si/SiO interface donot affect the field distribution in dielectrics!

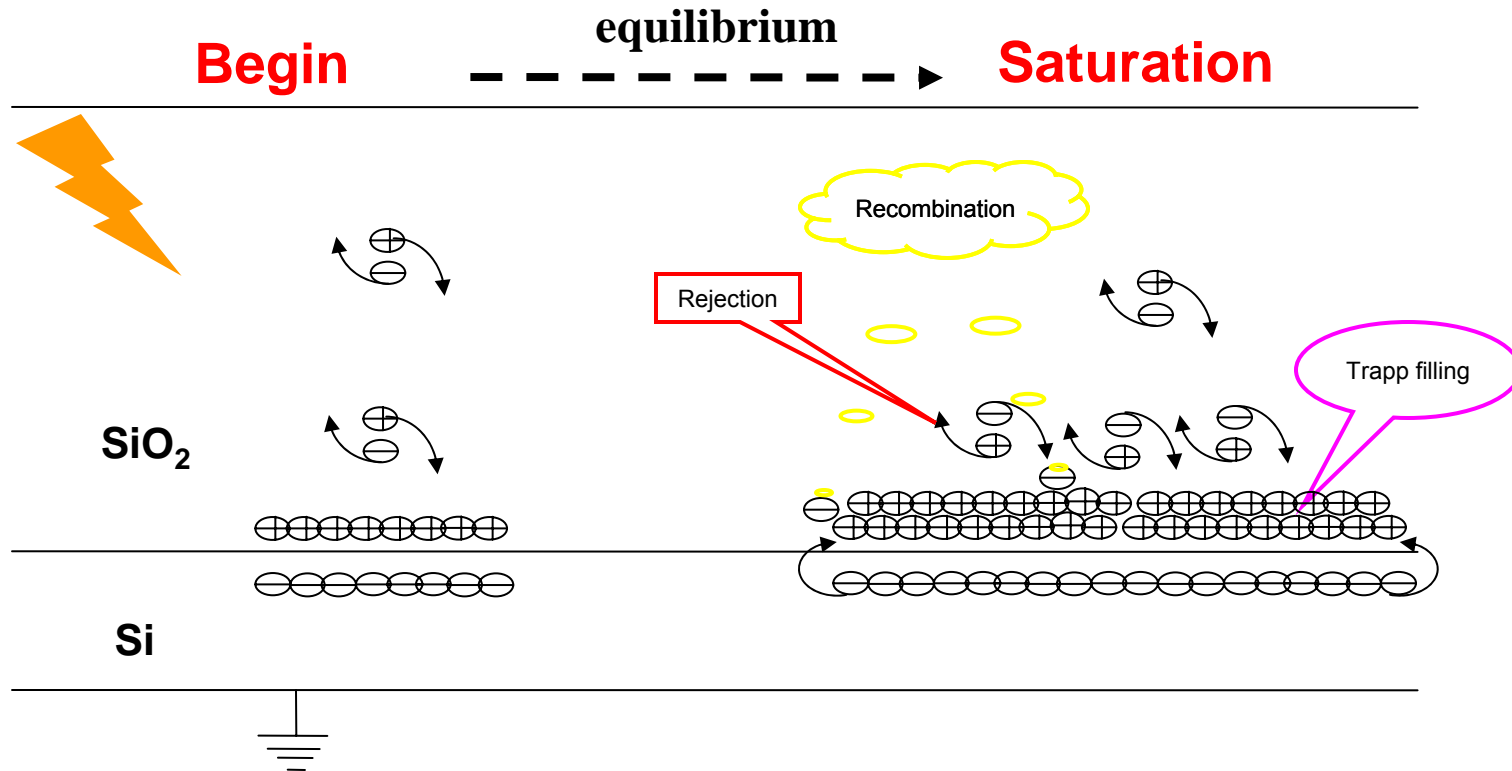
Damage mechanism II



Damage mechanism III



Saturation mechanism



- **Reservoir:** hole traps are not exhausted, unless a larger bias voltage is applied on the gate!
- **Saturation:** equilibrium between trapped filling and recombination
 - Generated holes are pushed away!
 - Recombination of trapped holes with electrons
 - Recombination of tunneled electrons from silicon into interface with trapped holes!

Experiment Conditions and Methods



• **Irradiation (X-Ray):**

- Co⁶⁰ (1.17 MeV and 1.33 MeV)
 - GSF – National Research Center for Environment and Health, Munich
- CaliFa (17.44 KeV)
 - Max-Planck-Institute Semiconductor Labor, Munich
- Roentgen facility (20 KeV)
 - Research center, Karlsruhe

• **Dose:** irradiation up to 1 Mrad with different dose rate (1rad=0.01J/kg)

• **Process:** No annealing during irradiation ~ irradiation duration from 1 day to 1 week

• **Radiation levels at the ILC VTX:** $D_{\text{ionization}} \approx 100 \dots 200 \text{ Krad}$
 $\Phi \approx 10^{10} \dots 10^{11} \text{ neq(1MeV) / cm}^2$

• **Comparison of different semiconductor devices**

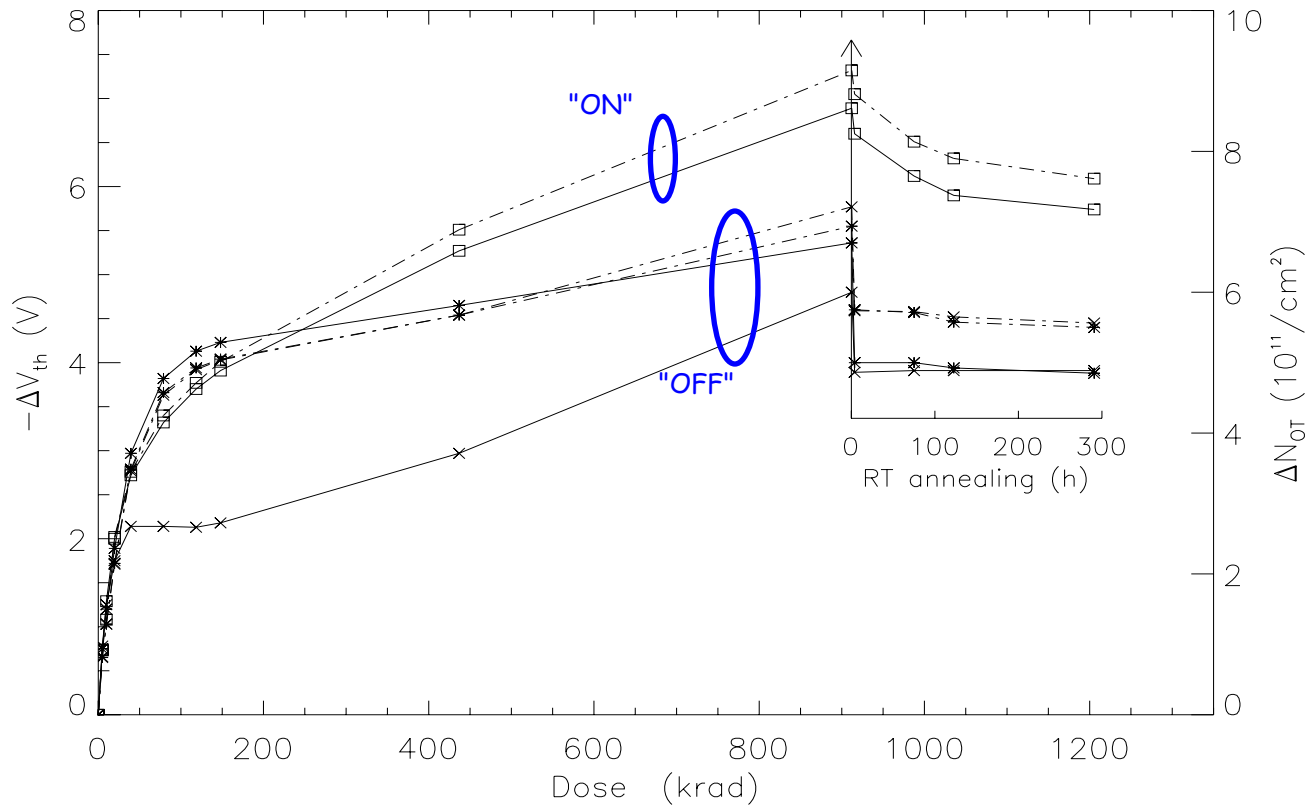
	DEPFET	MOS-C	Gated diode
N_{ox} (method)	ΔV_{t} (IV-Measurement)	ΔV_{FB} (CV-Measurement)	ΔV_{FB} & ΔV_{g} (CV-Measurement & gated diode technique)
N_{it} (method)	Subthreshold slope (Subthreshold technique)	Stretch-out (High-low frequency based on the CV)	Full width at 2/3 maximal of current (gated diode technique)
Other parameters	g_{m} (IV-Measurement)		S_0, τ (gated diode technique)

Results for MOSDEPFET

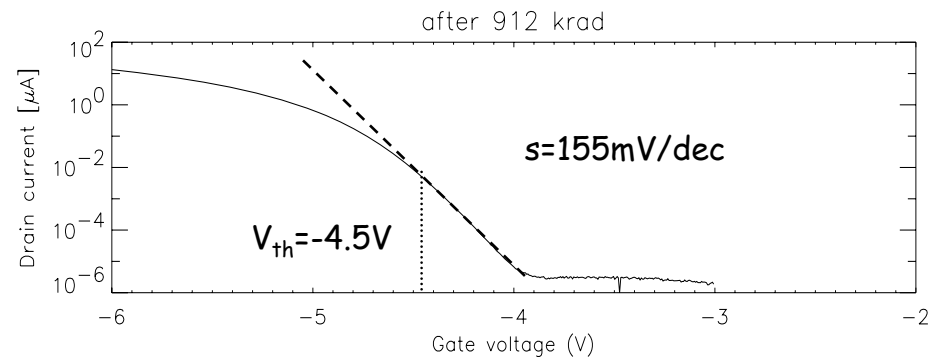
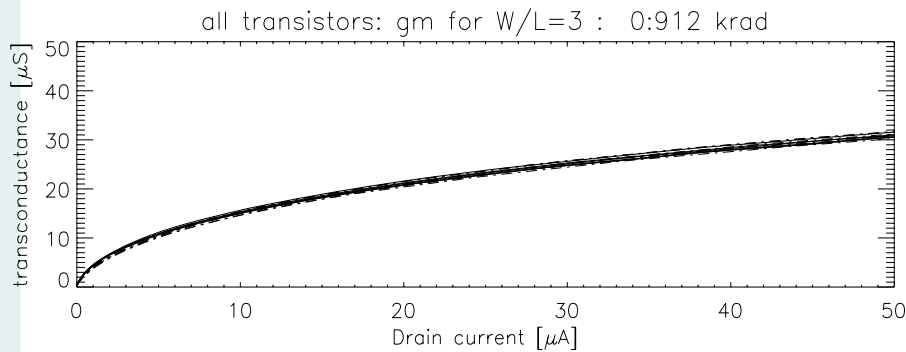
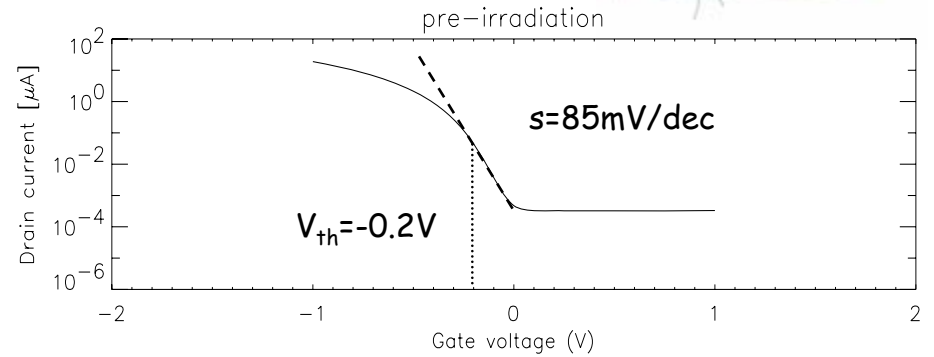
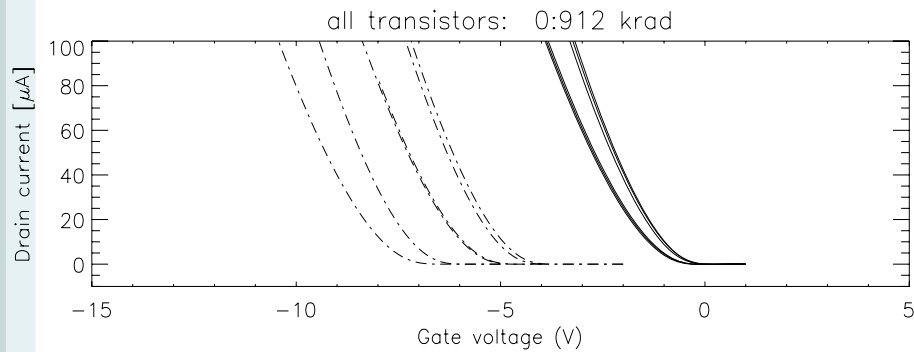


Bias during irradiation:

- 1: empty int. gate, in „off“ state, $V_{GS} = 5V, V_{Drain} = -5V \rightarrow E_{ox} \approx 0$
- 2: empty int. gate, in „on“ state, $V_{GS} = -5V, V_{Drain} = -5V \rightarrow E_{ox} \approx -250kV/cm$



Transconductance and Subthreshold slope



↓

No change in the transconductance g_m

$$N_{it} = \left[\frac{C_{ox}}{kT} \ln(10) \right] (S_{D2} - S_{D1})$$

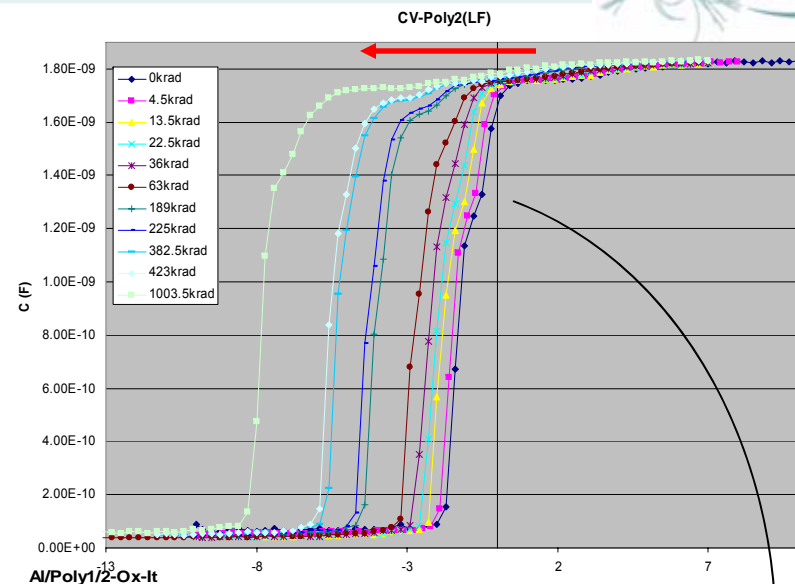
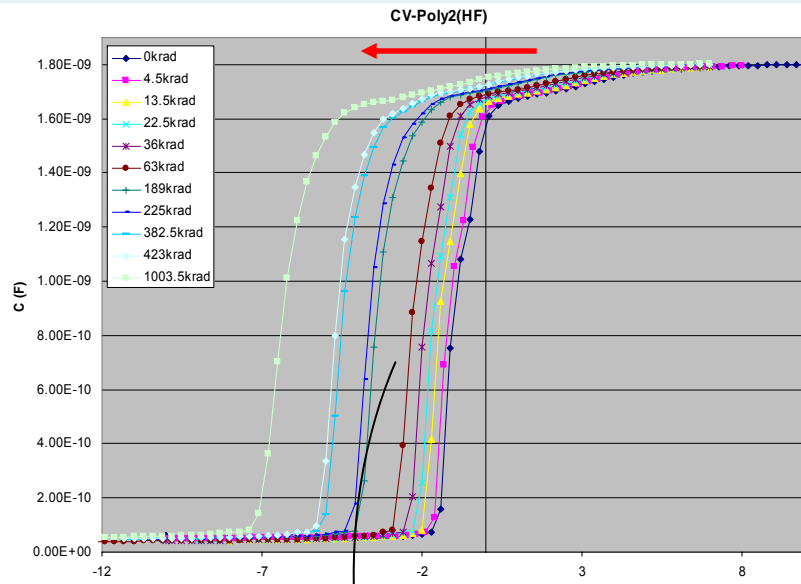
300 krad $\rightarrow N_{it} \approx 2 \cdot 10^{11} \text{ cm}^{-2}$

912 krad $\rightarrow N_{it} \approx 7 \cdot 10^{11} \text{ cm}^{-2}$

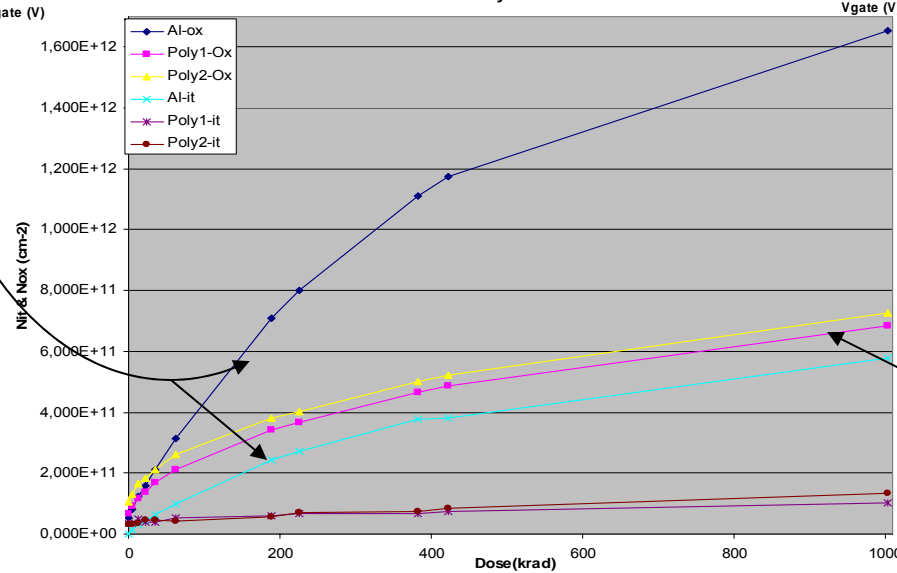
Literature:
After 1Mrad 200 nm (SiO_2):
 $N_{it} \approx 10^{13} \text{ cm}^{-2}$

Gate Bias conditions: 0V

Results for MOS-C



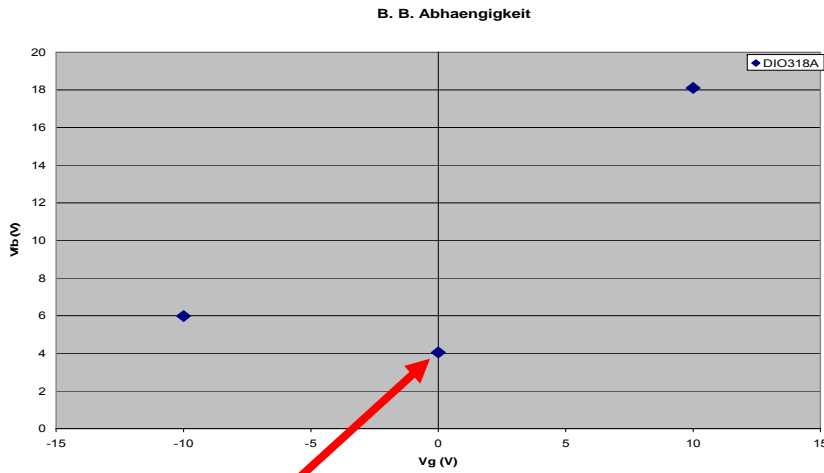
Flat band voltage Shift
→ N_{ox}



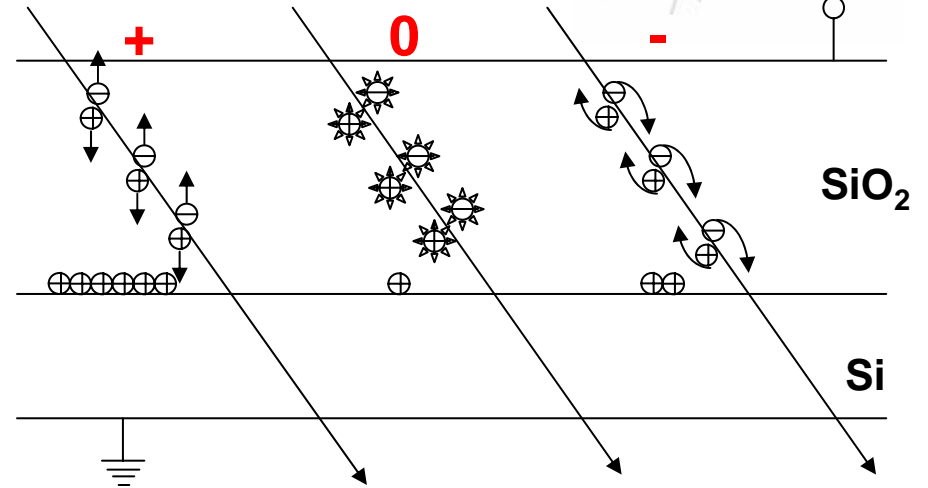
HF/LF CV
→ N_{it}

For MOS-C

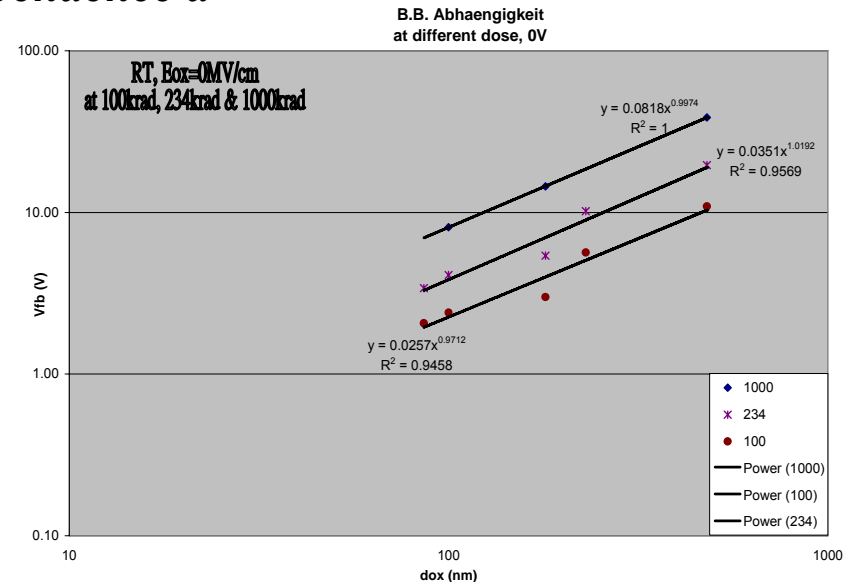
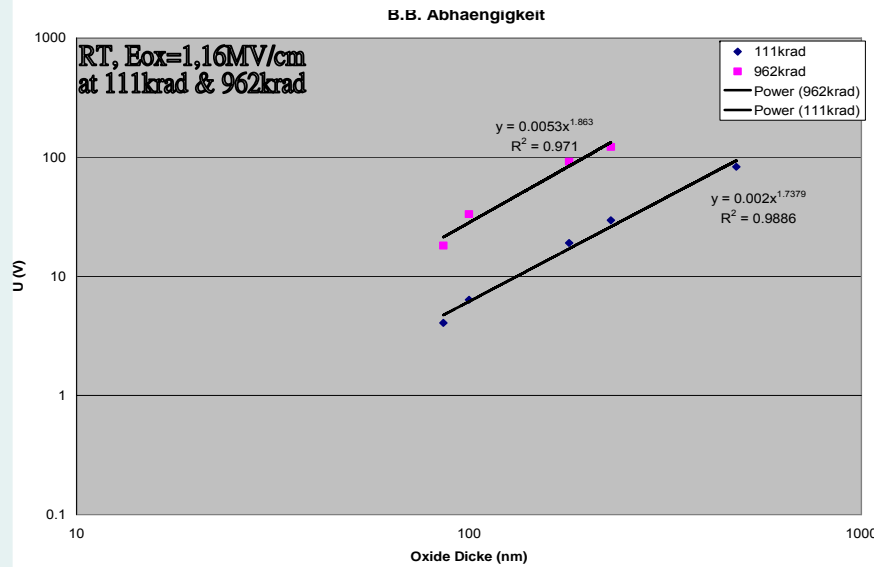
Bias Effect



DEPFET



thickness dependence d^n

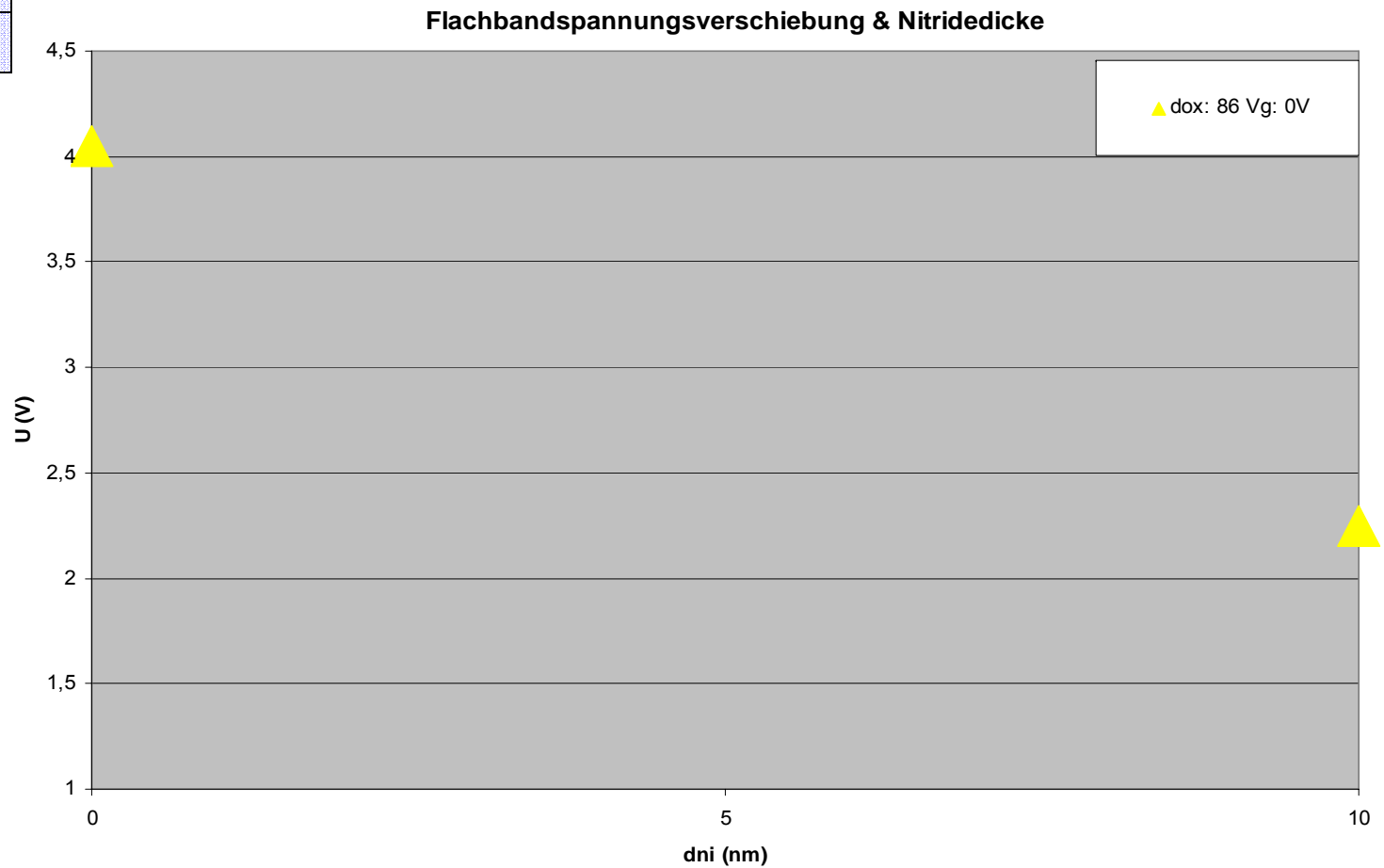


For MOS-C

Radiation hardness by Nitride-layer



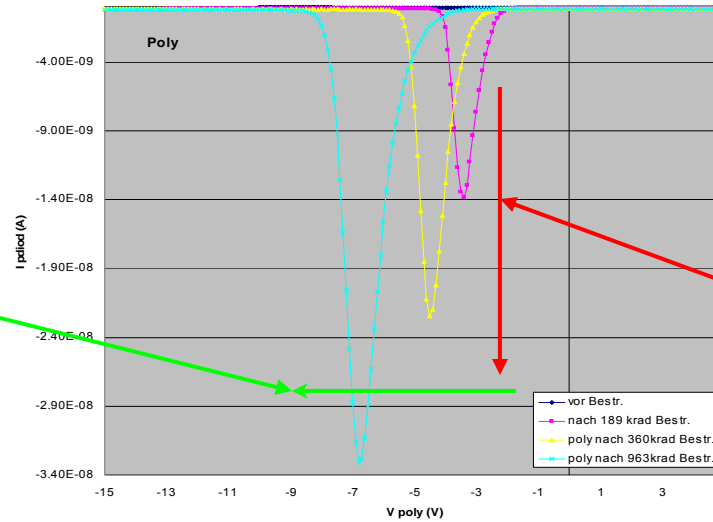
Al
LTO/Poly1/Poly2
Nitride
Oxide
Substrate n-Type



Results for gated diode

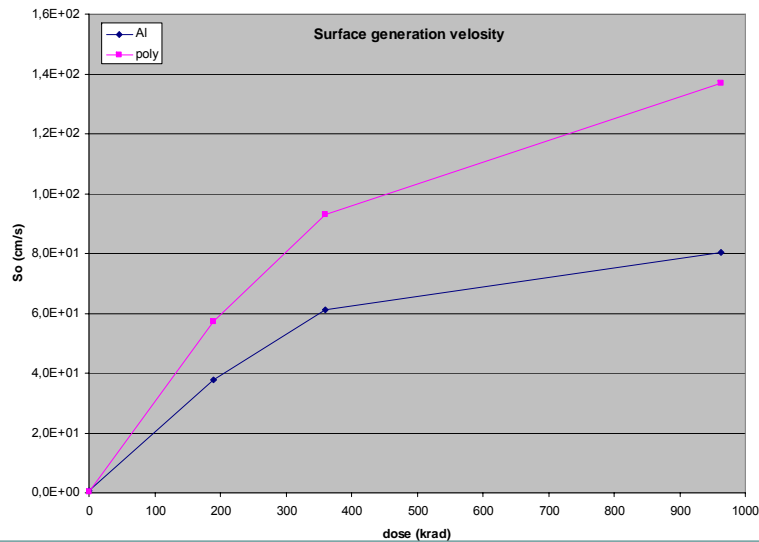


Shifts of generated current:



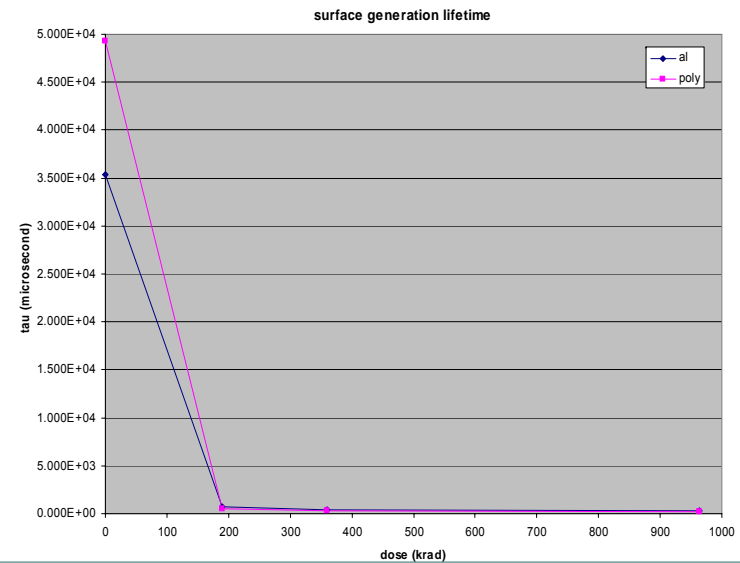
Increase of maximal current:

Increase of surface generation velocity



&

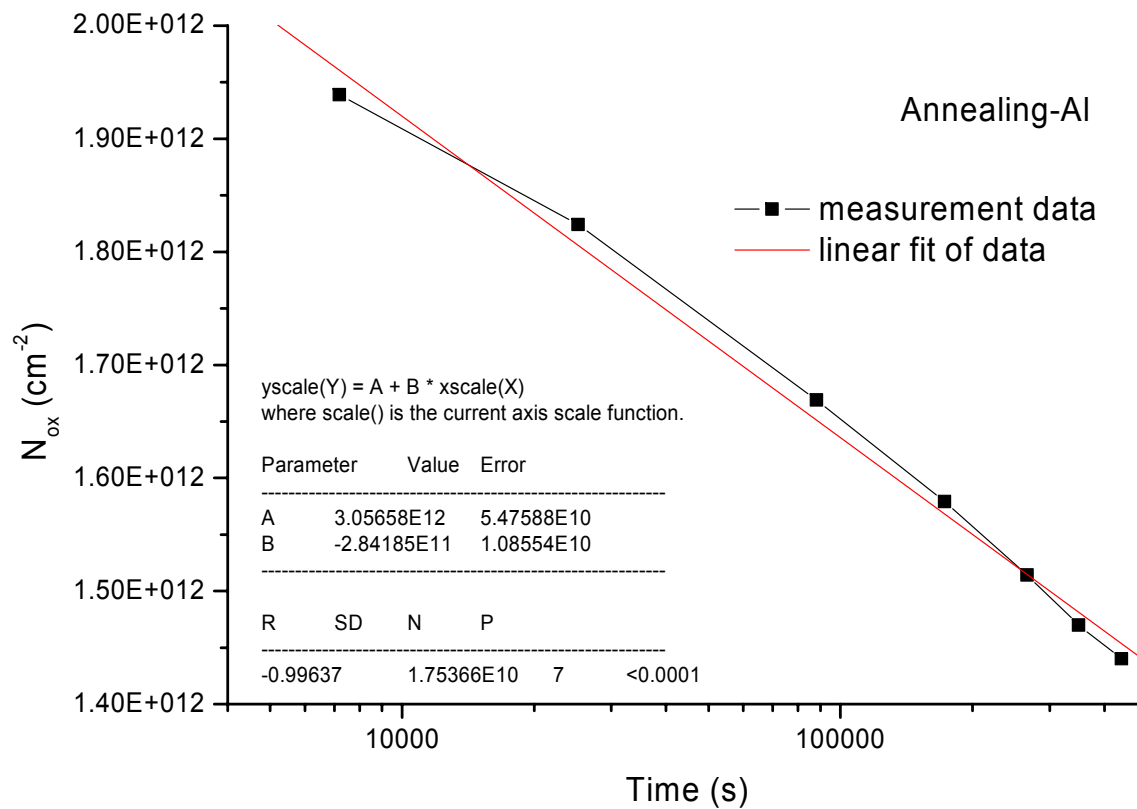
decrease of lifetime due to radiation:



Annealing for surface damage



Oxide charge decrease with time:
(Tunnel annealing @ RT)



Conclusion



◆ Radiation experiment

- Study of saturation effect for surface damage (equilibrium between generation and recombination)
- Study of bias dependence ("+", "0", "-")
- Study of different semiconductor devices, which are with different oxide thickness - to see the kind of relation between V_{fb} and oxide thickness (d_{ox}^n)

◆ Radiation hardness $\Gamma = N_{ox} / (\phi_h \times t) \leq 5\%$ ($\sim 1Mrad$)

- Reduced oxide thickness improves radiation hardness
- Additional Nitride layer serve as a good protection against ionizing radiation (*electron trapping!*)
- Surface damage can be reduced through annealing process with time