ATLAS Upgrade Plans and 3D Activities in UK

Phil Allport
University of Liverpool

Vertical Integration Technologies for HEP and Imaging Sensors Workshop
Ringberg Castle, Lake Tegernsee
7th April 2008

- **Proposed Tracker Layout and Simulations (Radiation and Occupancy)**
- **Sensor and FE Electronics R&D**
- **Microstrip Module and Engineering Concepts**
- **Material Issues and 3D Integration**
- **Conclusions**

ATLAS Upgrade Plans and 3D Activities in UK

Phil Allport
University of Liverpool

Vertical Integration Technologies for HEP and Imaging Sensors Workshop
Ringberg Castle, Lake Tegernsee
7th April 2008

- **Proposed Tracker Layout and Simulations (Radiation and Occupancy)**
- **Sensor and FE Electronics R&D**
- **Microstrip Module and Engineering Concepts**
- **Material Issues and 3D Integration**
- **Conclusions**

The European strategy for particle physics

http://council-strategygroup.web.cern.ch/council-strategygroup/

"The LHC will be the energy frontier machine for the foreseeable future, maintaining European leadership in the field; *the highest priority is to fully exploit the physics potential of the LHC, resources for completion of the initial programme have to be secured such that machine and experiments can operate optimally at their design performance.* A subsequent major luminosity upgrade (SLHC), motivated by physics results and operation experience, will be enabled by focussed R&D; *to this end,* ***R&D for machine and detectors has to be vigorously pursued now and centrally organized towards a luminosity upgrade by around 2015.***"

Why Discuss Upgrading the LHC Already?

Because we have to start the R&D now

Trigger Electronics:

- Most front-end electronics can probably stay but need faster clock speed and deeper pipelines
- Extensions to trigger capability required
- Need to maintain L1 output rate (more data per event)
  - Must upgrade detector backend electronics
    - increase bandwidth to deal with more data per event
  - Modify trigger algorithms to deal with high occupancy (and increase thresholds)

L-Ar:

- Performance degradation due to high rates in forward direction
  FCAL will probably need some detector upgrade

TileCal:

- Slow degradation due to radiation of scintillators
- New electronics probably required

Muon systems:

- Degradation in performance due to high rates, in particular in the forward regions:
  - Will need additional shielding for forward region
  - May need beryllium beampipe
  - Aging/radiation damage needs confirmation for SLHC operation
- Higher rate technologies may be needed to replace some forward chambers

Inner Detector tracking systems:

- **The entire Inner Detector will have to be rebuilt**

ATLAS Inner Detector Replacement

To keep ATLAS running more than 10 years the inner tracker will have to go ...
(Current tracker designed to survive up to 730 fb^{-1} ≈ 10Mrad in strip detectors)

For the luminosity-upgrade the new tracker will have to cope with:

- **much higher dose rates**
- **much higher occupancy levels**

To complete a new tracker for 2016, major R&D programme already needed.

Timescales:

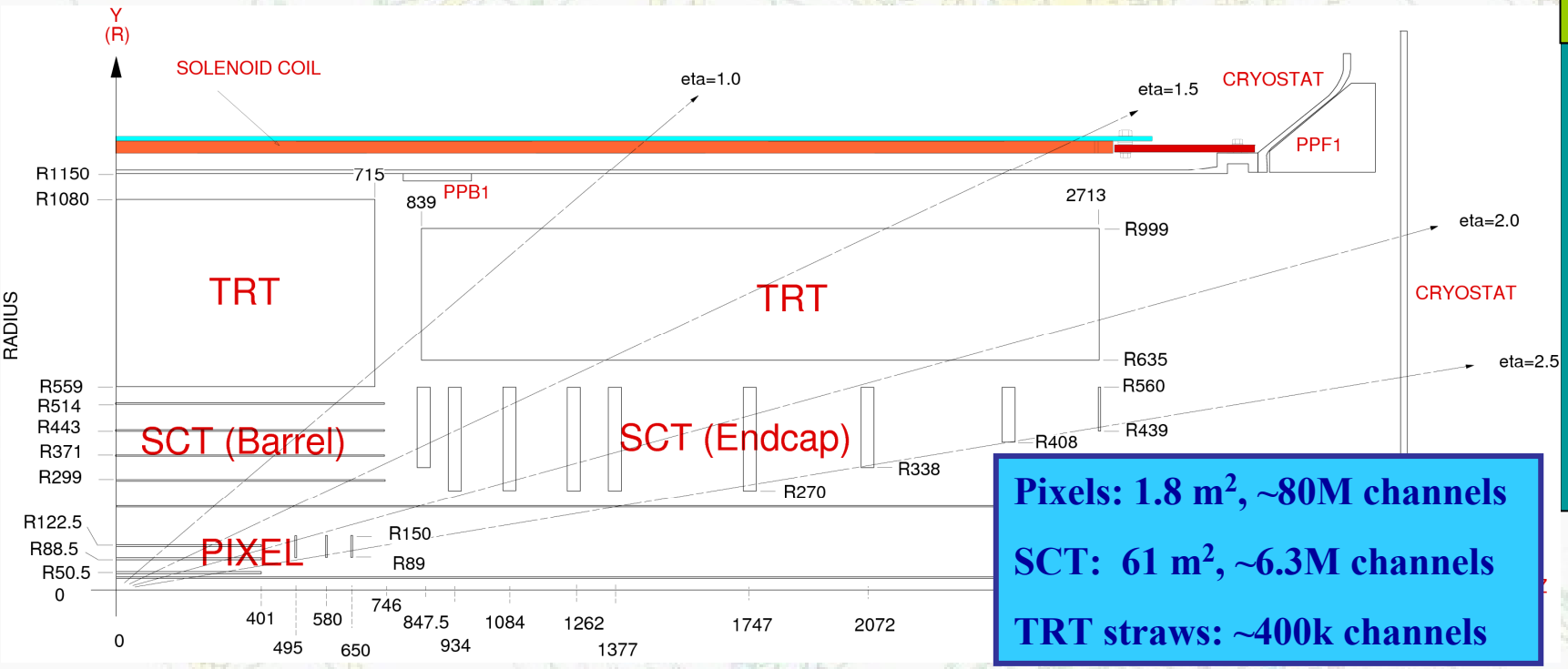
- **R&D leading into a full tracker Technical Design Report (TDR) in 2010**
- **Construction phase to start immediately TDR completed and approved.**

The intermediate radius barrels are expected to consist of modules arranged in rows with common cooling, power, clocking and cooling.

The TDR will require prototype super-modules/staves (complete module rows as an integrated structure) to be assembled and fully evaluated

All components will need to demonstrate unprecedented radiation hardness

Current Inner Tracker Layout

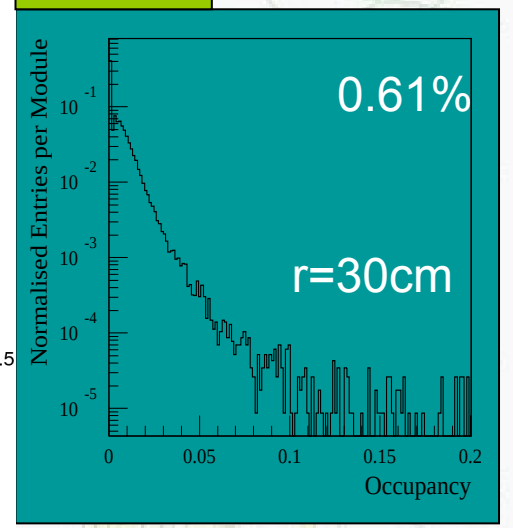


Pixels: 1.8 m², ~80M channels

SCT: 61 m², ~6.3M channels

TRT straws: ~400k channels

ID TDR



Mean Occupancy in Innermost Layer of Current SCT

Pixels (50 μm × 400 μm): 3 barrels, 2×3 disks — 5cm < r < 15cm

- Pattern recognition in high occupancy region
- Impact parameter resolution (in 3d)

Radiation hard technology: n^+-in-n Silicon technology, operated at -6°C

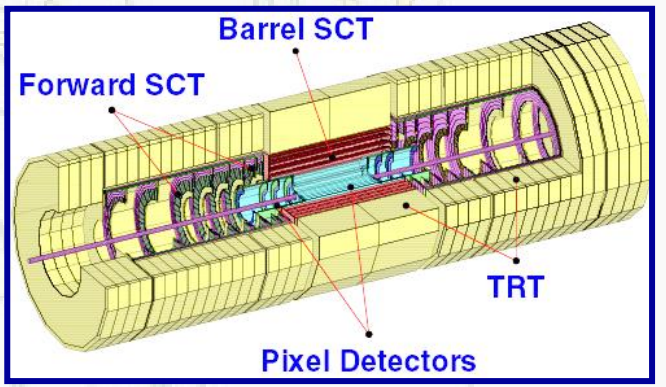
Strips (80 μm × 12 cm) (small stereo angle): "SCT" 4 barrels, 2×9 disks — 30cm < r < 51cm

- pattern recognition
- momentum resolution

p-strips in n-type silicon, operated at -7°C

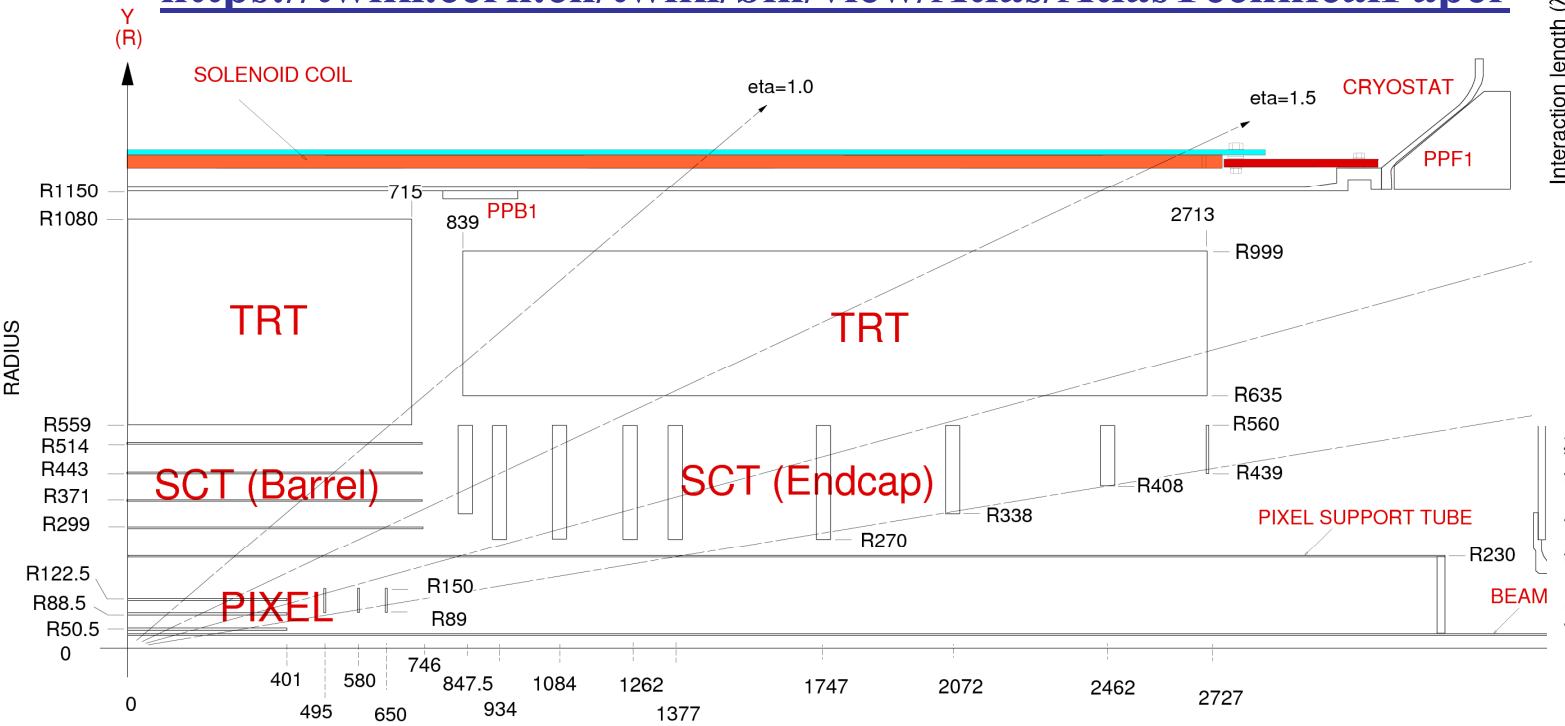
TRT 4mm diameter straw drift tubes: barrel + wheels — 55cm < r < 105cm

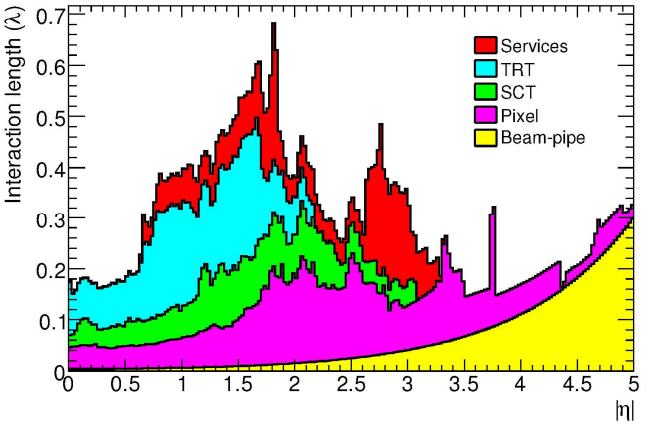
- Additional pattern recognition by having many hits (~36)
- Standalone electron id. from transition radiation

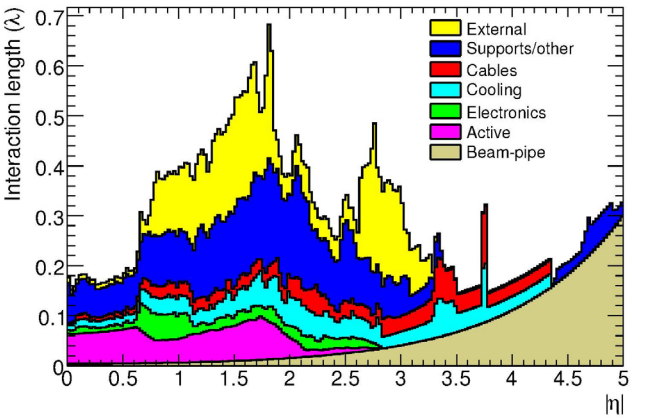


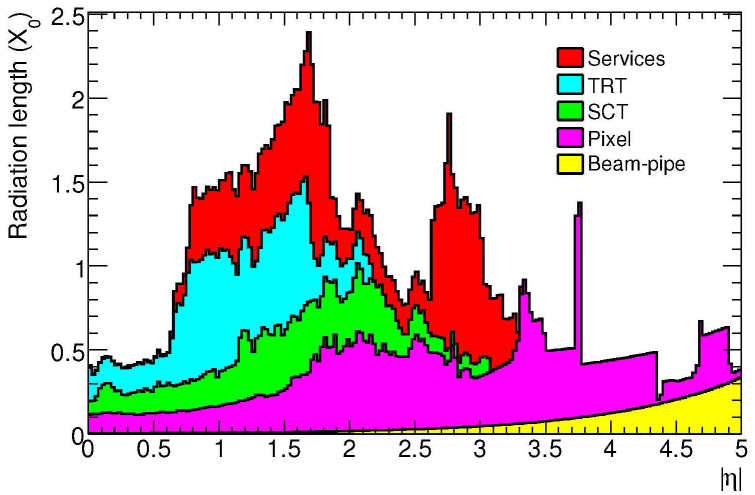
Current Inner Tracker Material

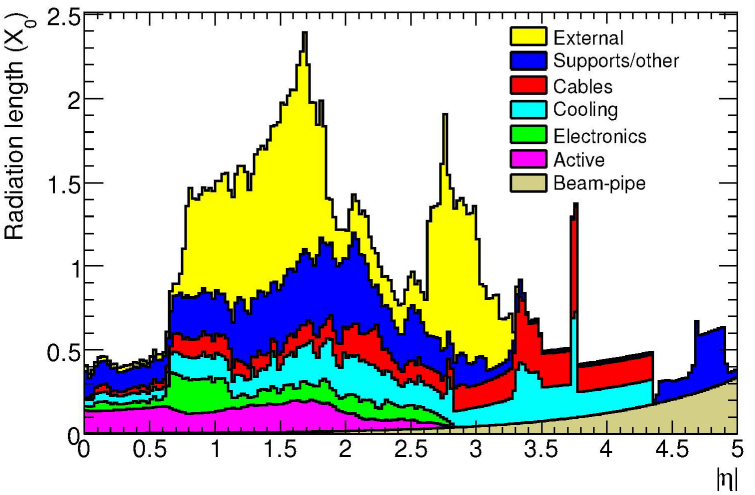
https://twiki.cern.ch/twiki/bin/view/Atlas/AtlasTechnicalPaper

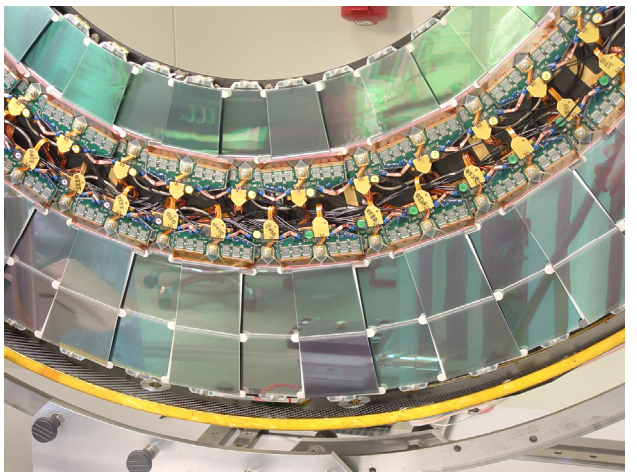




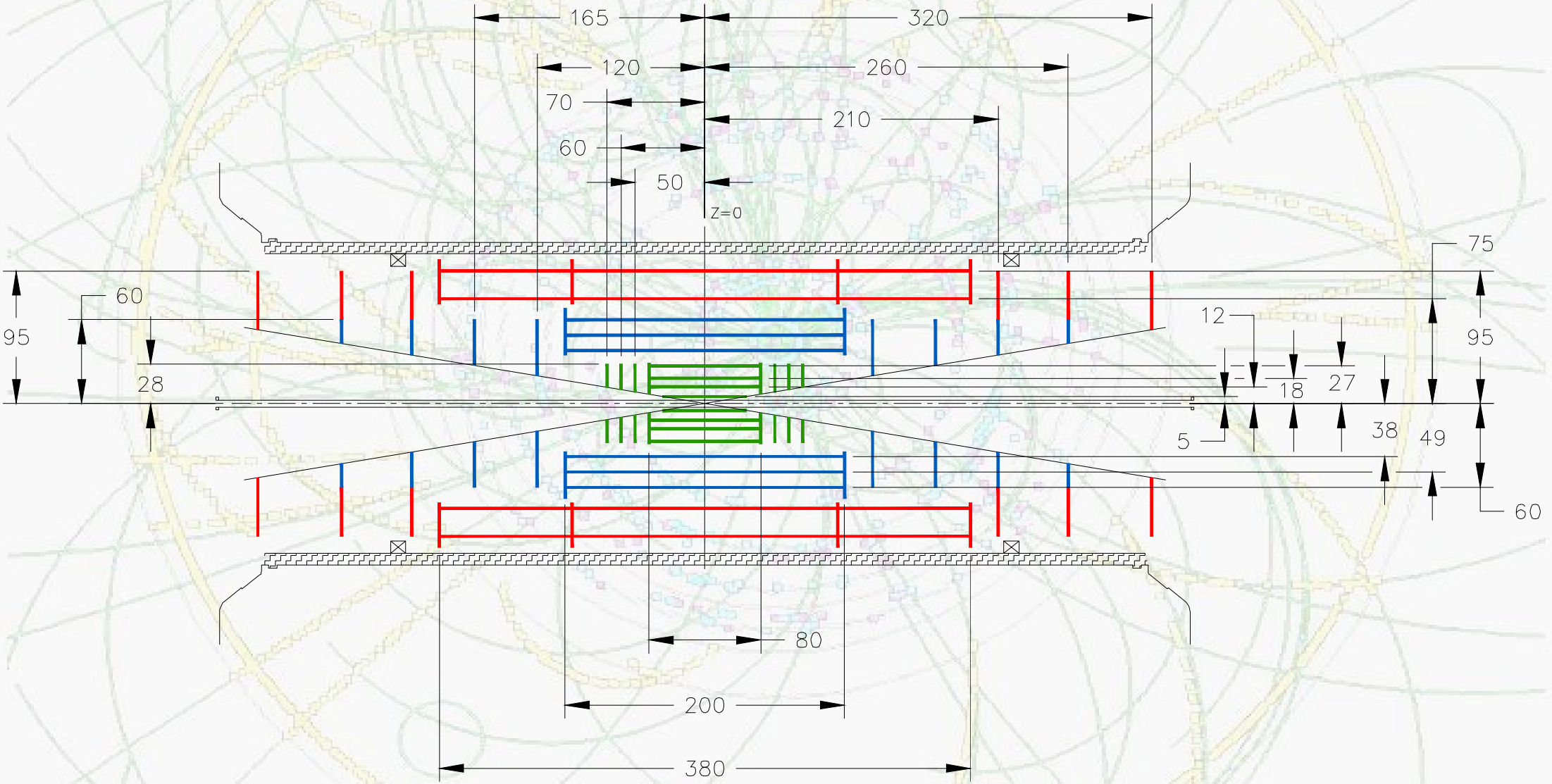








Proposed Upgrade Layout



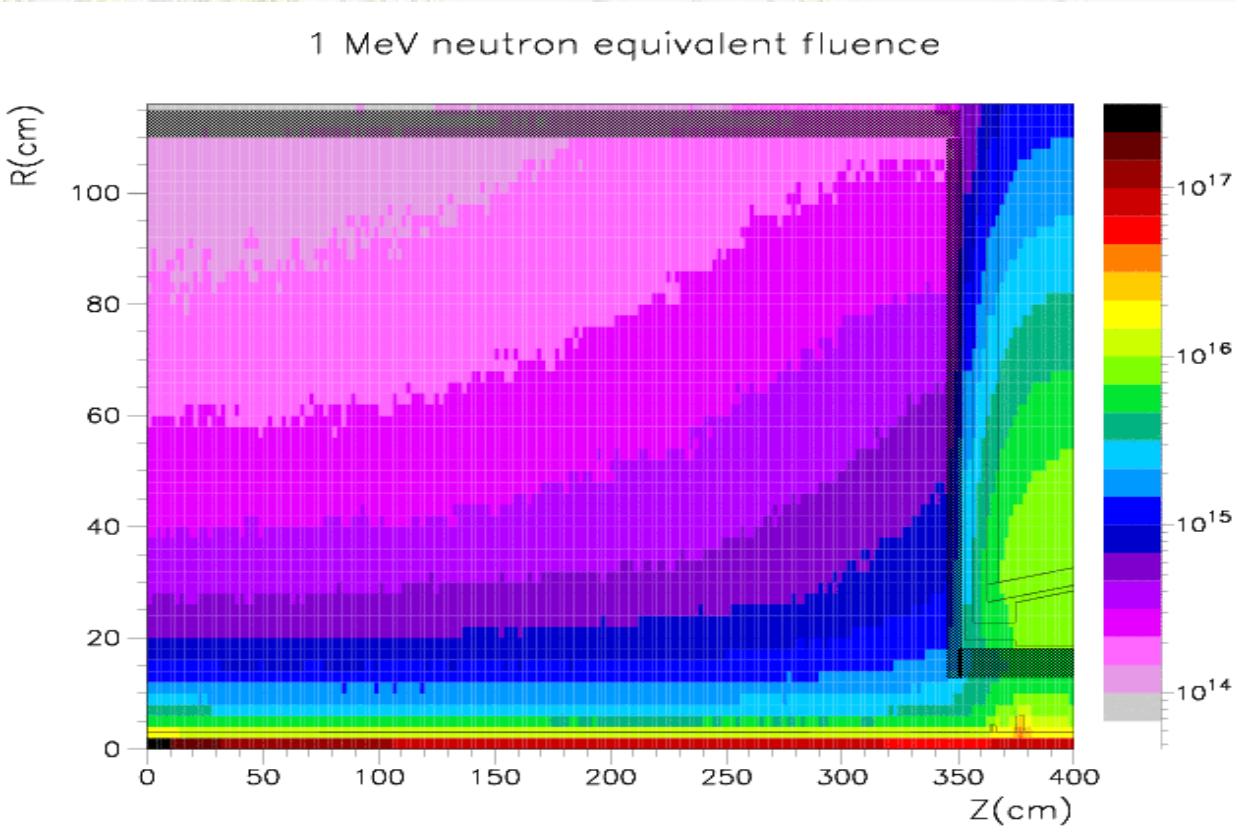
New SLHC Layout Implications: Radiation Dose

- With safety factor of two, need pixel b-layer to survive up to $10^{16} n_{eq}/cm^2$
- Inner microstrip layers to withstand $9 \times 10^{14} n_{eq}/cm^2$ (50% neutrons)
- Outer layers up to $4 \times 10^{14} n_{eq}/cm^2$ (and mostly neutrons)

→ Issues of thermal management and shot noise. Silicon looks to need to be at ~ -25°C (depending on details of module design).

→ High levels of activation will require careful consideration for access and maintenance.

Issues of coolant temperature, module design, sensor geometry, radiation length, etc etc all heavily interdependent.



Quarter slice through ATLAS inner tracker Region, with 5cm moderator lining calorimeters. Fluences obtained using FLUKA2006, assuming an integrated luminosity of 3000fb^{-1}.

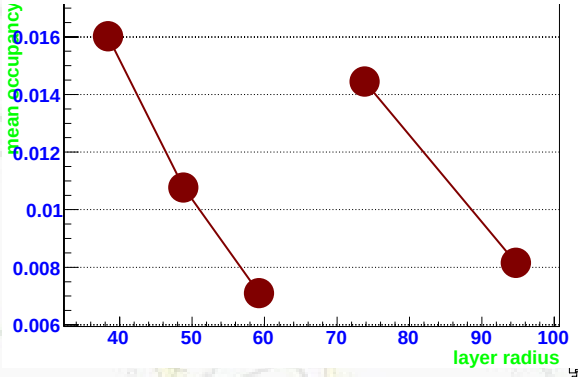
I. Dawson (Sheffield)

New SLHC Layout Implications: Occupancy

Strawman 4+3+2

Pixel Tracker Layers:	**r = 3–5cm, 12cm, 18cm, 27cm**	**z = ±40cm**
Short Strip (2.4 cm) μ-strips (stereo layers):	**r = 38cm, 49cm, 60cm**	**z = ±100cm**
Long Strip (9.6 cm) μ-strips (stereo layers):	**r = 75cm, 95cm**	**z = ±190cm**

Short and Long Strip Occupancy

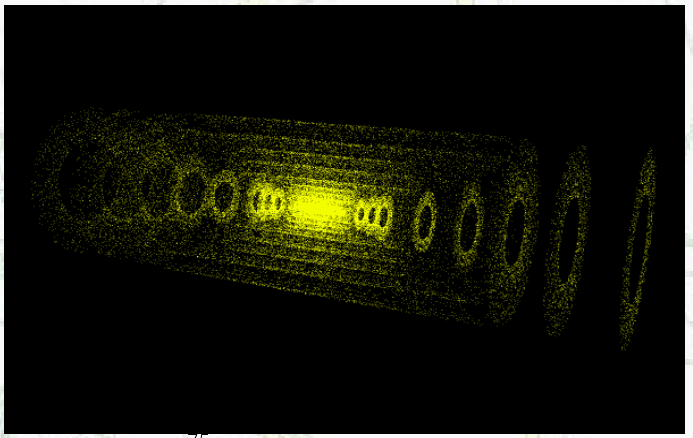


1.6%

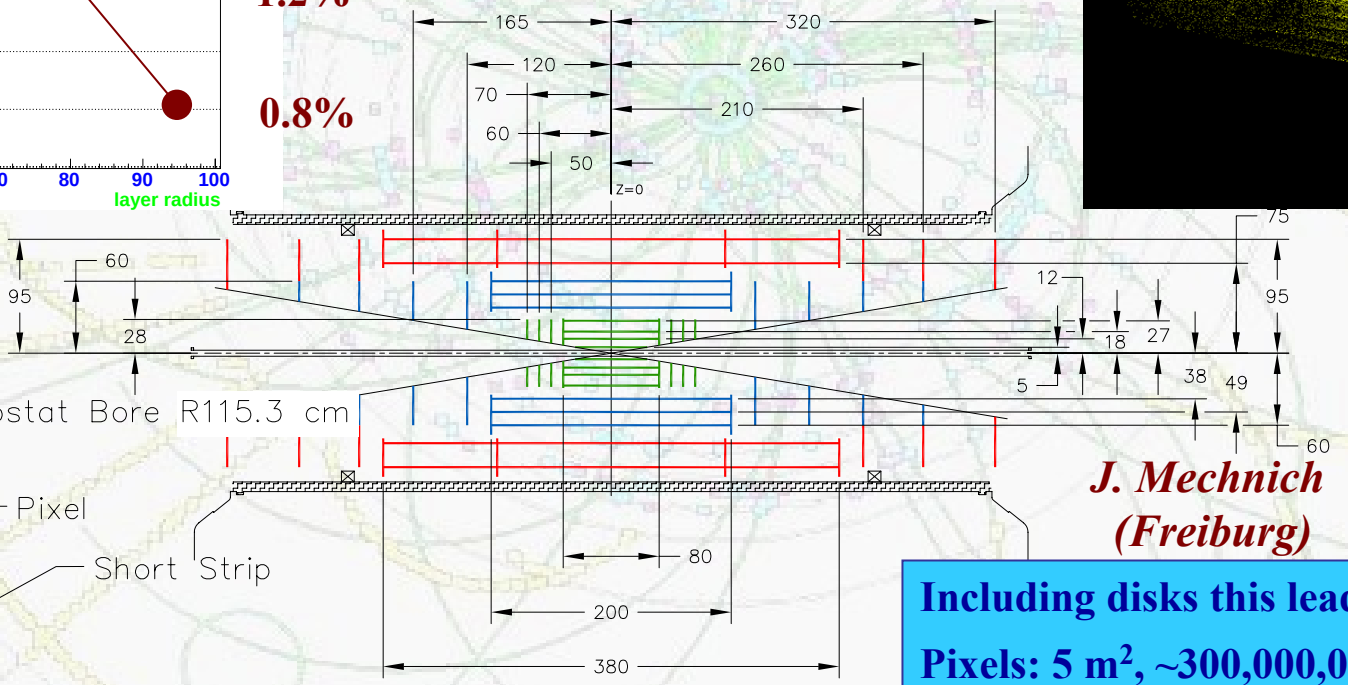
1.2%

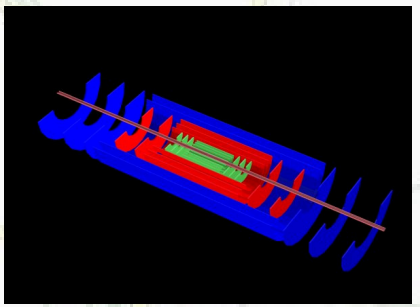
0.8%

Only LO MC (Pythia) . May need to include ×2 safety factor?

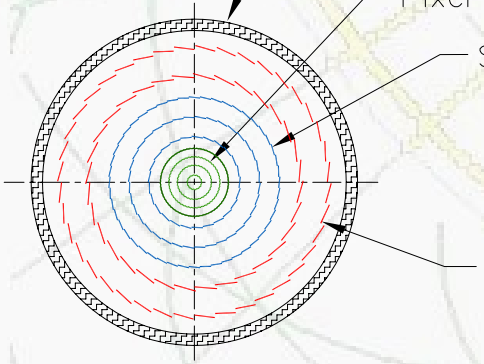


J. Tseng (Oxford)





J. Mechnich (Freiburg)



Including disks this leads to:

Pixels: 5 m^2, ~300,000,000 channels

Short strips: 60 m^2, ~30,000,000 channels

Long strips: 100 m^2, ~15,000,000 channels

ATLAS Upgrade Plans and 3D Activities in UK

Phil Allport
University of Liverpool

Vertical Integration Technologies for HEP and Imaging Sensors Workshop
Ringberg Castle, Lake Tegernsee
7th April 2008

- Proposed Tracker Layout and Simulations (Radiation and Occupancy)
- **Sensor and FE Electronics R&D**
- Microstrip Module and Engineering Concepts
- Material Issues and 3D Integration
- Conclusions

B-layer: Replacement → Upgrade

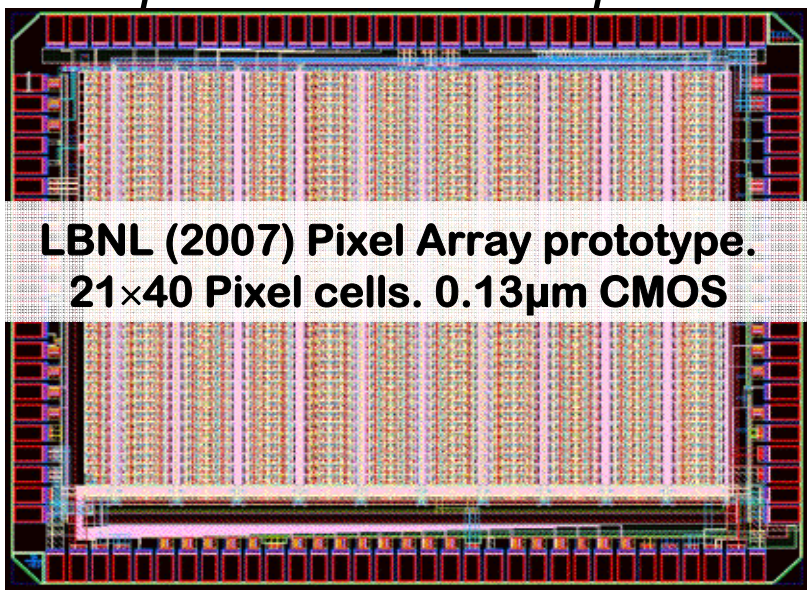
- *ATLAS considers to have a B-layer replacement after ~3 year of integrated full LHC luminosity **(2012)** and replace completely the Inner Tracker with a fully silicon version for SLHC (2016).*

- *The B-layer replacement can be seen as an intermediate step towards the full upgrade. Performance improvements for the detector (here some issues more related to FE chip):*
  - **Reduce radius** → Improve radiation hardness (→ 3D sensors, or possibly, thin planar detectors, diamond, gas, …?)
  - **Reduce pixel cell size and architecture related dead time** (→ deign FE for higher luminosity, use 0.13 μm 8 metal CMOS)
  - **Reduce material budget** of the b-layer (~3% X_0 → 2.0–2.5% X_0)
  - **increase the module live fraction** (→ increase chip size, > 12×14 mm^2) possibly use "active edge" technology for sensor.
  - **Use faster R/O links**, move MCC at the end of stave

- *The B-layer for the upgrade will need radiation hardness (10^{15} → 10^{16} n_{eq}/cm^2) and cope with detector occupancies up to (× 15)*

New Pixel FE-ASIC Design

- *Design of a new Front-End chip (FE-I4) is going on as a Collaborative Work of 5 Laboratories: Bonn, CPPM, Genova, LBNL, Nikhef*
- *FE-I4 tentative schedule*
  - 9/2007: Architecture definition
  - 10/2007: Footprint frozen
  - 01/2008: Initial Design review
  - 12/2008: Final Design review
- *Some prototype silicon made of small blocks and analog part of the pixel cell in 0.13 µm.*



LBNL (2007) Pixel Array prototype. 21×40 Pixel cells. 0.13µm CMOS

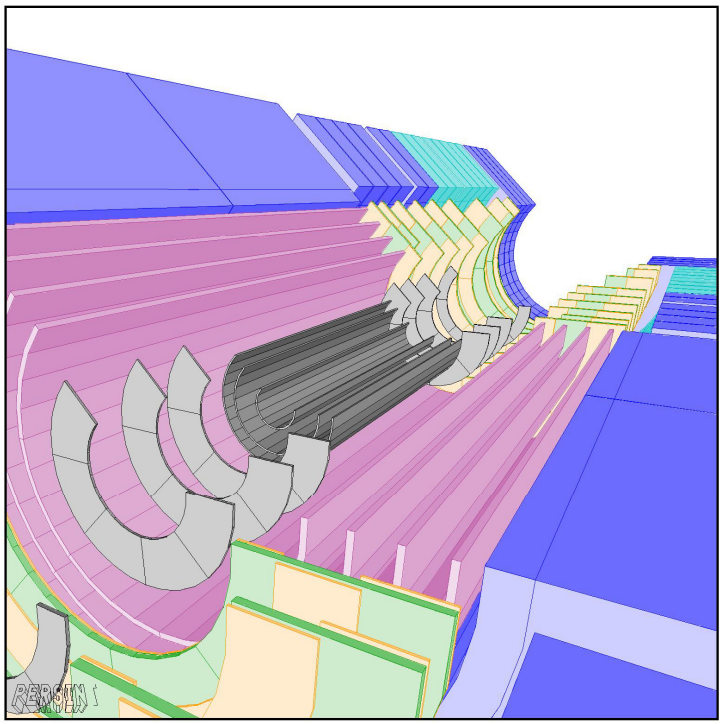
Main Parameter	*Value*	*Unit*
Pixel size	50 x 250	μm^2
Input	DC-coupled negative polarity	
Normal pixel input capacitance range	300Ö500	fF
In-time threshold with 20ns gate	4000	e
Two-hit time resolution	400	ns
DC leakage current tolerance	100	nA
Single channel ENC sigma (400fF)	300	e
Tuned threshold dispersion	100	e
Analog supply current/pixel @400fF	10	µA
Radiation tolerance	200	MRad
Acquisition mode	Data driven with time stamp	
Time stamp precision	8	bits
Single chip data output rate	160	Mb/s

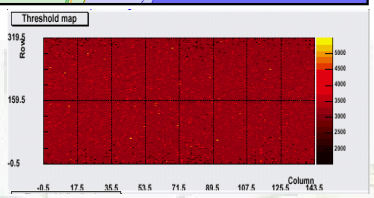
FE-I4 (B-layer Replacement) Specifications: main parameters

Innermost Detectors at Current LHC

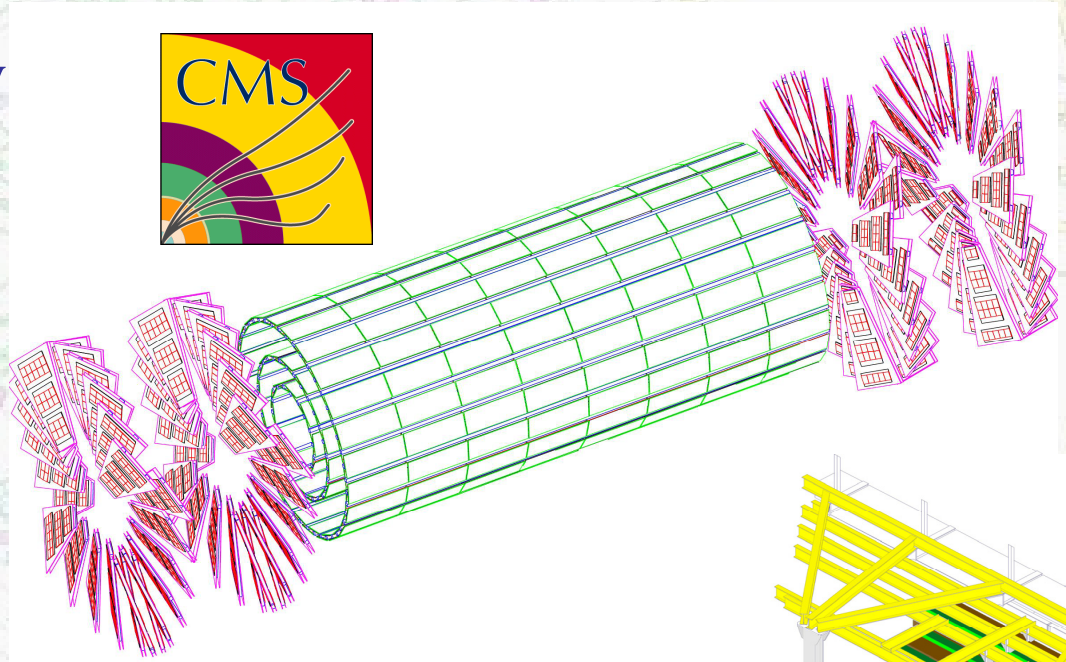
LHC vertex detectors all use n^+ implants in n^- bulk:

- Because of advantages after heavy irradiation from collecting electrons on n^+ implants, the detectors at the LHC (ATLAS and CMS Pixels and LHCb Vertex Locator) have all adopted the n^+ in n^- configuration for doses of $5 - 10 \times 10^{14}$ $n_{eq}cm^{-2}$
- Requires 2-sided lithography

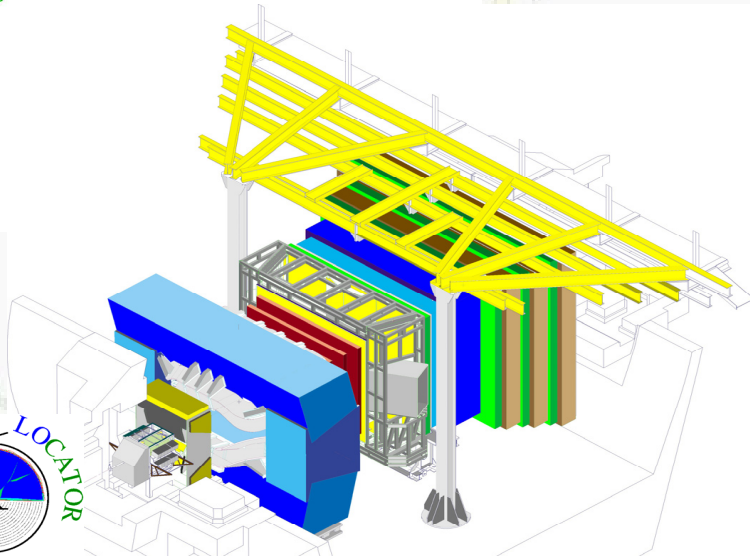




ATLAS 100 million Pixels



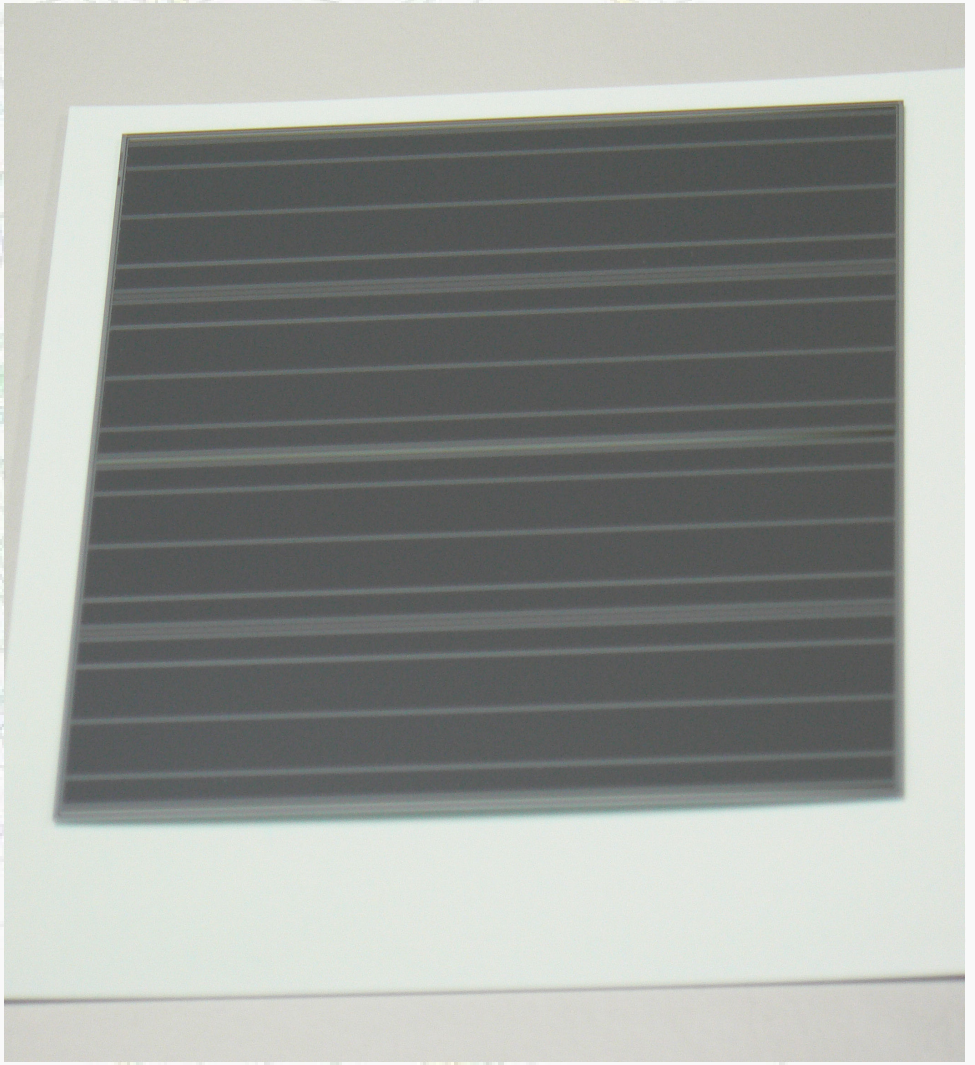
LHCb
Vertex Locator
Z(mm)=0-990



Motivations for P-type

Starting with a p^--type substrate offers the advantages of single-sided processing while keeping n^+-side read-out:

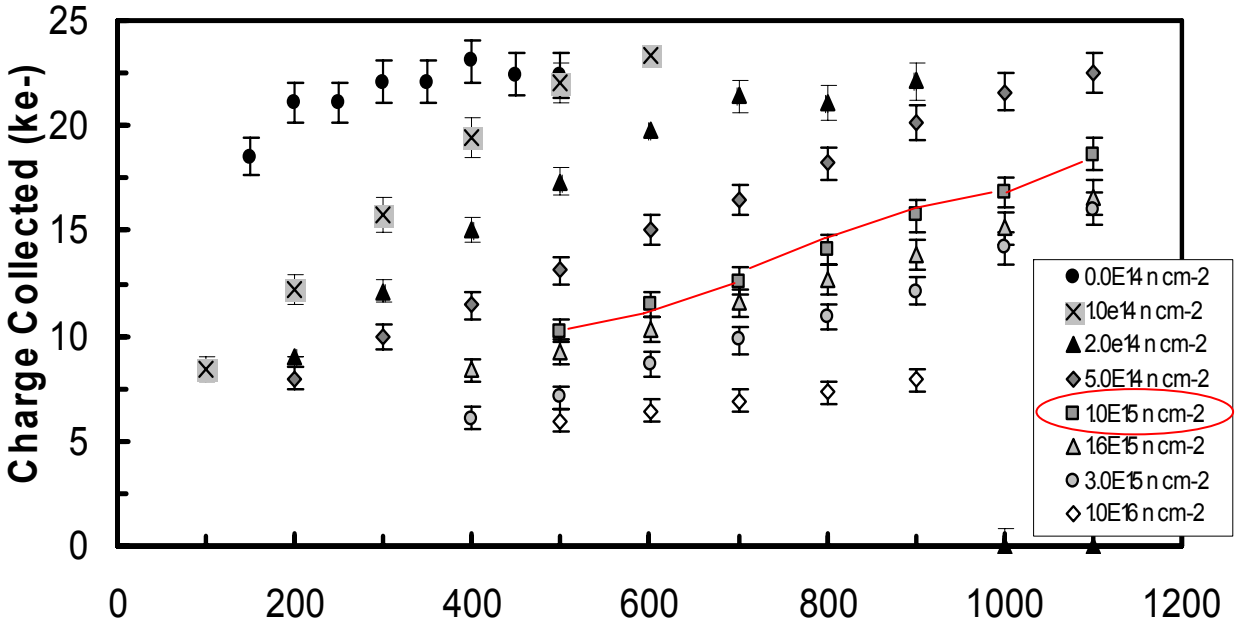
- Processing Costs (~50% cheaper).
- Greater potential choice of suppliers.
- High fields always on the same side.
- Easy of handling during testing.
- No delicate back-side implanted structures to be considered in module design or mechanical assembly.



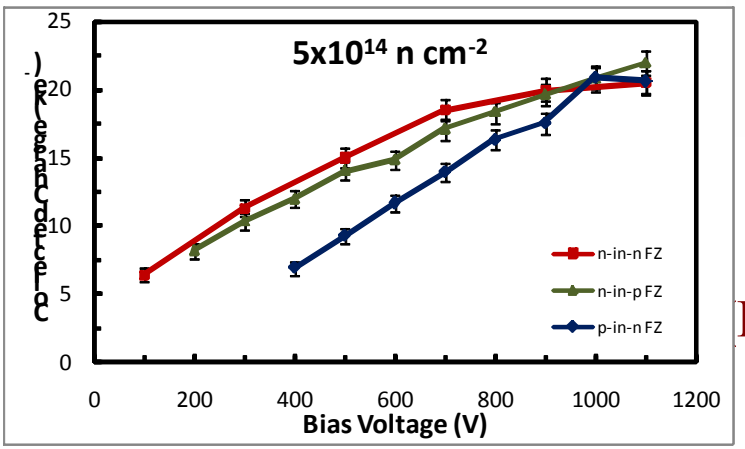
So far, capacitively coupled, polysilicon biased p-type devices fabricated to ATLAS provided mask designs by:

- Micron Semiconductor (UK) Ltd (existing ATLAS barrel: 6cm×6cm and RD50 miniatures: 1cm ×1cm),
- CNM Barcelona (RD50 miniatures: 1cm×1cm),
- ITC Trento (RD50 miniatures: 1cm×1cm)
- Hamamatsu Photonics HPK (1cm×1cm and 10cm×10cm Full ATLAS prototypes)

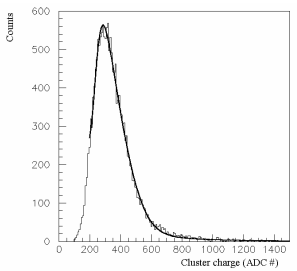
Microstrip Sensor Irradiation



m.i.p. CCE (V) planar neutron irradiated p-type



CCE (V) planar n-type and p-type Micron miniatures after 5×10^{14}n/cm^2 (Ljubljana reactor neutrons)

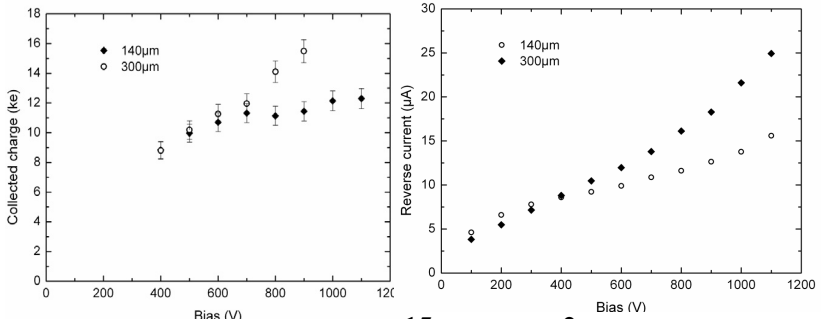


m.i.p. CCE (V) Micron RD50 planar P-type

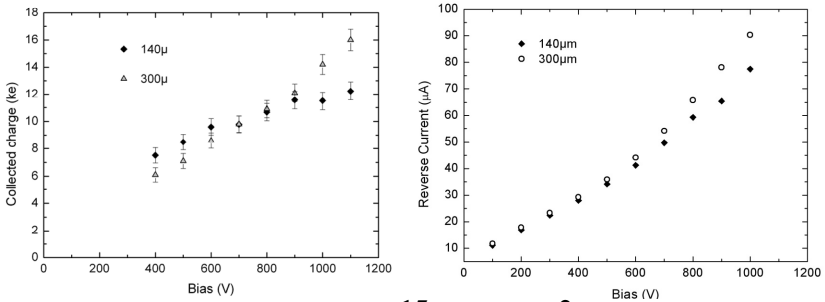
140µm and 300µm thickness

Doses up to 10^{16}n$_{eq}$/cm^2 Ljubljana reactor neutrons)

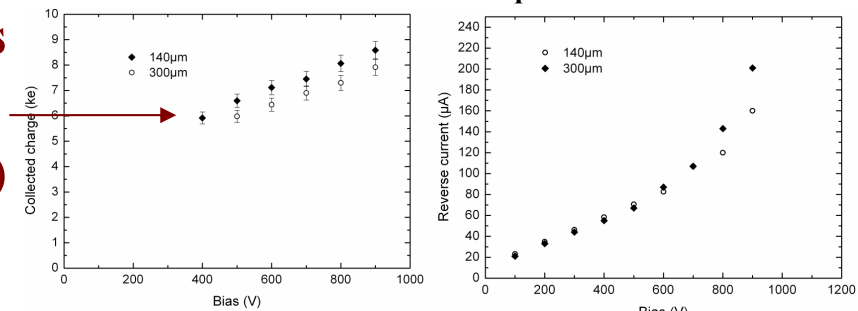
Short microstrip layers to withstand 9×10^{14}n$_{eq}$/cm^2 (50% neutrons) at 500V with 750e$^-$ noise → expect S/N ≈12



CCE(V) 1.6×10^{15} n$_{eq}$/cm^2 I(V)



CCE(V) 3.0×10^{15} n$_{eq}$/cm^2 I(V)

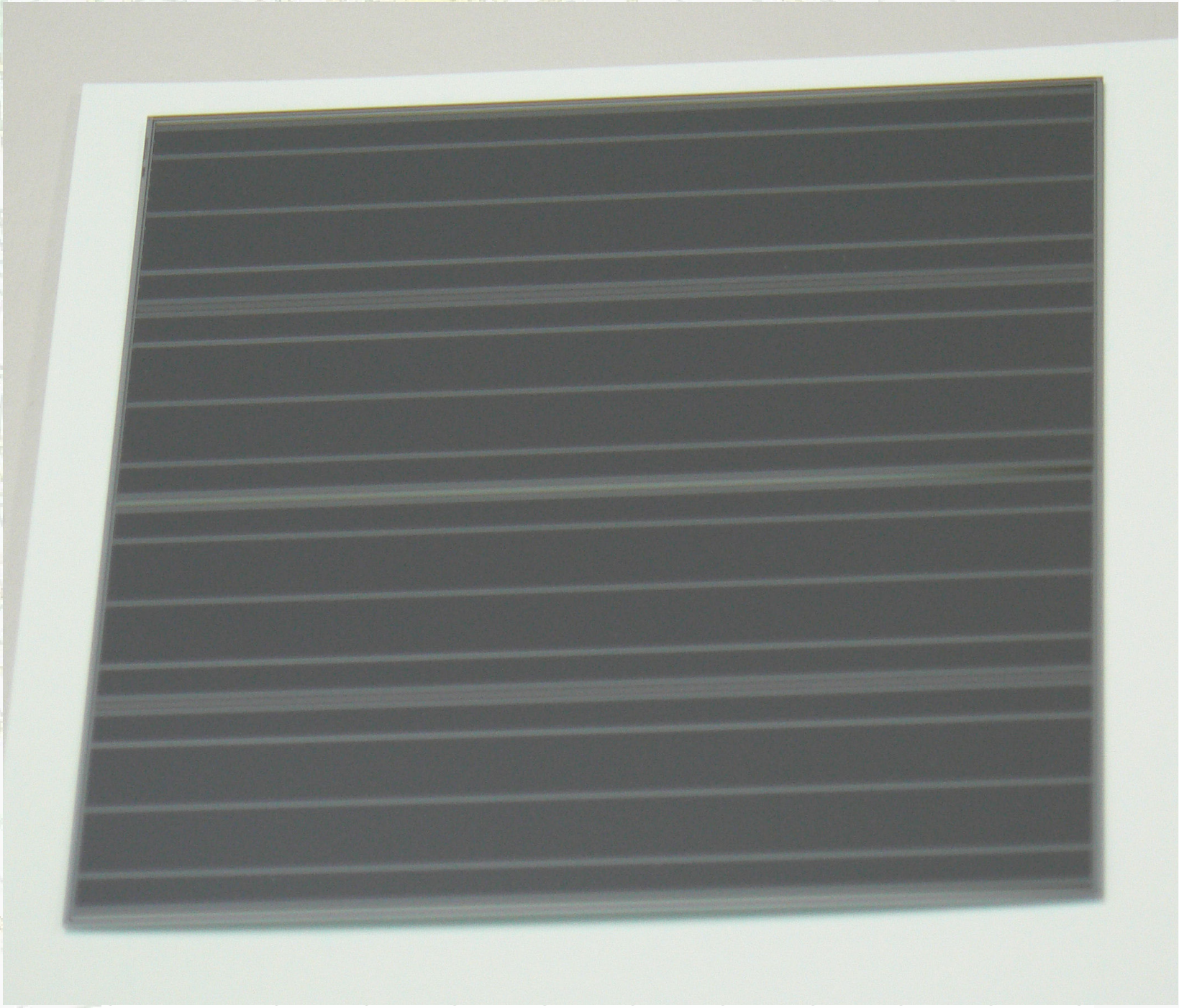


CCE(V) 10^{16} n$_{eq}$/cm^2 I(V)

Tony Affolder, Gianluigi Casse

HPK Sensor Mask Layout

- Strip segments
  - **4 rows of 2.38 cm strips (each row 1280 channels)**
- **Dimension**
  - **Full square**
- **Wafer**
  - **150 mm p-type FZ(100)**
  - **138 mm dia. usable**
  - **320 µm thick**
- **Axial strips**
  - **74.5 µm pitch**
- **Stereo strips**
  - **40 mrad**
  - **71.5 µm pitch**
- **Bond pads location**
  - **accommodating 24-40 mm distances**
- **n-strip isolation**
  - **P-stop**
  - **Spray on miniatures**



Microstrip Front-end ASIC (ABCn) Design Status

Front-End	Opt. short strip done Layout started	33mA/chip ✓ 750enc (2.5cm strips) Final S/N > 10 ✓
Back-End	Main change in DCL block to handle 160MHz	92mA/chip at 2.5V estimated
Powering	Integrated shunt regulators possible	Current limits to impose uniformity
Floor Plan	First Checks now	7.5mm by 6±1mm
P&R	Examples with pipeline and derandomizer OK	
Submission	Spring 2008	Deliver Summer 2008

ATLAS Upgrade Plans and 3D Activities in UK

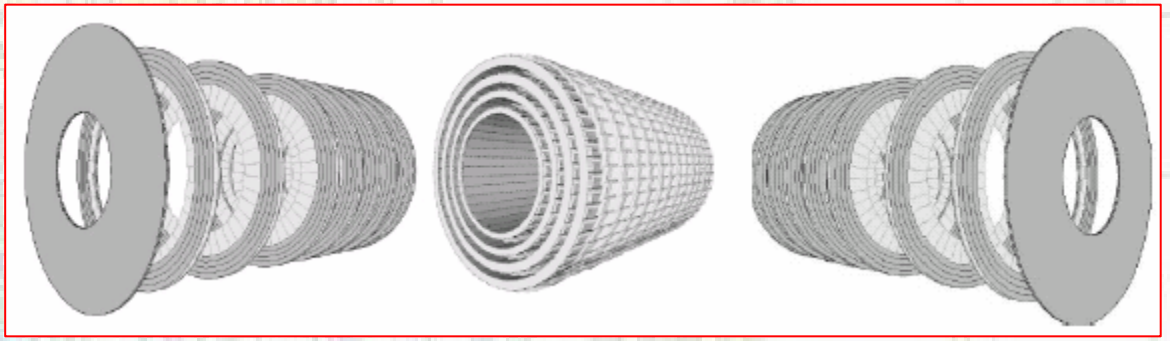
Phil Allport
University of Liverpool

Vertical Integration Technologies for HEP and Imaging Sensors Workshop
Ringberg Castle, Lake Tegernsee
7th April 2008

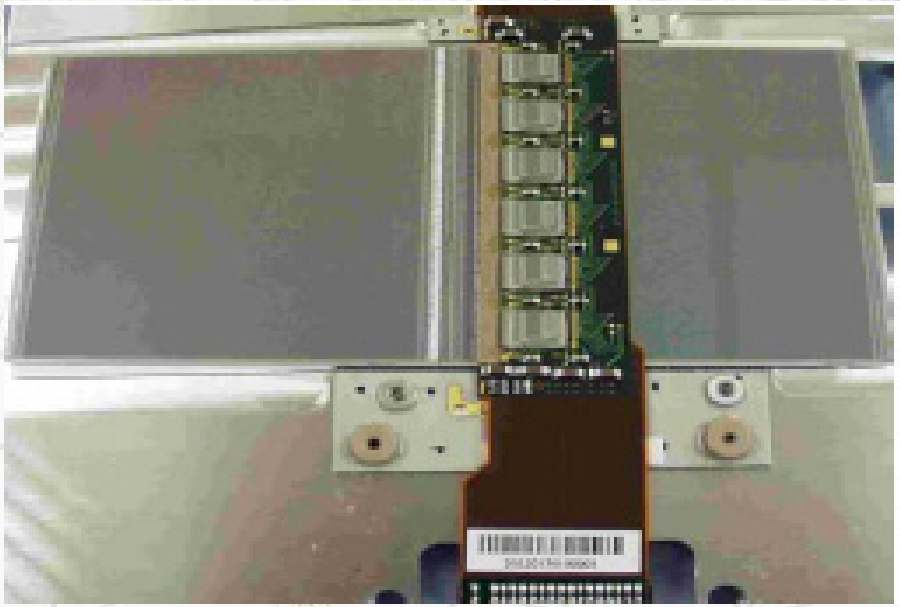
- Proposed Tracker Layout and Simulations (Radiation and Occupancy)
- Sensor and FE Electronics R&D
- **Microstrip Module and Engineering Concepts**
- Material Issues and 3D Integration
- Conclusions

Current SCT ATLAS Module Designs

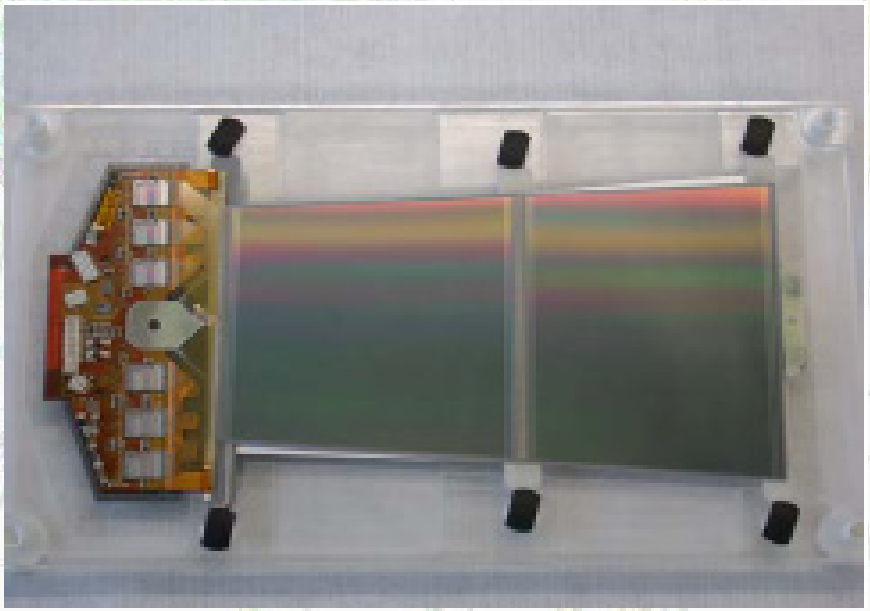
ATLAS Tracker Based on Barrel and Disc Supports



Effectively two styles of modules (with 2×6cm long strips)

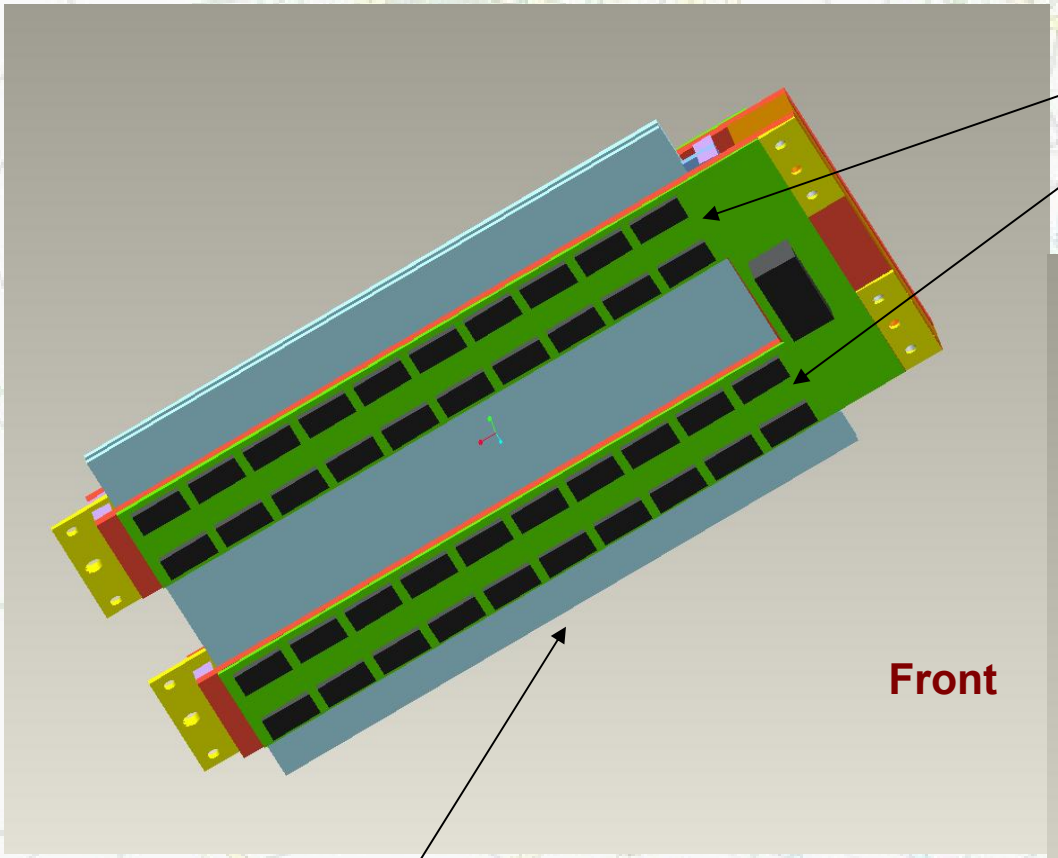


Barrel Modules
(Hybrid bridge above sensors)



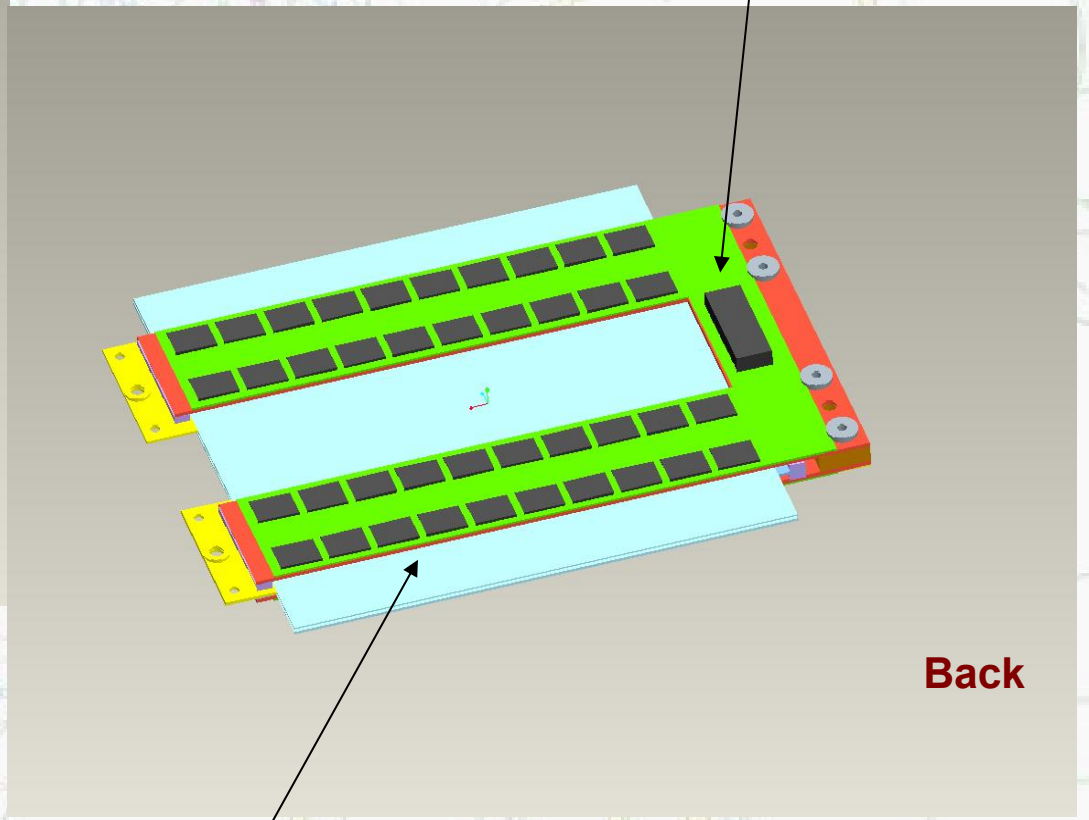
Forward Modules
(Hybrid at module end)

Super-LHC Double Sided Module



Sets of 10 FE Chips in 4 rows

Module Controller Chip



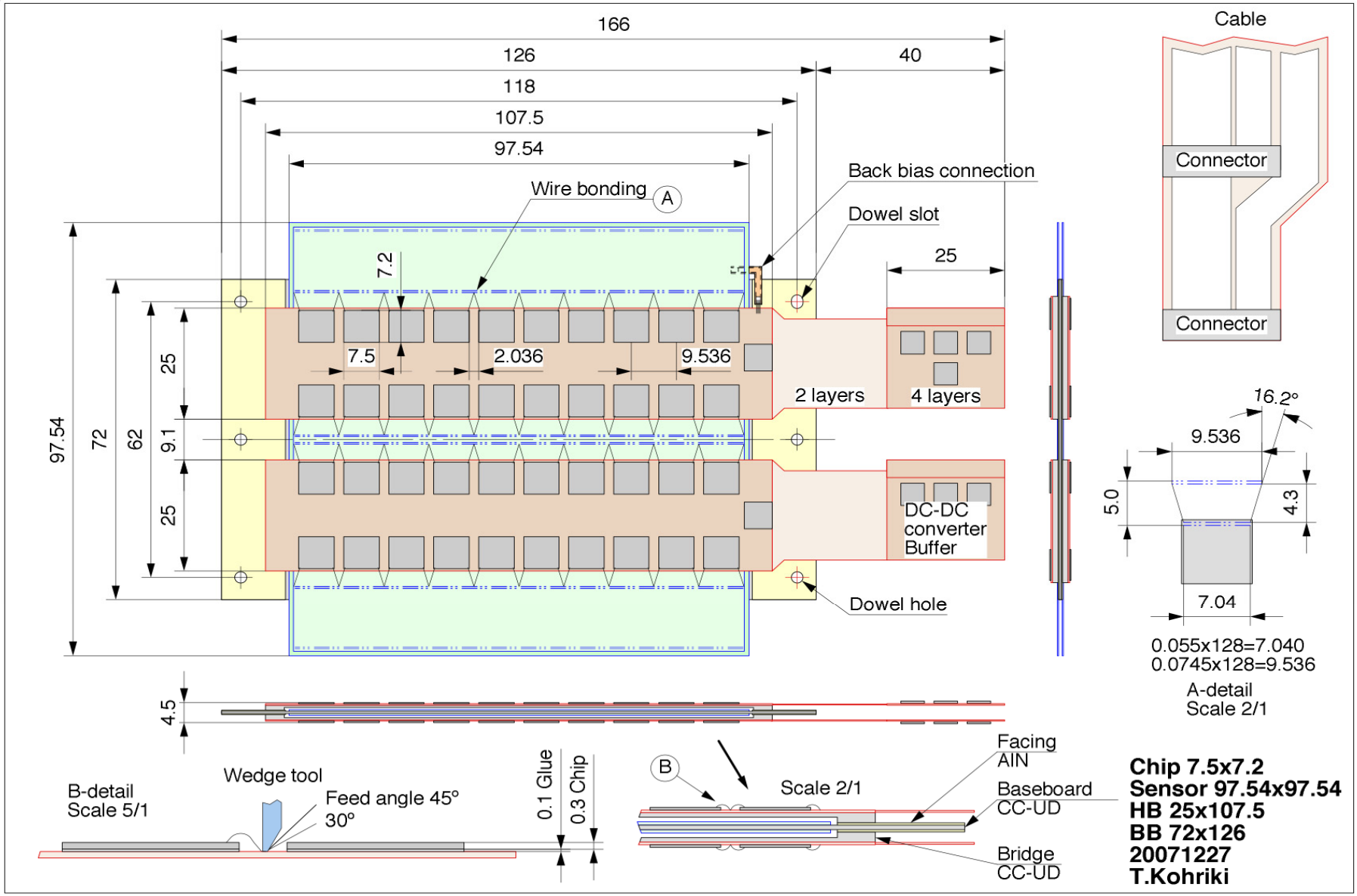
2 single-sided 10cm square detectors mounted back-to-back around a high thermal conductivity base board
Each detector has 4 rows of 1280 2.4cm long striplets

The Multi-layer kapton circuit in green is the “hybrid” which busses signals to/from/between the microchips and provide the electrical services to the front end electronics
Wire bonds connect the electronics to the hybrid and provide the high density connections down from the front-end to the 4 pad rows on the detectors

KEK Double-sided Module Details

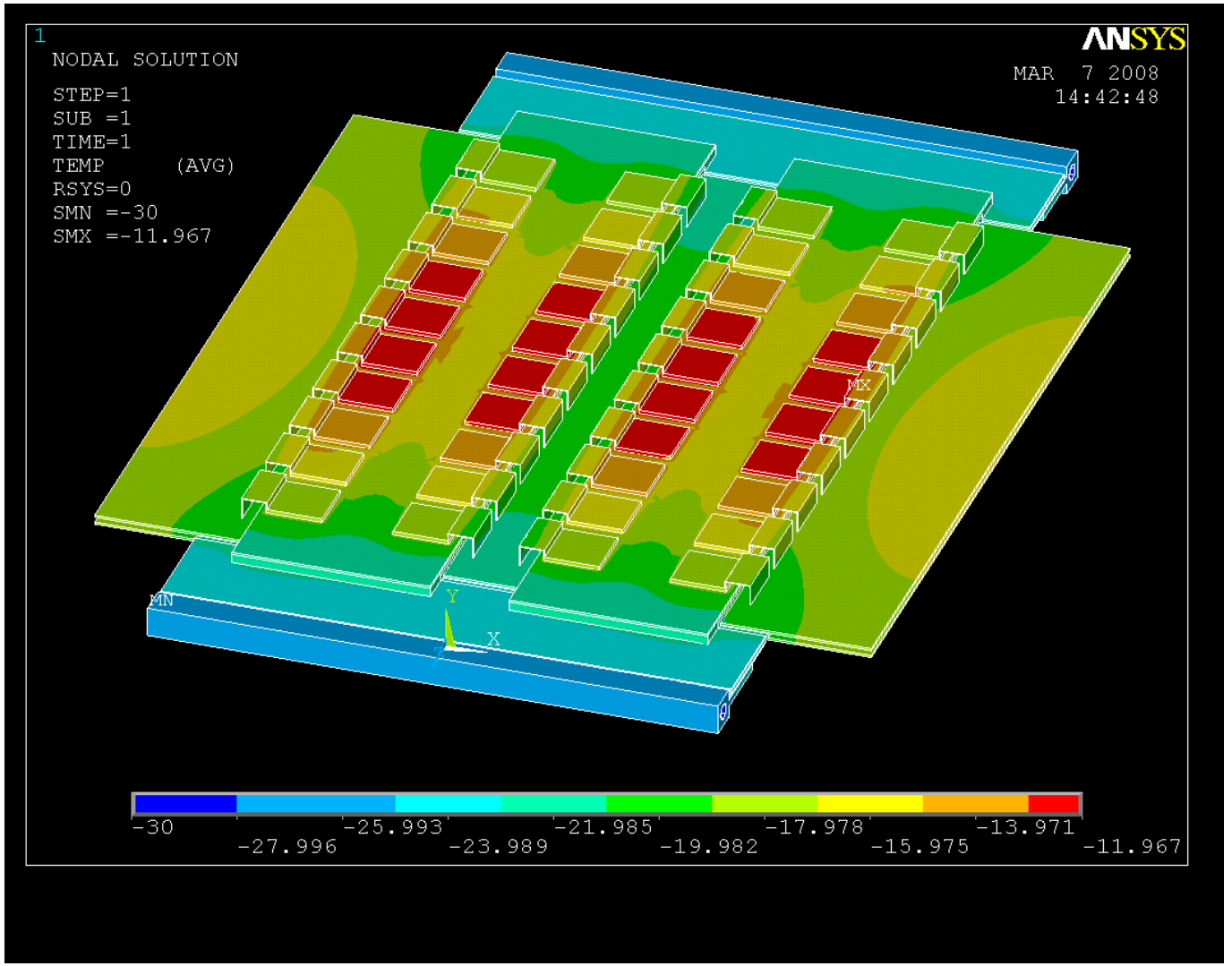
- Chip size 0.3mm x 7.5mm x 7.2mm
- Width of Hybrid 25mm

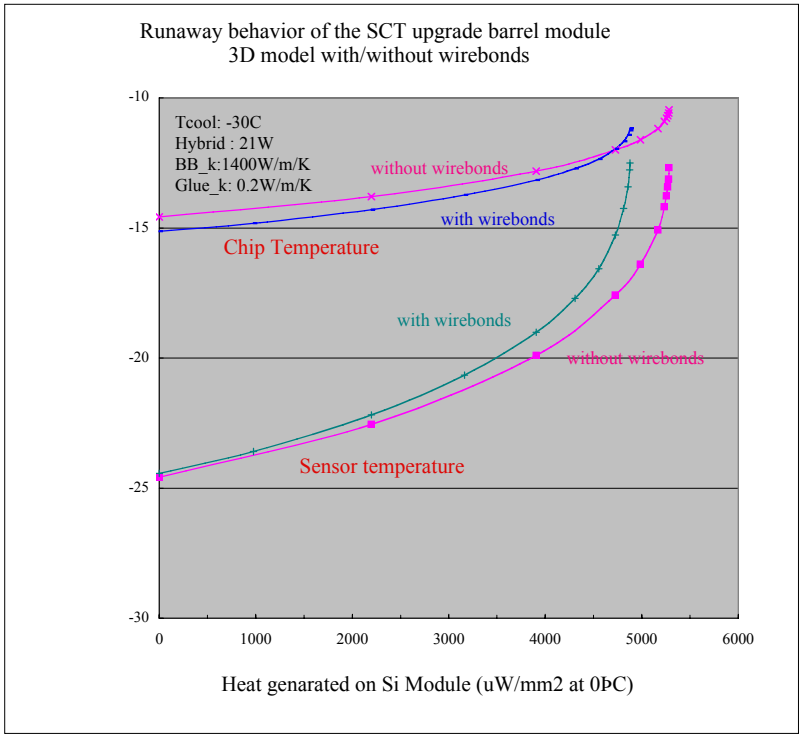
Y. Unno (KEK)

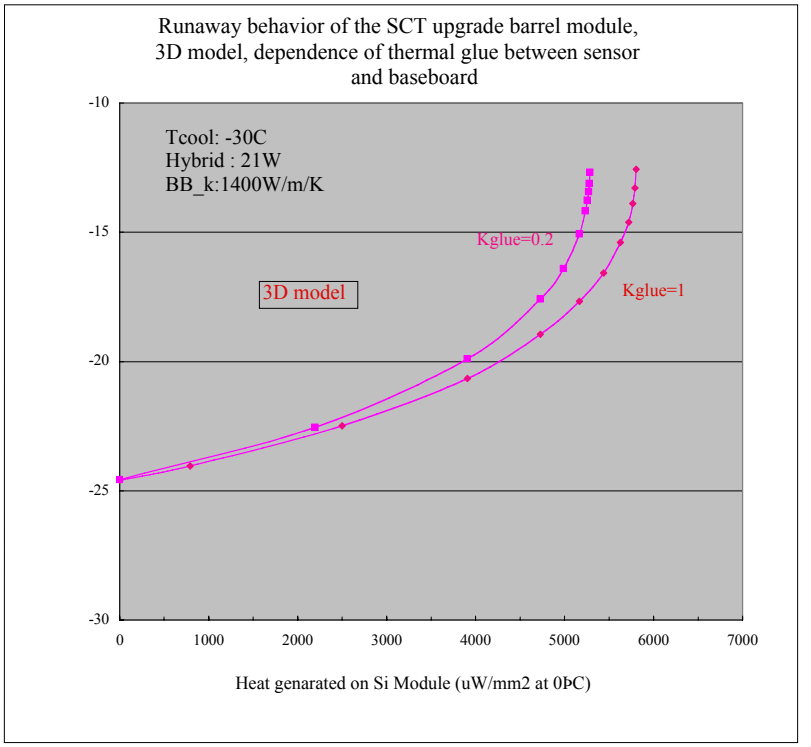


KEK FEA Thermal Analysis

3D model with wire-bonds

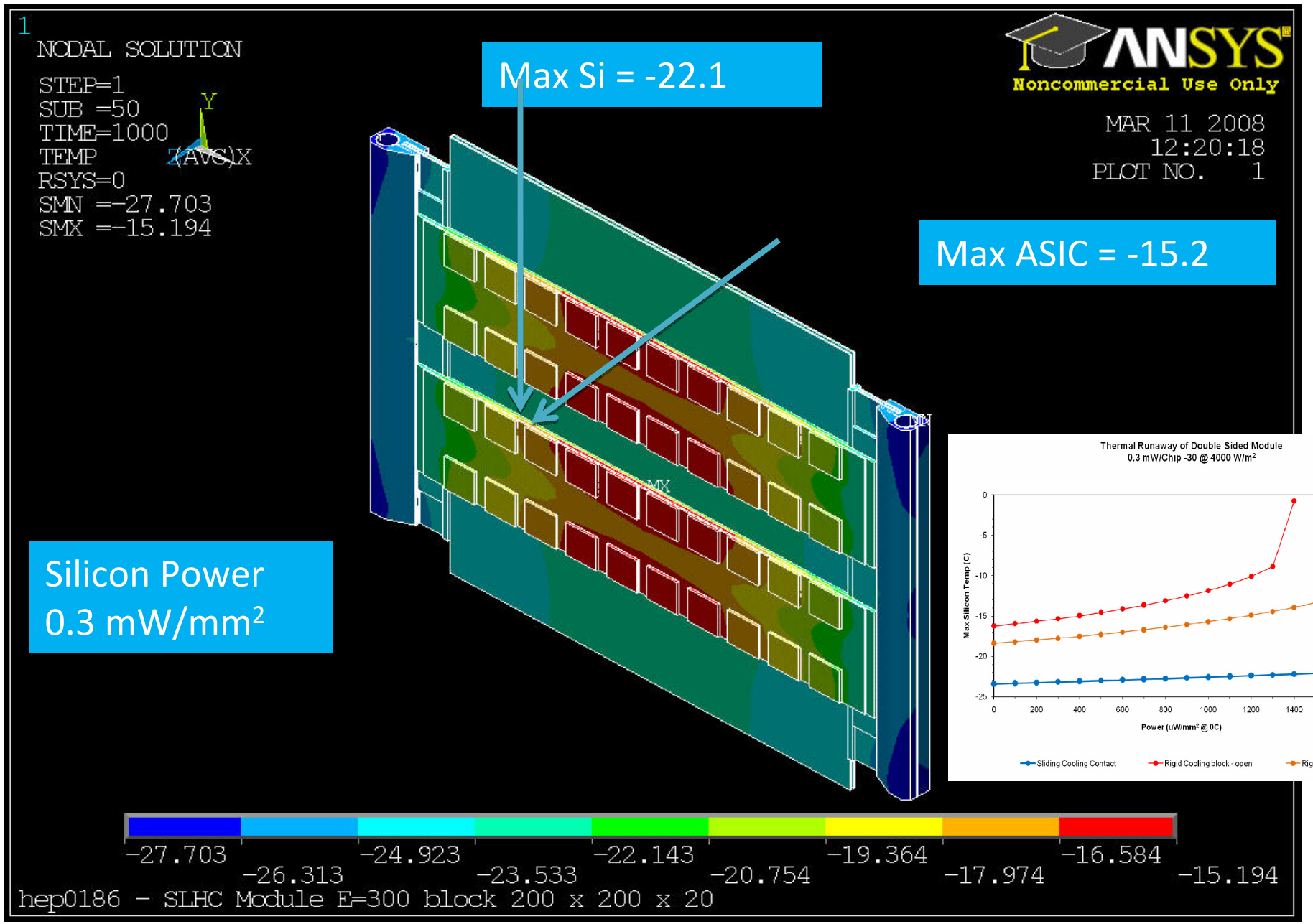




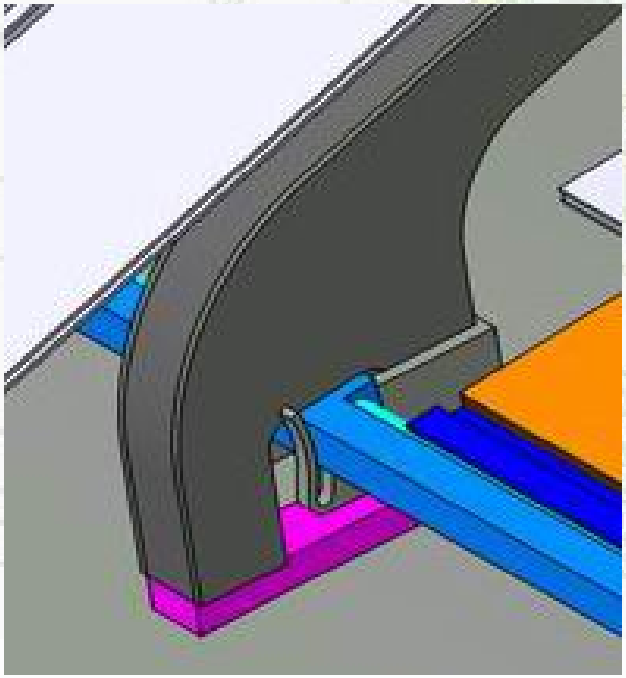


Geneva/Liverpool FEA Thermal Analysis

(Includes coolant to tube wall heat transfer effects)

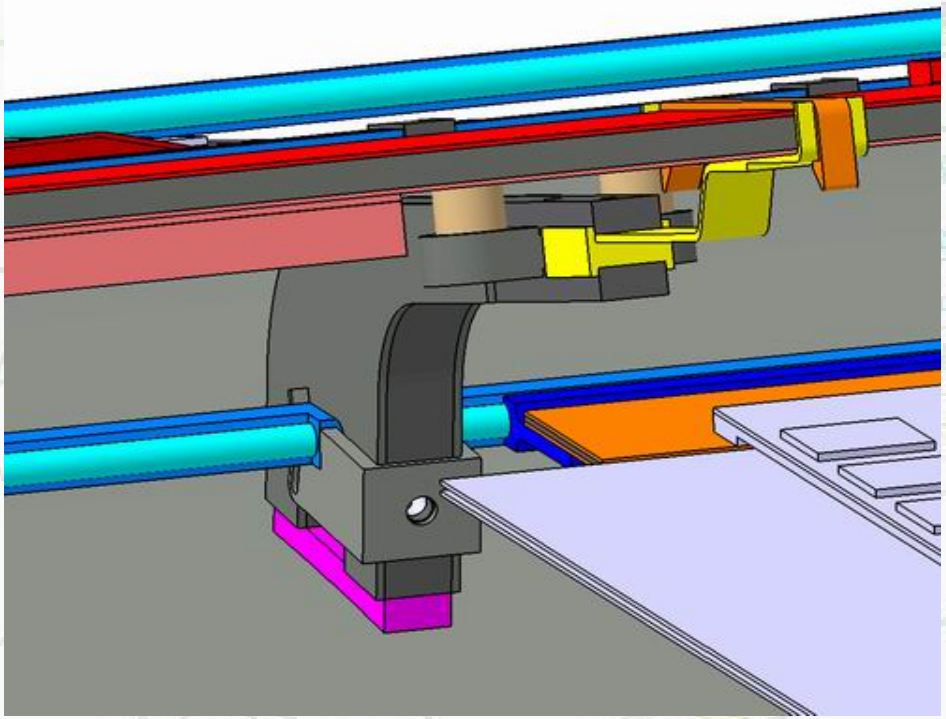


Individual Module - Direct Mounting

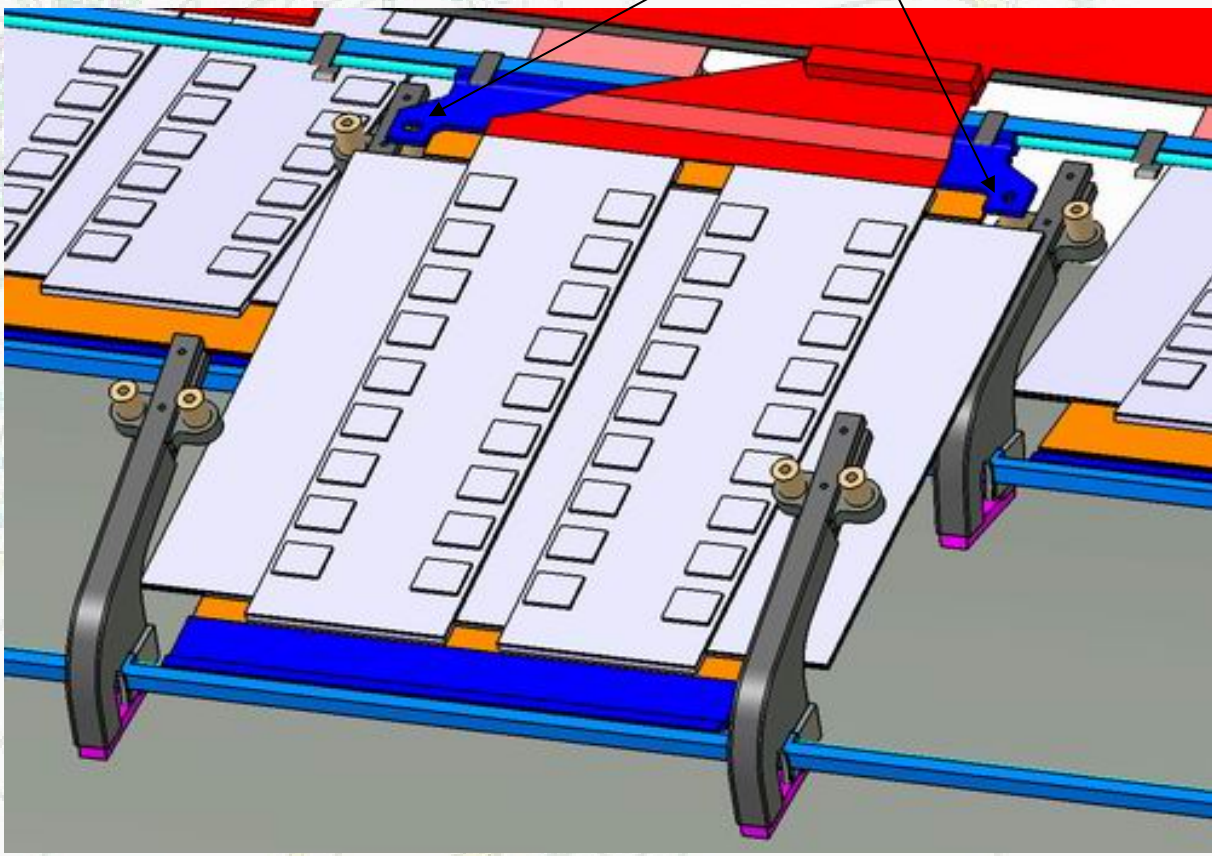


- 3rd “point” is defined by the pipe
- Cooling block is set with 2 fixation points on the pig-tail side
- 1 bracket is holding 2 neighboring modules
- The bottom left pipe is embedded in the brackets and must be assembled before the module.

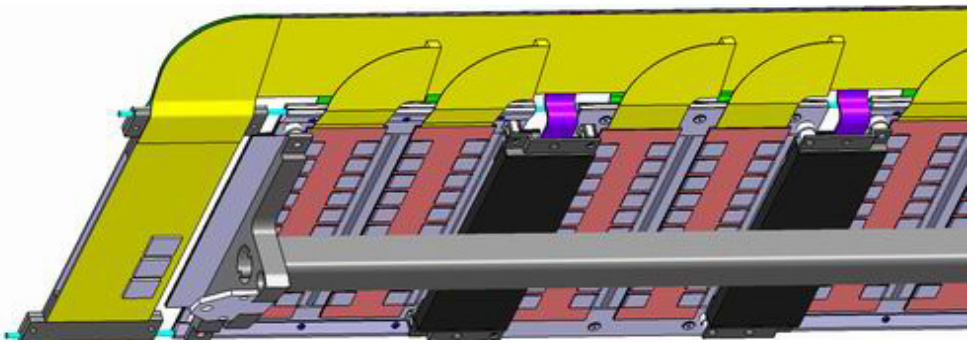
Y. Unno

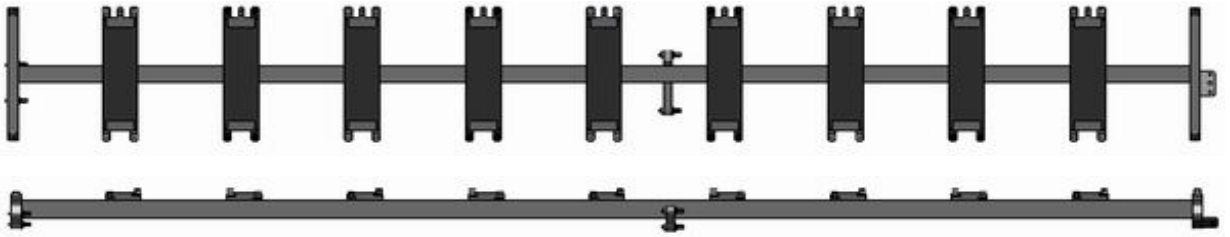


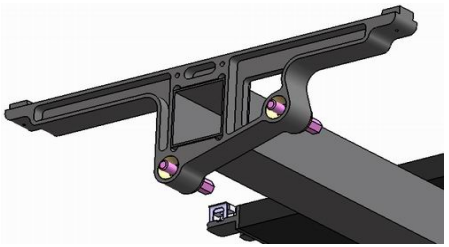
2 fixed mounting points

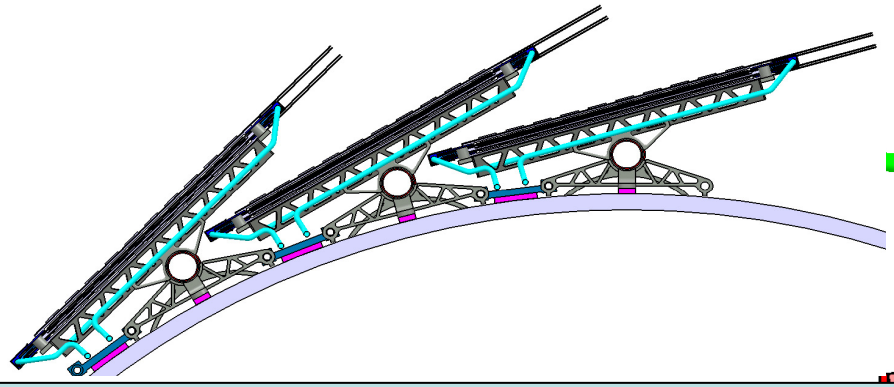


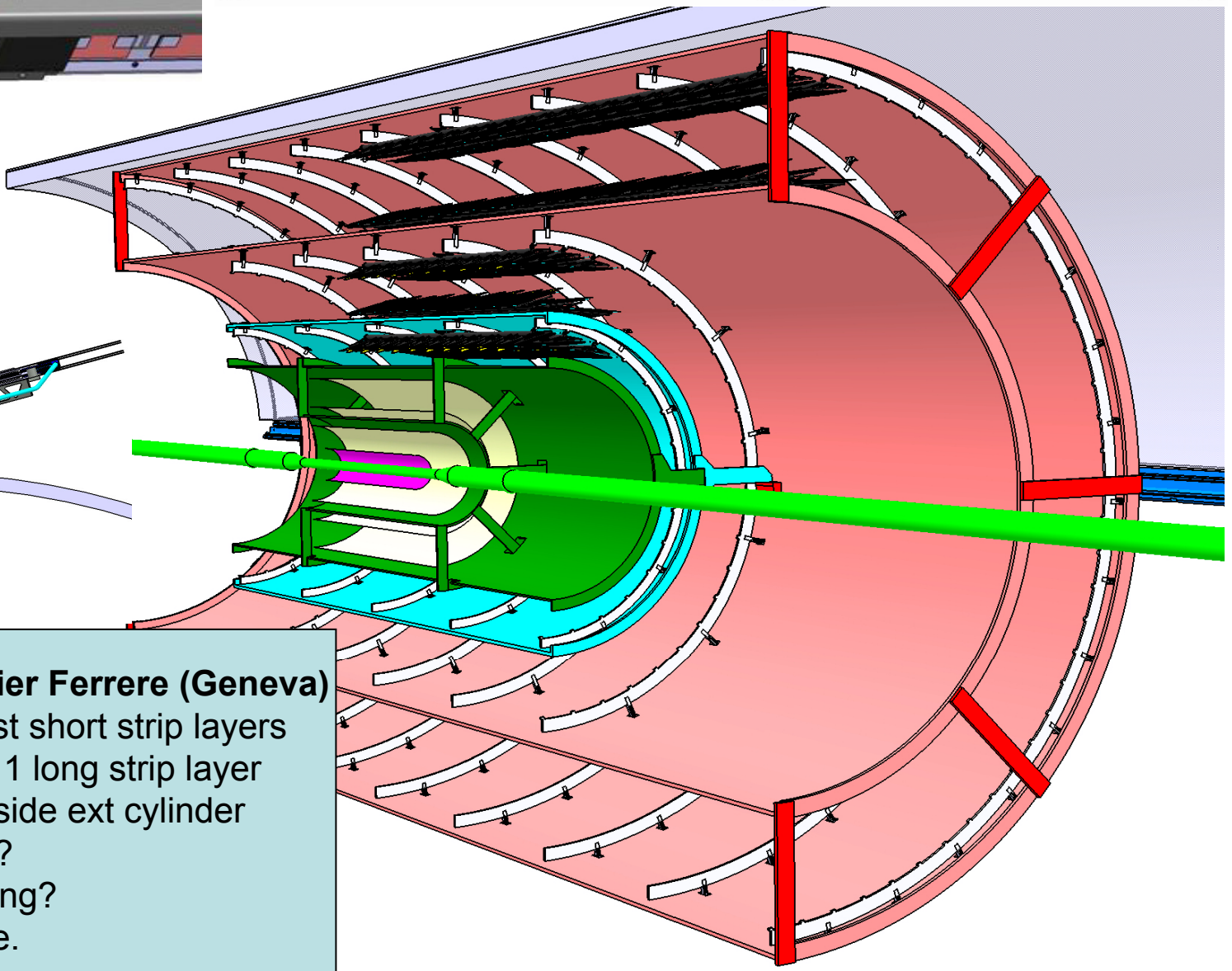
Integrated End-Inserted Bracket Support Structure









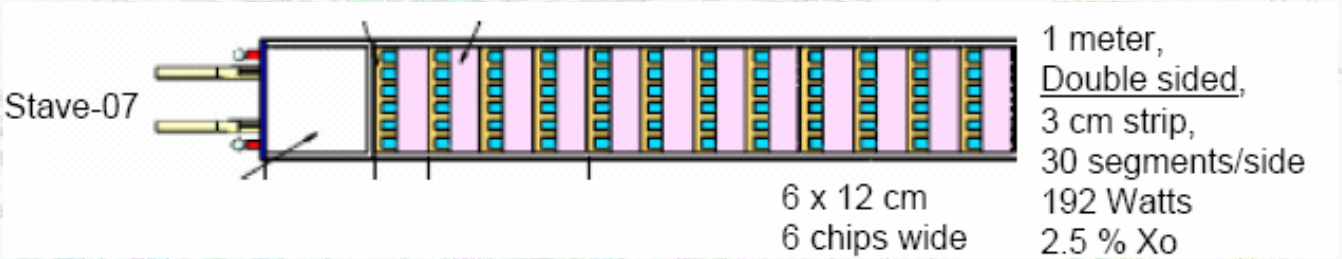


Proposal by Gerard Barbierand Didier Ferrere (Geneva)
Common cylinder for the two innermost short strip layers
Common cylinder for 1 short strip and 1 long strip layer
Outermost long strip layer mounted inside ext cylinder
Outside surface for thermal enclosure?
Space to develop a three point mounting?
Cylinder machining only on the outside.

US Stave Module Concept

- The "stave" concept has hybrids glued to sensors glued to cold support
- A first prototype version based on the CDF run-IIb concept but using ATLAS ASICs already exists

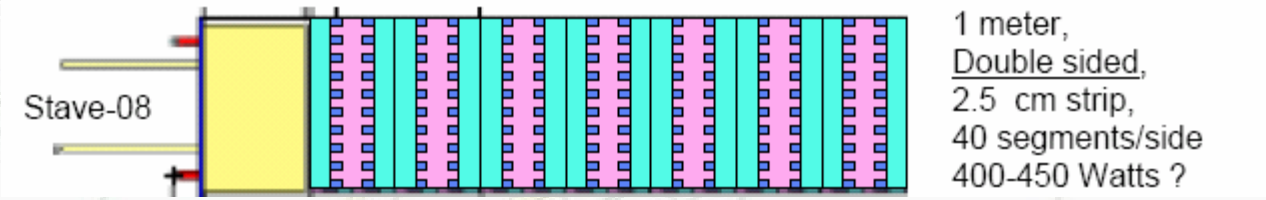
- A 6-chip wide version (Stave 2007) will use short p-in-n sensors and incorporate many of the final proposed, mechanical, thermal, electrical, serial powering and read-out features.



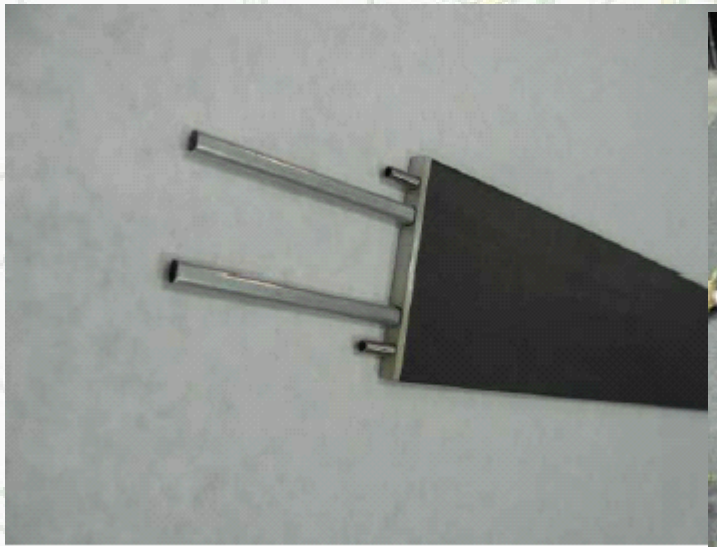
- The first prototype staves are expected by Autumn this year
- Stave core fabrication, BeO hybrid design, cooling concepts and automated assembly nearing completion.

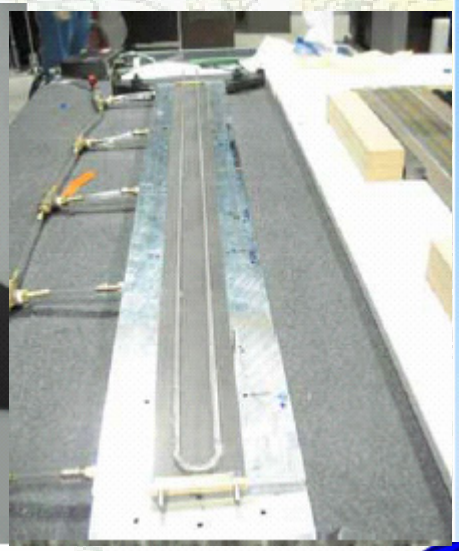
C. Haber (LBL)

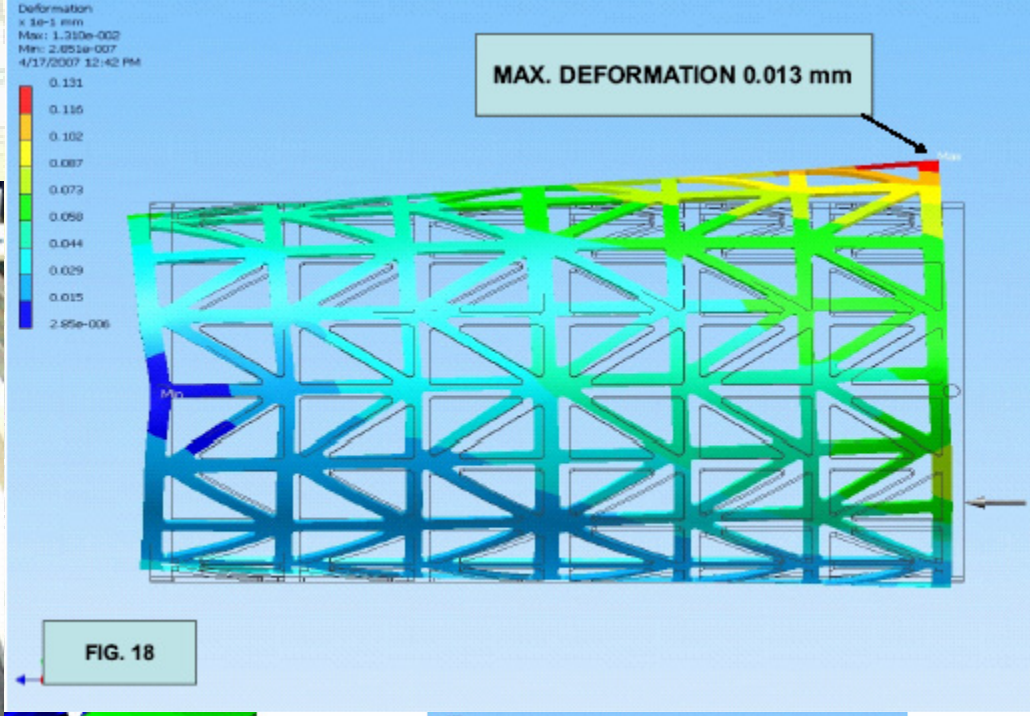
- 10 chip wide version under development

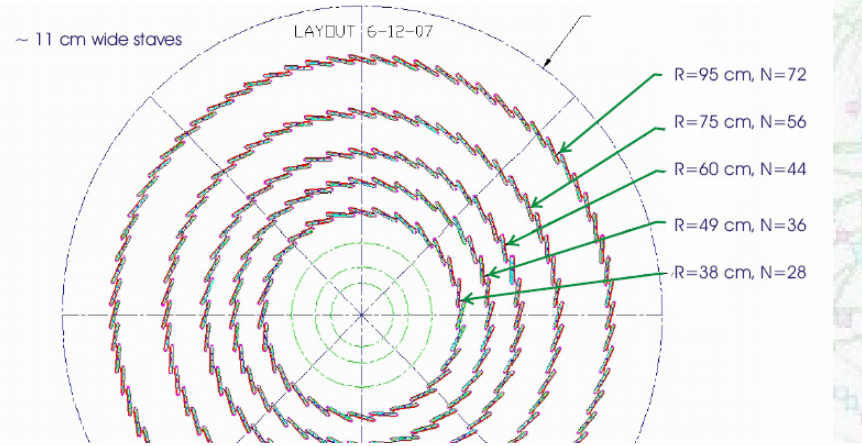


Stave R&D

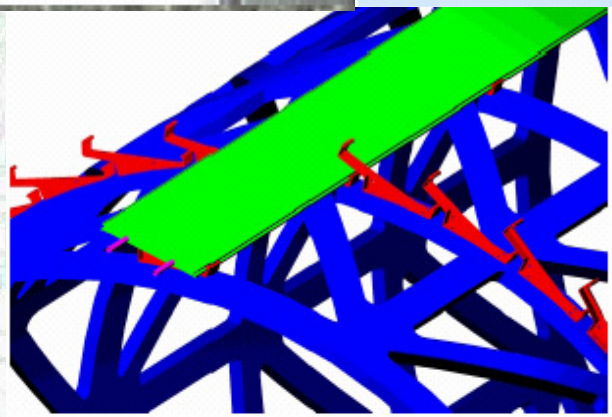


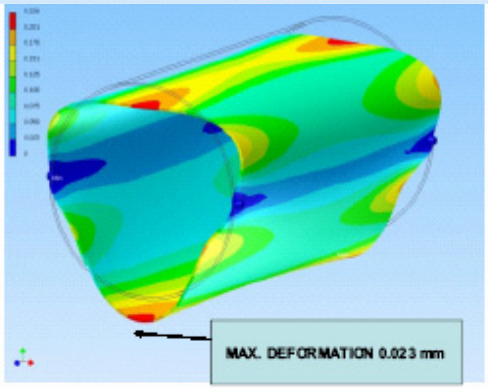


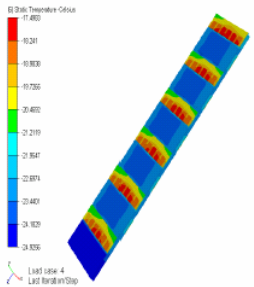


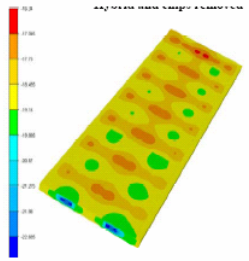


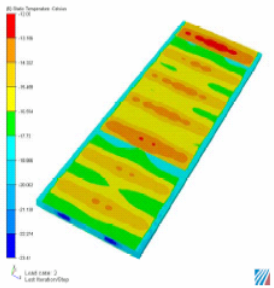
Single sided DS low cable TC DS high cable TC



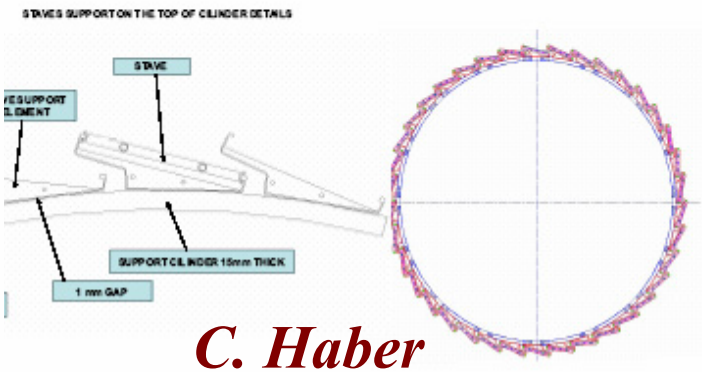


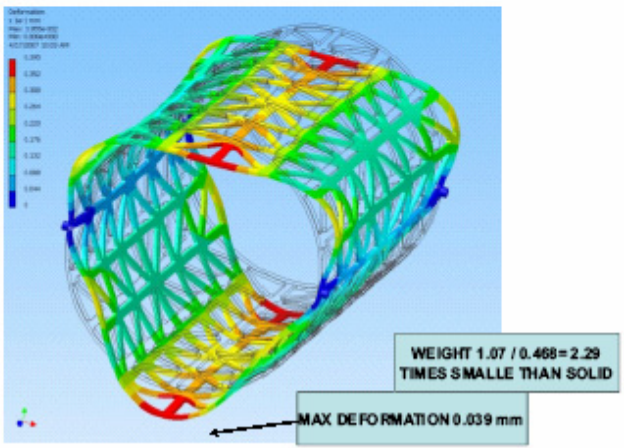






-17.5 C Chip/Silicon -23.5 C -12.6 C Chip/Silicon -13.6 C -16.7 C Chip/Silicon -17.4 C

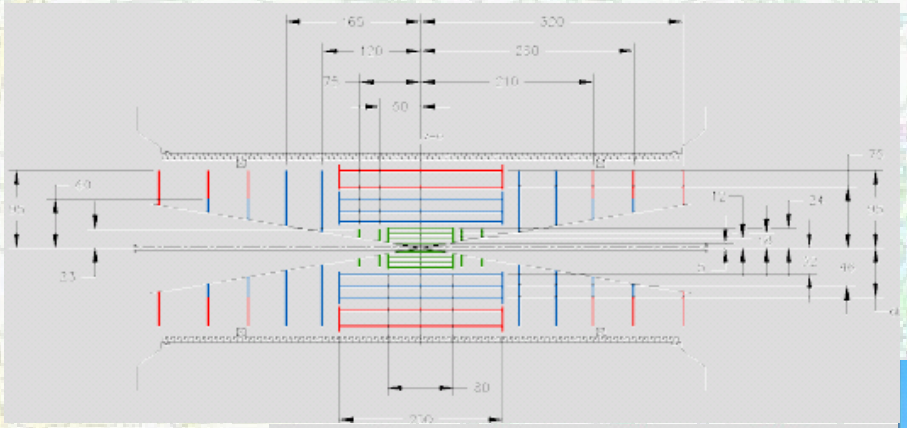




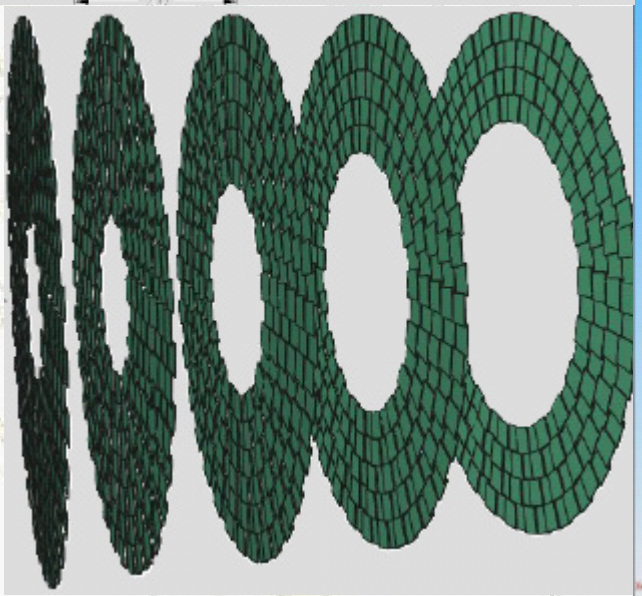
C. Haber

Forward Module Concepts

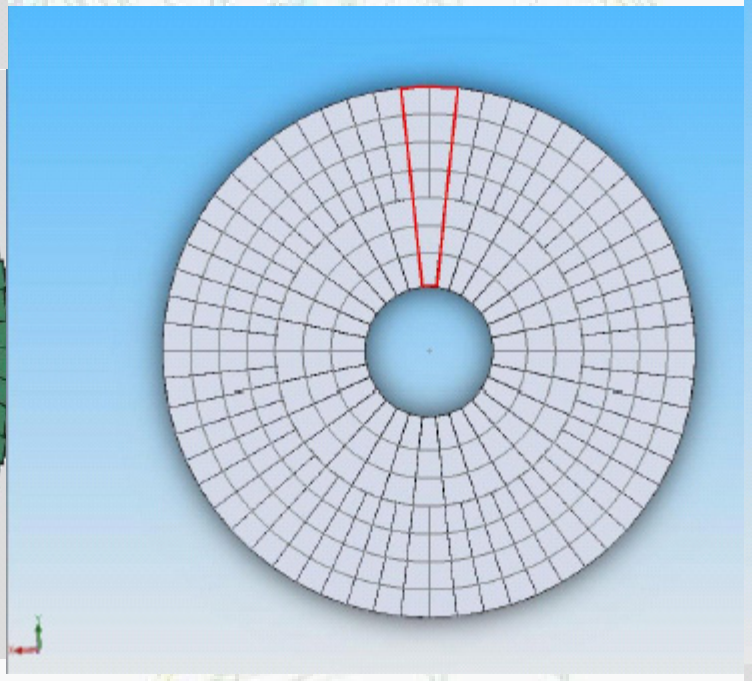
- As for current ATLAS SCT, Forward Modules likely to require several different wedge shaped sensors
- 5 discs on each side with outer radius 95cm and inner radii from 30cm

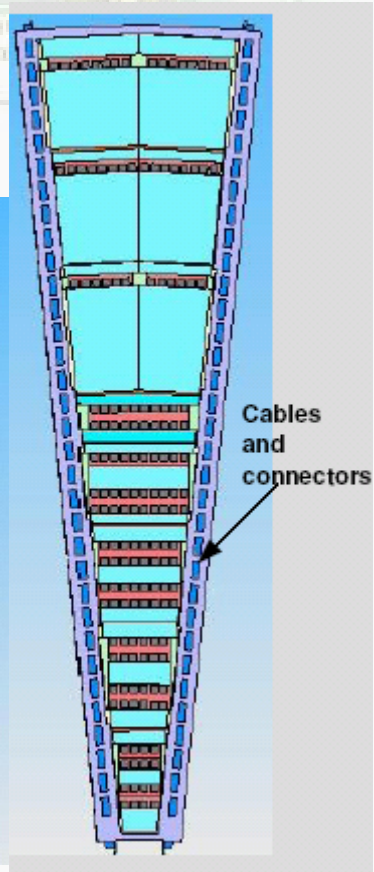


Can consider super-modules/staves or individual modules as now



Mean pitch about 80μm as at present





C. Lacasta (Valencia)

ATLAS Upgrade Plans and 3D Activities in UK

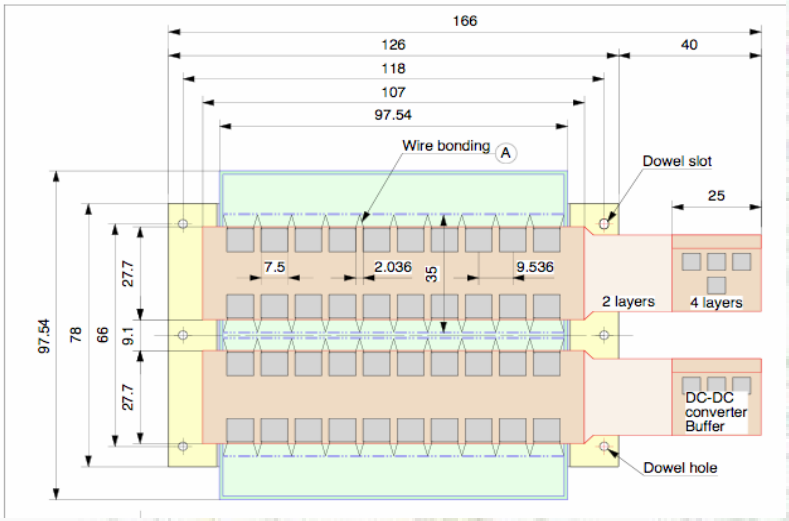
Phil Allport
University of Liverpool

Vertical Integration Technologies for HEP and Imaging Sensors Workshop
Ringberg Castle, Lake Tegernsee
7th April 2008

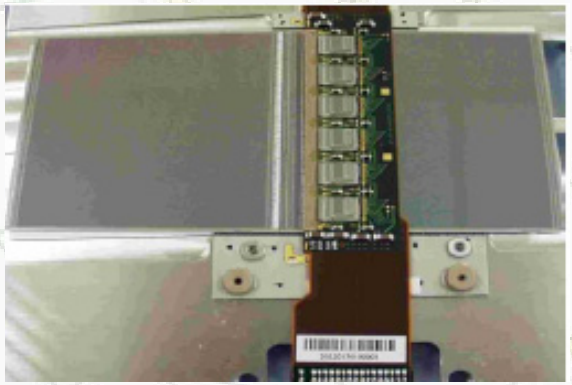
- Proposed Tracker Layout and Simulations (Radiation and Occupancy)
- Sensor and FE Electronics R&D
- Microstrip Module and Engineering Concepts
- **Material Issues and 3D Integration**
- Conclusions

Microstrip Tracker Module Material

New ATLAS SLHC-Tracker Module
(subject to design - indicative numbers)
80 ASIC's, thickness matters
(300μm assumed)



Old ATLAS Barrel Module
12 ASIC's of 300μm thickness



Module Short Strip (Low Radius)	Rad len (%)	Mass (gm)
Silicon sensors w/thermal adhesive	0.69	14.35
Baseboard w/AlN facings	0.30	10.40
ASIC's w/conductive adhesive and w-bonds	0.19	4.08
Hybrid w/passive compo's	0.77	25.26
Hybrid-facing thermal adhesive	0.00	0.11
Total	1.95	54

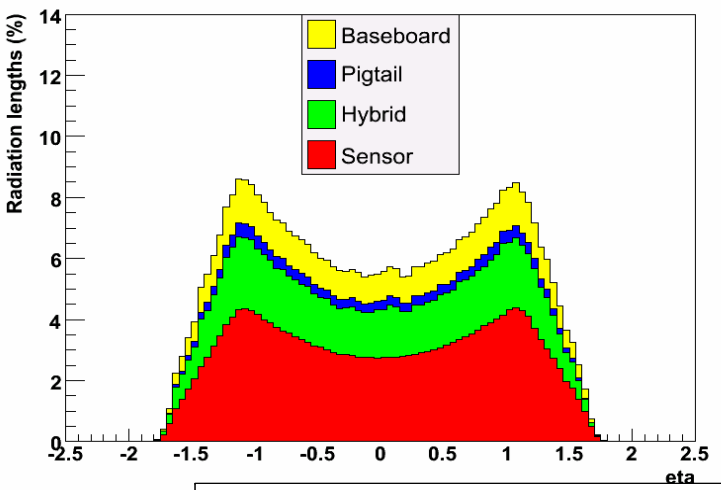
Module Long Strip (High Radius)	Rad len (%)	Mass (gm)
Silicon sensors w/thermal adhesive	0.69	14.35
Baseboard w/AlN facings	0.20	6.71
ASIC's w/conductive adhesive and w-bonds	0.05	1.02
Hybrid w/passive compo's	0.31	10.10
Hybrid-facing thermal adhesive	0.00	0.05
Total	1.24	32

Table 1
Radiation lengths and weights estimated for the SCT barrel module

Component	Radiation length [%Xo]	Weight [gr]	Fraction [%]
Silicon sensors and adhesives	0.612	10.9	44
Baseboard and BeO facings	0.194	6.7	27
ASIC's and adhesives	0.063	1.0	4
Cu/Polyimide/CC hybrid	0.221	4.7	19
Surface mount components	0.076	1.6	6
Total	1.17	24.9	100

Overall Impact of Hybrid Material

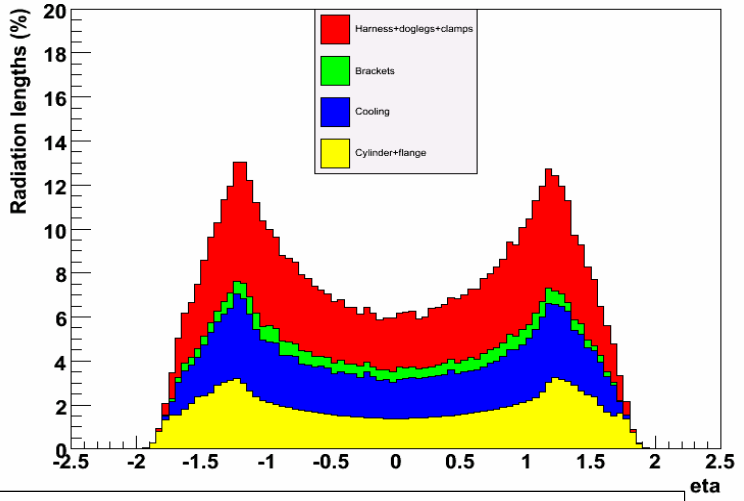
(P Ward, A. Tricoli)

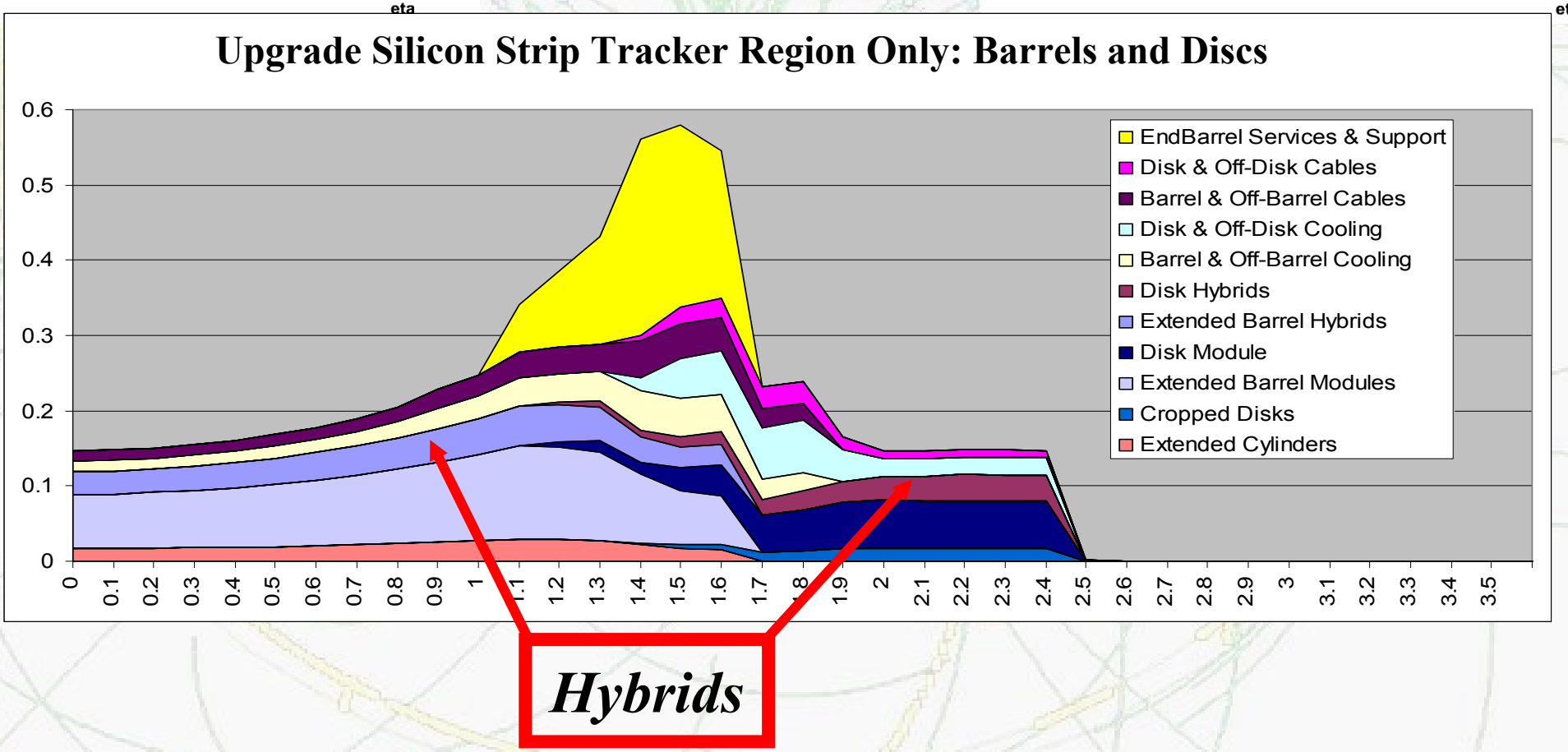


Current Silicon Tracker
(4 barrel strip layers)

Module Material

Support Material



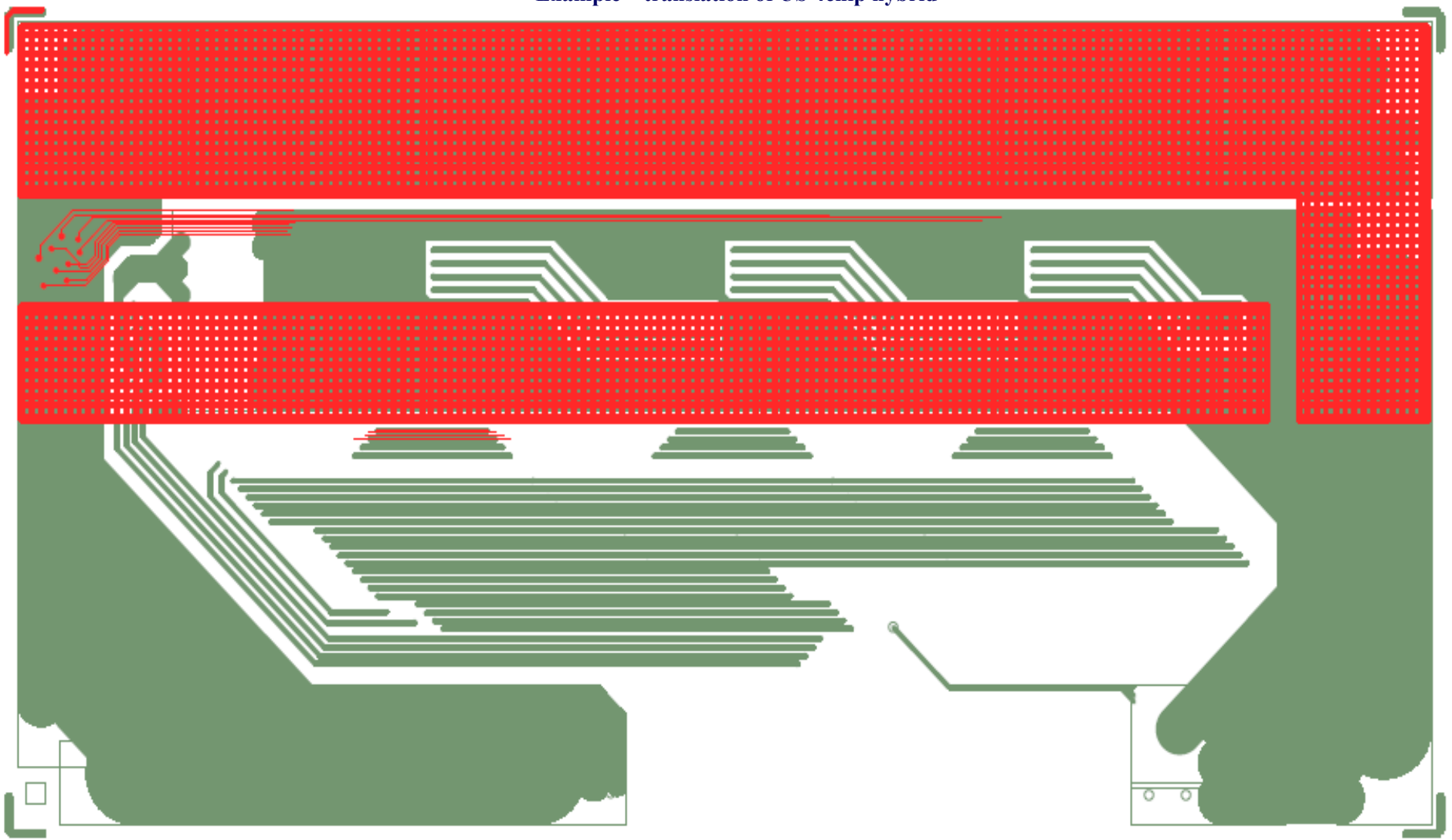


3D Programme for Short Strip Arrays

- **RD program to explore use of thin film processing on silicon**
- **Goal is to use thin film technology to reduce the hybrid area and material**
  - **For short strips (25mm), the hybrid is 35-50% of the material**
    - **Replacing conventional Kapton + heat spreaders by thin film**
      - ✓ **Potentially reduces the hybrid surface area by factor 2**
      - ✓ **Potentially reduces the hybrid material by factor of 2-4**
- **Technical program**
  - **i: Produce Silicon hybrid or MCMD (Interposer) – reduce area by x2**
  - **ii: Direct post processing on silicon sensor – reduce area & thickness**
  - **iii: Connectors for Kapton**
  - **iv: Replace wire-bonding with flip-chip (2nd phase)**

Implementation: Prototype Mask Design

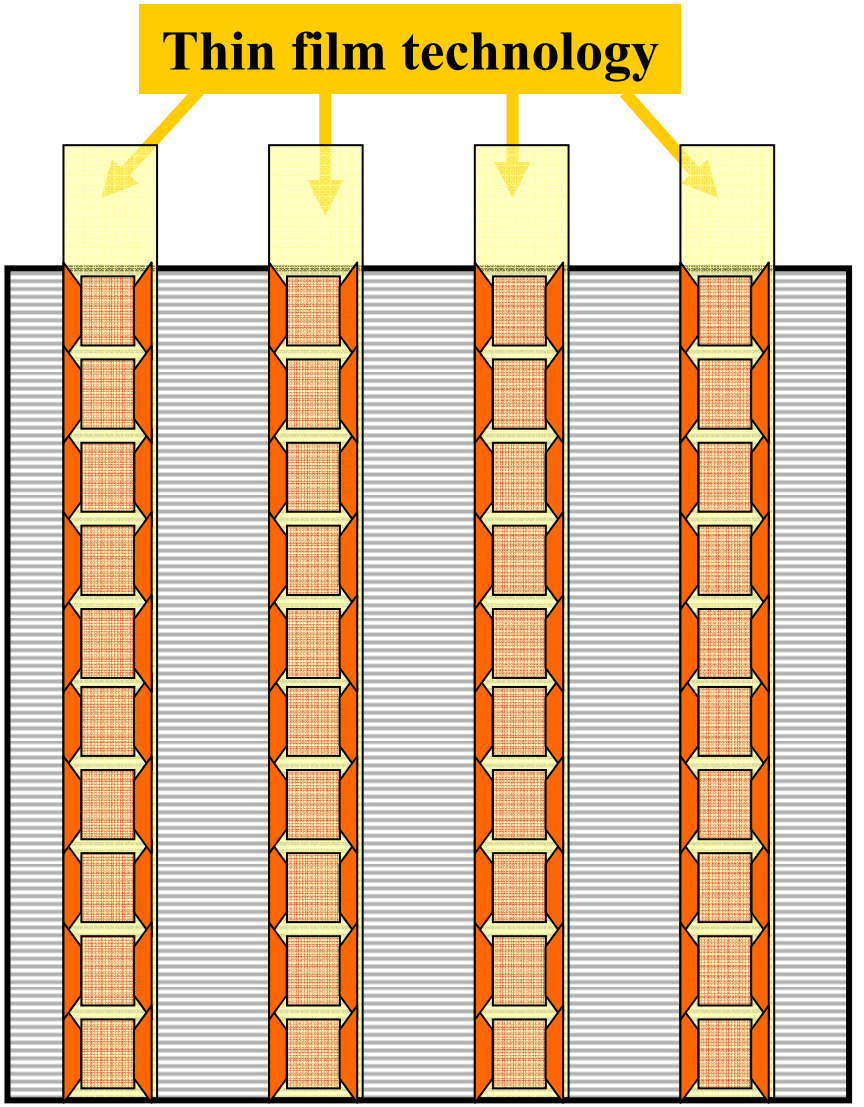
Example – translation of US 4chip hybrid



(i) Silicon Hybrid (Interposer)

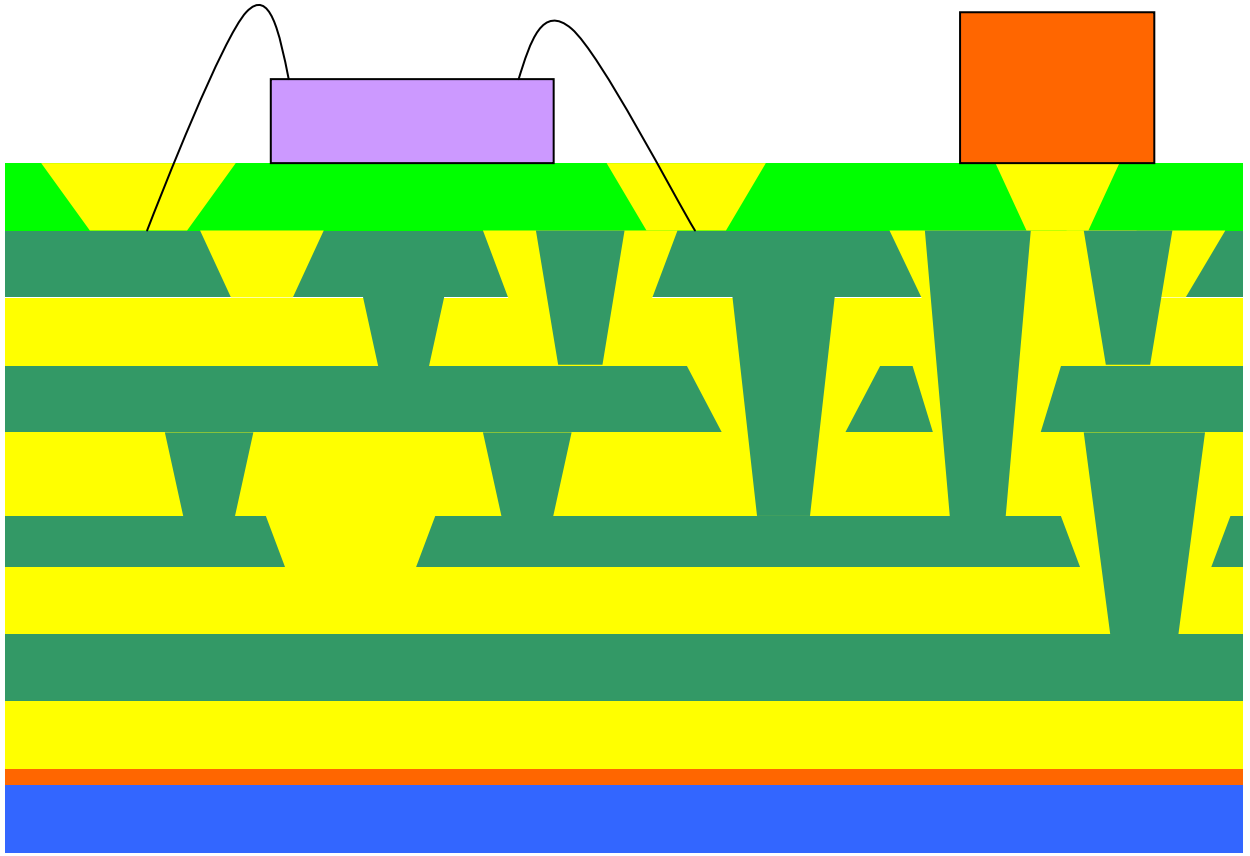
- Geometry & layer thickness of thin-film MCMs require changes in design.

- Issues are:
  - Transmission line impedance (impedances are lower in thin-film; pixel group achieved 50 Ωs rather than the usual ~70 Ωs with low cross talk)
  - Capacitances. Large capacitances because of thin dielectric help with decoupling
  - Area and thickness of power and ground planes
  - High voltage routing and decoupling for detector bias



Status – Will follow after ABCn Hybrid & technology development (2009)

(ii) Direct Processing on Silicon Sensor



SMD Solder (FC4b)

Wirebond + fanin Au (FC4a)

3rd dielectric BCB (FD3) / via fill (FV3)

Gnd/trace2 Cu (FC3)

2nd dielectric BCB (FD2) / via fill (FV2)

Power/trace1 Cu (FC2)

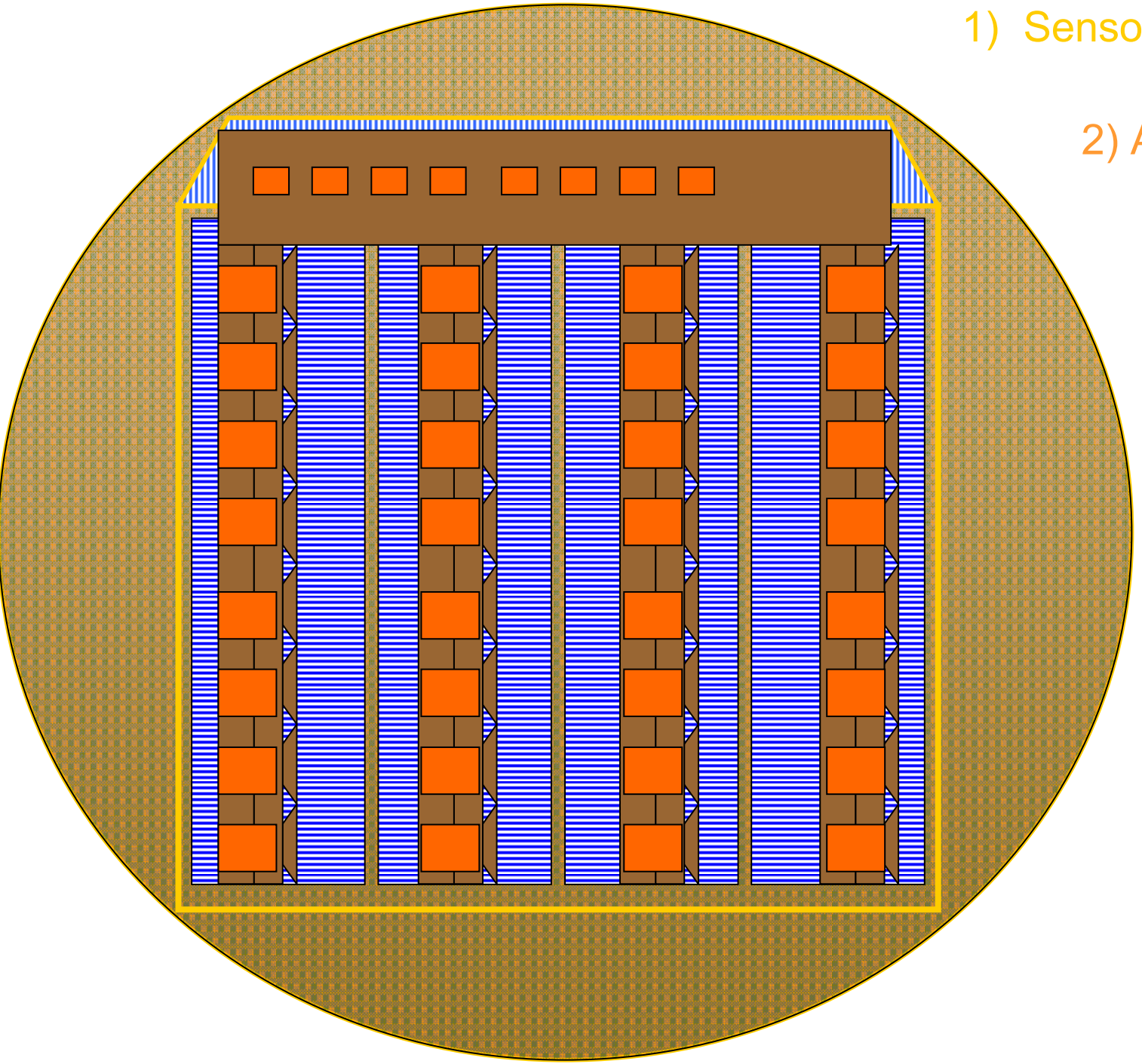
1st dielectric BCB (FD1) / via fill (FV1)

Shield layer Cu (FC1)

BCB (Benzocyclobutene) 5–15μm

Si base

Status – Will start May 2008 with Acreo AB (Sweden)



1) Sensor wafer

2) Add dielectric and open vias

3)Add metal layers and pattern

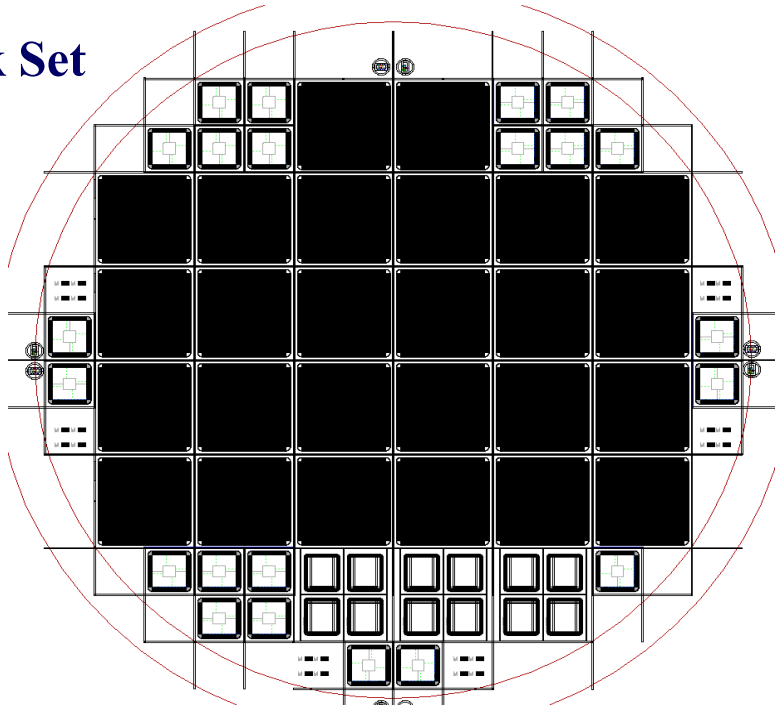
4) Repeat for required number of layers and dice wafer

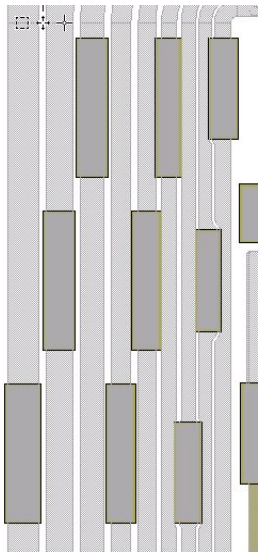
5) Wire-bond
or
Flip-chip ASICs

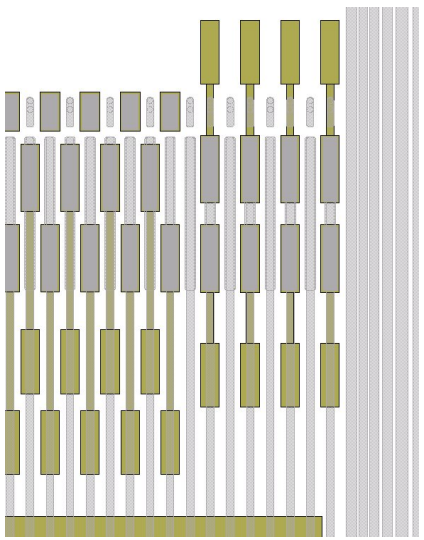
First Phase – Test Circuits Using Micron RD50 Wavers

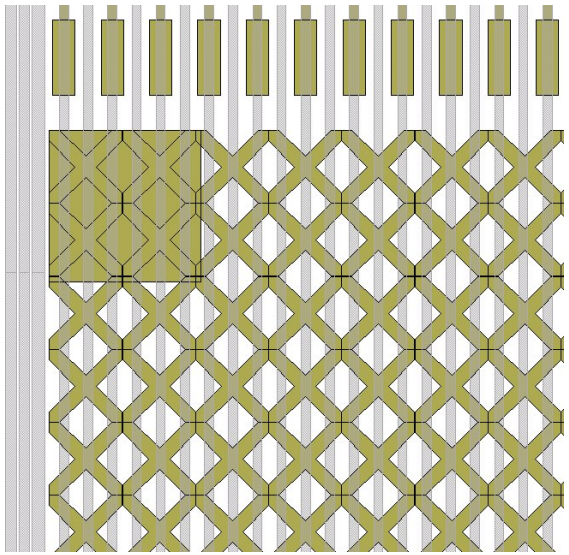
- **Test principle with 1BCB layer and 1 patterned Cu layer:**
  - **Yield**
  - **Defects**
  - **Connectivity (Cu to Al)**
  - **Fine pitch Lithography (50μm)**
  - **Capacitance**
  - **Mechanical stresses & deformation**
  - **….**

RD50 Mask Set





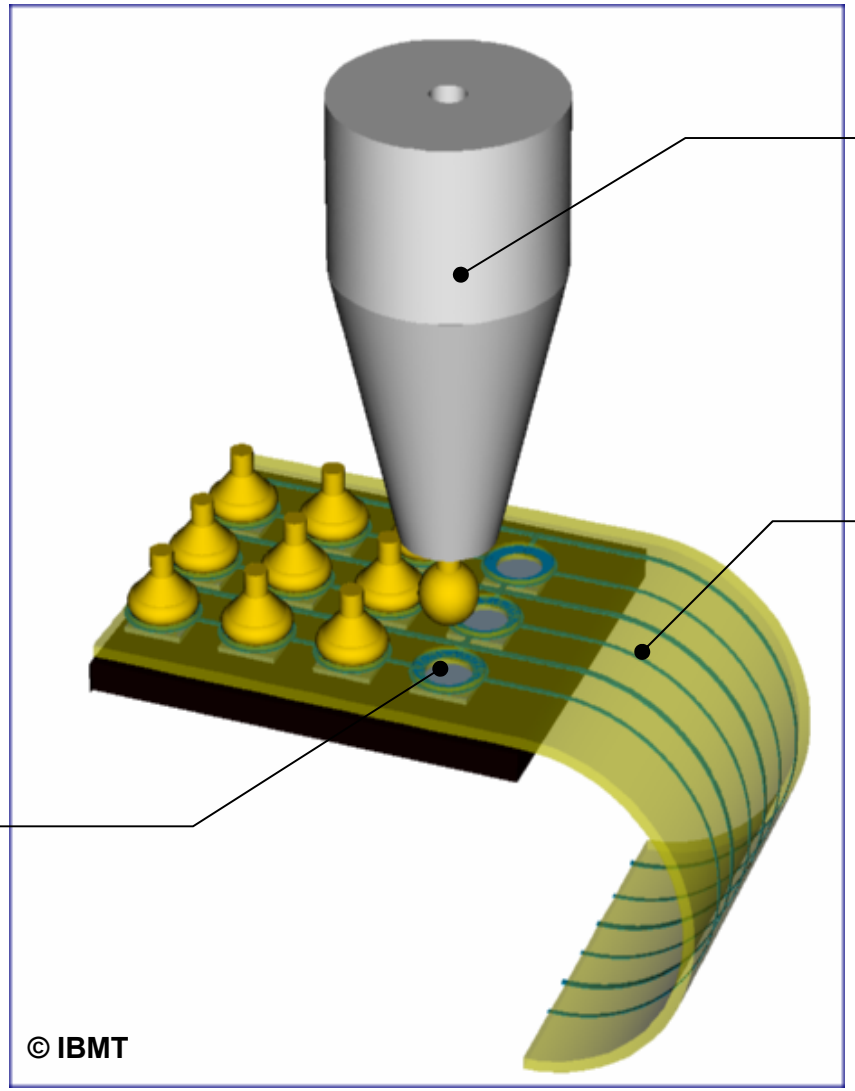




(iii) Connectors for Flex Circuits to Silicon

Upgrade PO

Stieglitz, T. , Beutel, H., Meyer, J.-U.: 'Microflex - A New Assembling Technique for Interconnects'. Journal of Intelligent Material Systems and Structures, 11 (6), pp. 417-426 (2000).



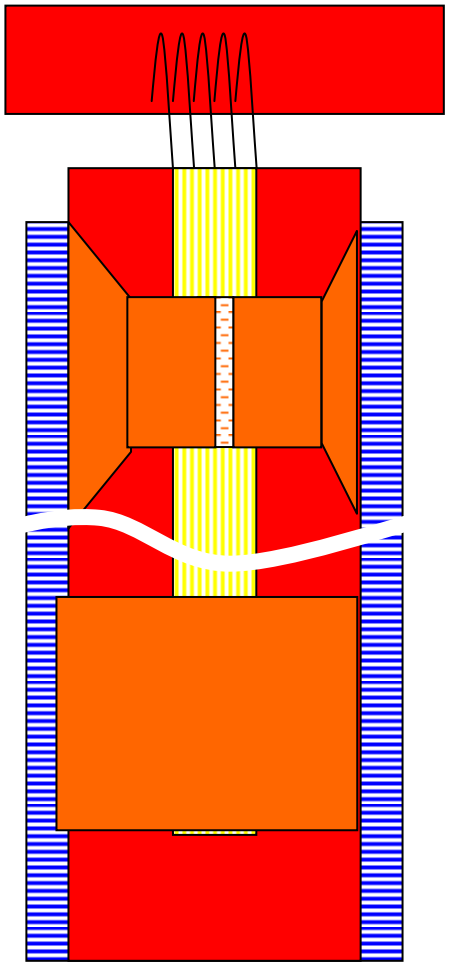
IEEE Trans. on Components, Packaging and Manufacturing Technology-Part B: Advanced Packaging (IEEE Trans. on Advanced Packaging), vol. 24 , no. 3, pp. 366-374 (2001).

Status – Will start April 2008 in-house at RAL

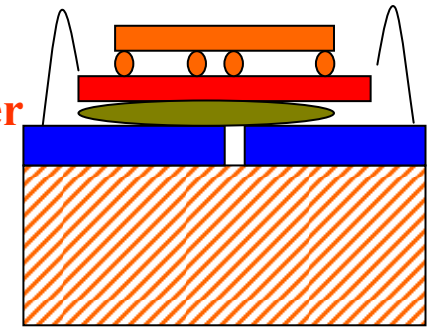
(iv) The Long-term Vision – :Larger ASICS & Flip-chip

Wire bonding to integrated Fan-in

Flip chip



ASIC
Flip chip
Silicon interposer
Strips
Silicon sensor

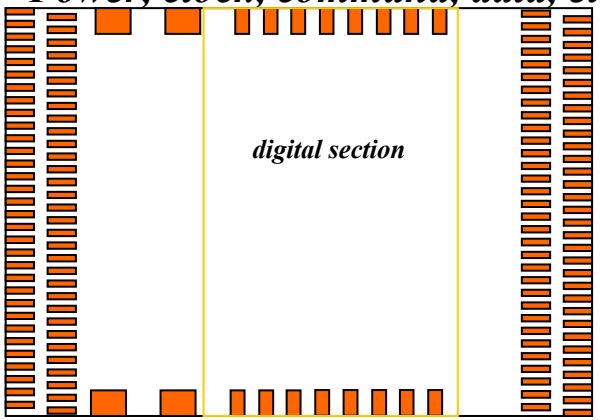


ABC-N 256Ch (WB)

Amplifier pitch : 50 μm

Wire-bonding pitch: 80 μm

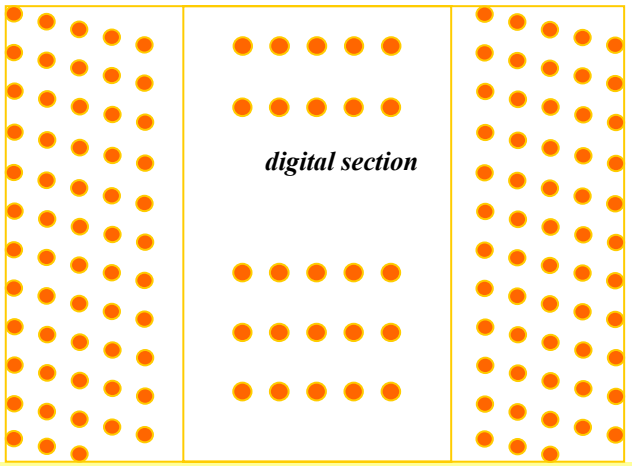
Power, clock, command, data, etc.



ABC-N 256Ch (FC)

Amplifier pitch: 50 μm

Bonding pitch: 300 μm



ATLAS Upgrade Plans and 3D Activities in UK

Phil Allport
University of Liverpool

Vertical Integration Technologies for HEP and Imaging Sensors Workshop
Ringberg Castle, Lake Tegernsee
7th April 2008

- Proposed Tracker Layout and Simulations (Radiation and Occupancy)
- Sensor and FE Electronics R&D
- Microstrip Module and Engineering Concepts
- Material Issues and 3D Integration
- **Conclusions**

Conclusions

- Activities in many areas getting underway but emphasis remains on completion and commissioning of current ATLAS Detector
- Management structure includes Upgrade Steering Group, Upgrade Project Office and 8 working groups in the area of the tracker replacement alone
- Major recent tracker workshops include: Genoa (18/7/05 - 20/8/05), Liverpool (6/12/07- 8/12/07) and Valencia (10/12/07- 12/12/07)
- Some impressive progress, but still plenty to do and not so much time to do it …

  ATLAS Inner Detector Technical Design Report now 10 years old
  http://atlas.web.cern.ch/Atlas/GROUPS/INNER_DETECTOR/TDR/tdr.html
- Material reduction key to achieving desired tracker performance
- For more presentations from past internal meetings see ATLAS *indico* pages *http://indico.cern.ch/categoryDisplay.py?categId=350*

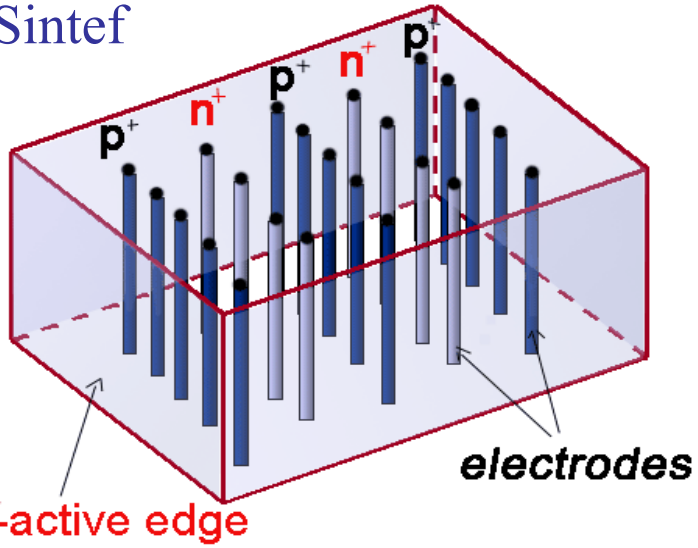
Back-up Slides

3D silicon sensors

Charge collection distance reduced → reduced charge trapping

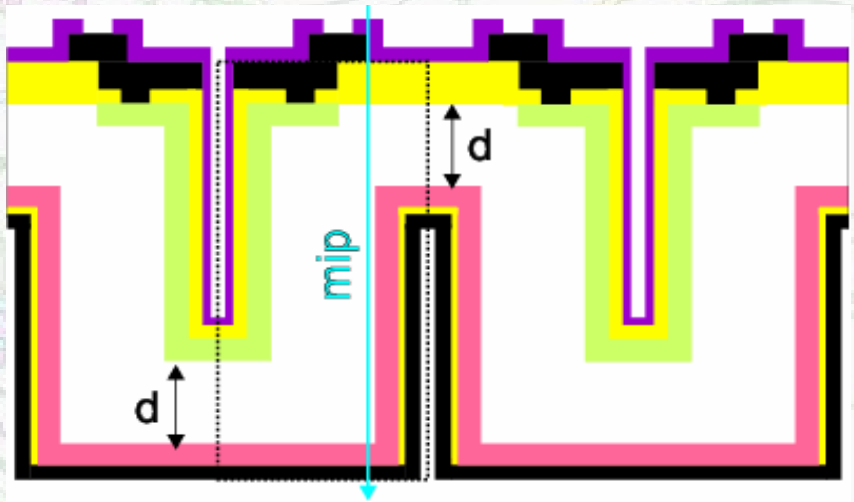
Stanford/Sintef
ICEMos

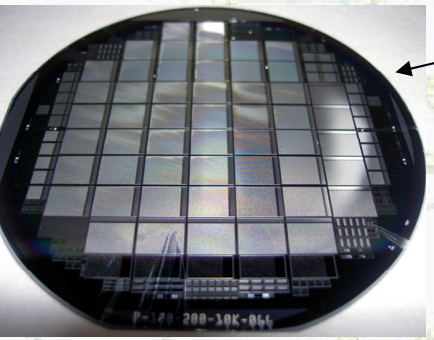
Glasgow



Alternative geometry with double sided electrodes

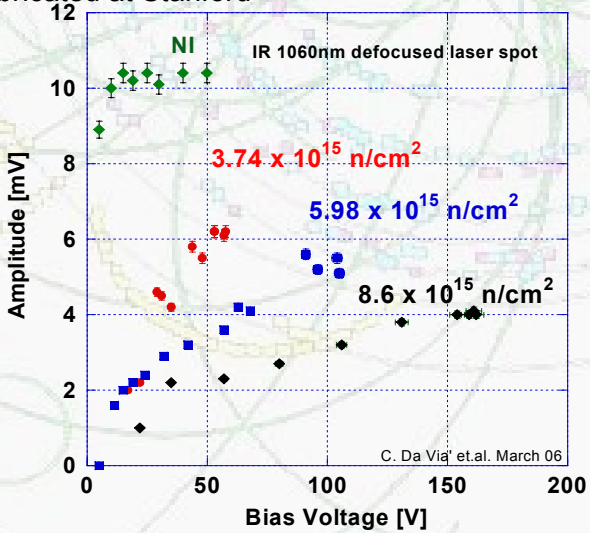
IRST
CNM



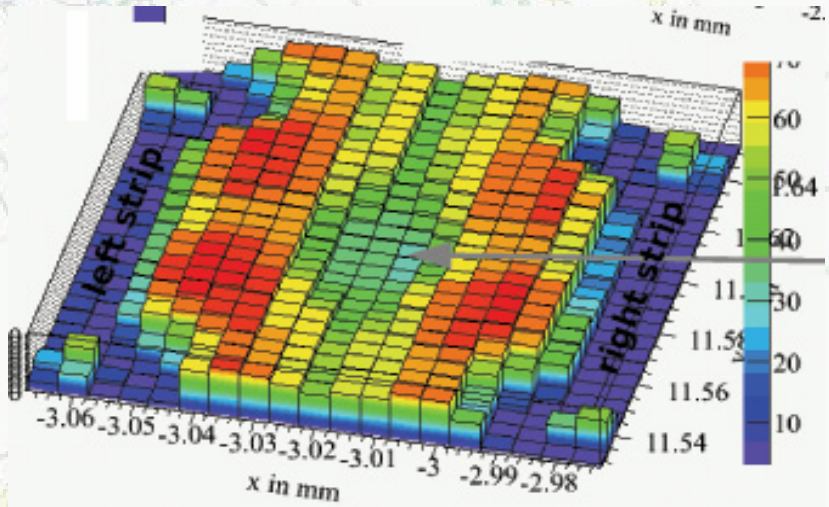


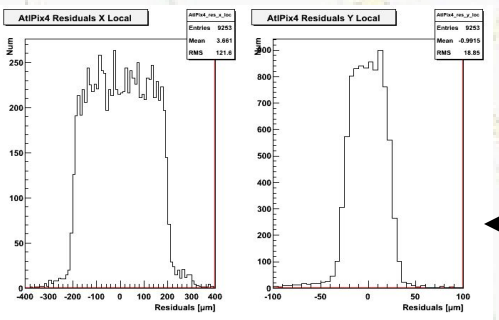
ATLAS pixel fabricated at Stanford

Radiation tests/Praha
CCE(V) with laser



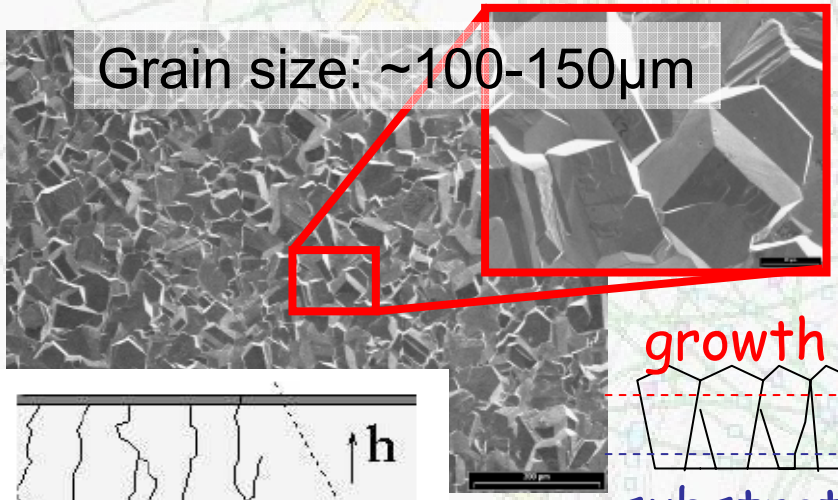
IR scan 3D- SCstrips/ Freiburg

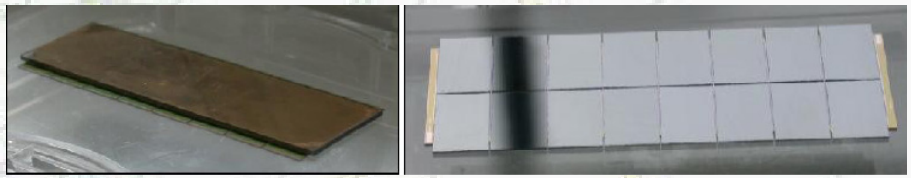




Test beam/data analysis from M. Mathes-Bonn

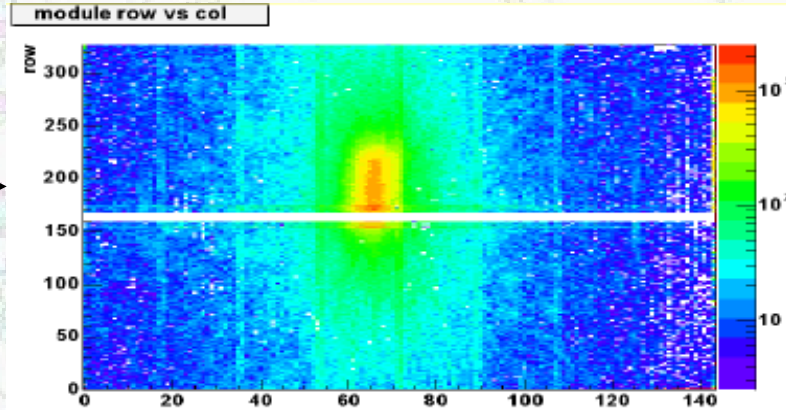
pCVD Diamond



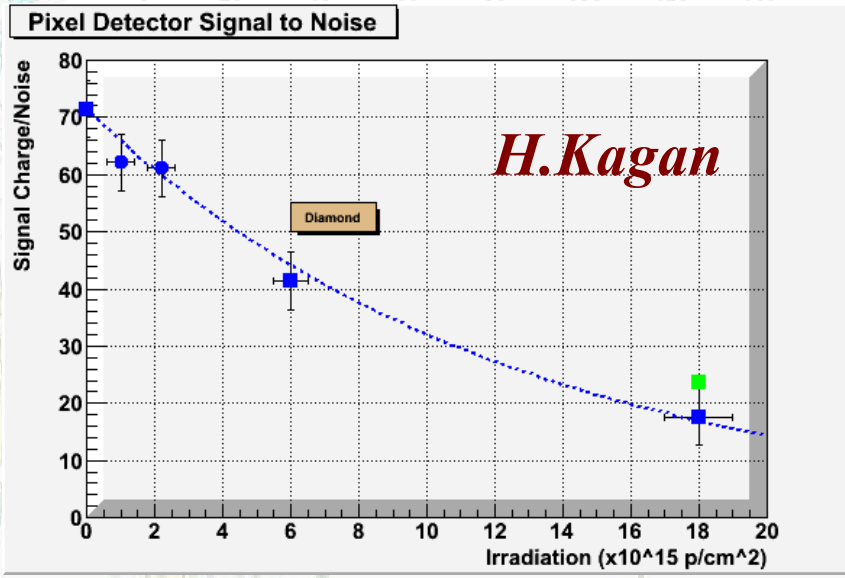


ATLAS pixel module

hitmap



- large band gap and strong atomic bonds promise fantastic radiation hardness
- **low leakage current and low capacitance both give low noise**
- 3 (1.5) times better mobility and 2x better saturation velocity give fast signal collection
- **Ionization energy is high: MIP≈ 2x less signal for same X_0 of SI**
  - –Diamond: ~13.9ke$^-$ in 361 μm (140 enc; bare threshold ~1500e)
  - –SI: ~22.5 ke$^-$ in 282 μm
- Grain-boundaries, dislocations, and defects can influence carrier lifetime, mobility, charge collection distance and position resolution
- Available Size ~2 x 6 cm^2 (12cm diameter wafer; ~2mm thick)



Some Compilation Plots

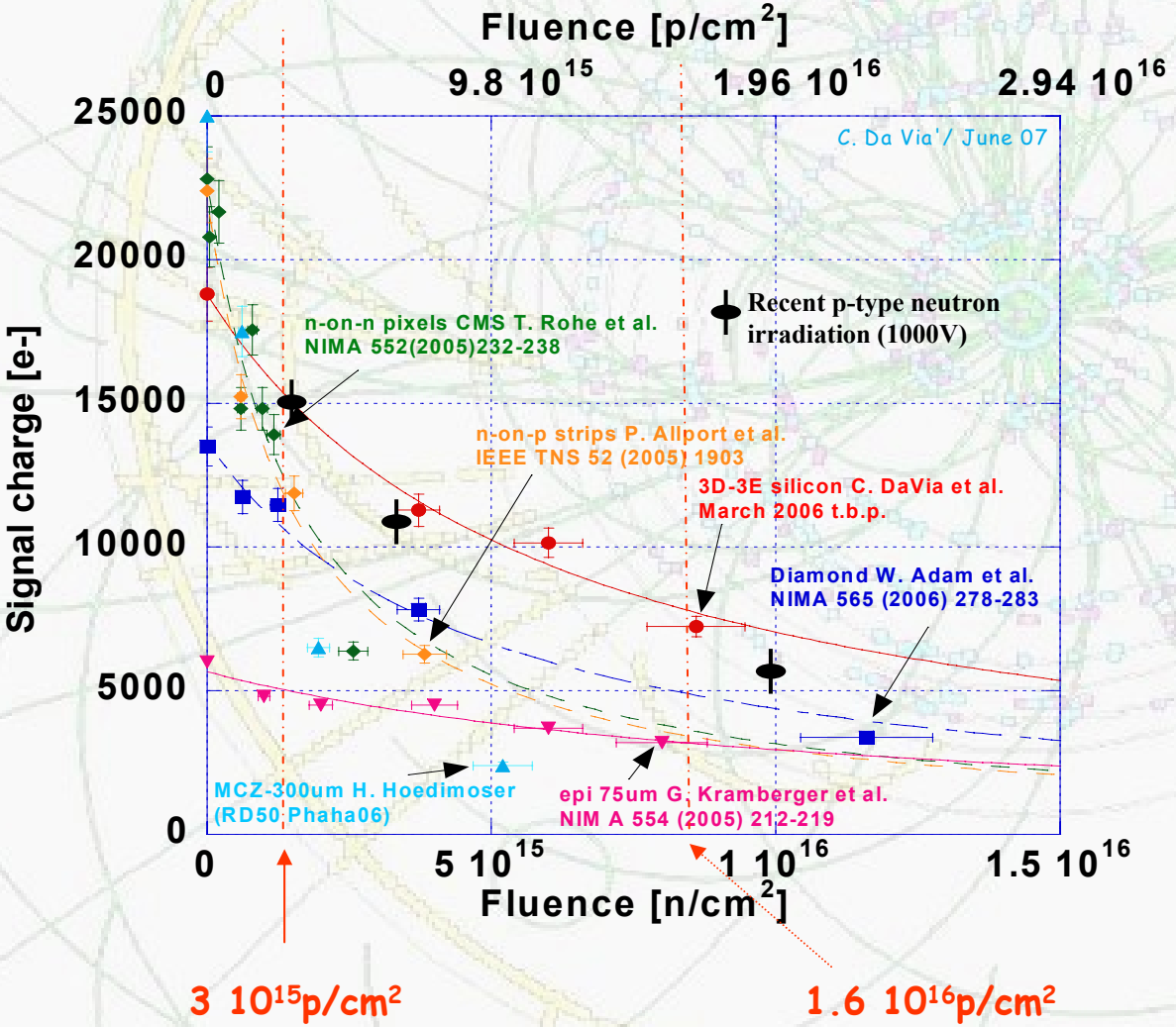
My (PPA) comments

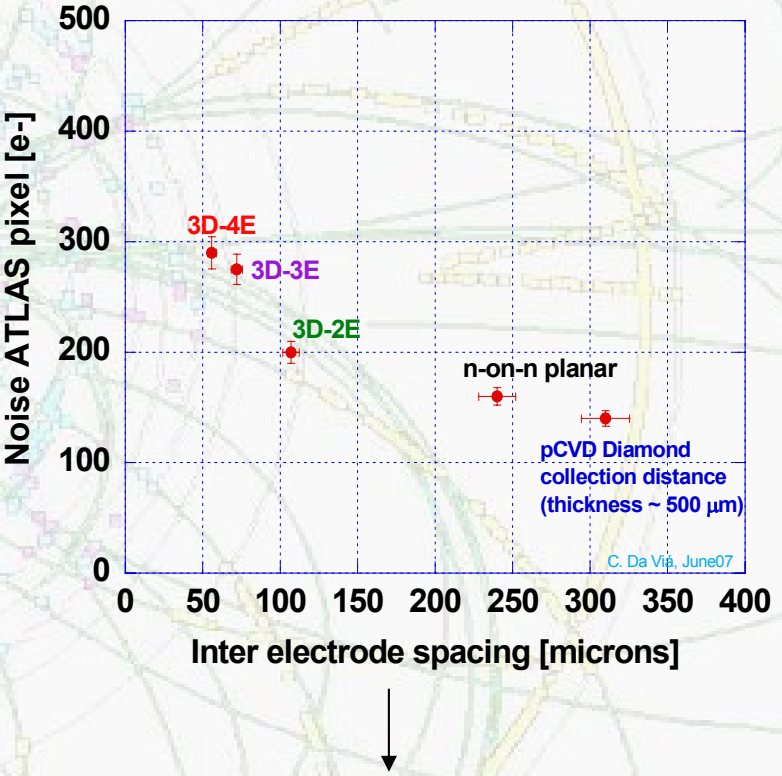
Planar n-in-n or n-in-p: Conservative solution but high operating voltages unless thin(?)

3D- sensors: Highest signal (Efficiency in columns? Commercial fabrication?)

Diamond: Lower currents, low noise (Cost? Uniformity?)

Comparisons of minimum ionising particle (m.i.p.) CCE(V) and S/N after $10^{16} n_{eq}/cm^2$ needed





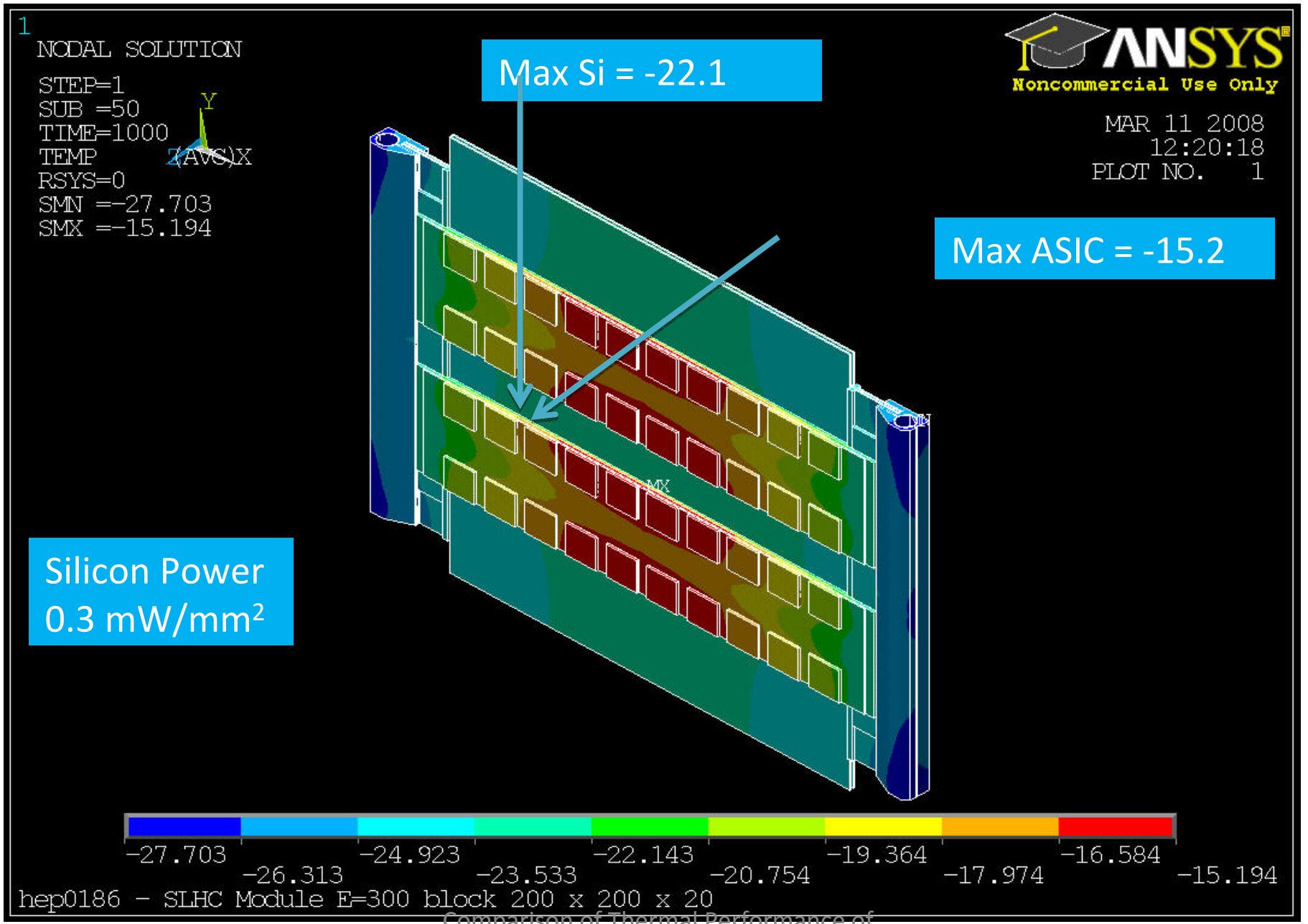
Atlas pixel assemblies

- Noise figure is very good for diamond
- 3D can still play with the substrate thickness
- Planar n-on-p can still play a role in case above technologies not ready

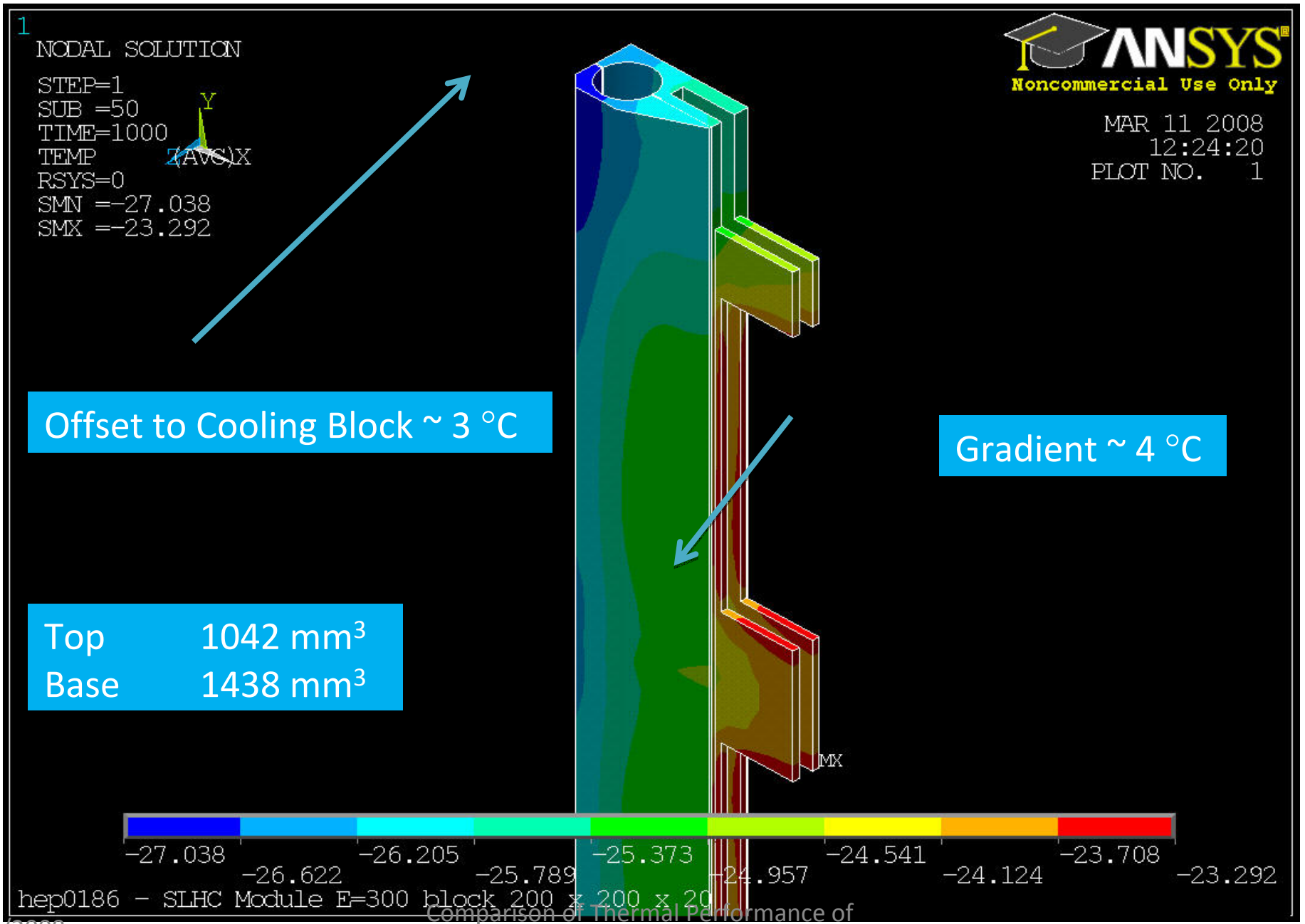
Thermal Simulation Parameters

Parameter	Value
Coolant Temperature	-30 °C
Heat Transfer Coefficient	4,000 W/m^{2}K
ASIC Power	0.3W per ASIC
Silicon Power	0,0.1,0.2,0.3,…… mW/mm^2 to runaway
Sliding thermal grease thickness	0.07 mm
Sliding thermal grease thermal conductivity	0.8 W/mK
Fixed thermal grease thickness	0.01 mm
Fixed thermal grease thermal conductivity	0.8 W/mK
Silicon thermal conductivity	148 W/mK

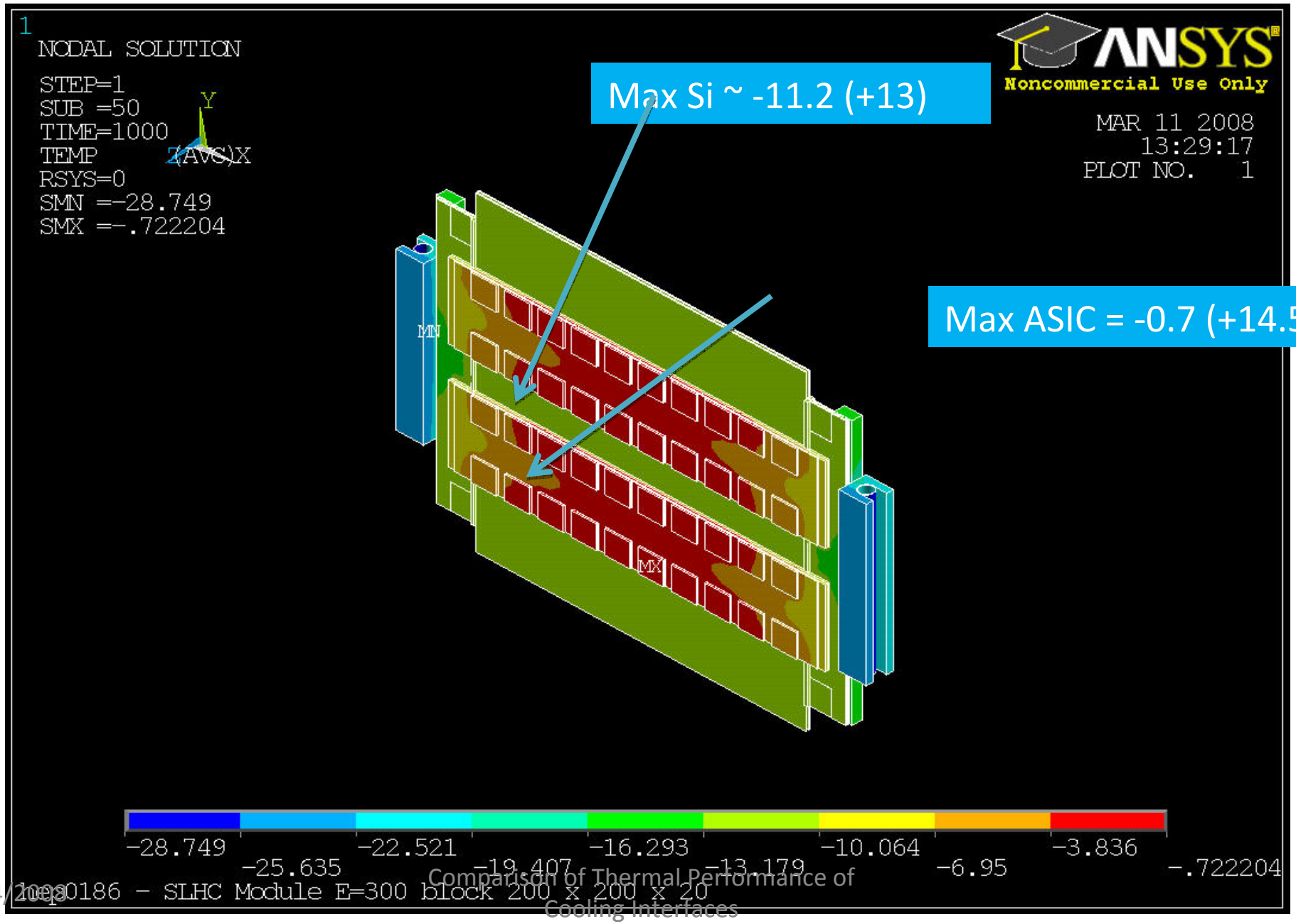
Geneva Module / Sliding



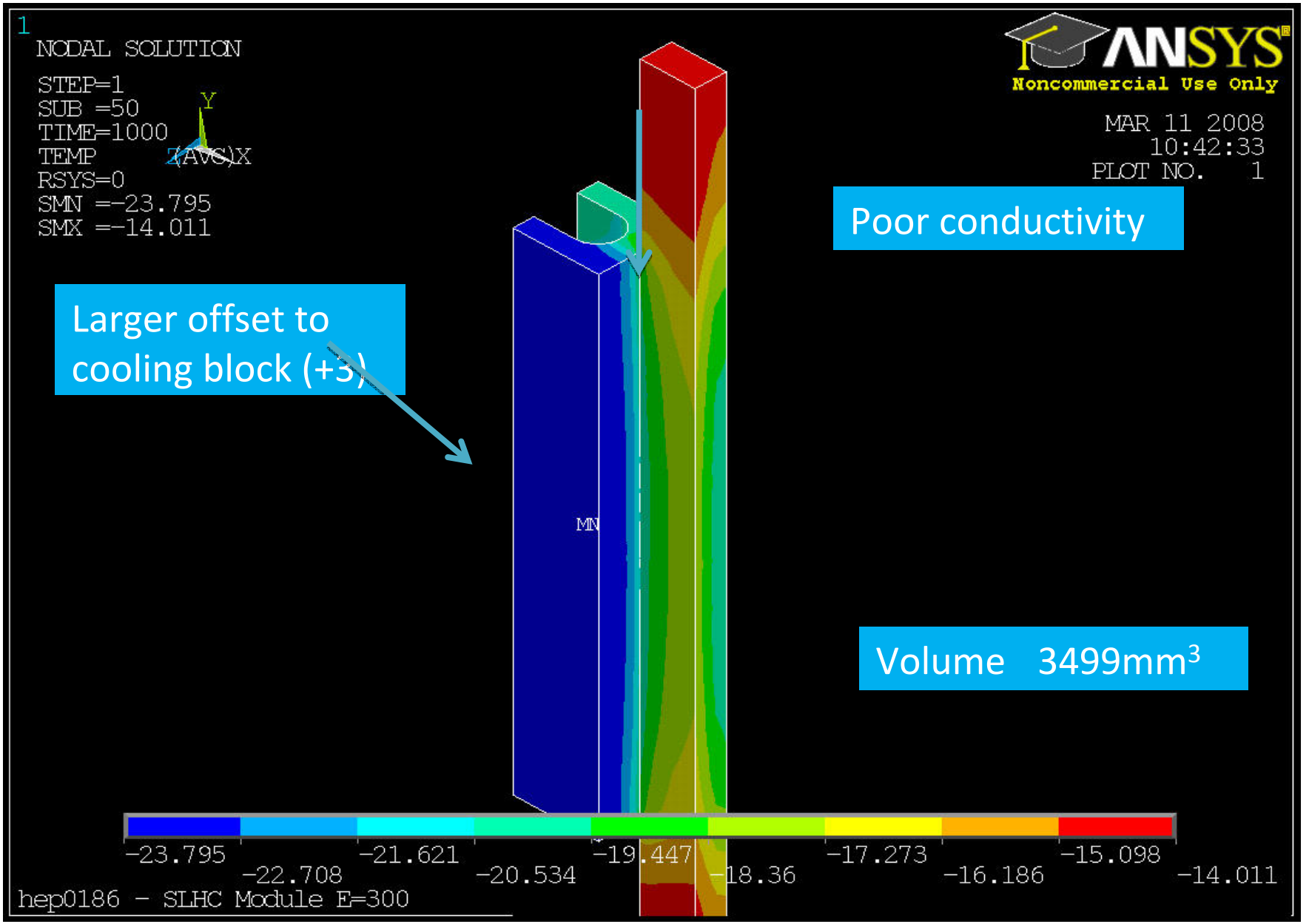
Sliding Grease Interface



Geneva Module / Rigid



Rigid Interface

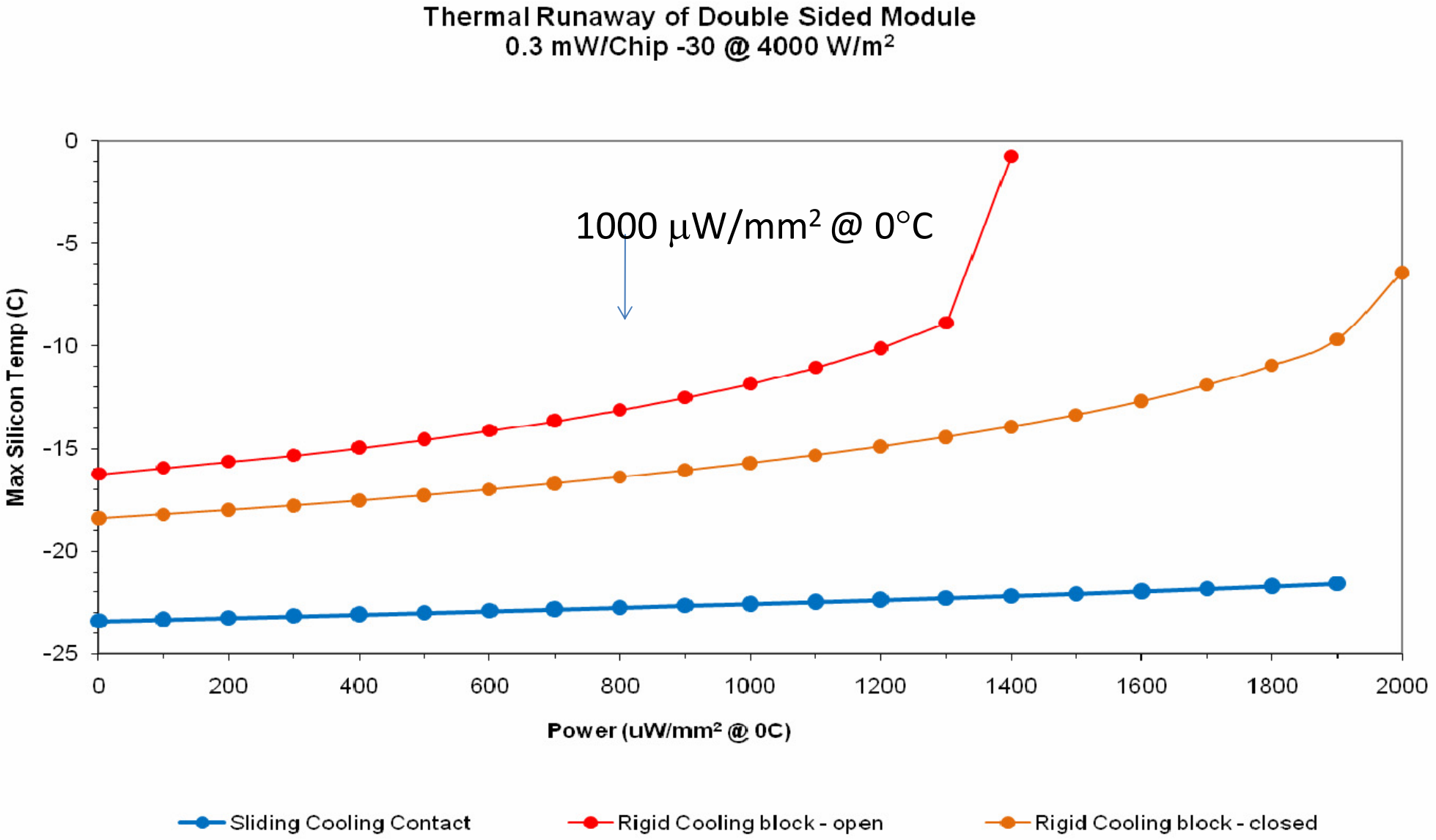


Results of further studies (Q_{si} = 0.3mW/mm^2@0°C)

Module	T Cool (min)	T ASIC (max)	T Si (max)
1. Sliding contact	-27.0	-15.2	-22.1
2. Rigid coupling ('Oxford Block')	-22.7	-4.7	-12.7
3. (2) + cooling block K(200,200,200)	-22.6	-5.7	-13.9
4. (2) + fully enclosed pipe	-25.1	-7.1	-15.2
5. (3) + fully enclosed pipe	-25.0	-8.2	-16.3
6. (5) + 0.01mm grease at interface	-25.0	-10.1	-18.4
7. (6) + cap on top of cooling block	Work in progress		

Cooling Block Conductivity	~ 1.0 °C
Enclosing the cooling tube	~ 2.5 ° C
Thinner grease layer	~ 2.0 ° C
Total	**~ 5.5 ° C**

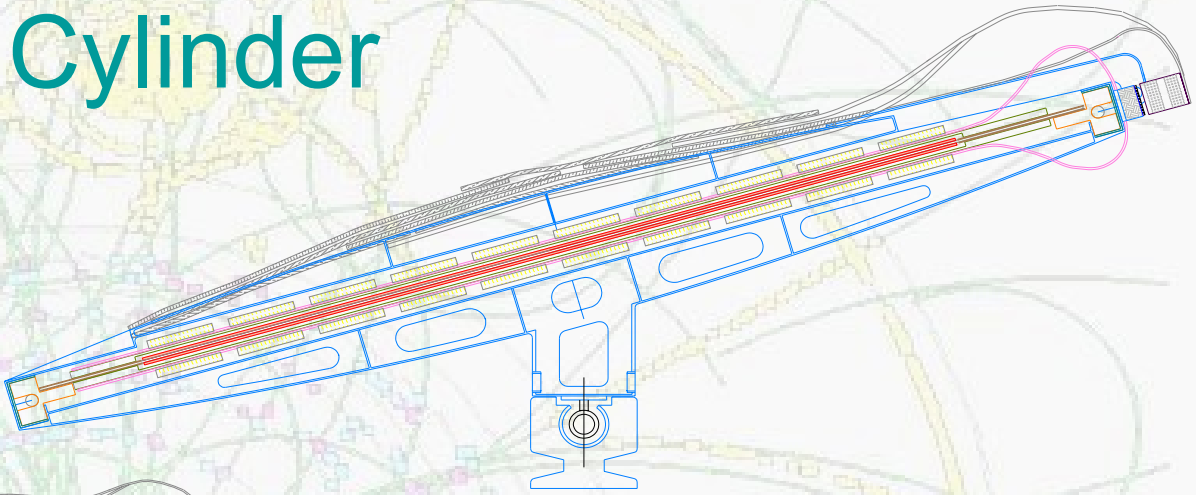
Thermal Runaway

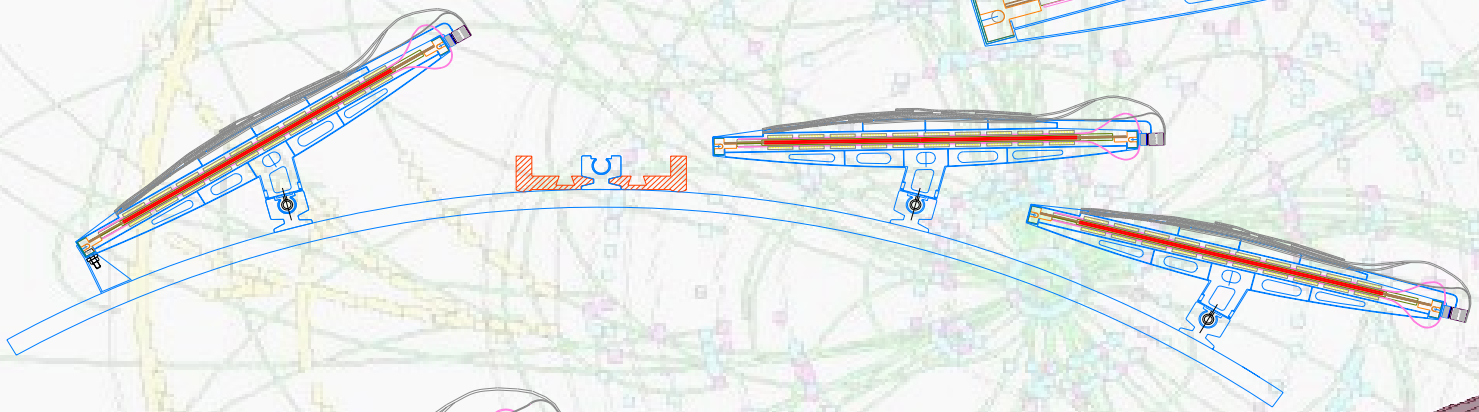


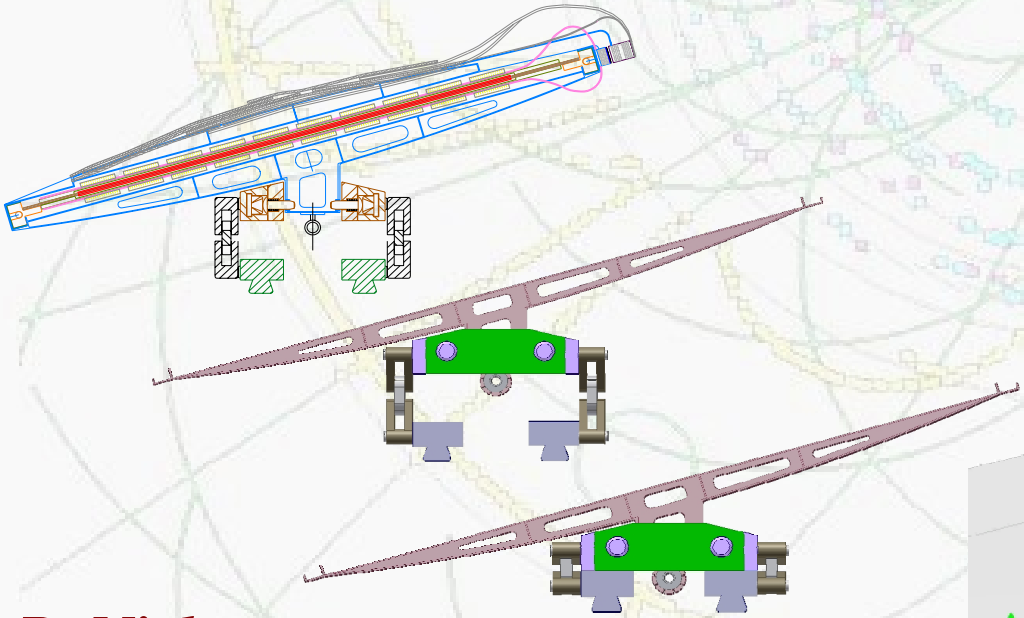
Alternative Mounting Scheme for Super-Module onto Cylinder

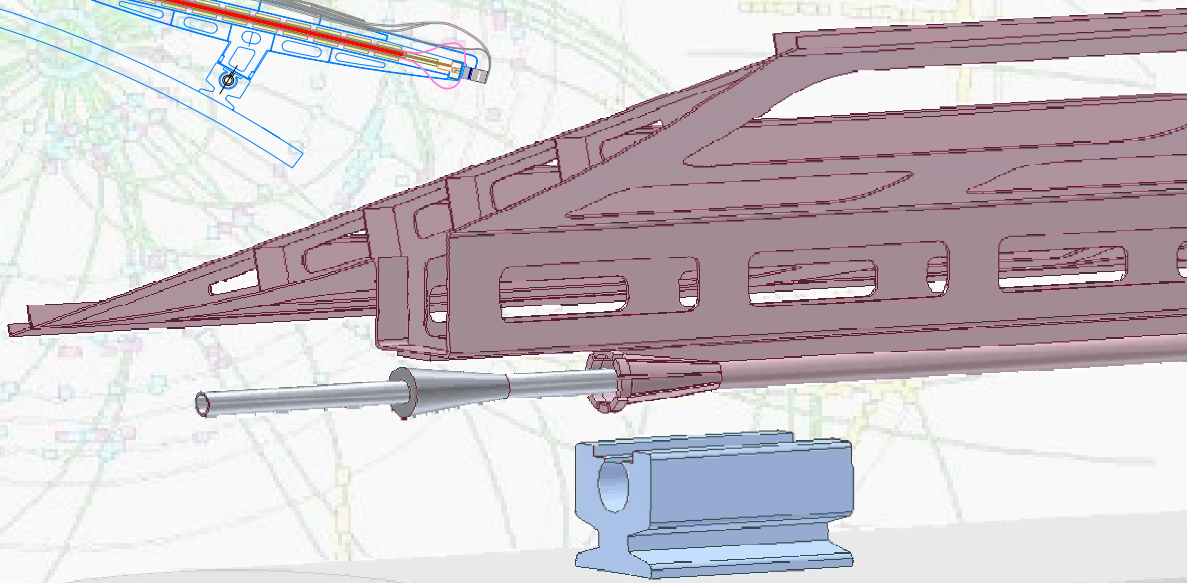
'Aerofoil Support'

- **Low mass structure enclosing modules**
- **Convenient cable support**
- **Allows simultaneous multiple precision mountings to cylinder**



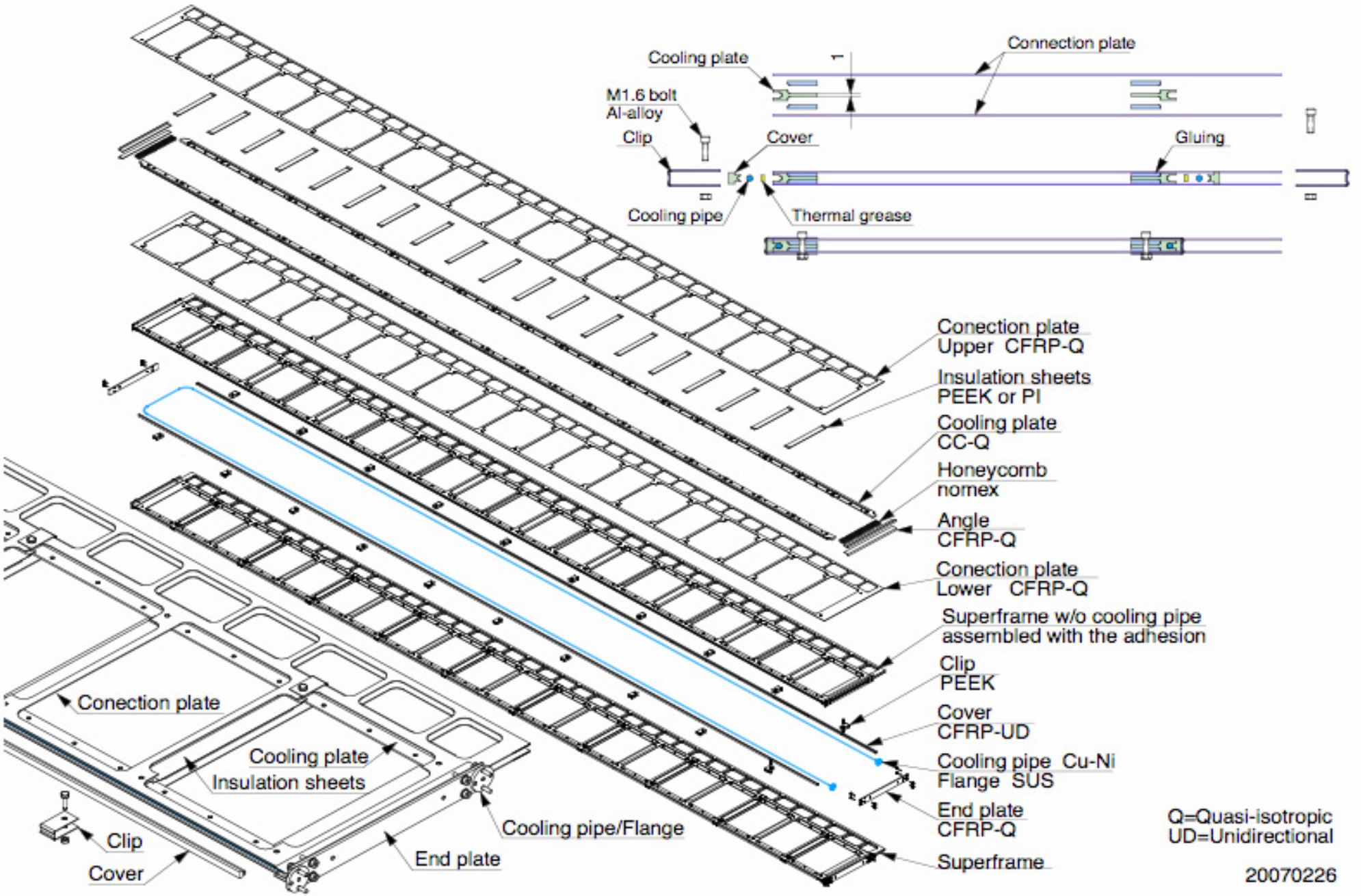






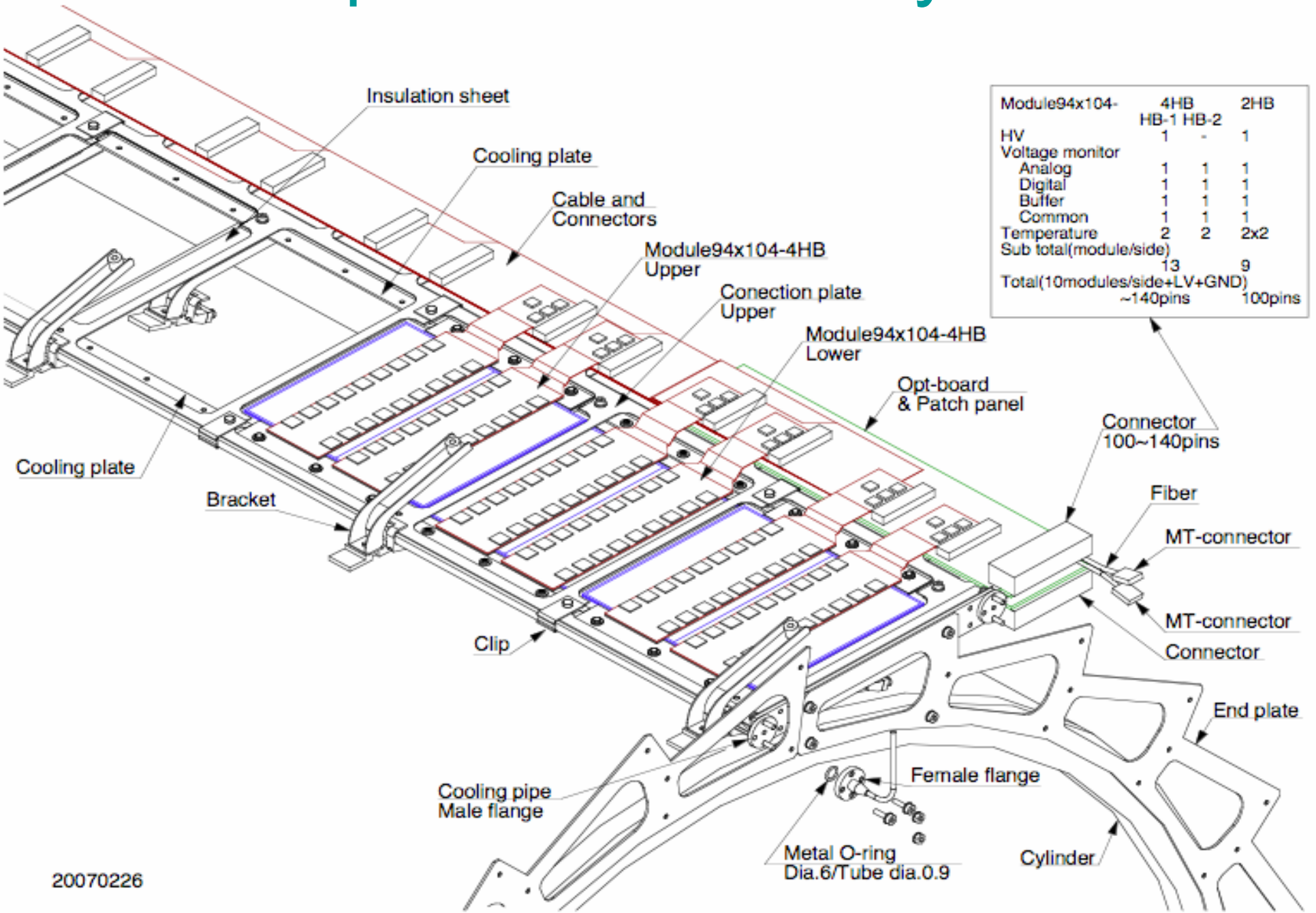
R. Nickerson

Super-Module Concepts: Super-Frame



Y. Unno

Super-Module on Cylinder



Module94x104-	4HB HB-1	4HB HB-2	2HB
HV	1	-	1
Voltage monitor			
Analog	1	1	1
Digital	1	1	1
Buffer	1	1	1
Common	1	1	1
Temperature	2	2	2x2
Sub total(module/side)	13		9
Total(10modules/side+LV+GND)	~140pins		100pins

Y. Unno

Total Microstrip Power

	BIS	BOS	ECA	ECB	Total
Power [kW]	71.8	45.7	18.3	18.3	154.2
	47%	30%	12%	12%	

- Going to P_{chan} = 2mW $\rightarrow$ P_{total} = 120kW,
- Several contributions missing (SMC, Opto-converter, DCS, etc…)
- Best guess (strips) P_{total} = 150kW within ±40kW (2-3×SCT).
- Dominated by barrel (even if BOS shortened).
- Investigating cooling using C_3F_8 (again), C_2F_6 or CO_2
- Reuse of existing services could represent a major challenge

G. Viehhauser

DCS: SLHC- Services

of rows (draft) - SLHC Strawman Layers for barrel:

Layer	# of rows	Radius (mm)
SS layer 1	28	380
SS layer 2	36	490
SS layer 3	44	600
LS layer 1	56	750
LS layer 2	72	950

Numbers not yet available for the ECs

Estimation of 2 interlock temperature sensors per cooling loop → 944 NTCs in total

SCT barrel DCS: 48 type 2-DCS cables of (28 pins Milli-Grid) → 672 twisted pairs!
SCT ECs DCS: 80 type 2-DCS cables of (28 pins Milli-Grid) → 1120 twisted pairs!

Barrel SS layers could use the current barrel DCS type 2 for the interlock
& LS could use part of the current EC DCS type 2.
→ Most probably NOT enough left for the SLHC ECs

Can existing cables be used?
What type of connectors required and where?

D. Ferrere

Powering Issues

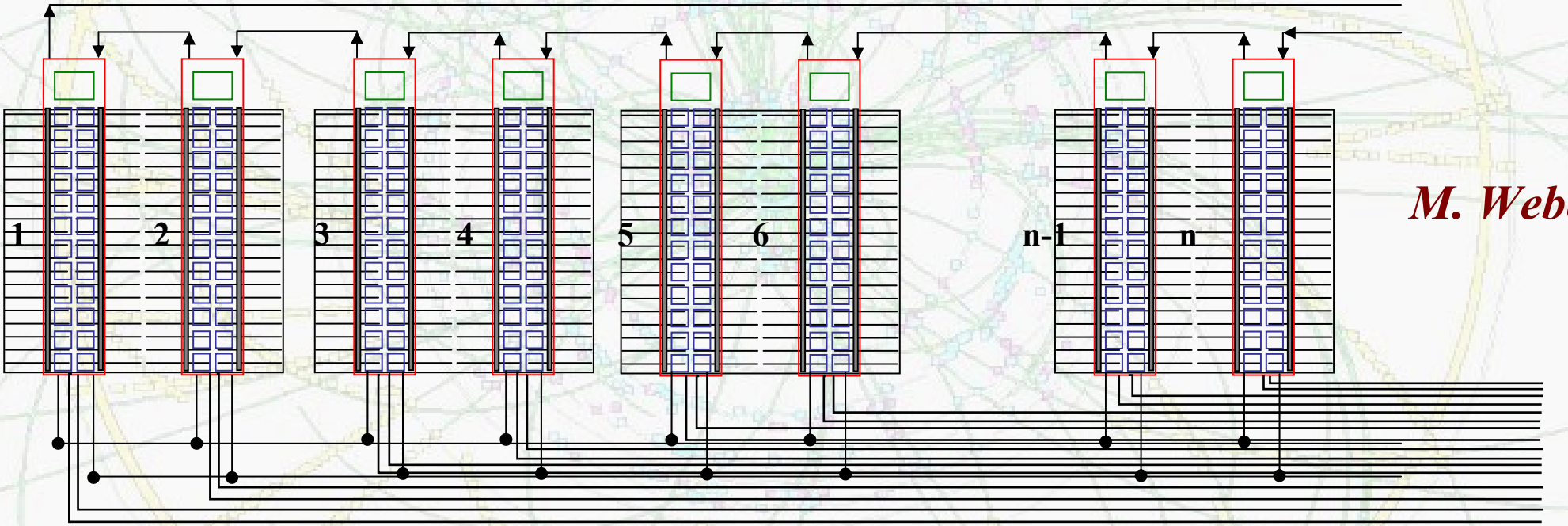
$V_{ABC\text{-}N}$ = 2.5 V; I_{Hybrid} = 2.4 A; 20 hybrids. **Low V + High I ➔ I^2R losses in cables**

(Want power transmission at High V + Low I)

Serial Powering: n=20; $I_H = I_{PS} = 2.4$ A; $V_{PS} = nV_{ABC\text{-}N} = 50$ V

Also saves factor ~8 in power cables/length over SCT

- Need detailed studies of failure modes and recovery



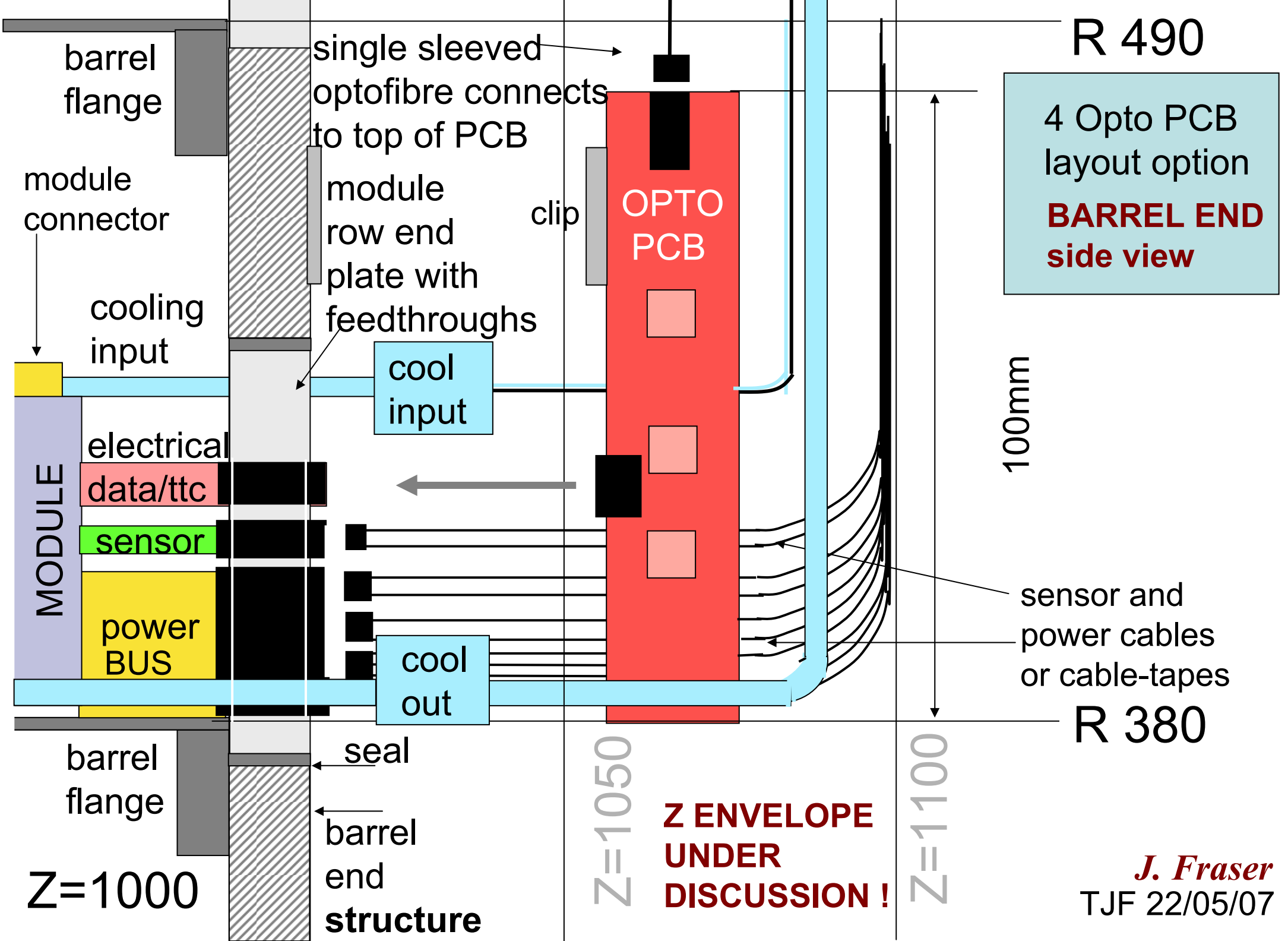
M. Weber

DC-DC Conversion : n=20; g =20; $I_{PS} = n/g\ I_H = 2.4$A; $V_{PS} = gV_{ABC\text{-}N} = 50$V

Parallel powering also saves factor ~8 in power cables as for Serial Powering

- Issues with switched capacitors (noise?) and need for custom design to get large g

(Independent powering with DC-DC costs too many cables)


barrel flange
single sleeved optofibre connects to top of PCB
R 490
4 Opto PCB layout option
BARREL END side view
module connector
module row end plate with feedthroughs
clip
OPTO PCB
cooling input
cool input
100mm
electrical
data/ttc
sensor
MODULE
power BUS
sensor and power cables or cable-tapes
cool out
R 380
barrel flange
seal
Z=1050
Z=1100
Z ENVELOPE UNDER DISCUSSION !
barrel end structure
Z=1000
J. Fraser
TJF 22/05/07