# Vertical Integration Technologies: An Overview

Armin Klumpp, Karl-Reinhard Merkel,
Lars Nebrich, Peter Ramm, Josef Weber, Robert Wieland,
Jürgen Wolf *

Fraunhofer Institute for Reliability and Microintegration, Munich Division
Hansastrasse 27d, 80686 Munich
* Fraunhofer Institute for Reliability and Microintegration,
Gustav-Mayer-Allee 25, 13355 Berlin
Germany

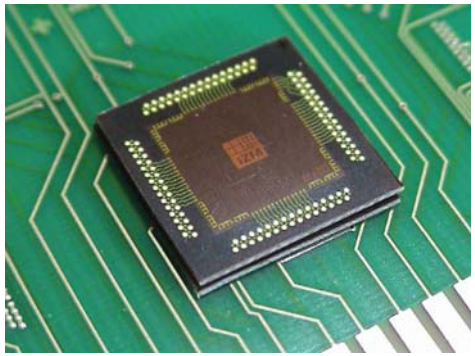


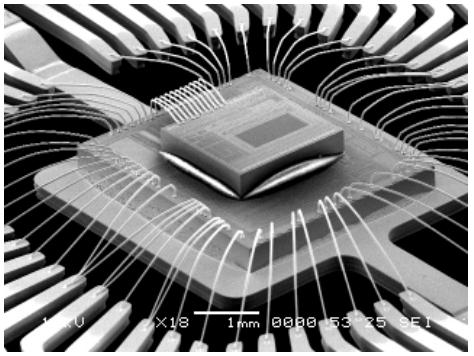
# Topics of 3-D Integration

- Drivers / Motivation for 3D Integration
- Basic 3-D Integration Technology
    - Metal system for electrical path
    - Fabrication of Through Silicon Vias (TSV)
    - Wafer or Die Bonding Technology
- Design for 3D Integration
- Electrical Performance and Test of 3D Circuits
- Thermal Management
- Applications of 3-D Integration



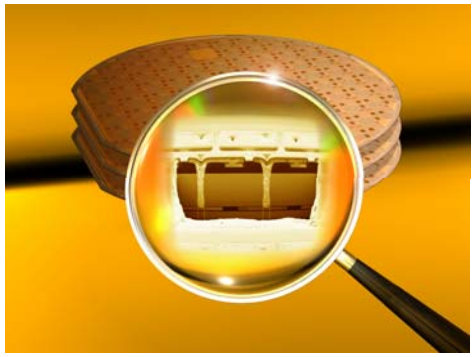
# 3-D System Integration





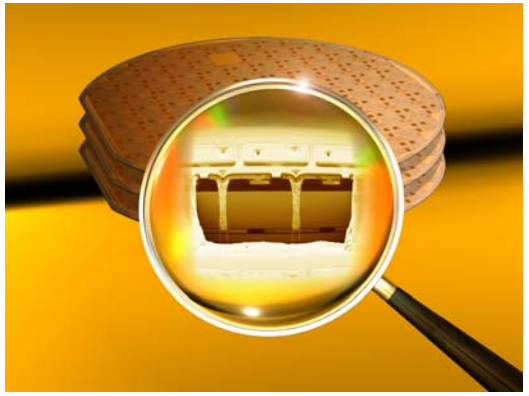
***Concepts:***

- **Package Stacking**
- **Die Stacking**
- **Vertical System Integration**



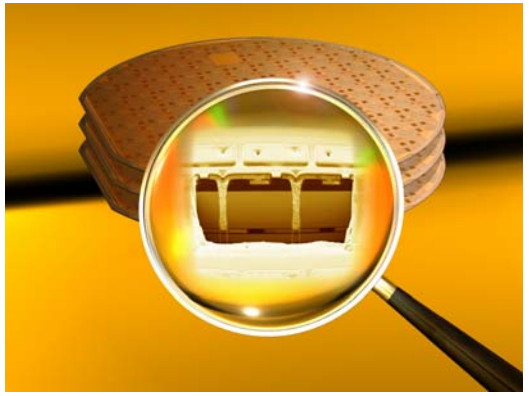
## *Concepts:*

- Package Stacking
- Die Stacking
- **Vertical System Integration**
  - by **Bonding** of thinned device substrates
  - by freely selectable **through-Si vias** (TSV)
  - with potential for **High density** vertical wiring
  - as **expanded backend technology** without intervention into standard processing of devices (except design for TSV placement)





## Vertical System Integration



- Basic 3-D Integration Technology
  - Metal system for electrical path (interconnects)
  - Mechanical bond of silicon layers
  - Fabrication of Through Silicon Vias (TSV)

- Handling Concepts
  - Wafer or Die Bonding Technology

## State of the art on mainstream 3D integration concepts

| | RPI | Fraunhofer IZM M/B | IMEC | LETI | Infineon | MCNC-RDI | IBM | Tezzaron | AllVia, Inc. | Toshiba | Tohoku Univ. Japan | ASET Japan |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Wafer to wafer** | X | | X | | | | X | X | | X | X | |
| **Chip to wafer** | | X | | | X | X | | | | | | |
| **Chip to chip** | | | | | | X | | | X | | | X |
| **SOI or bulk wafer** | SOI | Bulk | Bulk | SOI | Bulk | Bulk | SOI | | Bulk | Bulk | Bulk | Bulk |
| **Via size [µm]** | 2x2 | 2.5, 3x10, > 5 | 5 / > 100 | | - | 4 | | | > 20 | 30 | 2.5 | 10 |
| **Via etch process** | SF6 | SF6 or HBr | SF6 | SF6 | - | SF6 | | SF6 | SF6 | SF6 | SF6 | SF6 |
| **Peripheral vias** | | X | | | | | | | X | X | | X |
| **Area array vias** | X | X | | | | | | | | | | |
| **Via dielectric** | SiO2 | SiO2 | SiO2 / Parylene | Polymer | SiO2 | Polymer | | SiO2 | SiO2 | SiO2 | SiO2 | SiO2 |
| **Barrier layer** | TiN | TiN | TiN | | TiN | TiN | ? | TiN | ? | TiN | | TiN |
| **Metal plug** | Cu | W-CVD Cu (> 5) | Cu | Cu | Cu | Cu | Cu W-CVD | Cu | Cu | Cu | Poly-Si or W-CVD | Cu |
| **Handle wafer** | No | Yes | Yes | | No | | Yes | No | No | | Yes | Yes |
| **Bonding scheme** | Polymer | Cu/Sn SLID; SnAg-µBump | Cu-Cu | Cu-Cu | Cu/Sn SLID | Polymer or bumps | Cu/Cu Si Fusion | Cu-Cu | Solder | Bumps | In/Au bumps | Cu/Sn SLID |

by Armin Klumpp

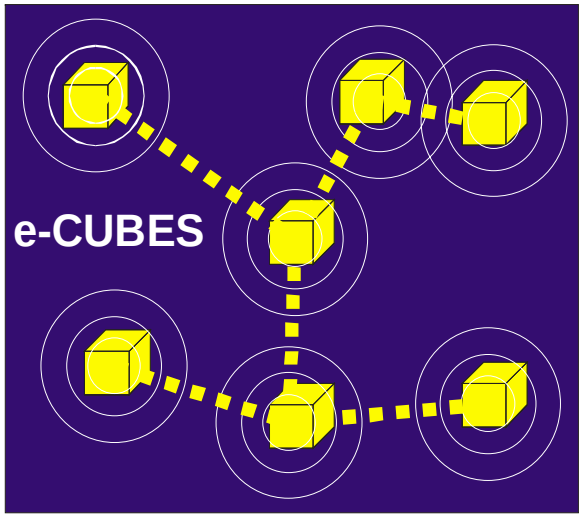
IZM
Fraunhofer Institut Zuverlässigkeit und Mikrointegration

## Project Frame of Development Activities IZM-Munich

- Past basic technology development
  - *within two projects funded by BMBF, Germany ( 01M2926 D/E & 01M2999/A )*
- Actual development of remaining keypoints and adaption for applications
  - **KASS** (*Communication and Automotive Applications in Stacked Silicon*)
    BMBF, Germany (01M3163B); 01.09.2005 – 31.08.2008
  - **e-CUBES** (3-D-Integrated Micro/Nano Modules for Easily Adapted Applications)
    European Community (IST-026461); 01.02.2006 – 31.01.2009
- European R&D Platform
  - **MNT** (Micro- and Nano-Technology)
    European Community; 01.01.2005 – 31.12.2007



## e-CUBES (1)




Wireless communicating “small sensor cubes” (ad-hoc network )

Possible multi-disciplinary applications

- Distributed smart monitoring for Aeronautics and Space applications
- Wireless sensor networks for Health and Fitness
- Distributed intelligent Automotive Control.

Particular focus of e-CUBES is on the following technologies:

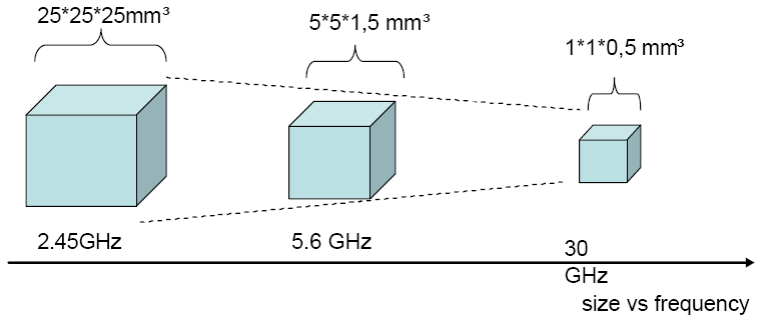
- Individual technologies at various layer levels, suitable for 3D integration,
- Layer processing/thinning technologies for 3D integration,
- 3D assembling and packaging,
- New communication means, e.g. antennas, passive and RF integration, and communication networks,
- Power supply and power management for portable applications,
- Design methodologies for the 3D SoC and related simulation tools

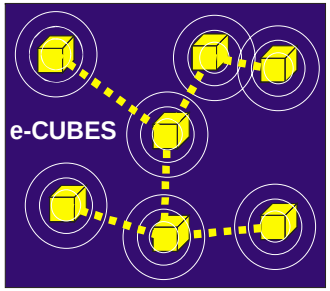


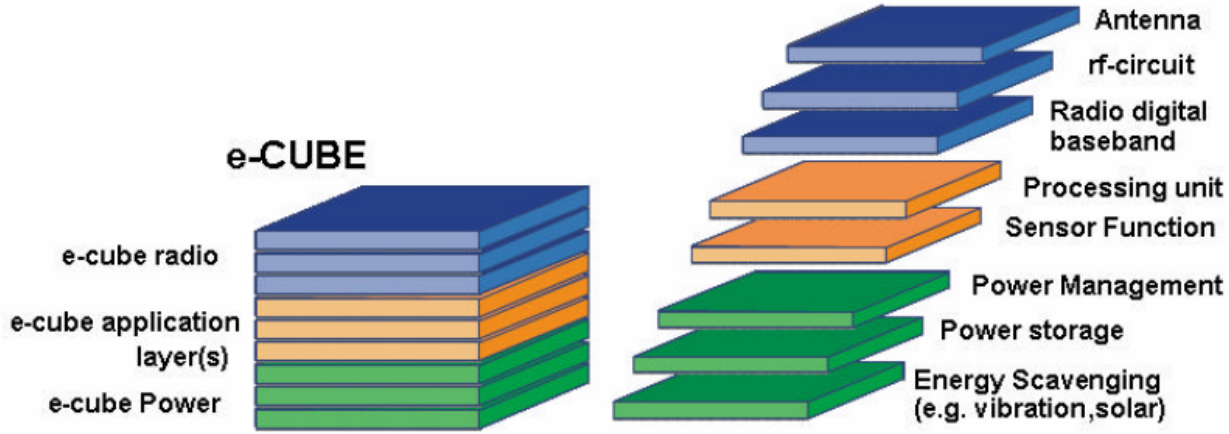
## e-CUBES (2)

Specific challenge

- increasing frequencies
- heterogeneous integration




by Armin Klumpp

Fraunhofer IZM Institut Zuverlässigkeit und Mikrointegration

## *Semiconductor 3-D Equipment and Materials Consortium*

- ***EMC-3D consortium created for the development of cost-effective 3D Thru-Silicon-Via interconnect* for device stacking and MEMS/sensors packaging**
- **Development of processes for creating micro vias between 5 and 30 µm on thinned 50 µm 300mm wafers via-first and via-last techniques**
- **Cost of ownership goal for the integrated 3D process is $200usd per wafer.**
- **Founding equipment companies: Semitool, Alcatel, EV-Group and XSiL.**
- **Associate research members: SAIT (Samsung Advanced Institute of Technology), KAIST (Korea Advanced Institute of Science and Technology), Fraunhofer IZM and TAMU (Texas A&M University).**
- **Material members: Rohm and Haas, Honeywell, Enthone, and AZ with wafer service support from Isonics.**
- **For more information, see www.EMC3D.org**



# 3-D Integration of ICs

## *MNT: Micro and Nano Technologies*

- ✓ *RF communications.*
- ✓ *Optical communications.*
- ✓ *Bio sensing.*
- ✓ *Mechanical MEMS*
- ✓ *Generic activities: WLP, attach technologies, through wafer vias, reliability, integration of power sources.*

*Partners :*

- *Léti (France)*
- *IMEC (Belgium)*
- *CSEM (Switzerland)*
- *Tyndall (Ireland)*
- *Fraunhofer IZM / IISB (Germany)*

LETI

IMEC

CSEM

Tyndall

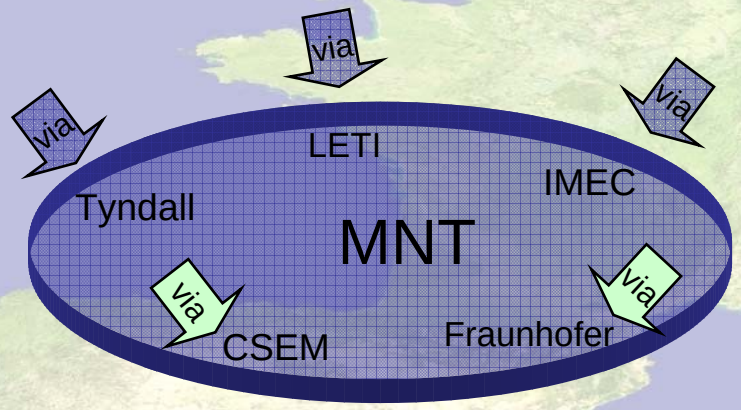
Fraunhofer

by Armin Klumpp

Fraunhofer Institut Zuverlässigkeit und Mikrointegration

## *MNT: Micro and Nano Technologies*

- *to integrate the Micro and Nano Technologies research capabilities under the form of a distributed platform for R&D*
- *to share equipments and technologies*
- *open for interested companies and research institutes*
- *one entry point of your choice for use of the complete platform*




*More information @*
*http://www.mnteurope.org/*

*http://www-leti.cea.fr/*
*http://www.csem.ch/*
*http://www.fraunhofer.de/*
*http: www.imec.be/*
*http://www.tyndall.ie/*

LETI
IMEC
CSEM
Tyndall
Fraunhofer

by Armin Klumpp

**Fraunhofer** Institut Zuverlässigkeit und Mikrointegration

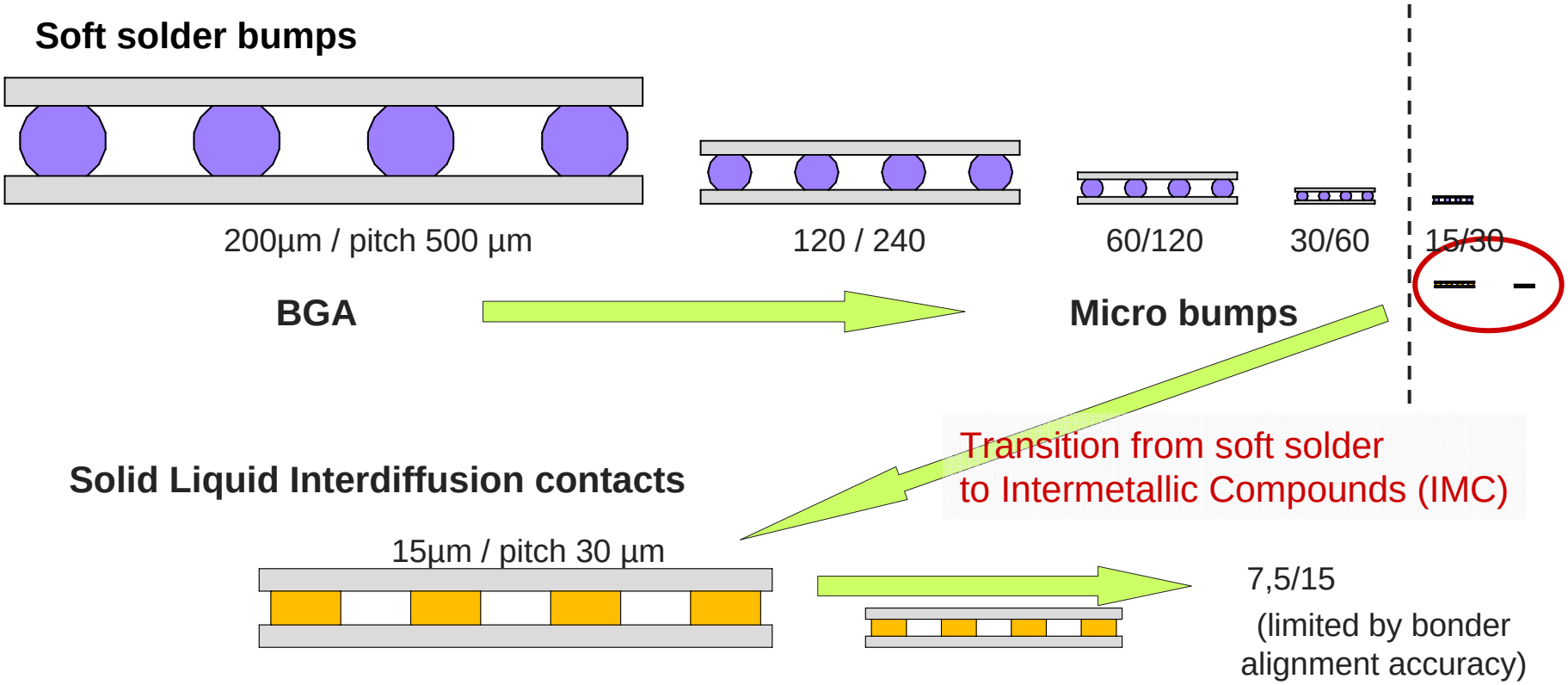
# Vertical System Integration

- Basic 3-D Integration Technology
  - Metal system for electrical path (interconnects)

**from Solderballs to Interconnetion Pads**

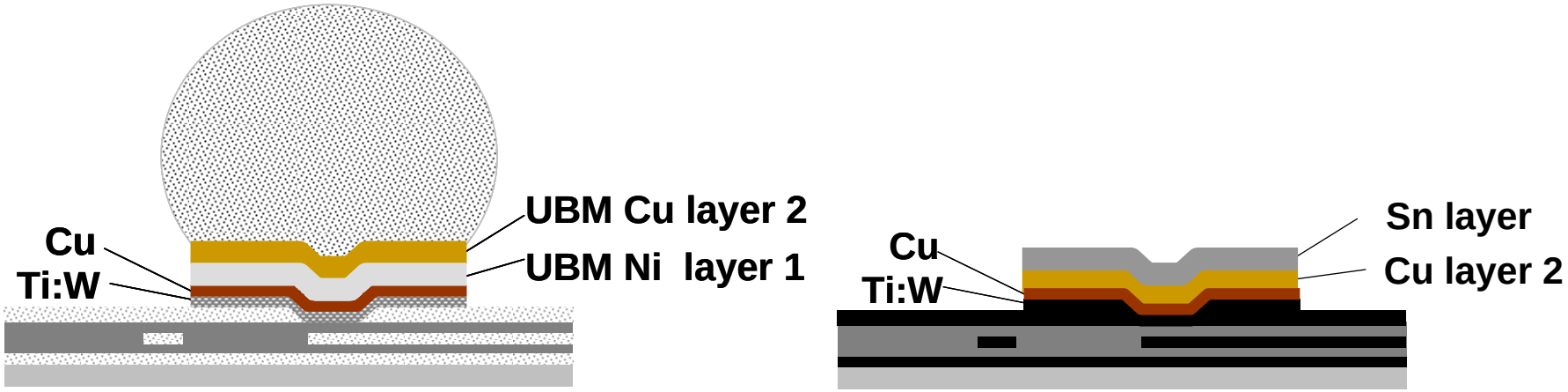


# 3-D Integration of ICs




*Ref.: H.Hübner et al., Infineon; MAM 2006, Grenoble*

# From solder ball to solder pad

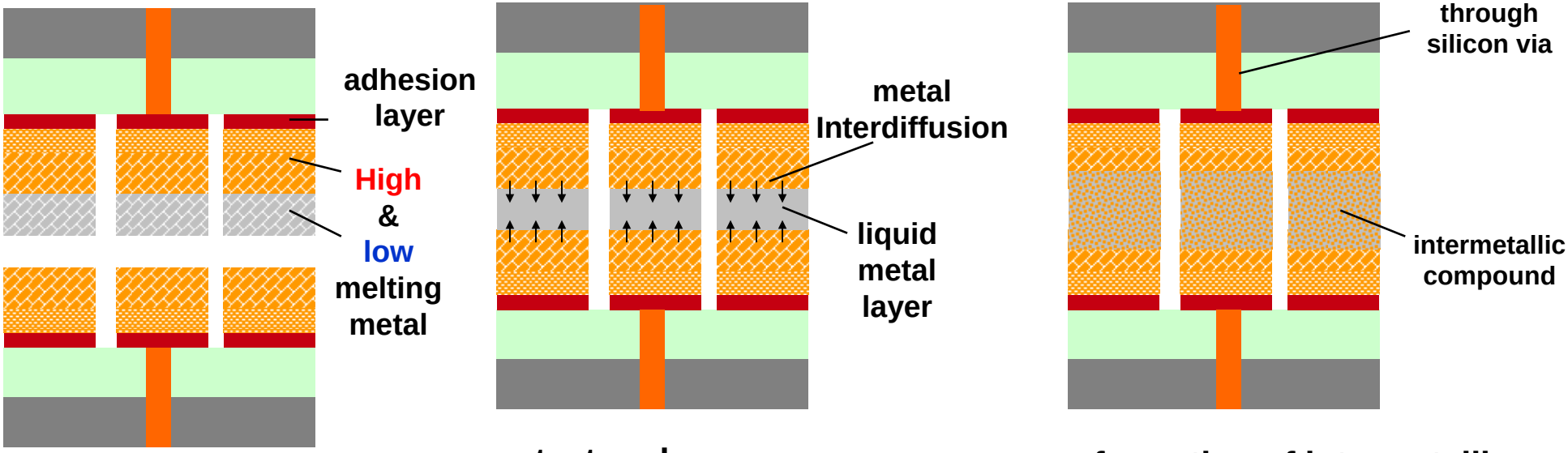



***Reference: Engelmann, Wolf, Jurenka ECTC***



# Metallization SLID (Solid Liquid Interdiffusion)

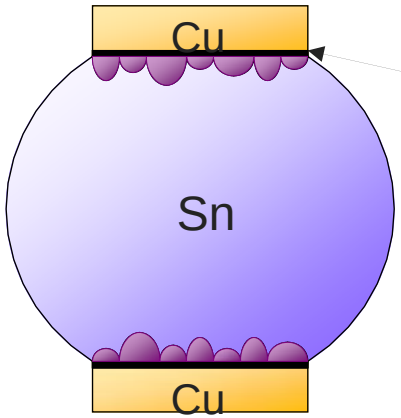
Thermal management of dissipated power -> no polymeric underfiller






# 3-D Integration of ICs

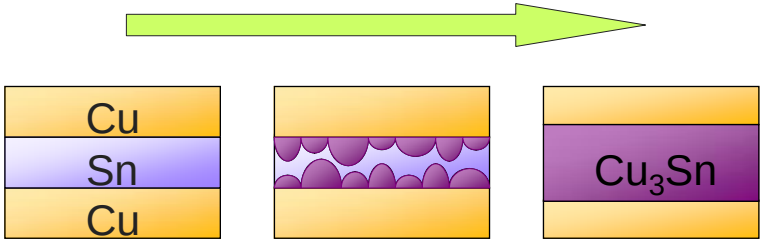
## BGA - Solder bump




diffusion barrier

- Large solder volumen
- Phase growth is controlled by
  - diffusion barrier (Ni/Au) and
  - low temperature budget
- Solidification by cooling

## SOLID interface




- Very thin solder layer
  - No barrier
  - Simple metallurgy
- Sn is completely consumed
- Solidification isothermally

*Ref.: H.Hübner et al., Infineon; MAM 2006, Grenoble*

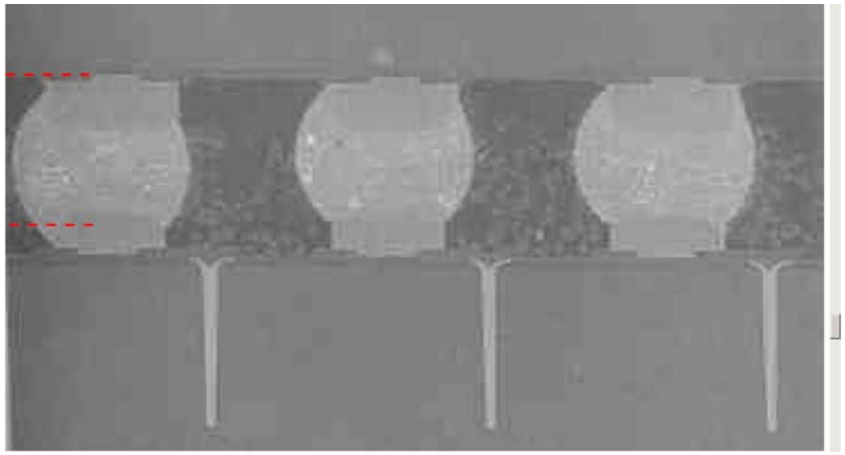
| Ball Grid Array | SOLID |
|---|---|
| Same processing for solder apply, but | |
| reflow defines shape of the balls *before* pick & place | reflow and soldering in a single step *after* pick & place |
| ▪ All pads must be the same size | ▪ Different sizes possible |
| ▪ All pads must be the same shape | ▪ Different shapes possible |
| ▪ Larger spacing between balls, because balls expand | ▪ Smaller spacing (only limited by the bonder alignment) |
| ▪ Complicated metallurgy (barrier, multiple IMCs) | ▪ Only two metals involved (barrier free, one IMC) |
| ▪ Phase growth not finished | ▪ Thermodynamical stable |
| ▪ High homologous temperature | ▪ Low homologuos temperature |

*Ref.: H.Hübner et al., Infineon; MAM 2006, Grenoble*



- **Through-Silicon-Vias**

  in combination with BGAs
  (Ø 20 µm)

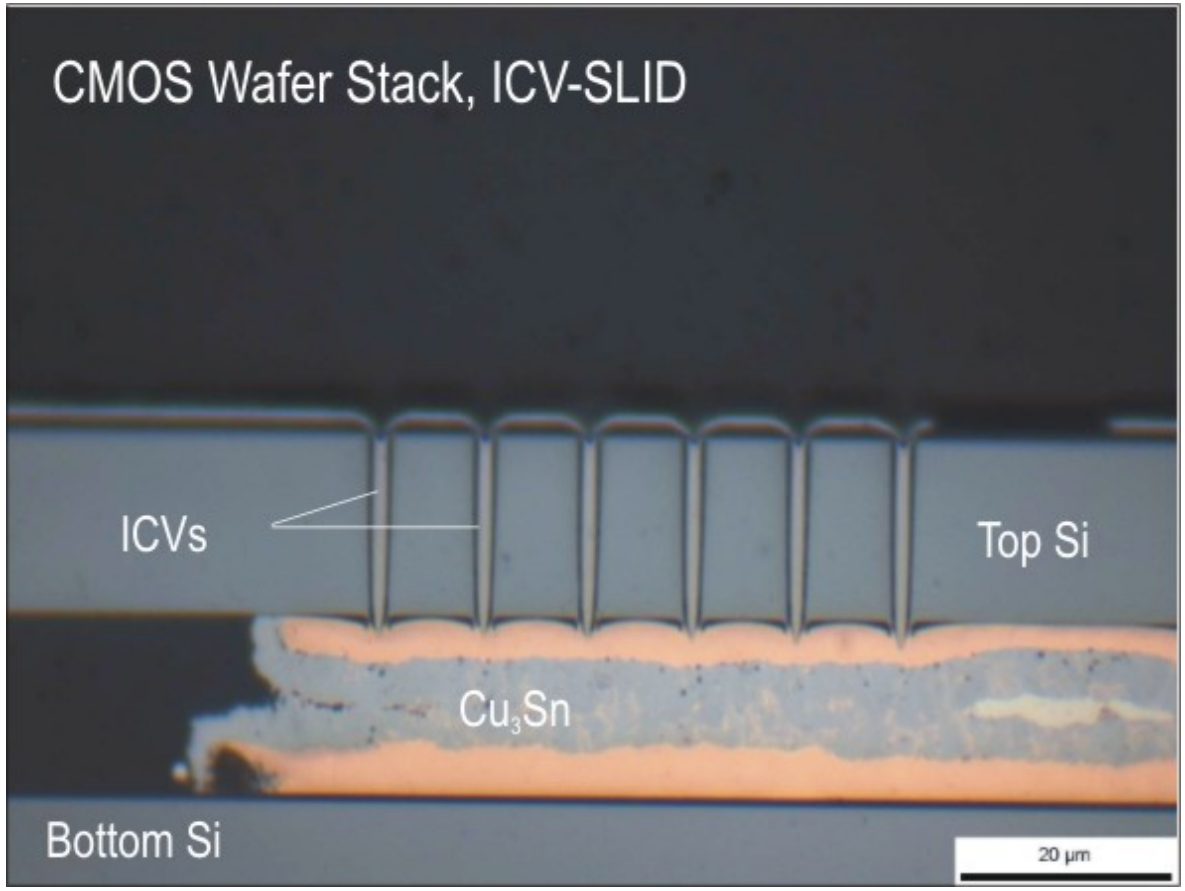


*Ref.: IZM Munich; internal report*



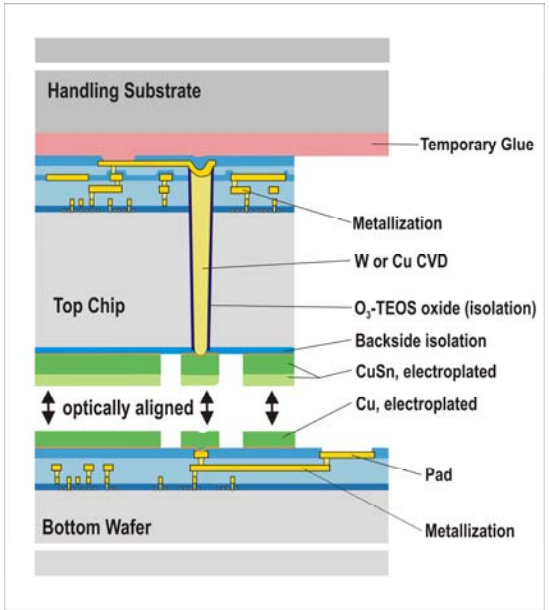
- **ICV-SLID Technology**

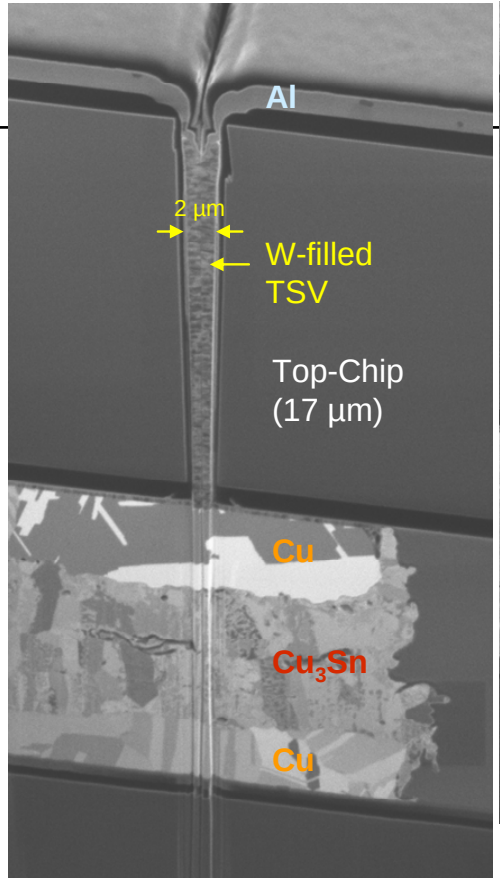
  3D integrated CMOS device stack (micrograph)



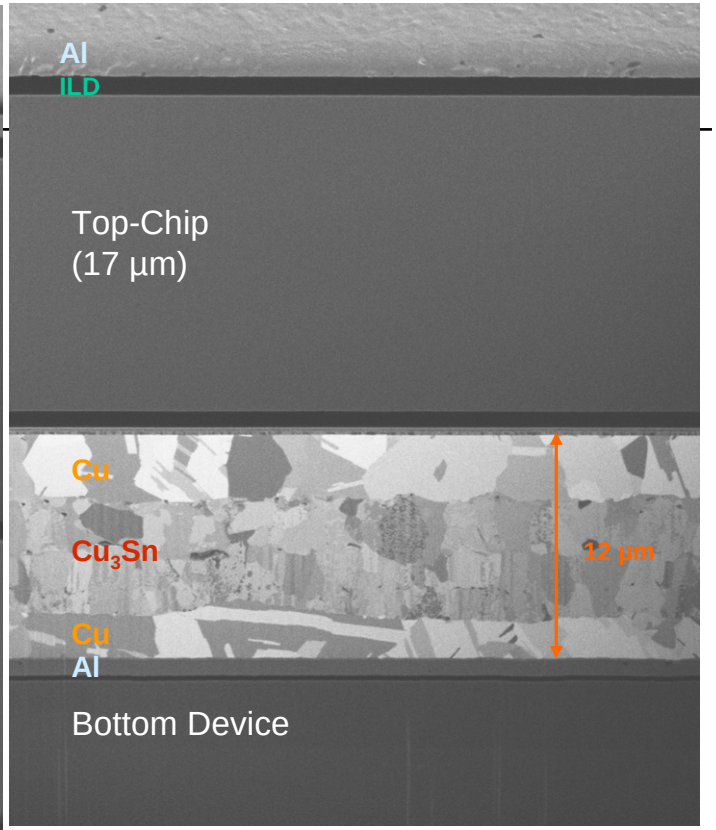
# 3-D Integration of ICs

Results of focused ion beam analysis (FIB) on chip-stack formed by ICV-SLID technology



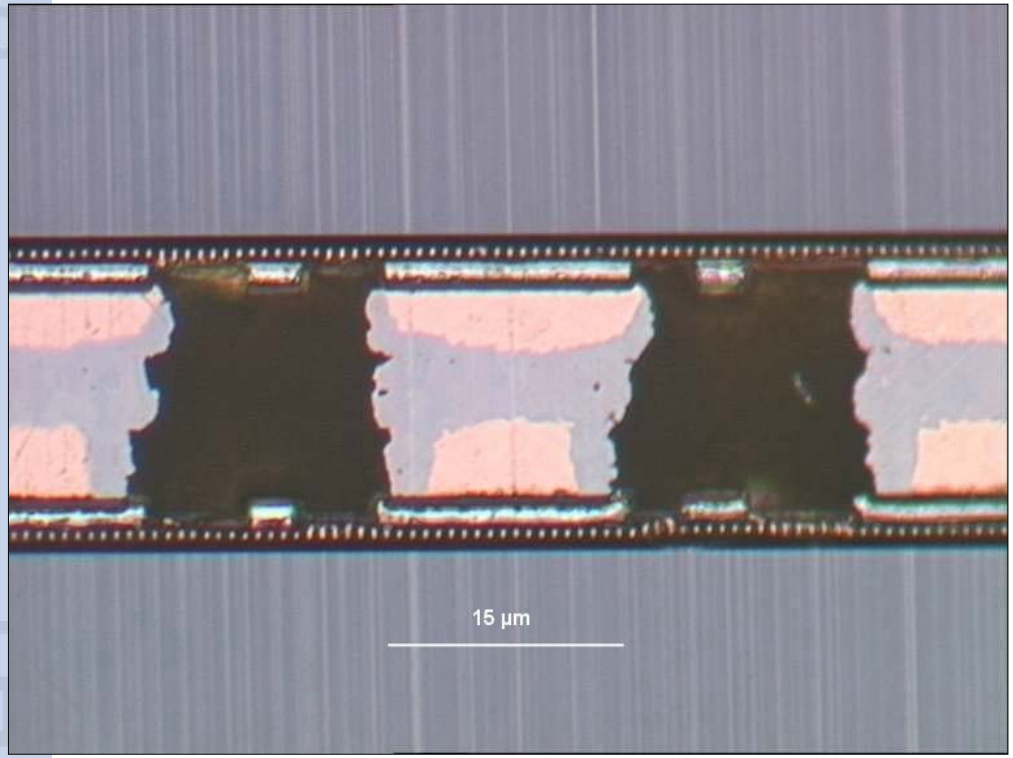

Cross section of ICV-SLID inter-connect between bottom device-chip and top-chip (Al on the top is used for rewiring)

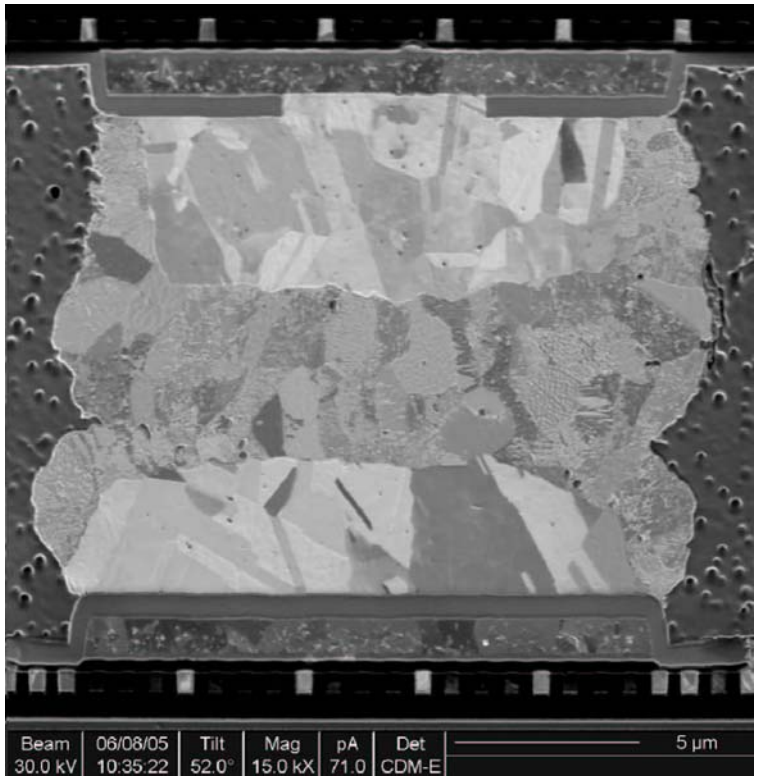



Detail of Cross section ICV-SLID interconnect between bottom device-chip and top-chip (Al-pad on the bottom chip)

*Ref.: IZM in e-CUBES, IST-026461*

# Contact after 500 T-cycles - 65 …150°C



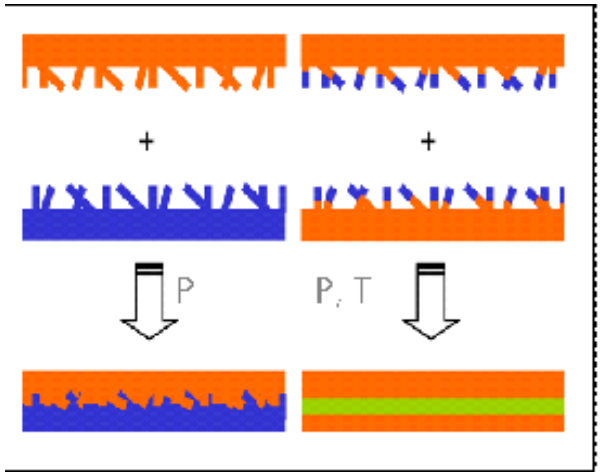

**Void-free joint**

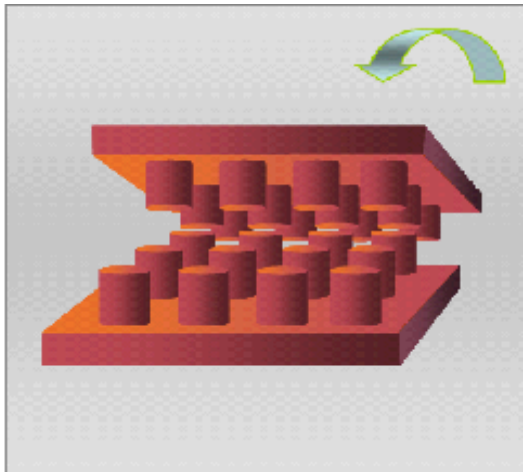
**No degradation, no recristallization**

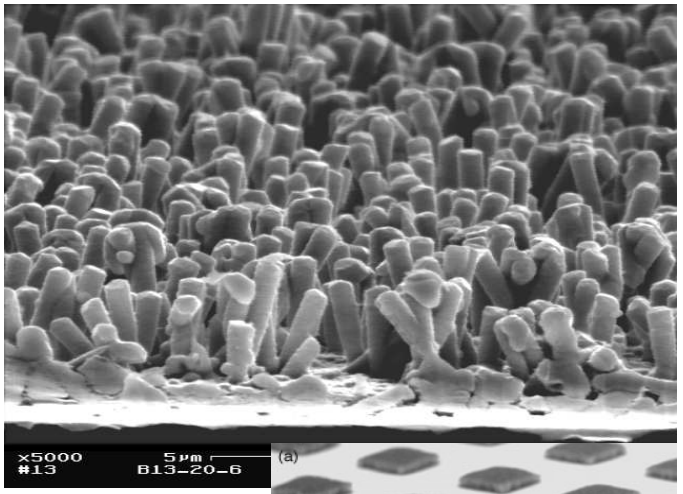
(Source: Infineon Technologies)

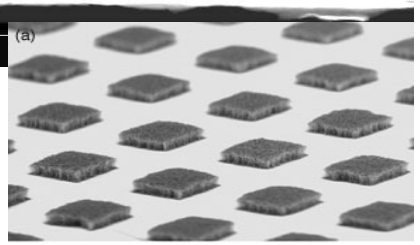
Dr. H. Hübner
AIM CC SCM
June 2005

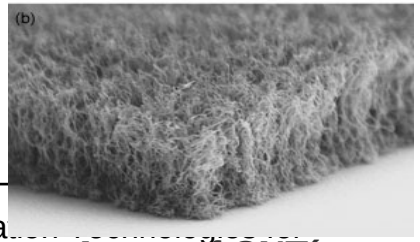
# Interconnects: Nano Structured Surfaces








Areas of CNT´s

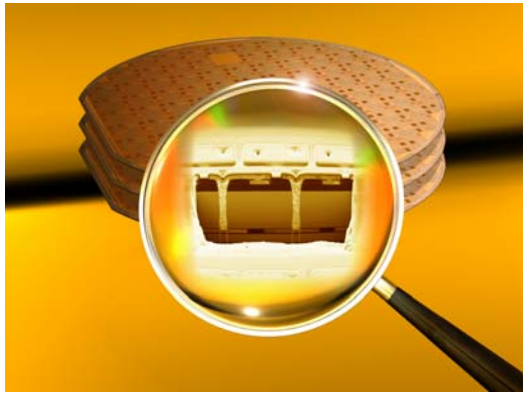
Use of nanoscale enhanced structures such as dents (NanoPierce), NanoLawn (IZM) or CNTs (multiple approaches).

by Armin Klumpp

Fraunhofer Institut Zuverlässigkeit und Mikrointegration

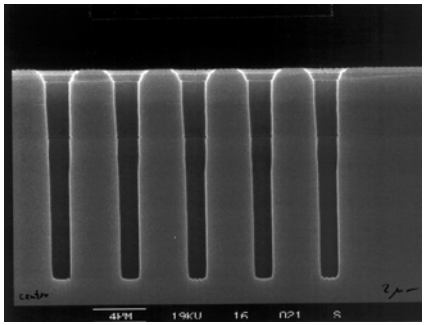
## Vertical System Integration

- Basic 3-D Integration Technology
  - Metal system for electrical path (interconnects)
  - Mechanical bond of silicon layers
  - Fabrication of Through Silicon Vias (TSV)
  - Wafer or Die Bonding Technology

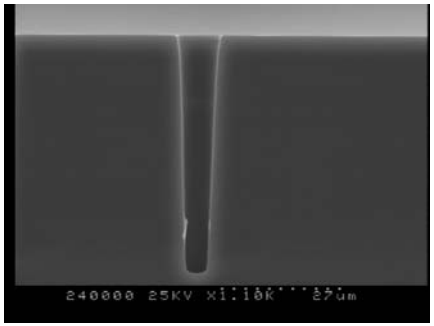


# Via Formation for VSI – *Via Etching*

| 1.0 | 2.0 | 3.0 | 5.0 | 10 | 100 | Via-Diameter [µm] |
|---|---|---|---|---|---|---|



16 µm,
8:1

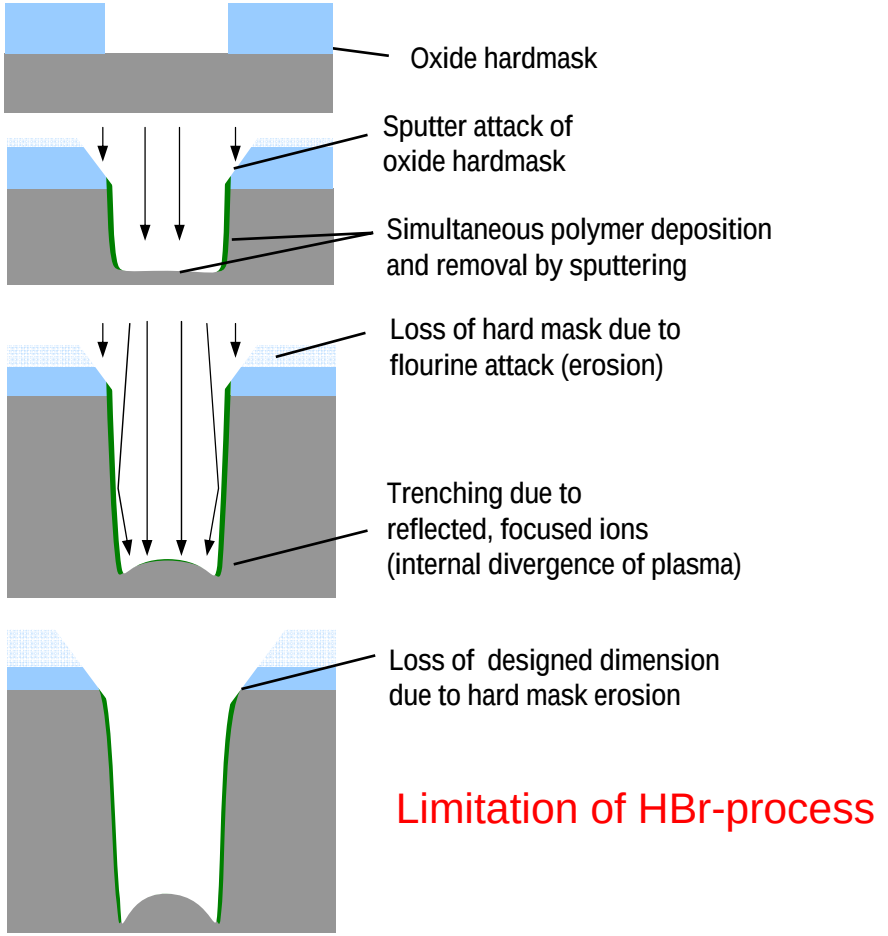


40 µm,
4:1

Etch Capability
IZM-M

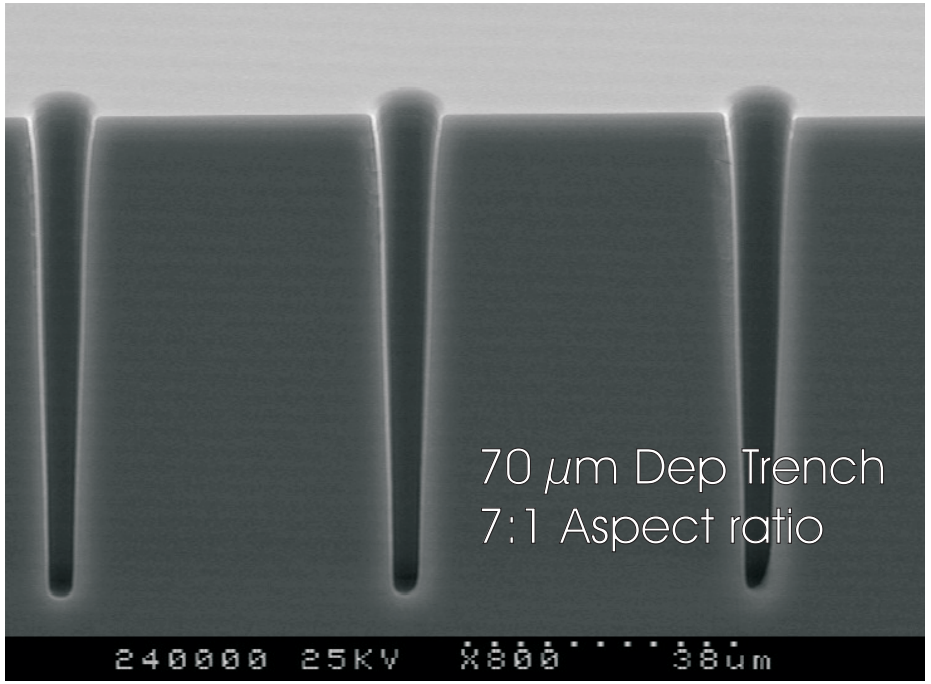
| 10 | 16 | 20 | | 40 | 60 | 70 | Via-Depth [µm] |
|---|---|---|---|---|---|---|---|
| 10:1 | 8:1 | 7:1 | | 4:1 | 6:1 | | Aspect Ratio |

# 3-D Integration of ICs




Limitation of HBr-process

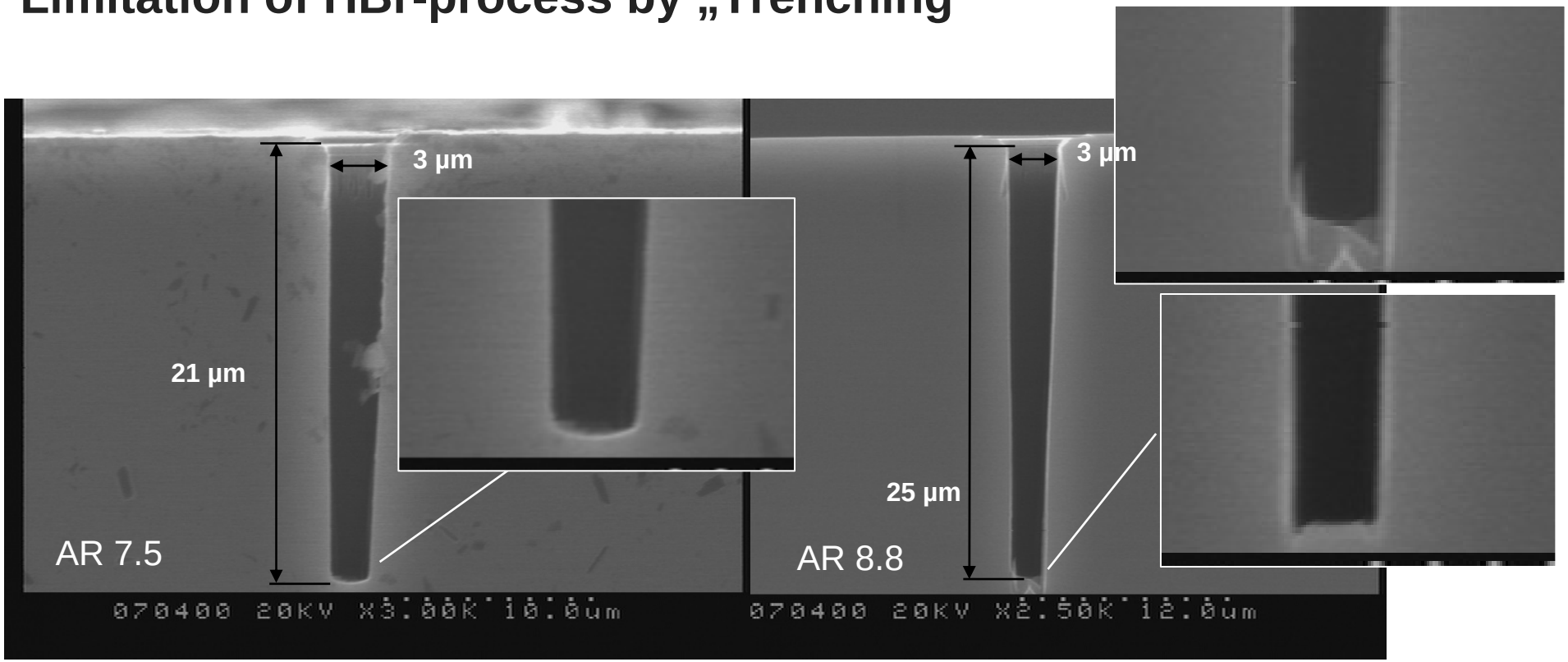
Applied Materials Equipment:
Etch chemistry based on
HBr / NF3 / He-$O_2$-Mix




by Armin Klumpp

Fraunhofer Institut Zuverlässigkeit und Mikrointegration

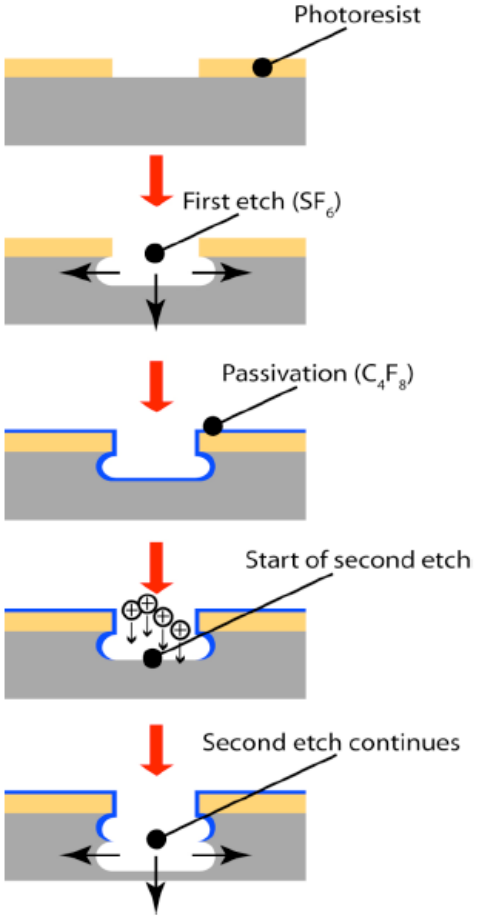
# Limitation of HBr-process by „Trenching

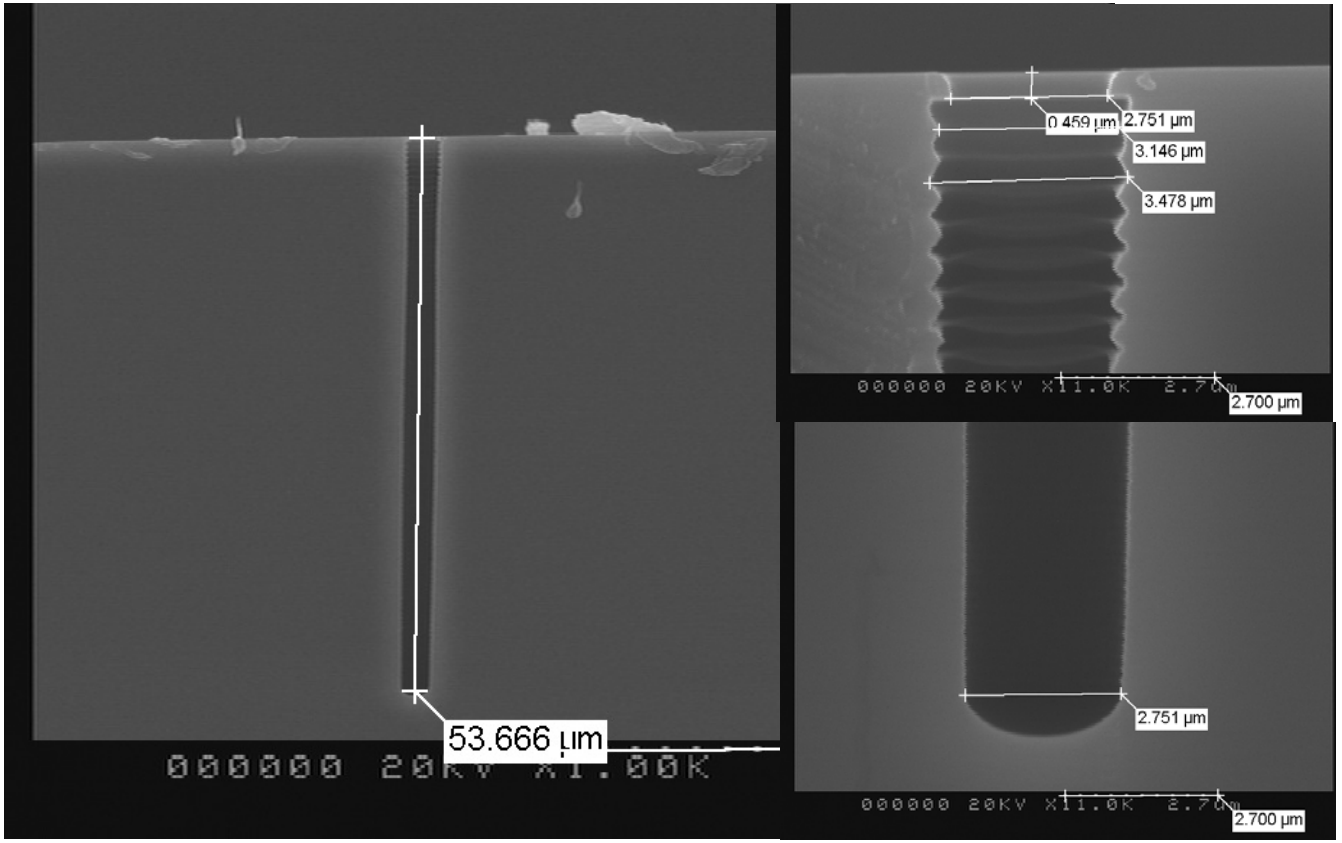



by Armin Klumpp
R. Wieland

Fraunhofer Institut Zuverlässigkeit und Mikrointegration

# 3-D Integration of ICs




*Sketch-Ref.: F. Roozeboom et al., 'Deep Reactive Ion Etching in Through-Silicon Via Technology', in '3D Interconnect and Packaging Technology', P.E. Garrou, P. Ramm and C.A. Bower, editors, J. Wiley, New York, 2007*

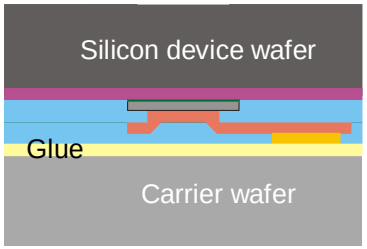
by Armin Klumpp

IZM
**Fraunhofer** Institut Zuverlässigkeit und Mikrointegration

Vertical Integration Technologies for HEP and Imaging Sensors
Workshop Ringberg, April 6-9, 2008

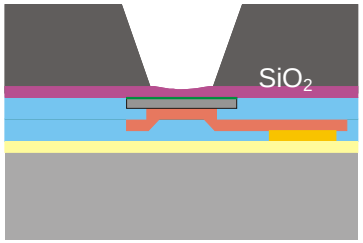
# 3-D Integration of ICs

- Small angle tapered sidewalls by simultaneously applying etch gas SF6 and passivation gas C4F8

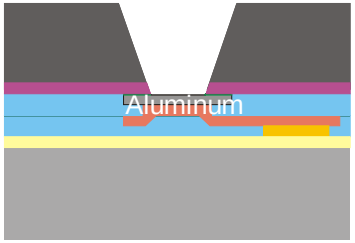



(a)

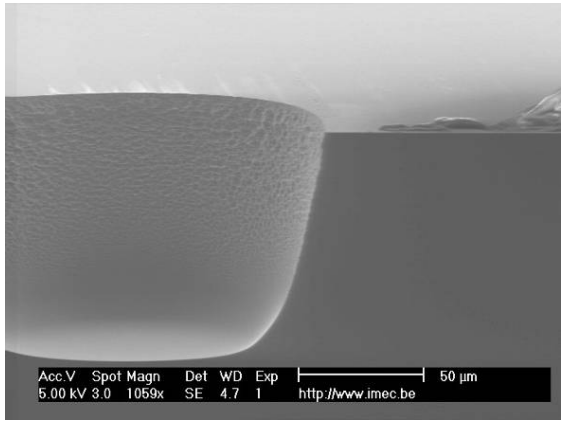
(b)




(c)



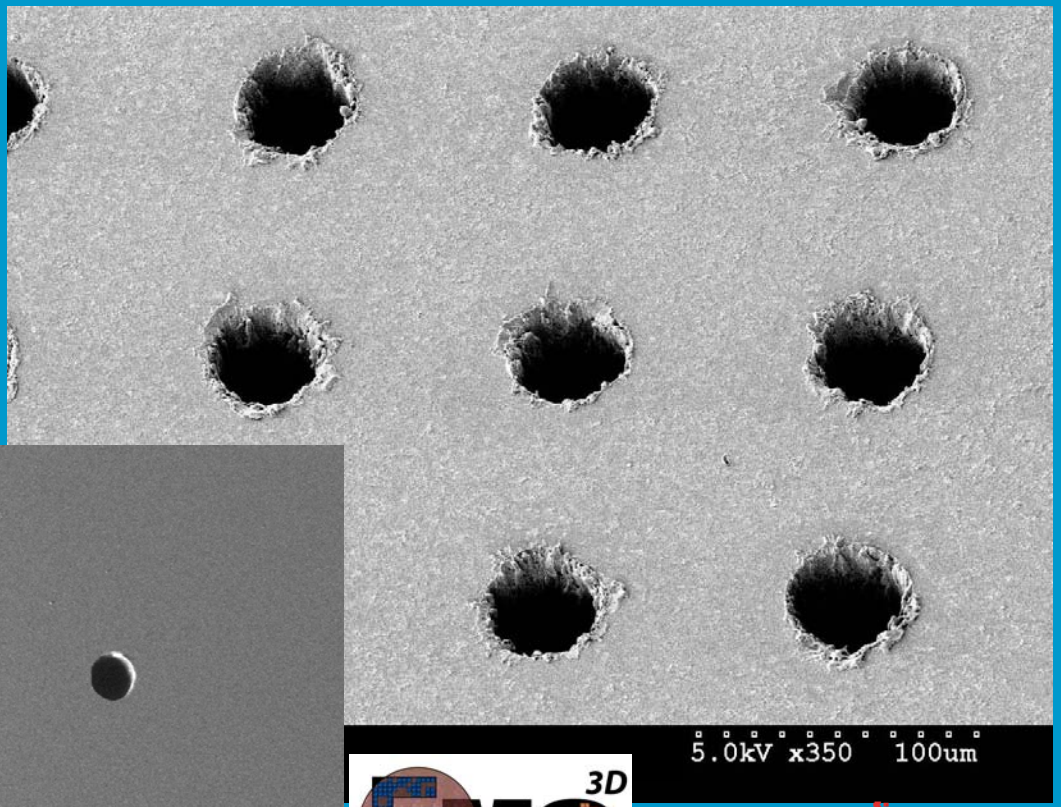

(d)

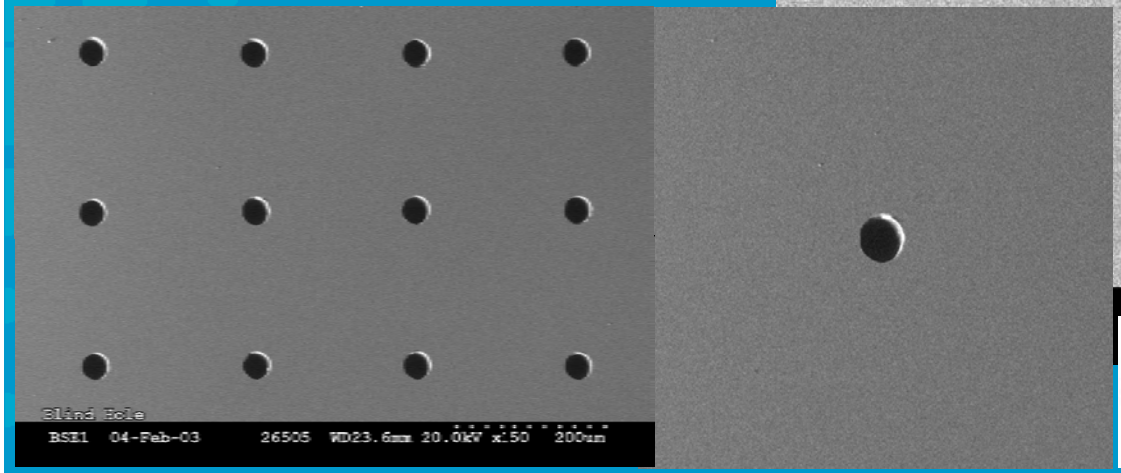



*Ref.: IMEC in e-CUBES, IST-026461, deliverable report D 2.2.2 and D 2.2.5*

# 3-D Integration of ICs

- 25 um diameter,
- 700 micron thick Si.
- Debris around entrance removed with post machining etch




3D EMC
Semiconductor 3-D Equipment and Materials Consortium

XSiL Enable

by Armin Klumpp

IZM
Fraunhofer Institut Zuverlässigkeit und Mikrointegration

Vertical Integration Technologies for HEP and Imaging Sensors
Workshop Ringberg, April 6-9, 2008

# Via Formation for VSI – *Via Metal Filling*

1.0 µm 3.5 µm 5 µm 10 µm .... 100 µm Via-Diameter

CVD of
- copper
- tungsten
- TiN

Electroplating of
- copper

&

PVD of Seedlayer
- Ti:W / Cu

Process for filling

new !

Electroplating of
- copper

&

CVD of Seedlayer
- tungsten

10 µm
10:1 3:1 2:1 ..

70 µm .... 100 µm Via-Depth
7:1 1:1 Aspect Ratio



# Material Properties – *Via Metal Filling and Intermetallic Compound*

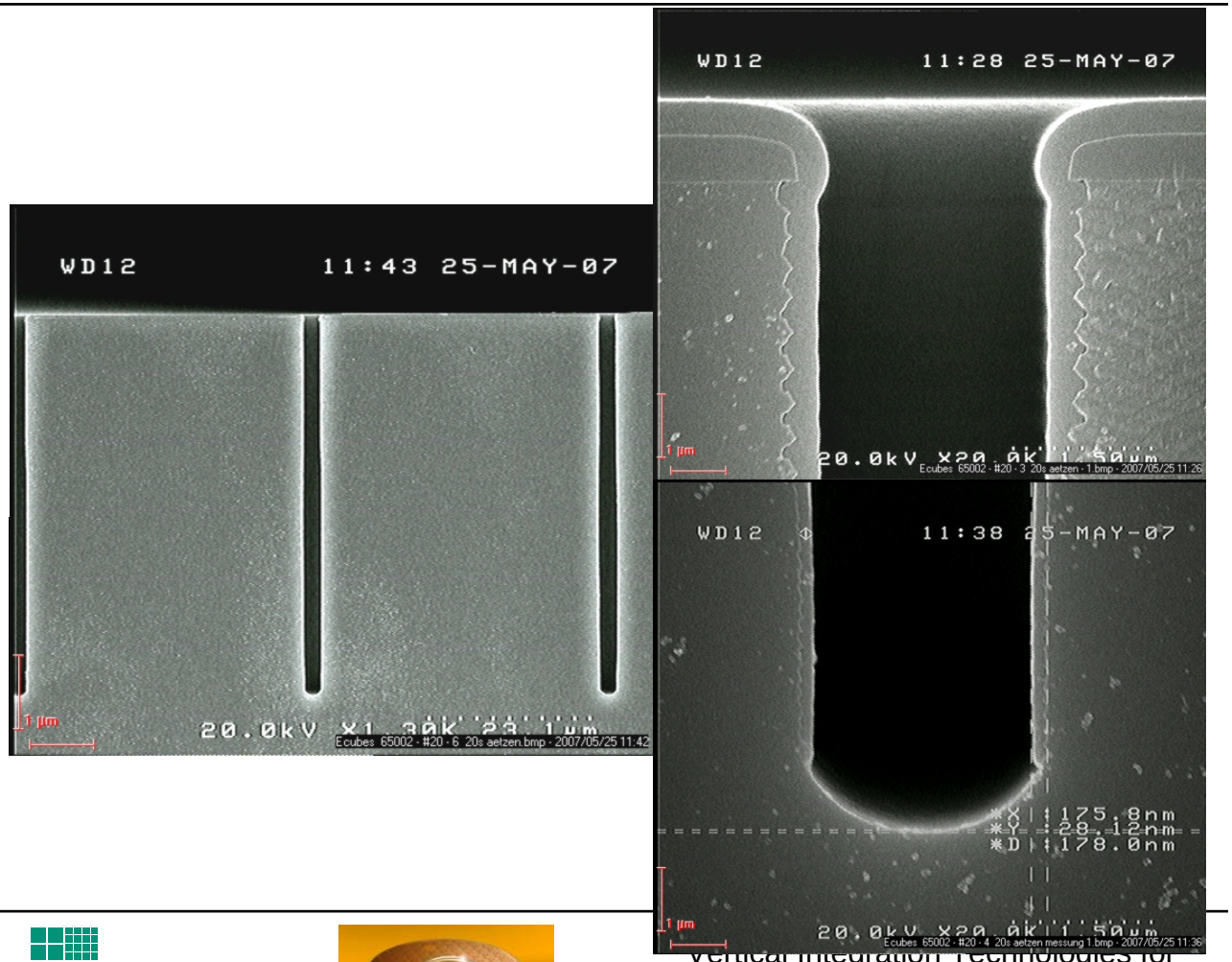
| Material | E [MPa] | Poisson's Ratio | CTE [ppm/K] | $\sigma_y$ [MPa] | M [MPa] |
|---|---|---|---|---|---|
| Cu | 90.000 | 0.35 | 16.5 | 180 | 6.600 |
| Cu3Sn | 100.000 | 0,3 | 18.0 | *480* | *5.800* |
| AlSiCu | 50.000 | 0.3 | 24.0 | *190* | *1.400* |
| W | 145.000 | 0.28 | 4.4 | *1600* | *10.000* |
| Si | 168.000 | 0.22 | 2.8 | - | - |
| SiO2 | 75.000 | 0.28 | 0.55 | - | - |

Measured Material Properties, all material properties are given at room temperature

*Ref.: IZM in e-CUBES, IST-026461*

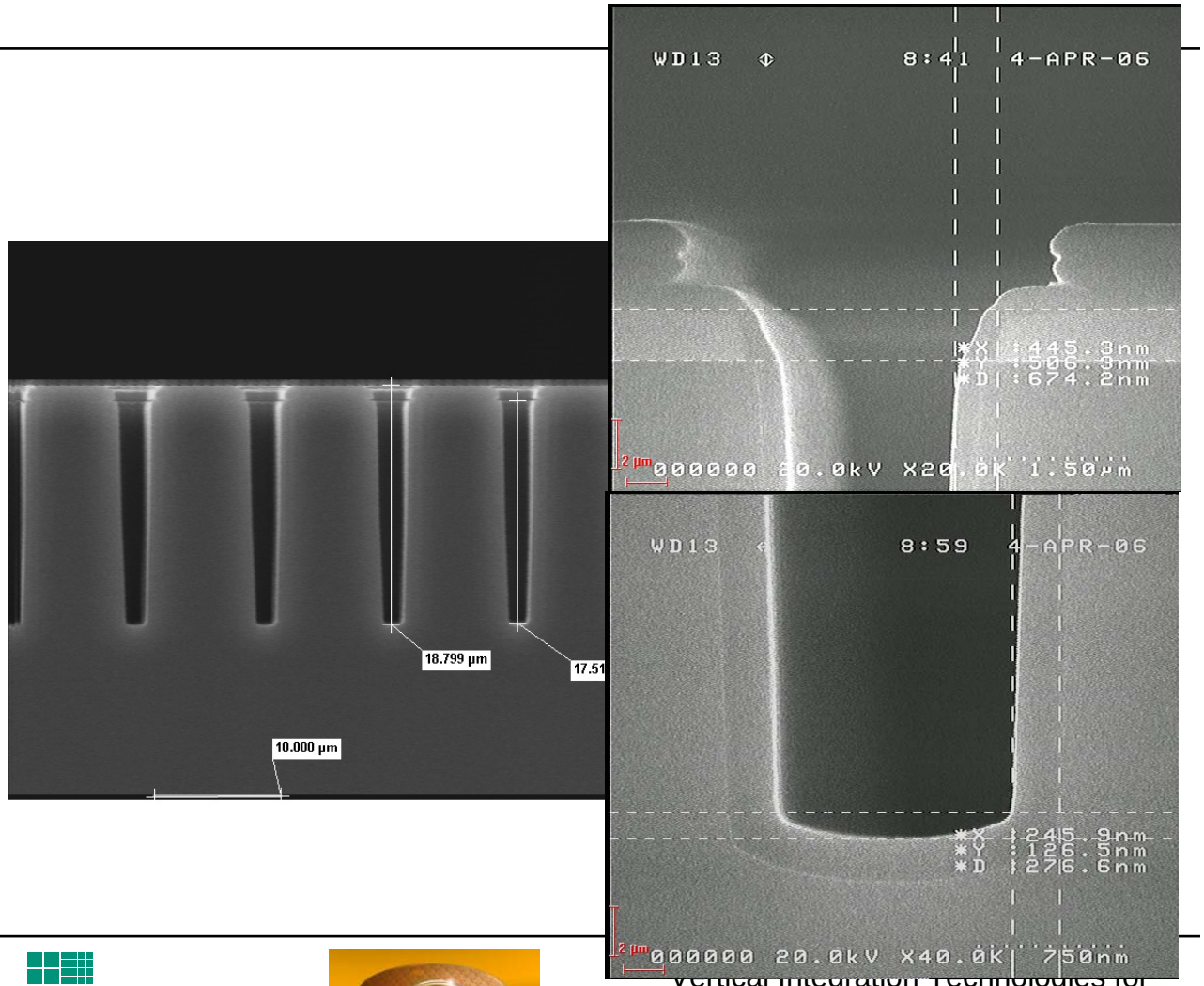
# 3-D Integration of ICs

- **SA-CVD O3/TEOS oxide after Bosch process**
- **Conformity of ~43 % -**
- **AR >16:1; taper angle of the trench hole ~ 89.5 - 90°**



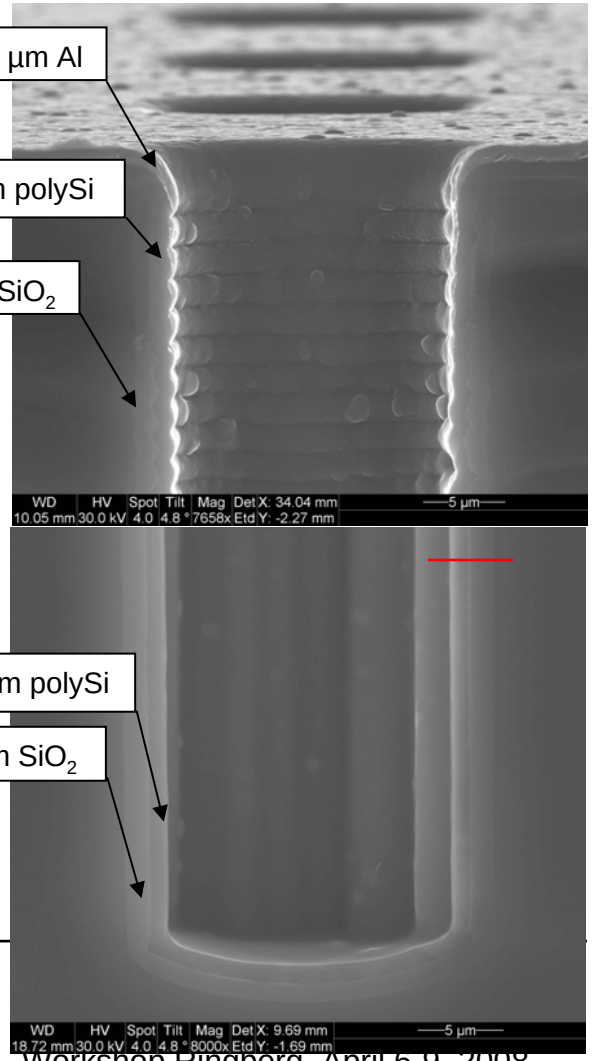
# 3-D Integration of ICs

- **Thermal Oxidation**
- **Conformity of ~55 % -**
- **AR >6:1; taper angle of the trench hole ~ 89 °**



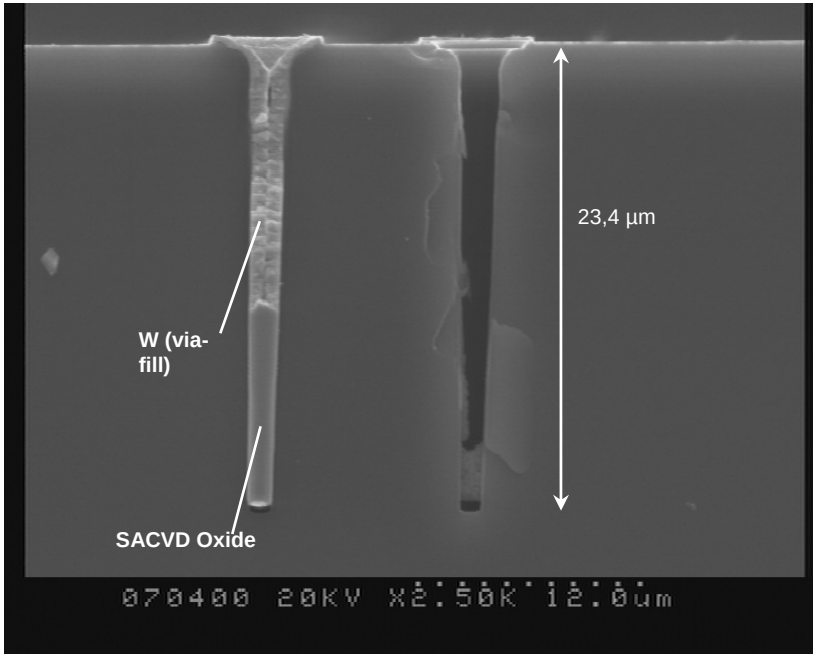
# 3-D Integration of ICs

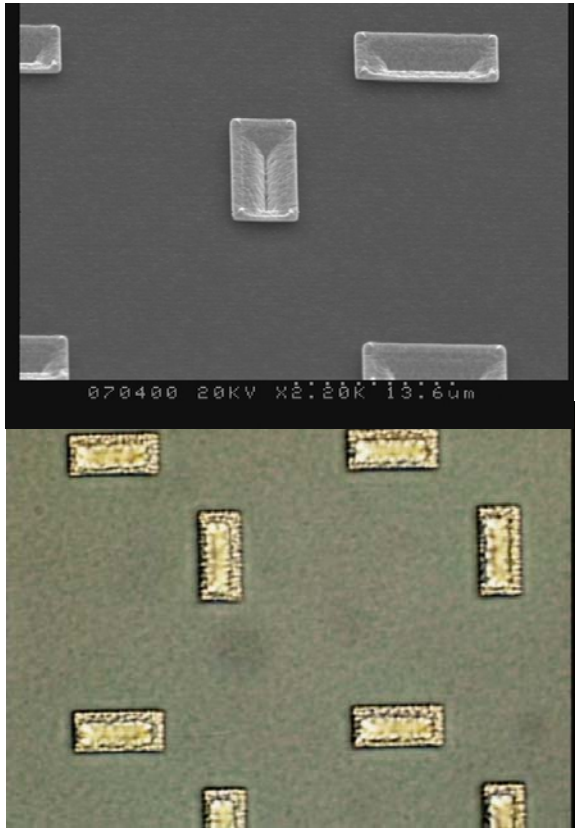
- **Bosch process**
- **AR >16:1**
- **taper angle of the trench hole ~ 89.5 - 90°**
- **Thermal oxidation & poly-Si deposition with conformity of ~100 %**




*Ref.: SINTEF in e-CUBES, IST-026461, deliverable report D 2.2.5*

## Tungsten filled ICVs



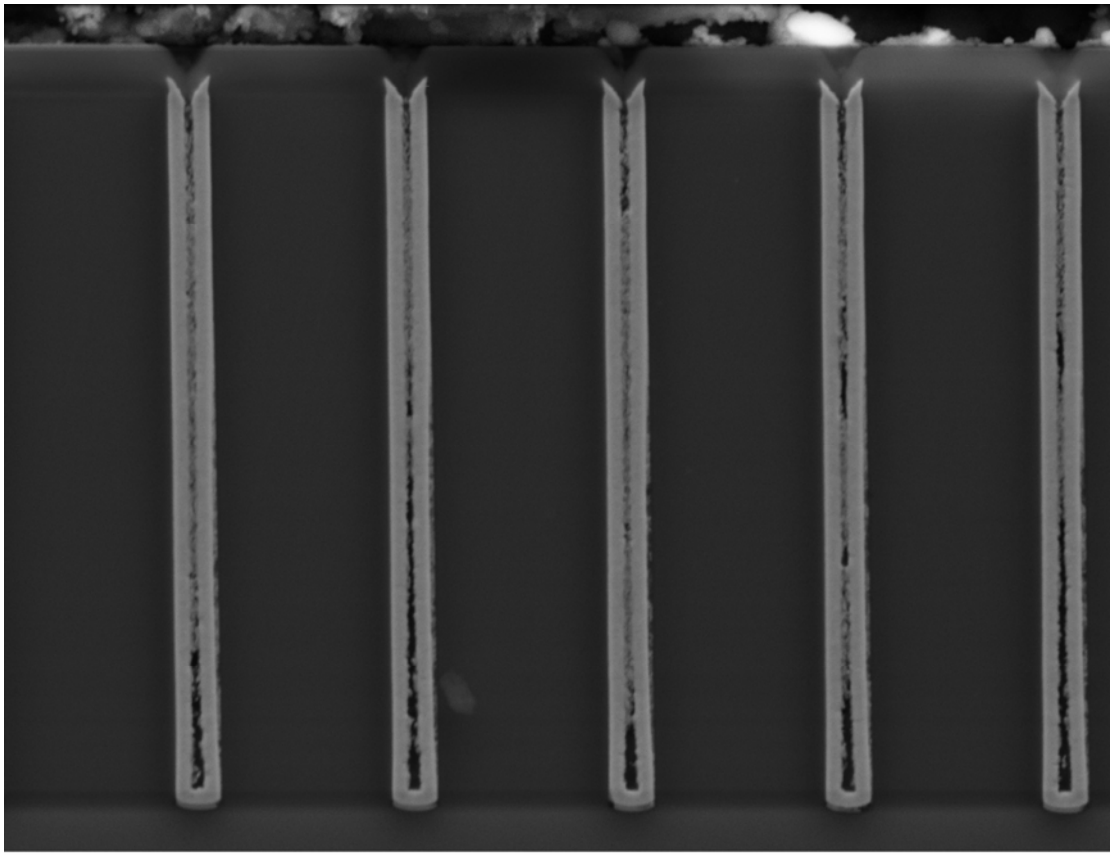






# W- Fill of High Aspect Ratio Trench

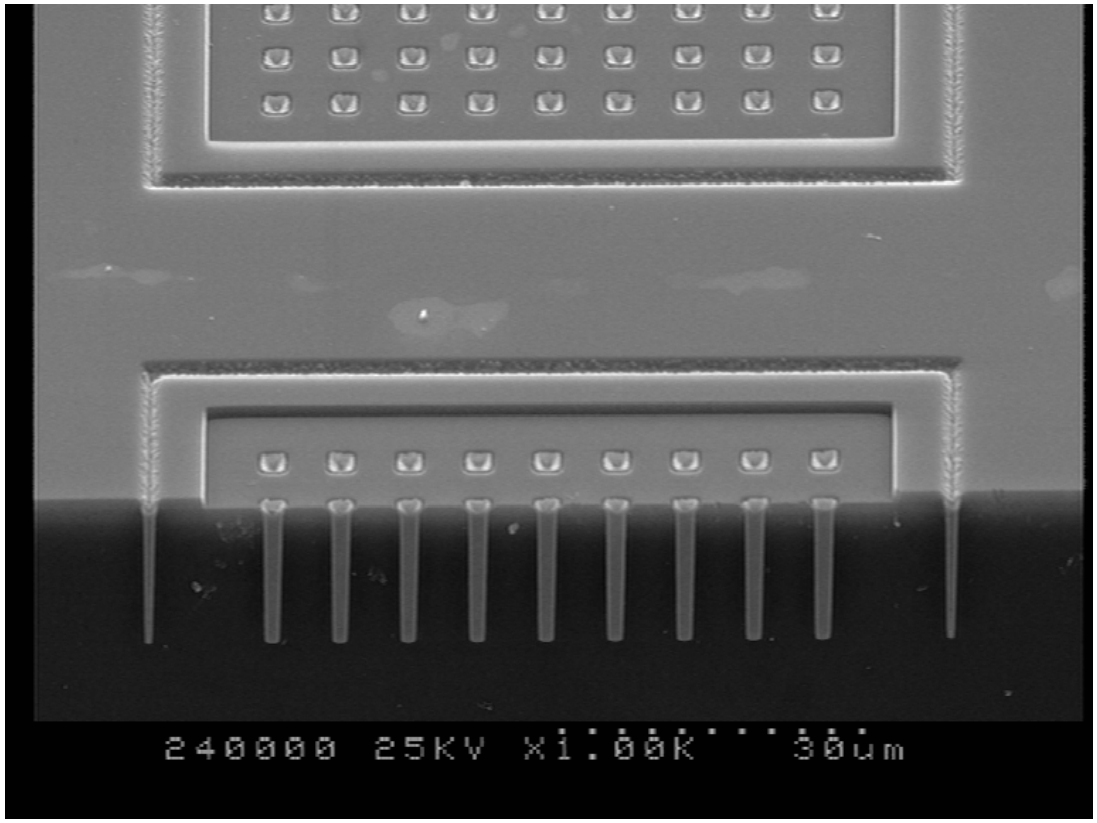
ICV-Dimensions:
3 µm x 10 µm x 50 µm

300 nm SACVD TEOS
20 nm TiN CVD
900 nm W CVD und W Backetch
800 nm M1 (AlSiCu, structured)
850 nm PN/POX (Passiviation)

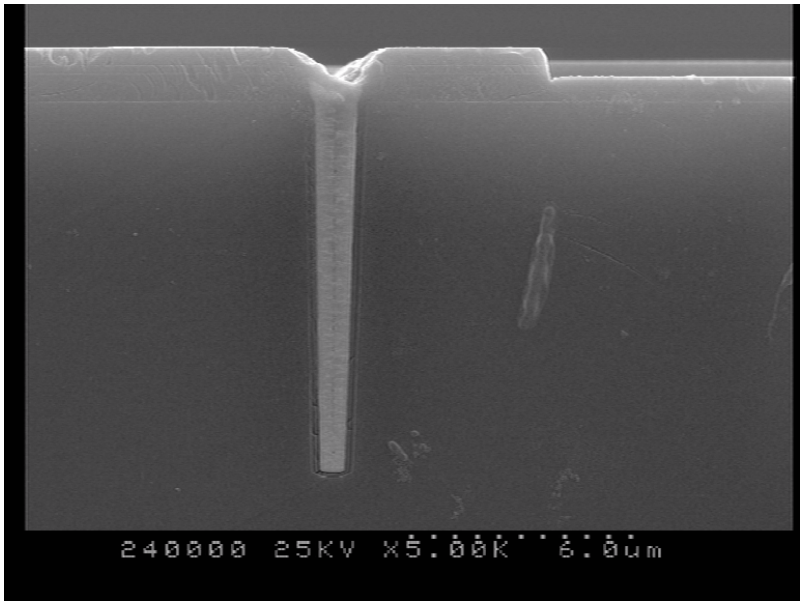





# WL-CS-3D *- „low – Accuracy Placement“ Layout (1)*

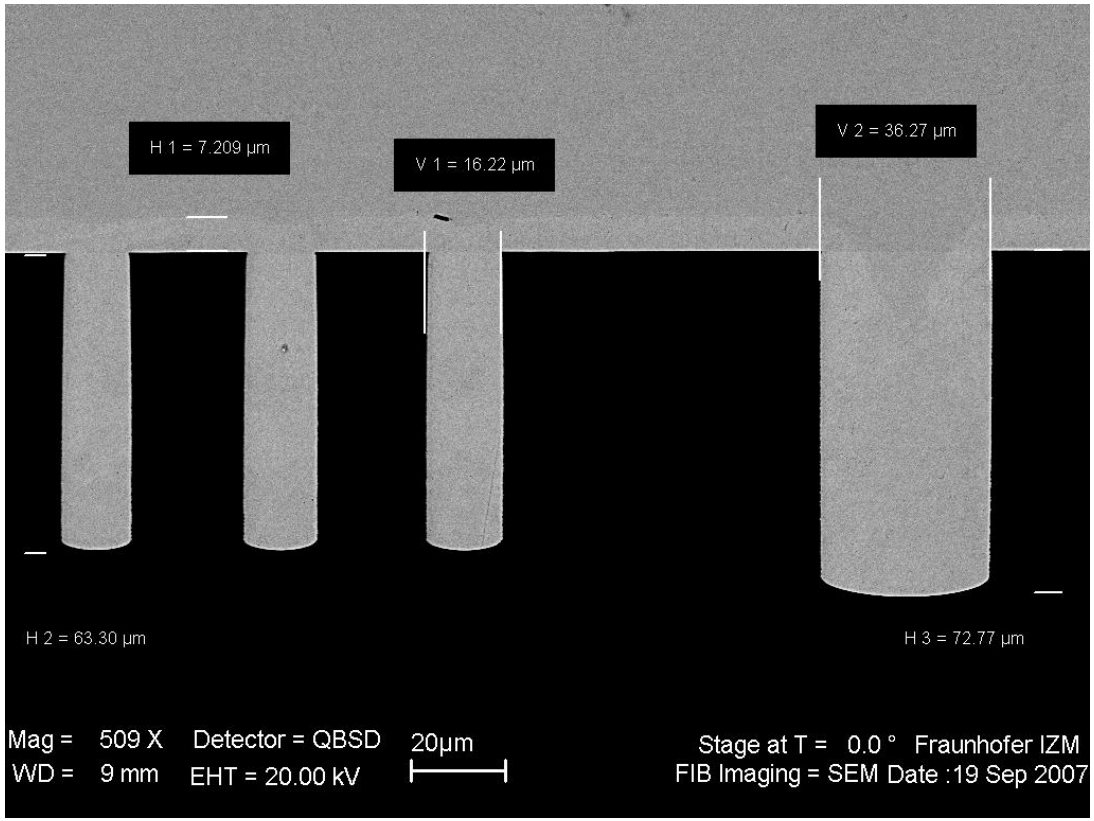



- Pin-Array and Isolation trenches
- combination of contact printing with stepper lithographie is possible



# Copper Electroplating *(1)*

- Cu Filled TSV by Electrodeposition
- Via Size. diameter 18/35 µm
- Depth  63/72 µm
- AR 3.5 / 2.05
- Seed layer sputtered Ti:W/Cu

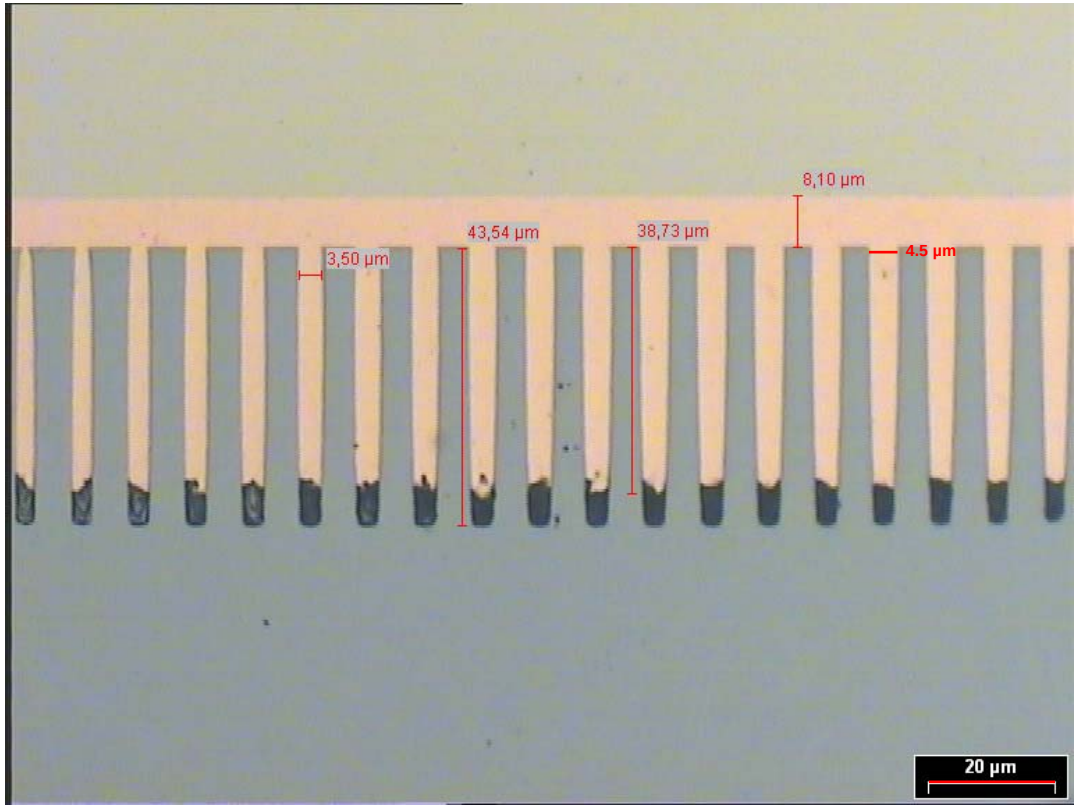



*Ref.: IZM-Berlin; Jürgen Wolf*

# Copper Electroplating *(2)*

Process Limitations
with sputtered seed layer

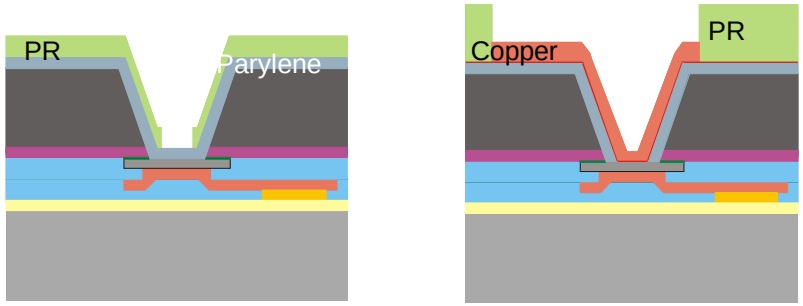
- Cu Filled TSV by Electrodeposition
- Via Size. diameter 4.5 µm
- Filling-Depth ~35 µm
- Filling-AR 7.7
- Seed layer sputtered Ti:W/Cu

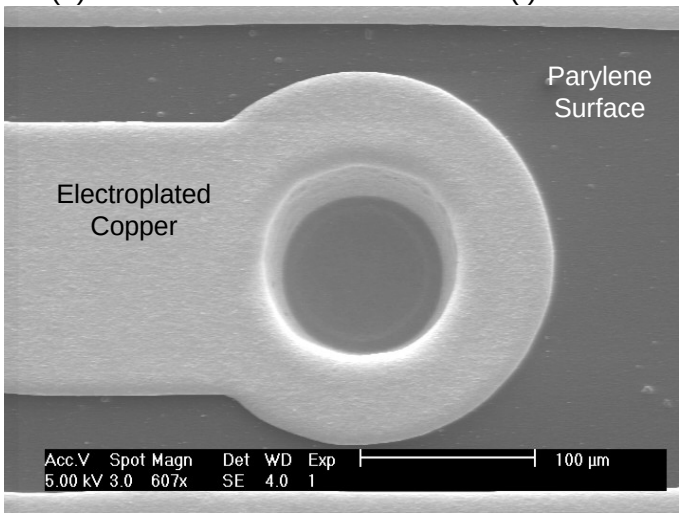



*Ref.: IZM-Berlin; Jürgen Wolf*

# 3-D Integration of ICs

- Example from IMEC
- Glue requires evaporation deposition of parylene as isolation
- Access to device pad from backside
- Metallisation is performed as copper electroplating
- Via diameter: 140 µm (top) and 100 µm (bottom)

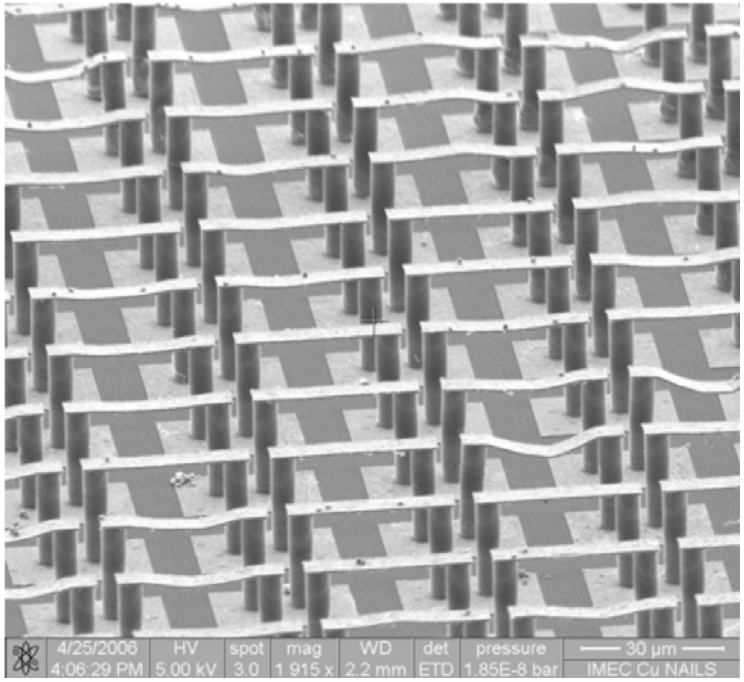



*Ref.: IMEC in e-CUBES, IST-026461, deliverable report D 2.2.5*

# 3D-Interconnection

- Example from IMEC
- Copper / copper bond
- 25 µm depth at via Ø 5 µm




reference: http://imec.be/wwwinter/mediacenter/en/SR2006/681446.html

# *Concepts for Integration and Handling*

by Armin Klumpp

Fraunhofer IZM
Institut Zuverlässigkeit und Mikrointegration

Vertical Integration Technologies for HEP and Imaging Sensors
Workshop Ringberg, April 6-9, 2008

# *Concepts for Integration and Handling*

- Tightly connected
  - to avoid handling of thin material (< 100 µm)
  - to achieve processing accuracy (via diameter, via depth, alignment accuracy of vias)
  - to minimize number of critical process steps
  - to reduce risk of critical process steps
  - to avoid processing of single chips
- Different for two different types of basic substrates: SOI or Bulk-silicon
- Via-Formation
  - after backend-of-line (processing on standard substrate thickness; add-on from external service)
  - after first metal layer of device
  - integral part of front-end-of line
  - after thinning; access to device pads from backside
  - after tinning and bonding to base substrate (equal wafer layout [chip size; chip pitch])



# *Concepts for Integration and Handling*

- Device orientation
  - face down (face-to-face, f2f)
  - face up (back-to-face, b2f)
- Type of device transfer
  - wafer-to-wafer (w2w)
  - chip-to-wafer in single chip mode (flip-chip assembly tool)
  - chip-to-wafer with intermediate handling substrate
    - temporary glueing layer
    - electrostatic force



# *Concepts for Integration and Handling*

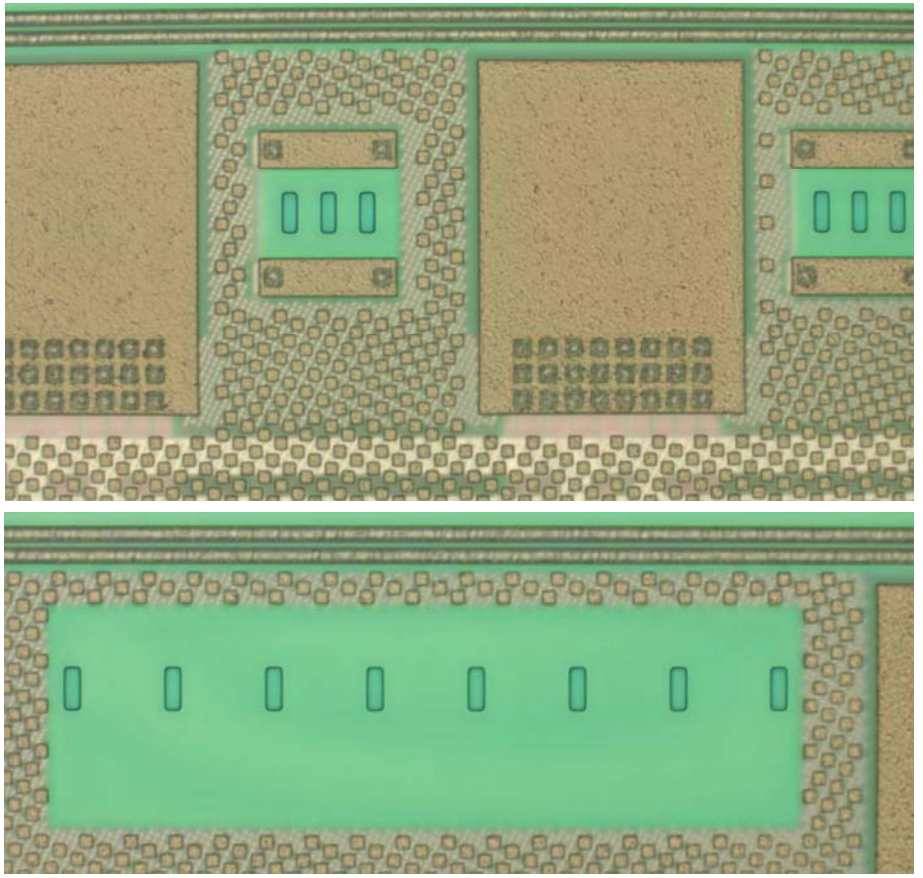
- Electrical interconnection
  - Copper / copper
  - SLID-intermetallic compound
  - Solder ball (e.g. SnAg-µbumps)
  - Au-stud bumps

- Mechanical interconnection between layers
  - Copper / copper
  - SLID-intermetallic compound
  - underfiller
  - Polymeric glue



## Through-Silicon-Vias in Device Chip

- i-line stepper lithography of IZM adapted to delivered wafer with Transceiver-Chips
- 3 µm x 10 µm TSVs in resist

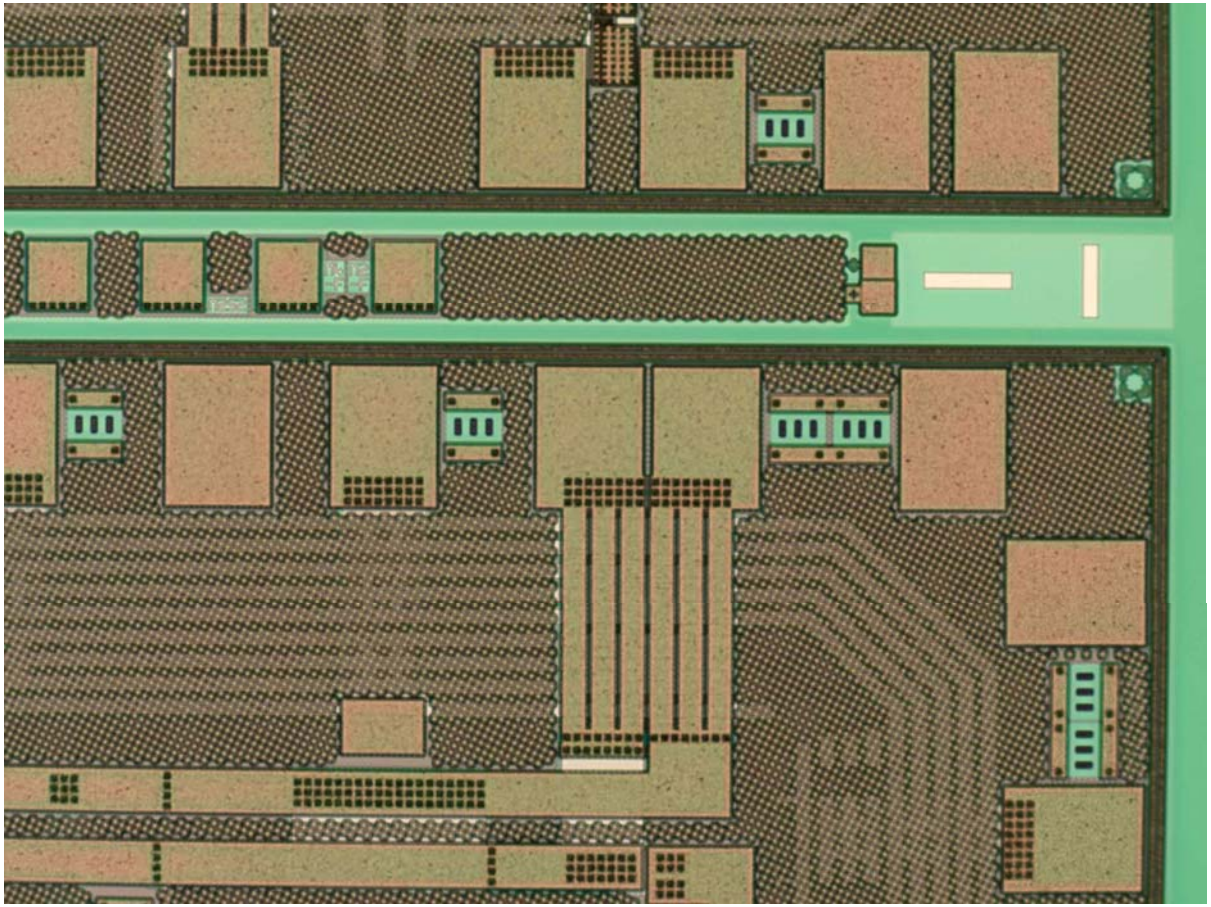


*Ref.: IZM in e-CUBES, IST-026461*



## Through-Silicon-Vias in Device Chip

- i-line stepper lithography of IZM adapted to delivered wafer with Transceiver-Chips
- 3 µm x 10 µm TSVs

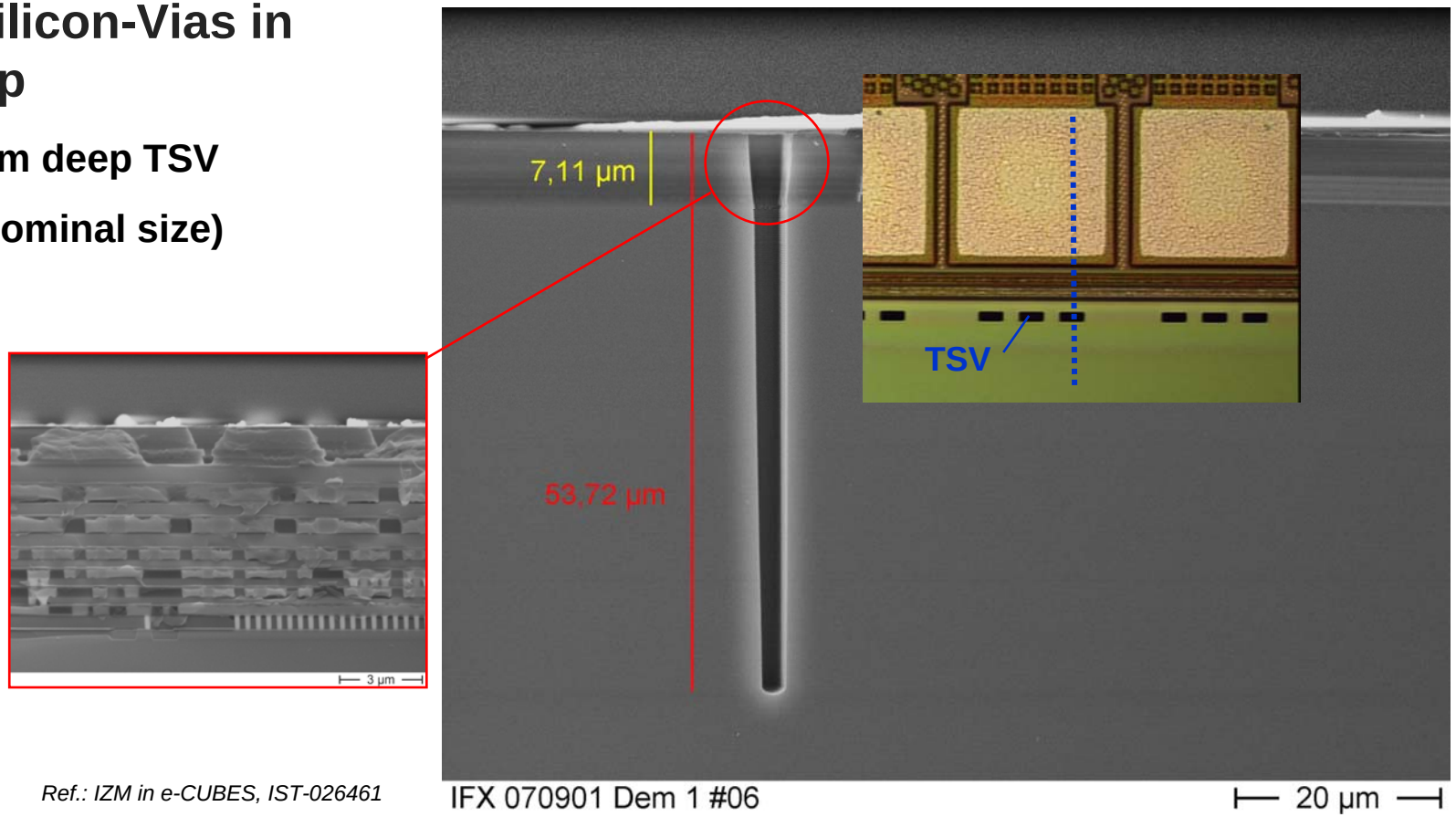


*Ref.: IZM in e-CUBES, IST-026461*



## Through-Silicon-Vias in Device Chip

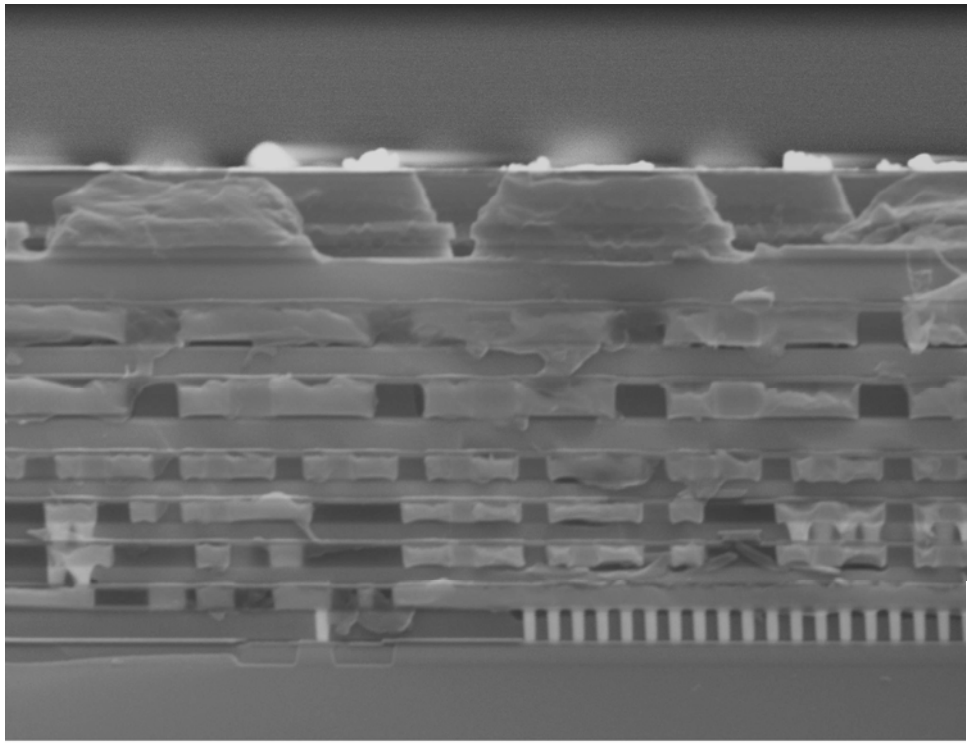
- **SEM of 54 µm deep TSV**
- **10 x 3 µm (nominal size)**




*Ref.: IZM in e-CUBES, IST-026461*

## Keypoint Low Cost

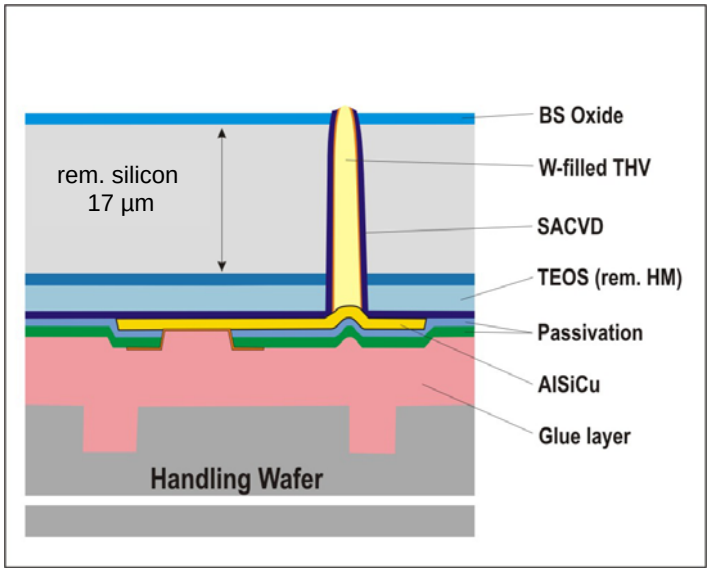
- 3D-Integration as Via-Last Concept after regular Backend-Processing
  - Thick and mixed Intermetal-Dielectrics to be etched before TSV formation in silicon
  - ☞ Formation of TSV before first metal layer would reduce process complexity and formation cost

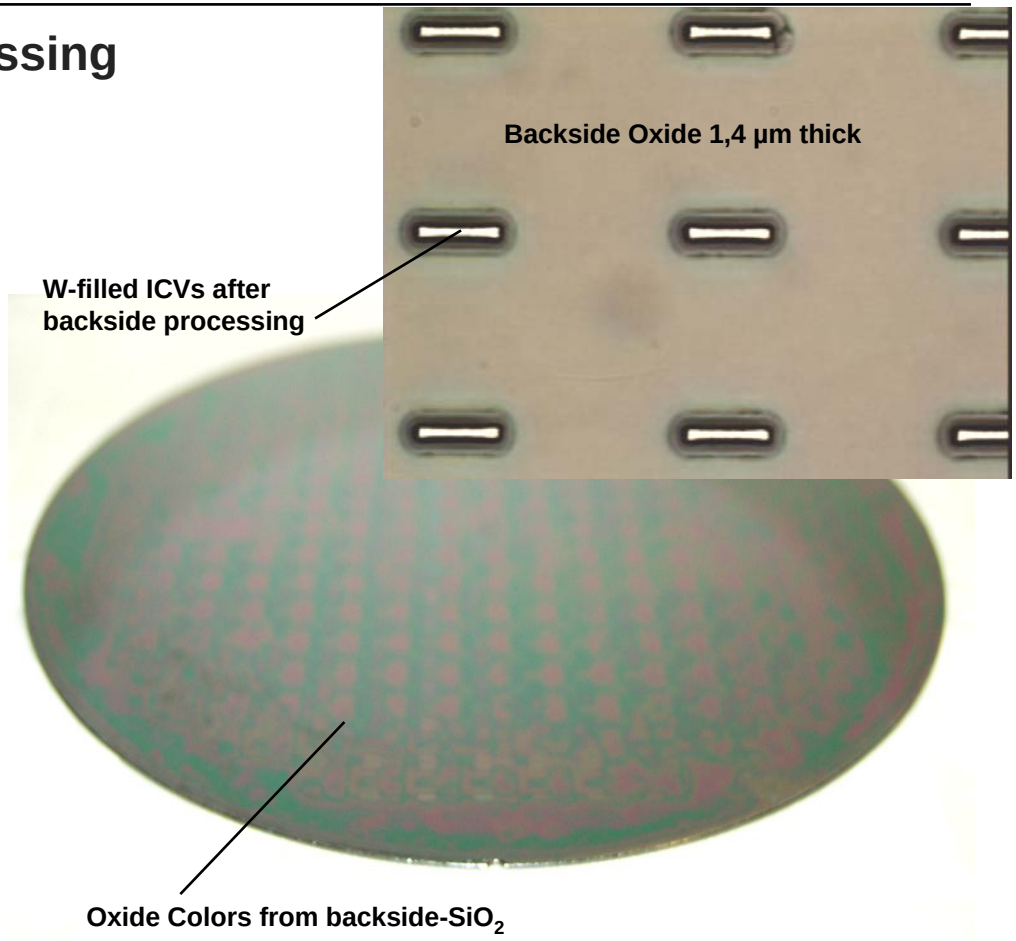




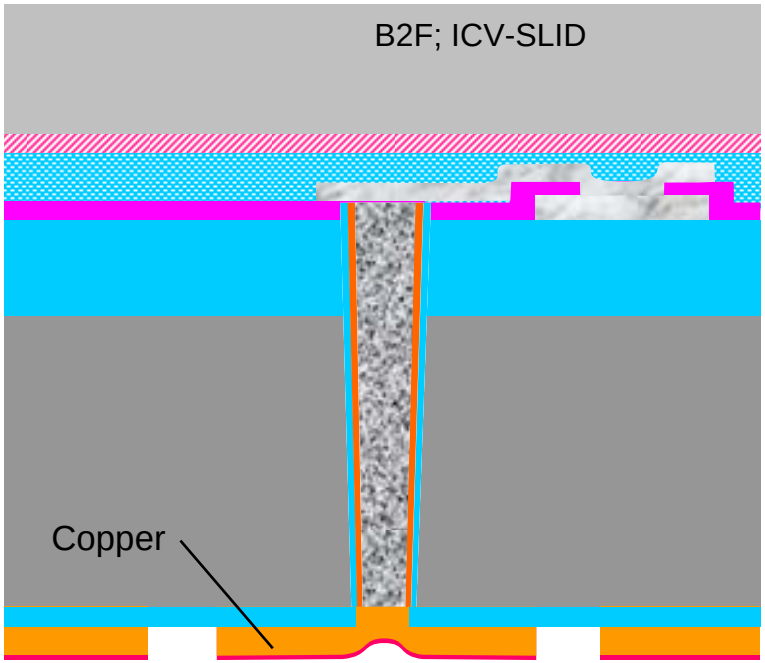

## B2F-HW–Stack during backside processing

- **Glued to handling wafer**
- **Thinning of wafer until opening of TSV**
- **Backside plasma-oxide deposition**
- **CMP-Opening of oxide on inter chip via**





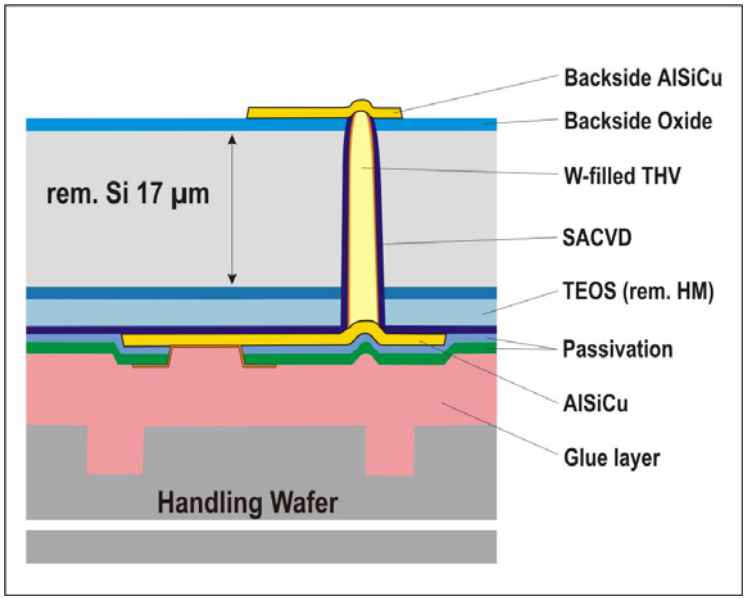

## ICV-SLID Technology

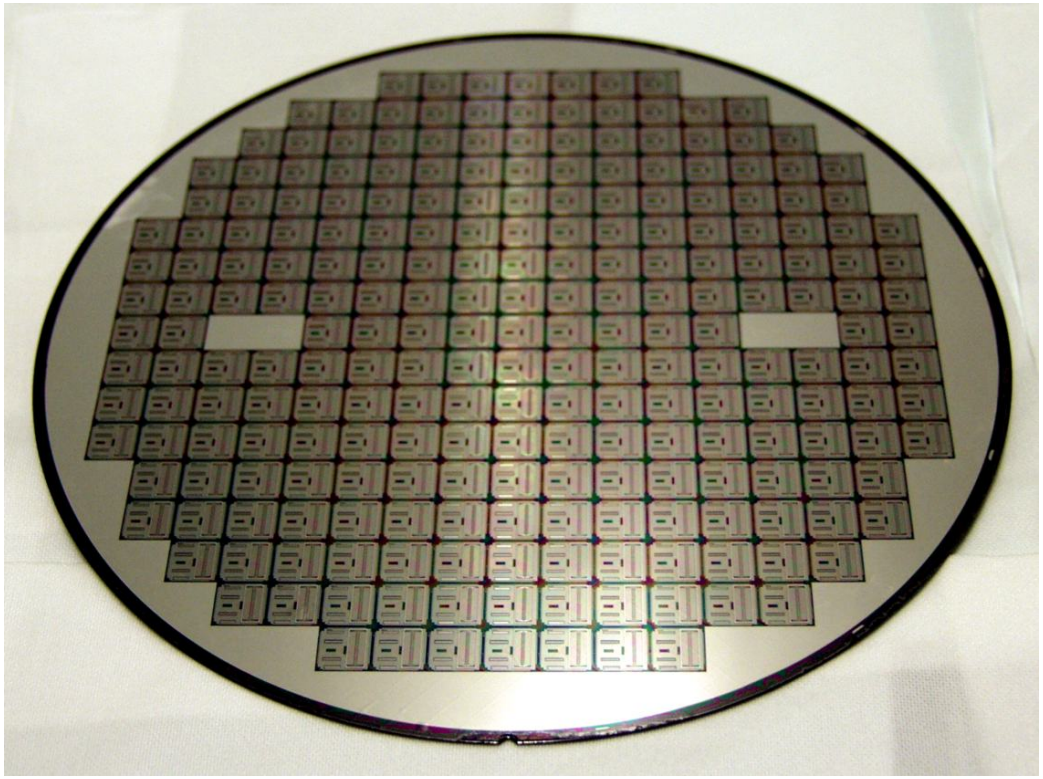
- Fabrication of Tungsten-filled InterChip Vias on Top Substrate
- Via Opening and Metallization
- Thinning
- Opening of Plugs
- Electroplating



## B2F-HW–Stack after backside metallization

- **After backside metallization (AlSiCu)**
- **Stepper uses etched through alignment marks on thinned backside**
- **Electrical characterisation of ICVs**
- **Ready for SLID processing**





# Handling Concept
## for
## Thinning
## and Transfer

by Armin Klumpp

Fraunhofer Institut Zuverlässigkeit und Mikrointegration

Vertical Integration Technologies for HEP and Imaging Sensors
Workshop Ringberg, April 6-9, 2008

# Handling Concepts for Thin Silicon

## Bonding temporarily to a Handling Substrate

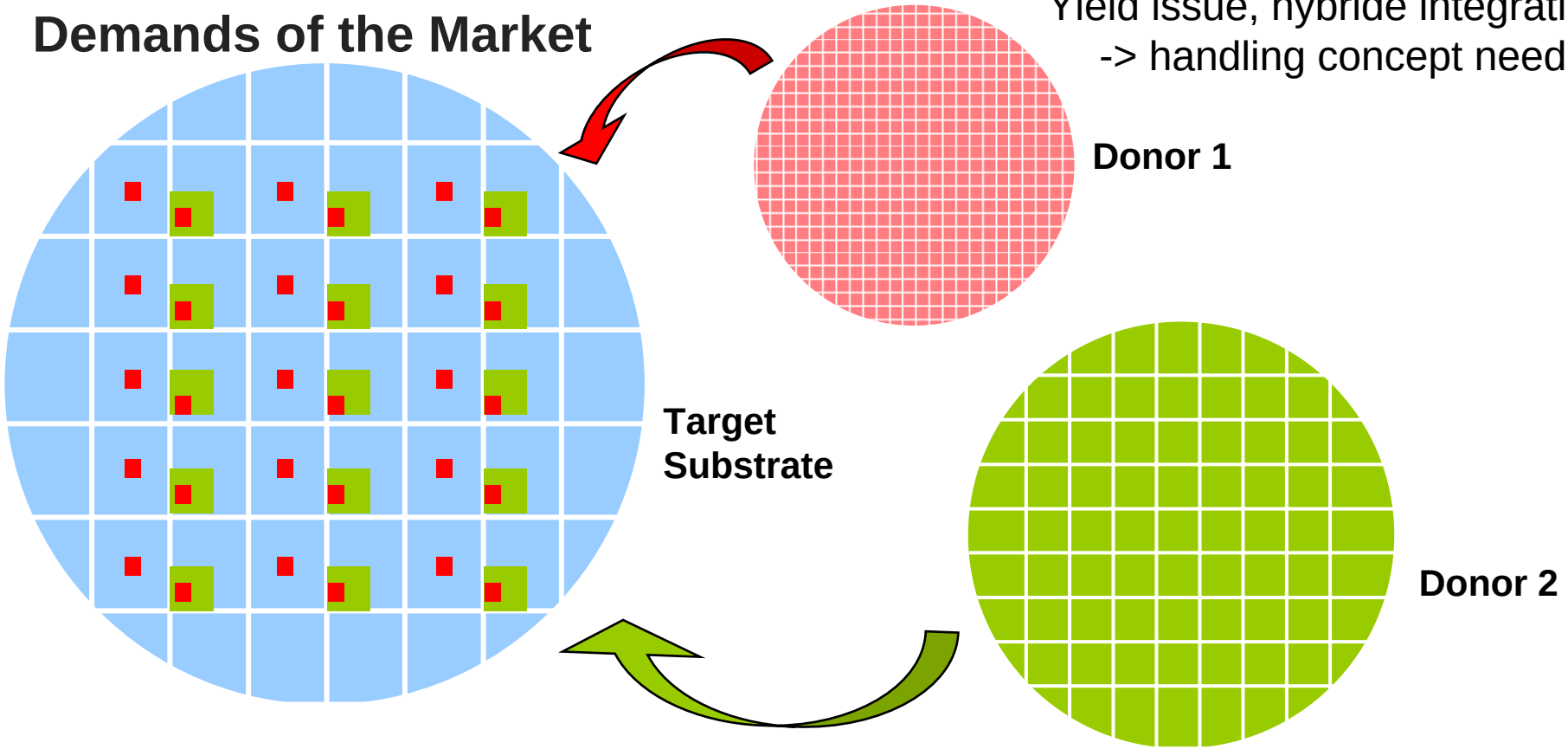
- Polyimide, BCB, porous Oxide (SOG), (Epoxy)
  - Backside Processing at elevated Temperatures; Difficult to Remove
- Thermoplastics, (Grinder Tapes)
  - Temperature limited Backside Processing; Easy to Remove

## Electrostatic Handling Substrate

- Ceramic E-Chuck Substrate
  - High Temperatures; Flatness and TTV Accuracy for precise thinning not available at large diameters
- Si-Based E-Chuck (Mobile Carrier)
  - High Temperatures; very well defined mech. parameters (TTV < 1 µm)
  - 200 mm, 300 mm & compatible to Front End Technology



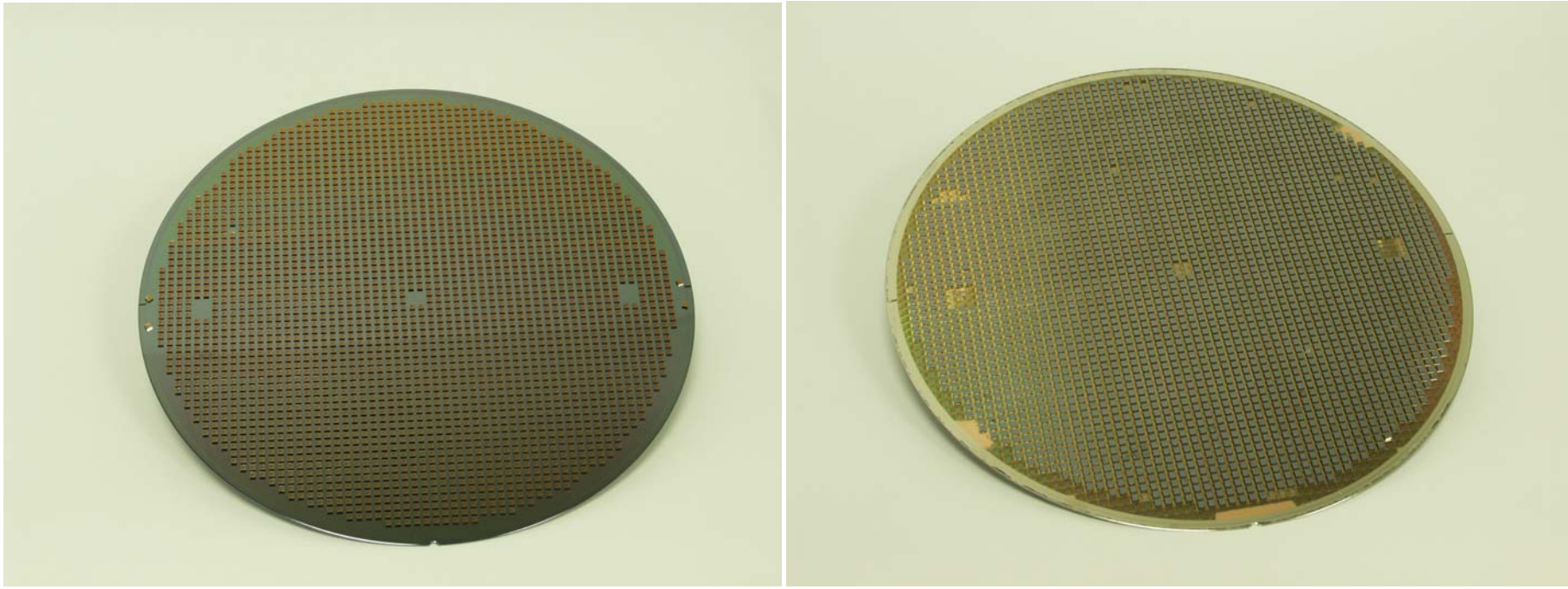
## Device Transfer
## Demands of the Market




by Armin Klumpp

Fraunhofer IZM Institut Zuverlässigkeit und Mikrointegration

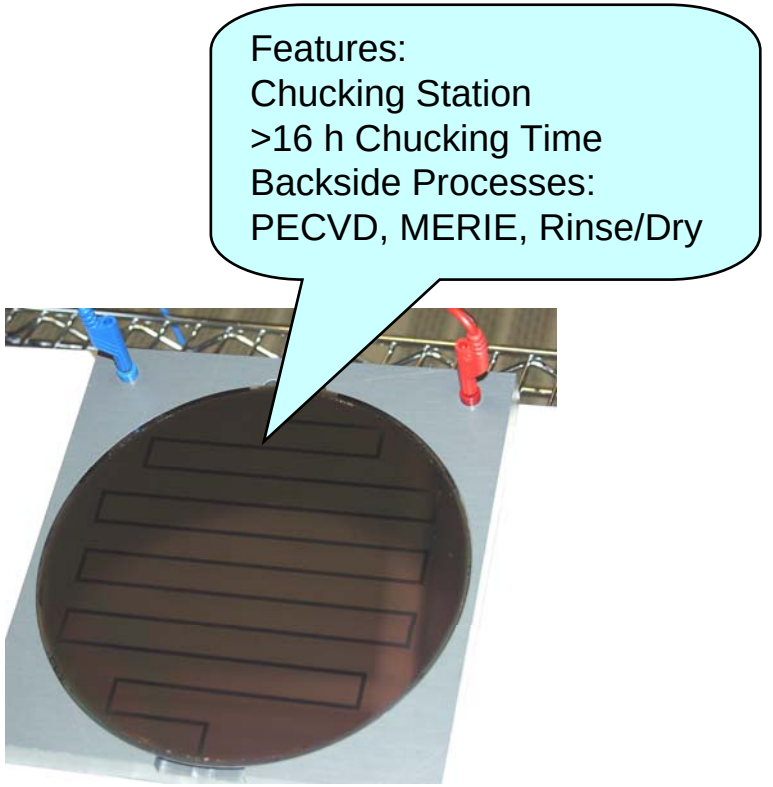
# VSI by Soldering: „Chip-to-Wafer“



Chip transfer: on handling substrate (left); on target wafer (right)

# Low Cost Handling Concept: E-Chuck on Si-Wafer

- **Mobile electrostatic carrier**
- **Prototype Electrostatic Chuck successfully tested (200 mm)**
- **Chucking Principle: Bipolar electrostatic**
- **Built on Si-Wafers, CMOS compatible**
- **Chuck-Wafer Thickness: 100 µm < d < 720 µm**



# Electrostatic-Chuck (3)

e-Chuck action: thin sample on chuck, without (left) and with (right) applied voltage

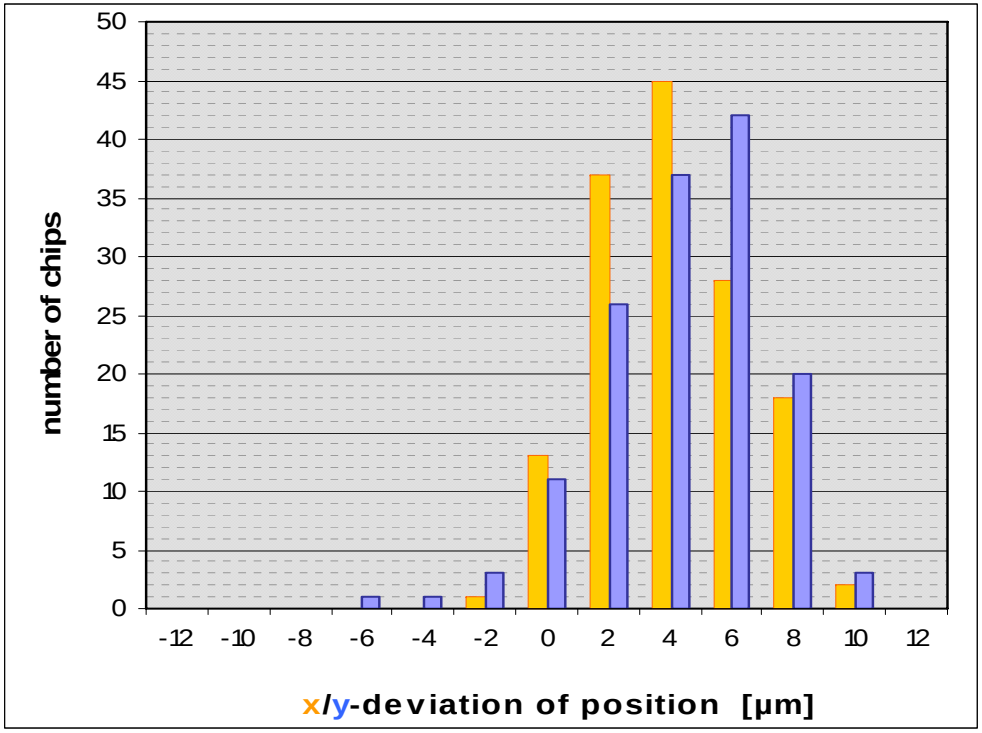


# Handling Concept

- Achievable adjustment acurracy with Datacon tool

  - Placement of chips at temperatures near 160°C (softening of the polymer glue)

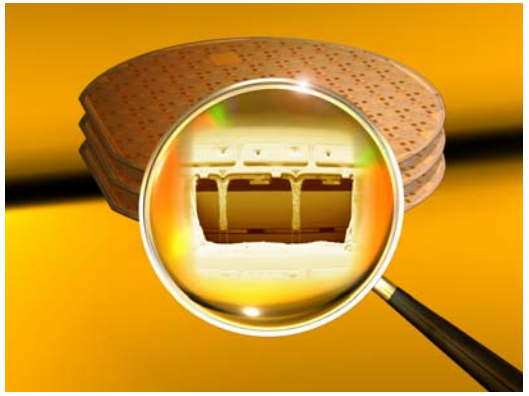
  - Displacement less than 10 µm in both directions






# Vertical System Integration

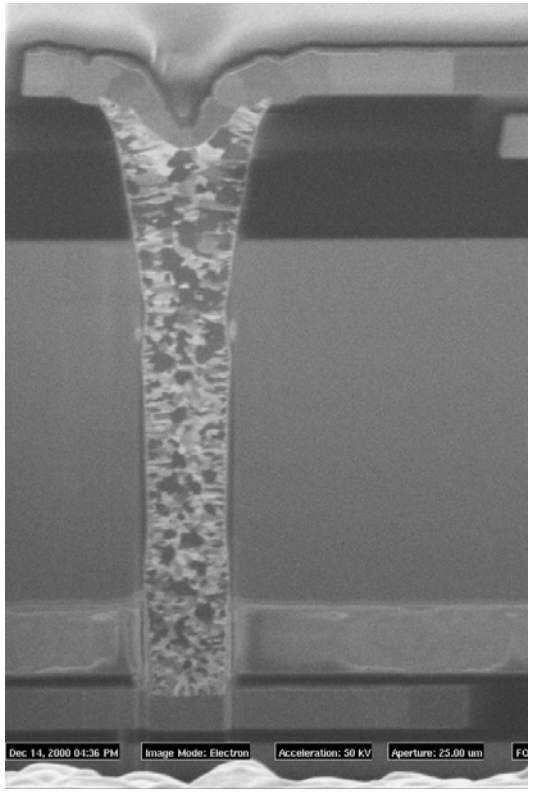
Electrical Characterization

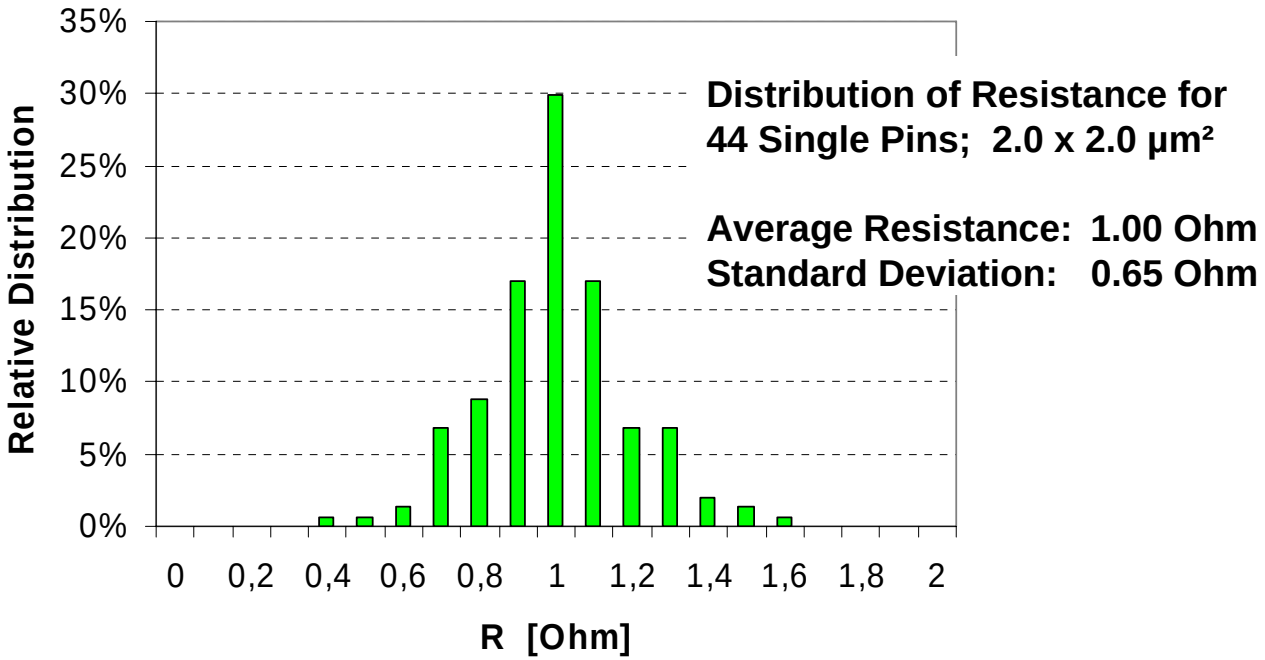


by Armin Klumpp

Fraunhofer Institut Zuverlässigkeit und Mikrointegration

# Via Formation for VSI – *Tungsten Pin Resistance*



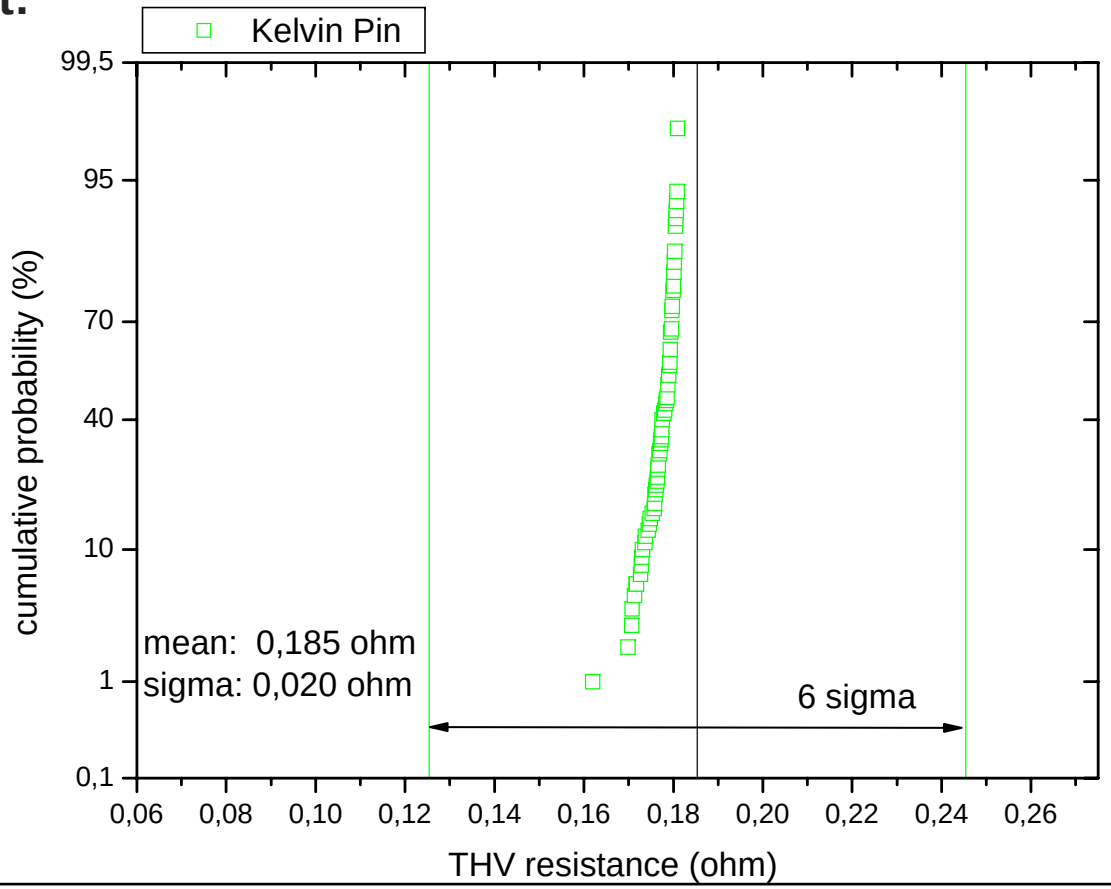




by Armin Klumpp

Fraunhofer IZM
Institut Zuverlässigkeit und Mikrointegration

## Electrical Measurement: Single pins 20 µm

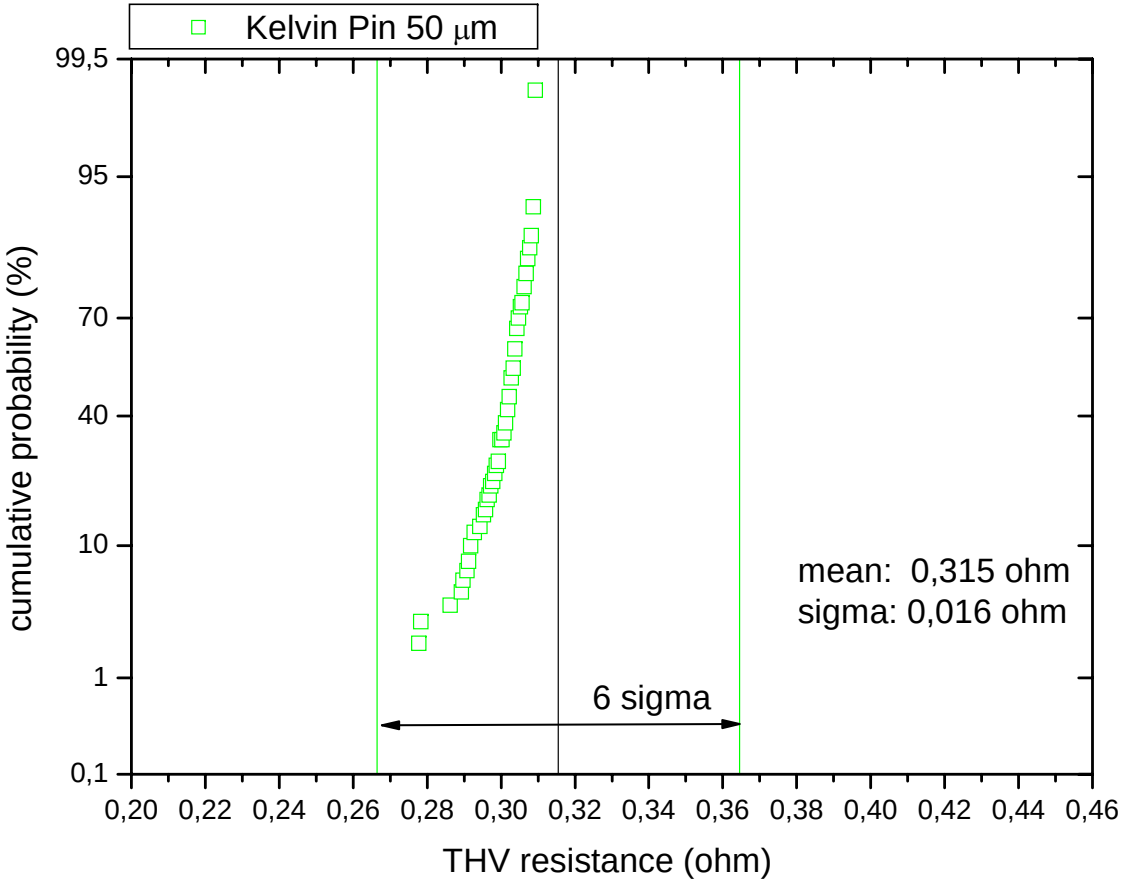
- Yield on thinned silicon 97%
- Daisy chain with 997 elements
- AlSiCu metallization for chain formation






## Electrical Measurement: Single pins 50 µm

- Yield on thinned silicon 98%
- Daisy chain with 997 elements
- AlSiCu metallization for chain formation






## Conclusion

- For 3D-Integration there are a lot of technological solutions, with demonstrated feasibilites
- Decision for Application depends on Target Products and Cost of Ownership

- There still remain some keypoints to be worked out:
  - Thin Silicon Handling ( < 50 µm) for Backside Processing
  - Thermal Management (Simulation and Test Devices)
  - Compatibility to High Frequency Signal Transmission (2.5 ...30 … x GHz)
  - Development of Very Low Cost Integration Sequences
  - Reliability



Thank you for your attention !