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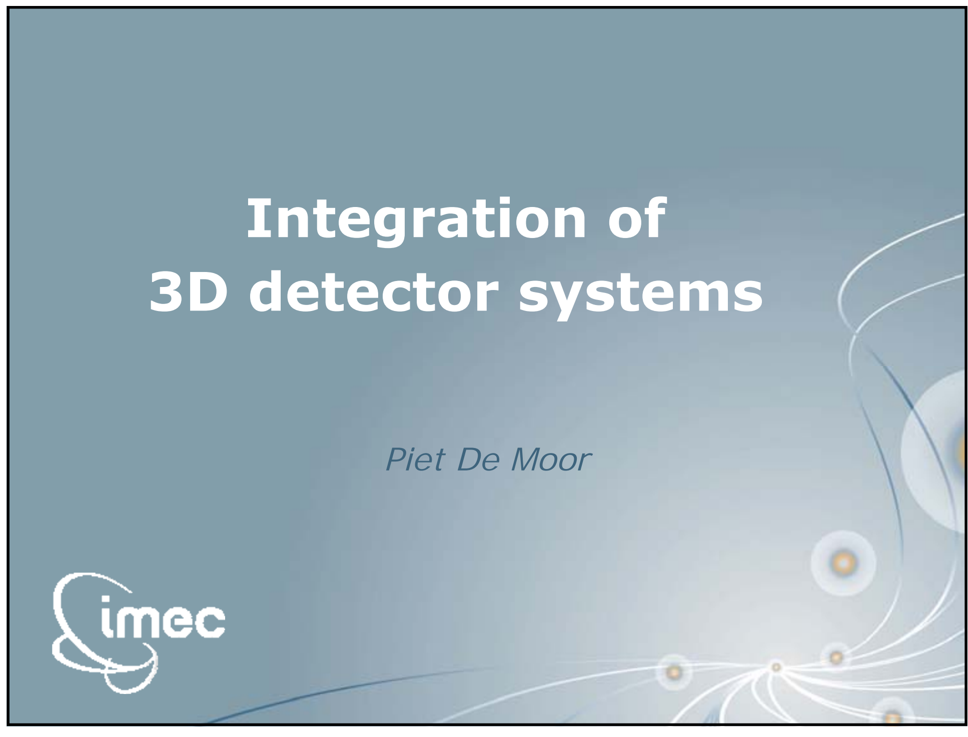

Introduction

- Evolution in radiation detection/imaging:
  - single pixel → linear array → 2D array
  - increase in resolution = decrease in pitch (down to few um)
- = thanks to development in **microelectronics fabrication technology**:
  - CMOS scaling
  - hybridisation using solder bumps
- Question: what's next ?
  - which new technologies become available ?
  - what are the benefits ?
- Answer:
  - advanced packaging including flex and/or 3D integration

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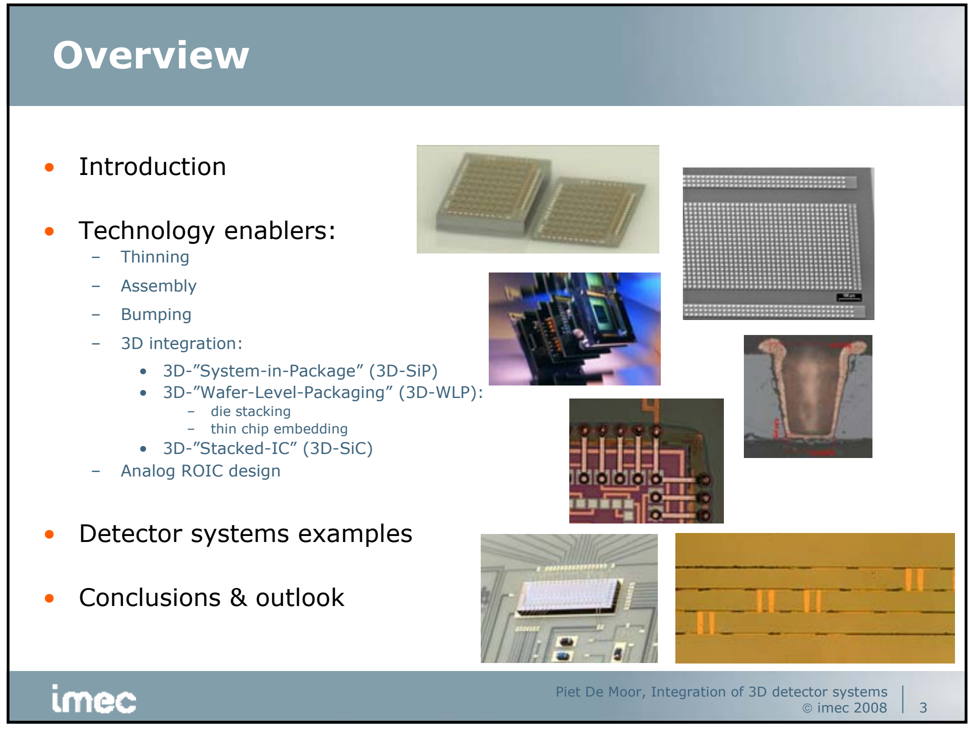

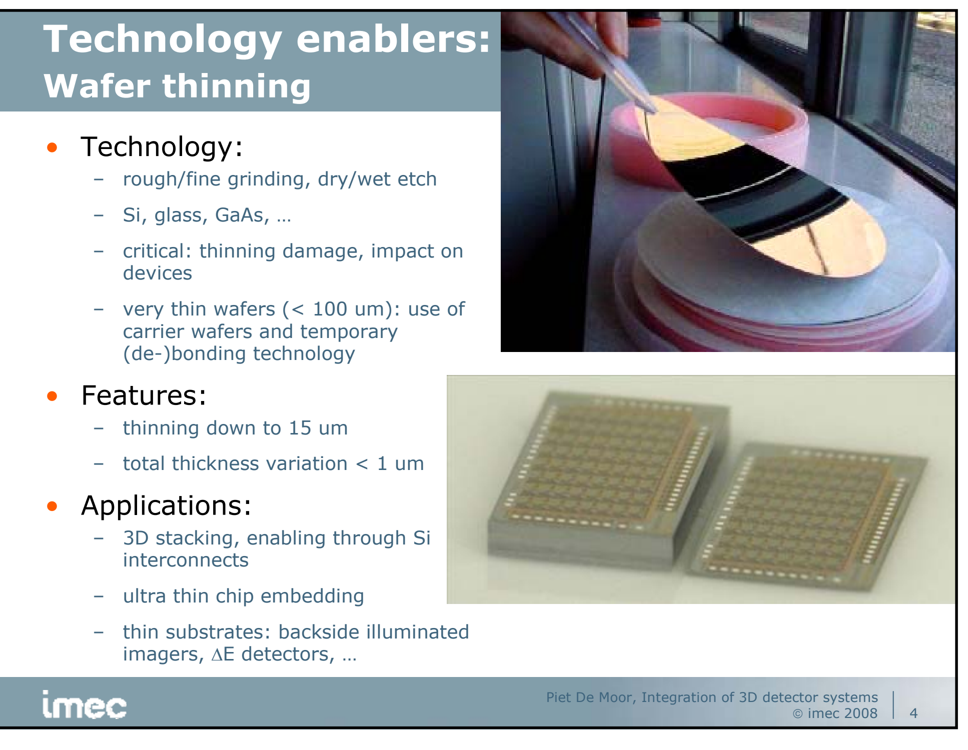

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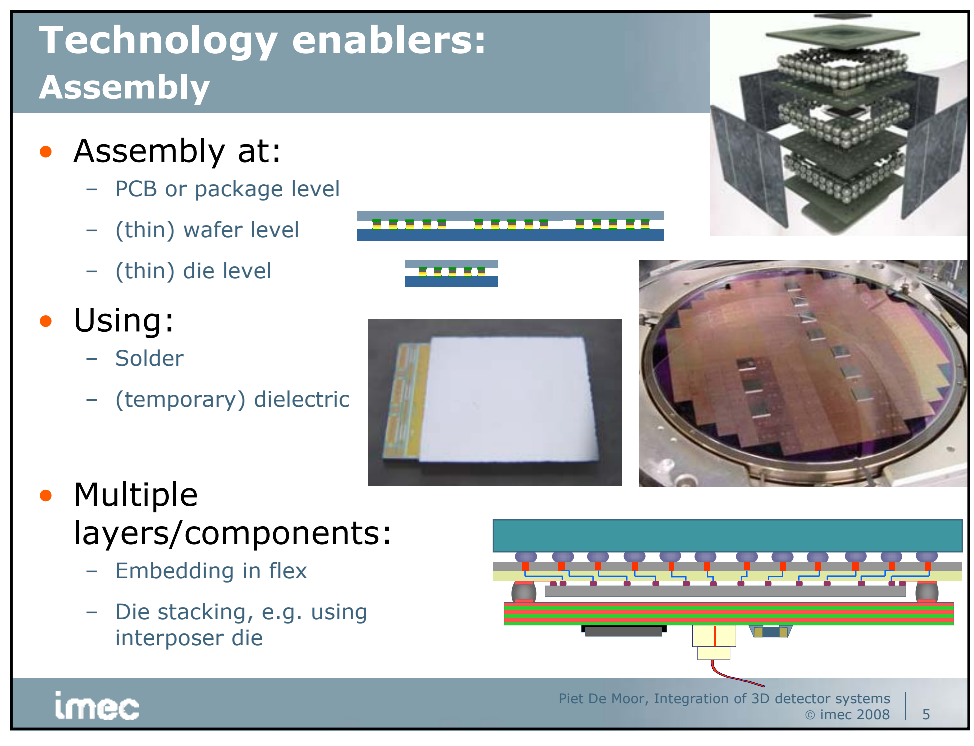

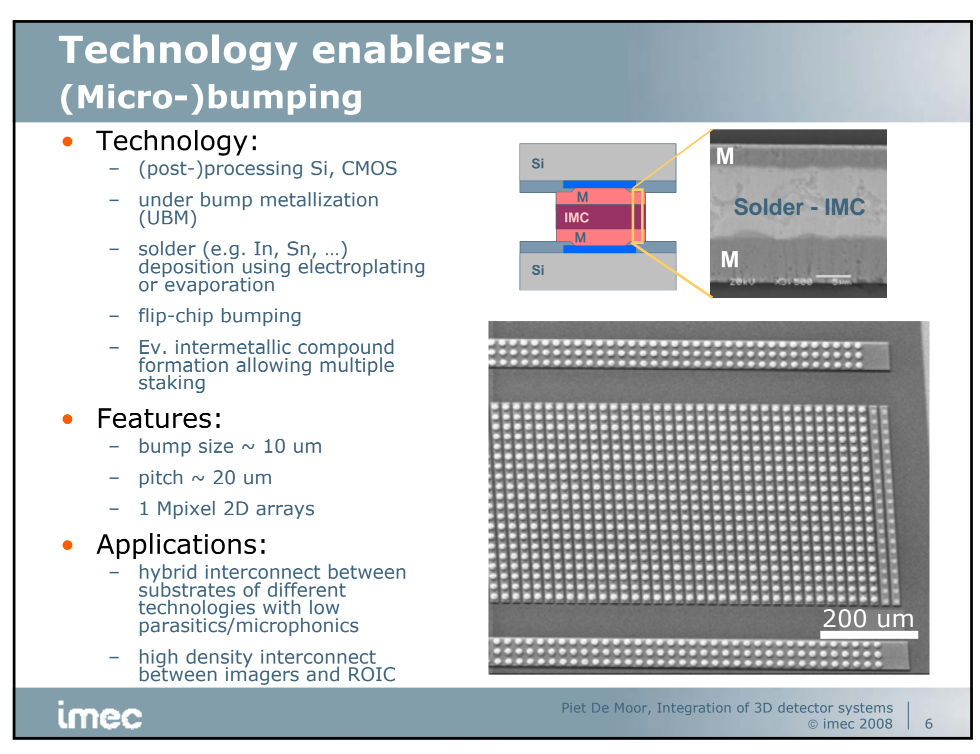

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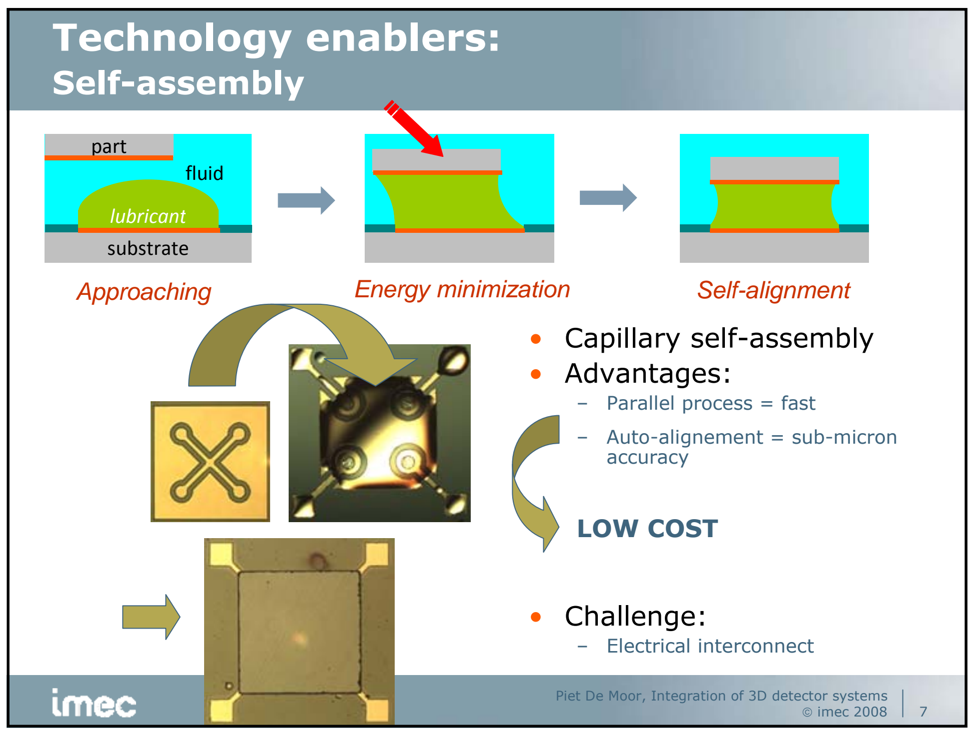

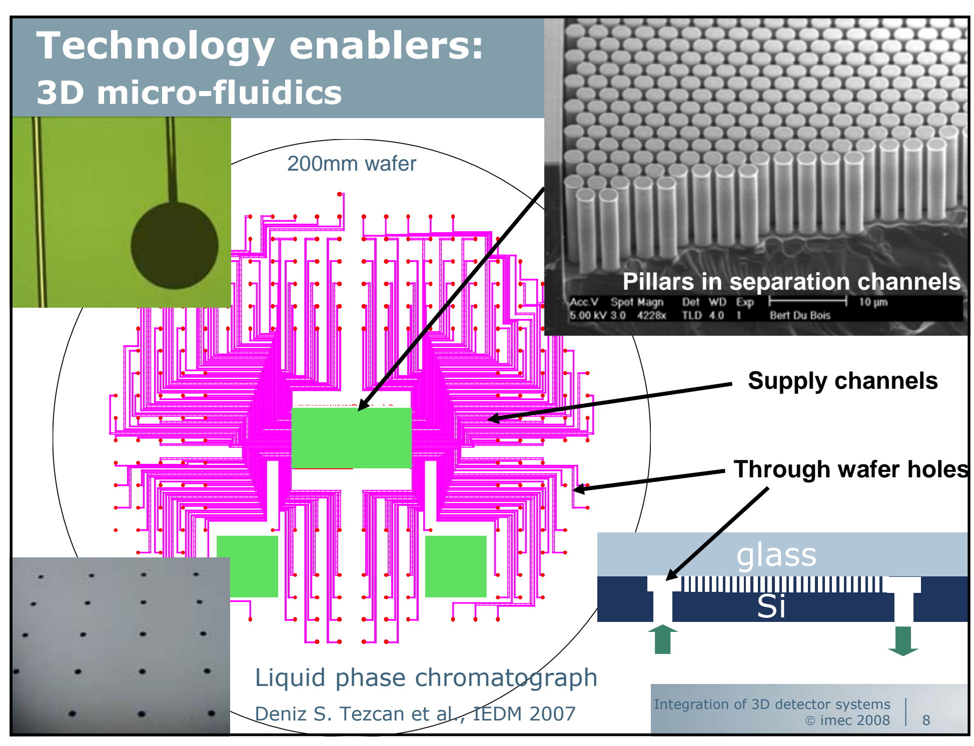

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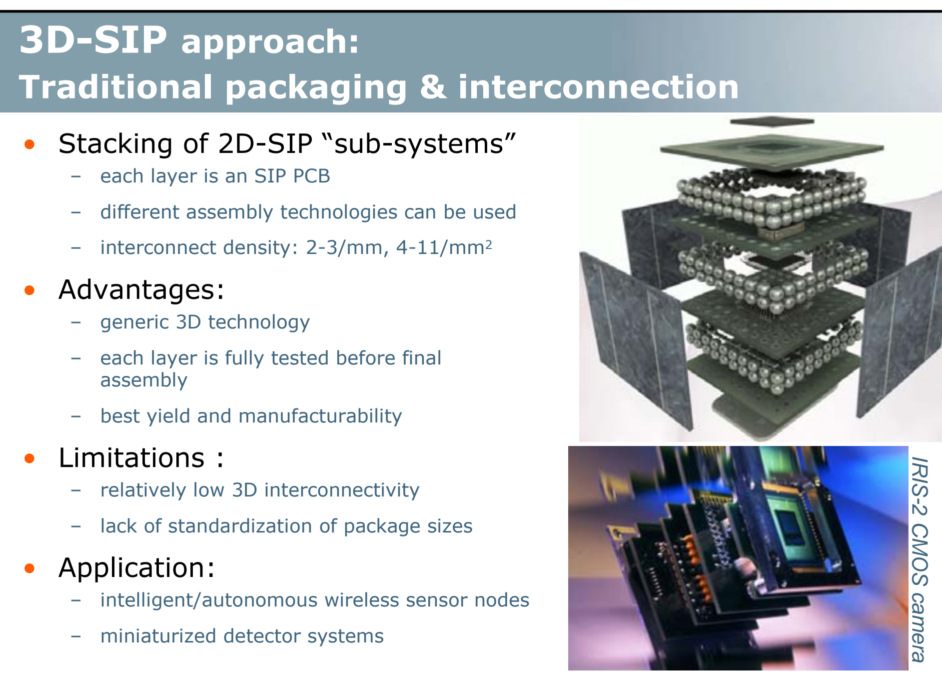

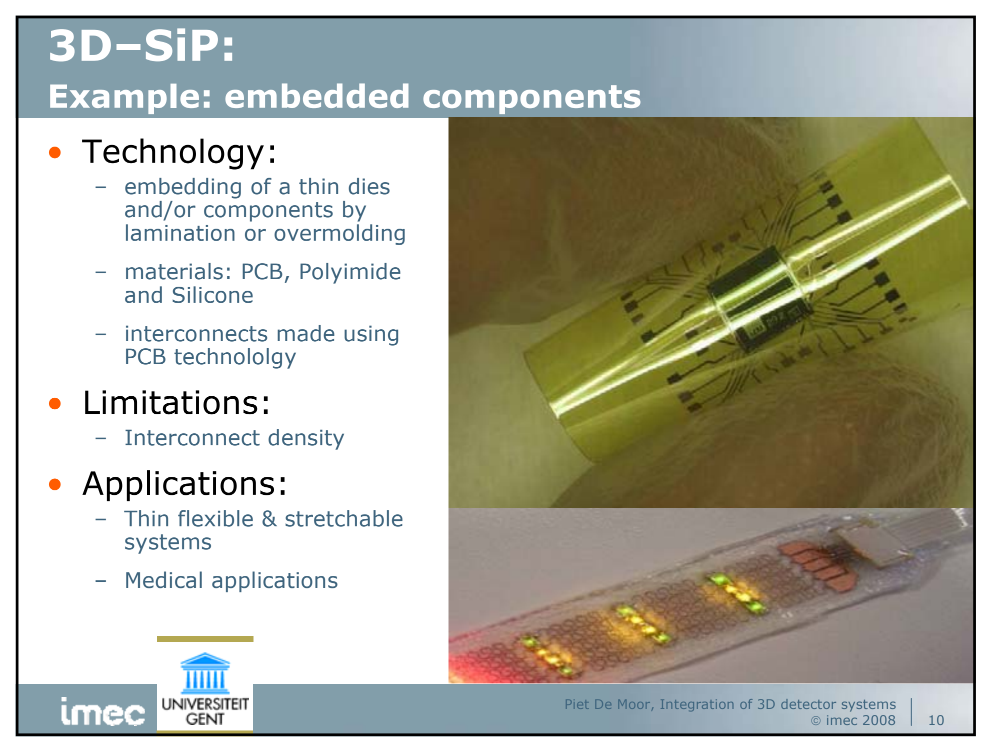

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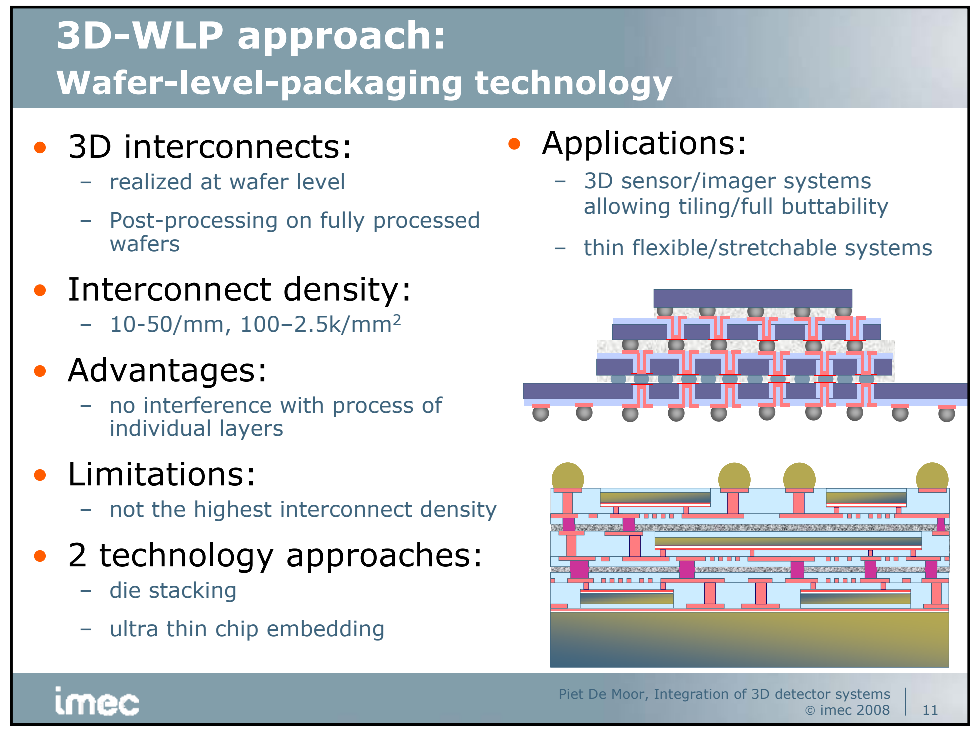

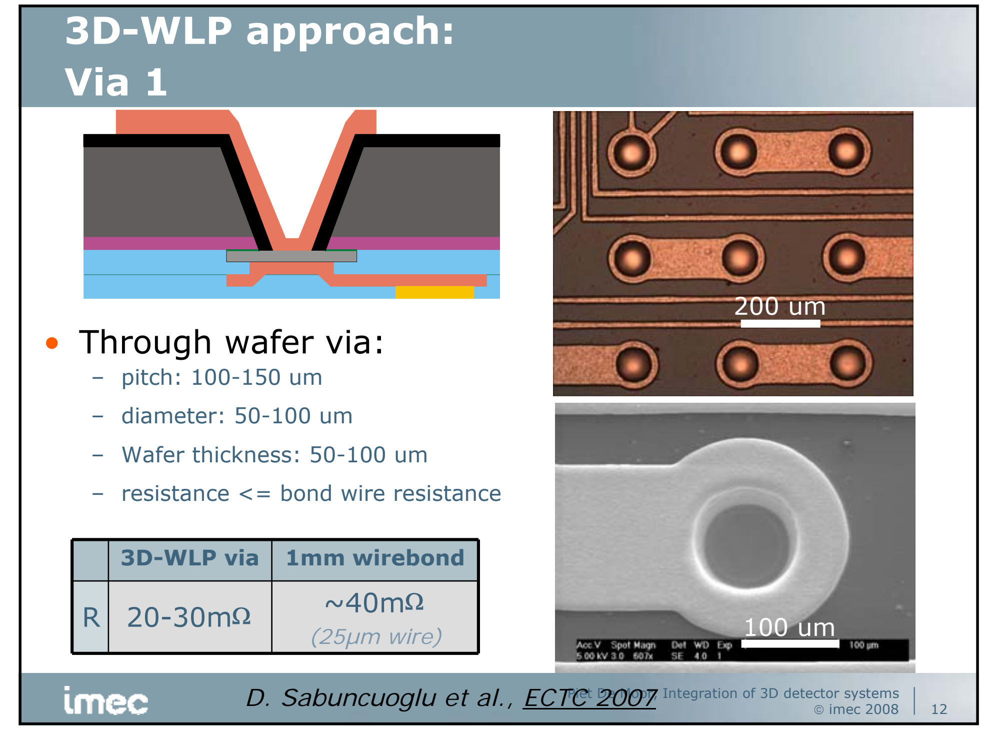

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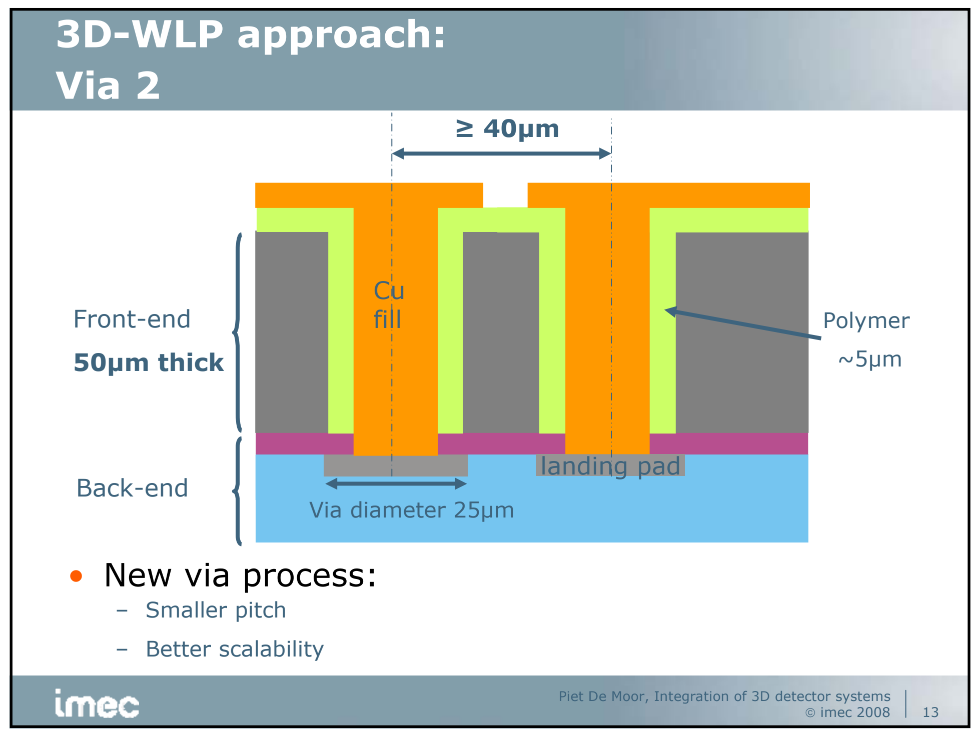

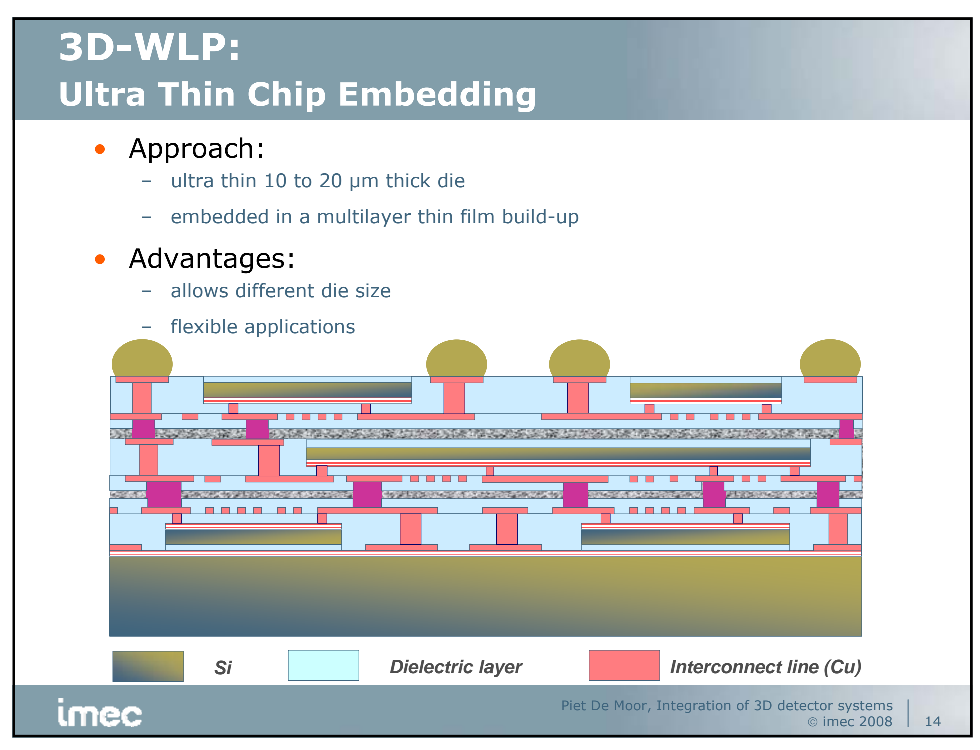

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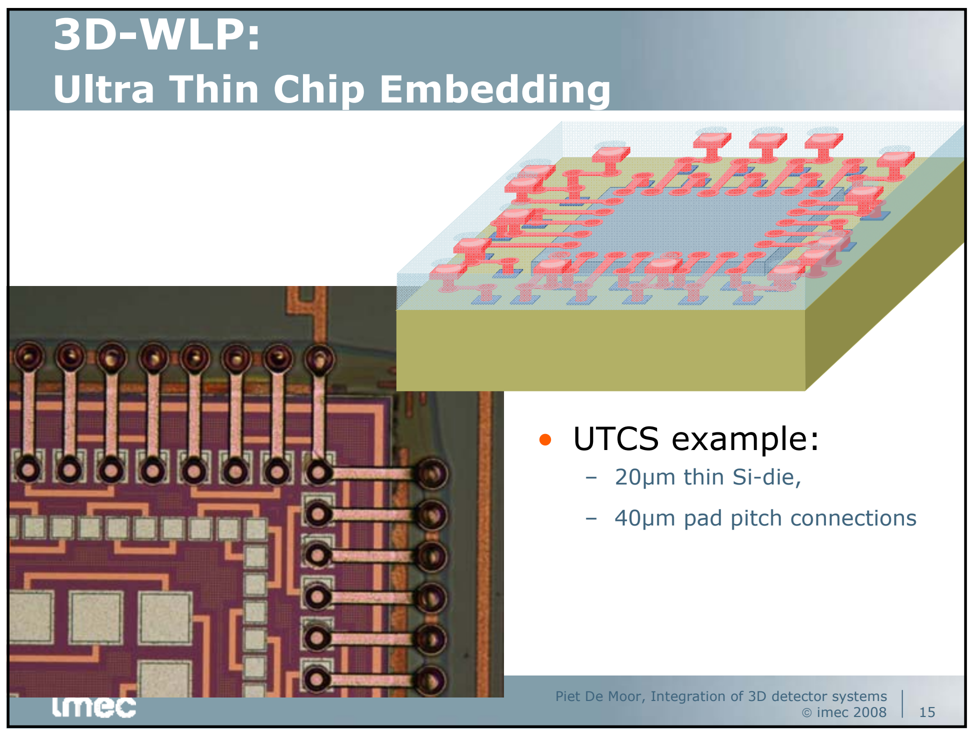

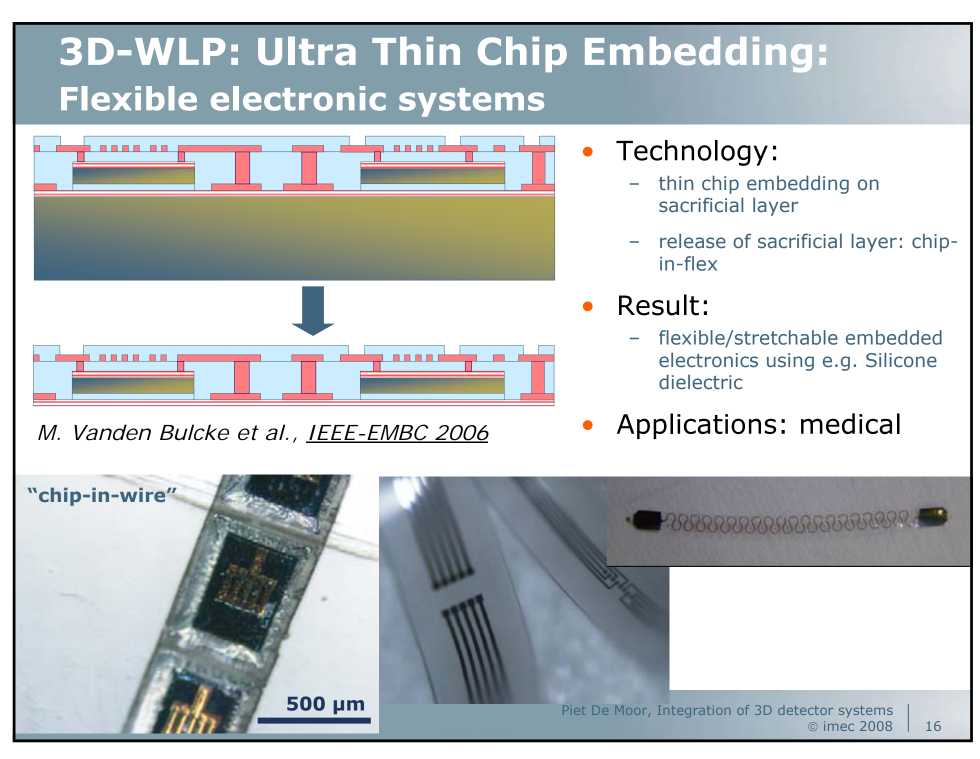

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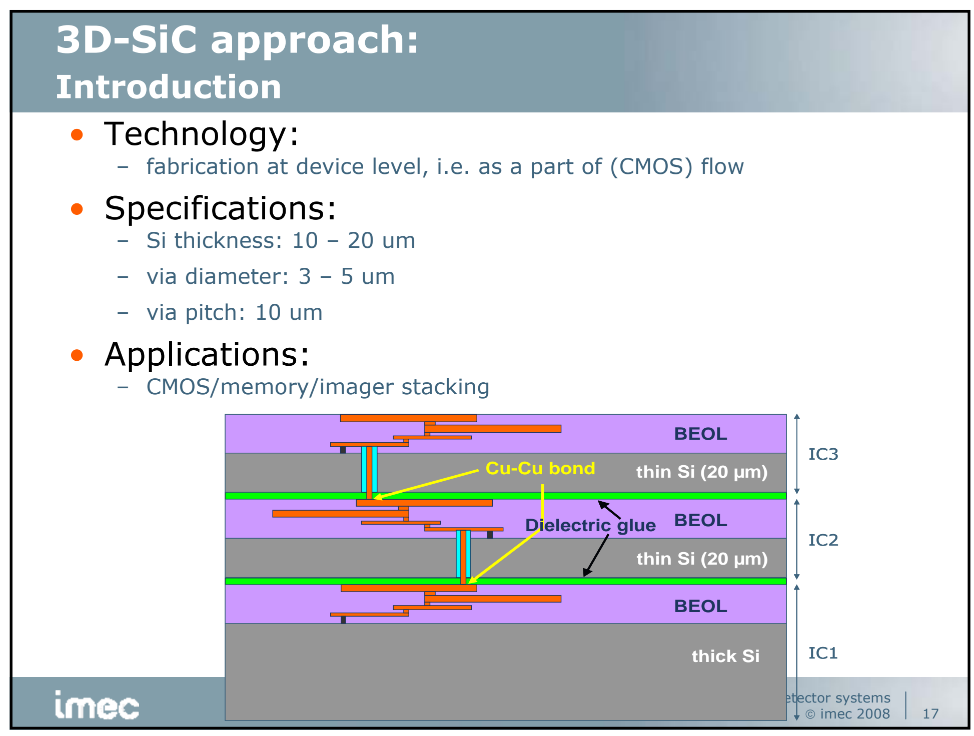

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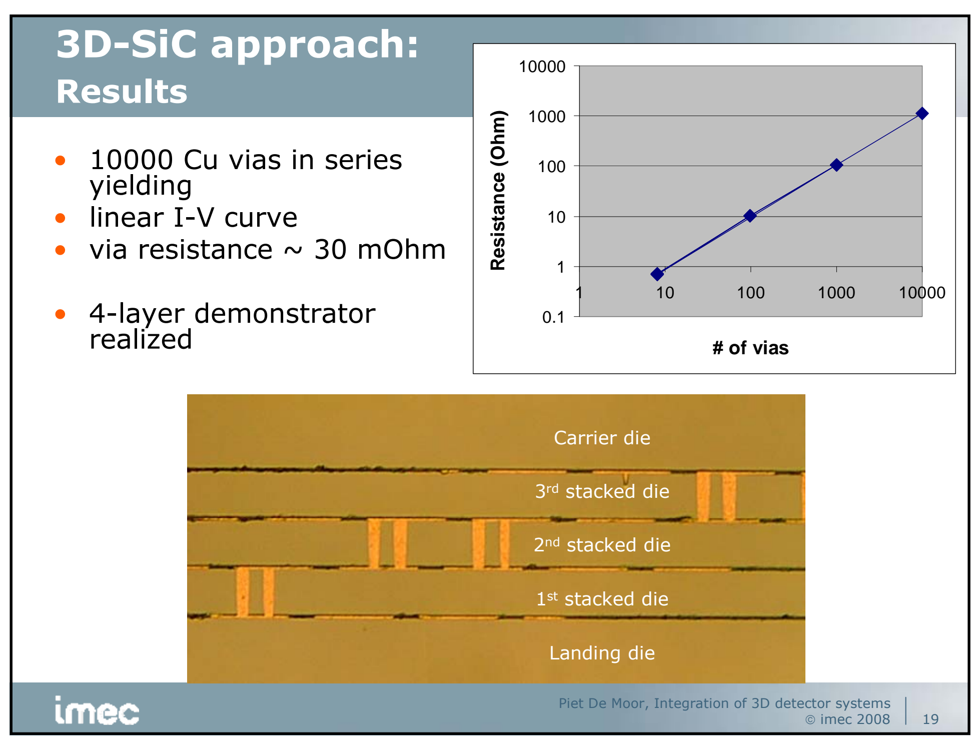

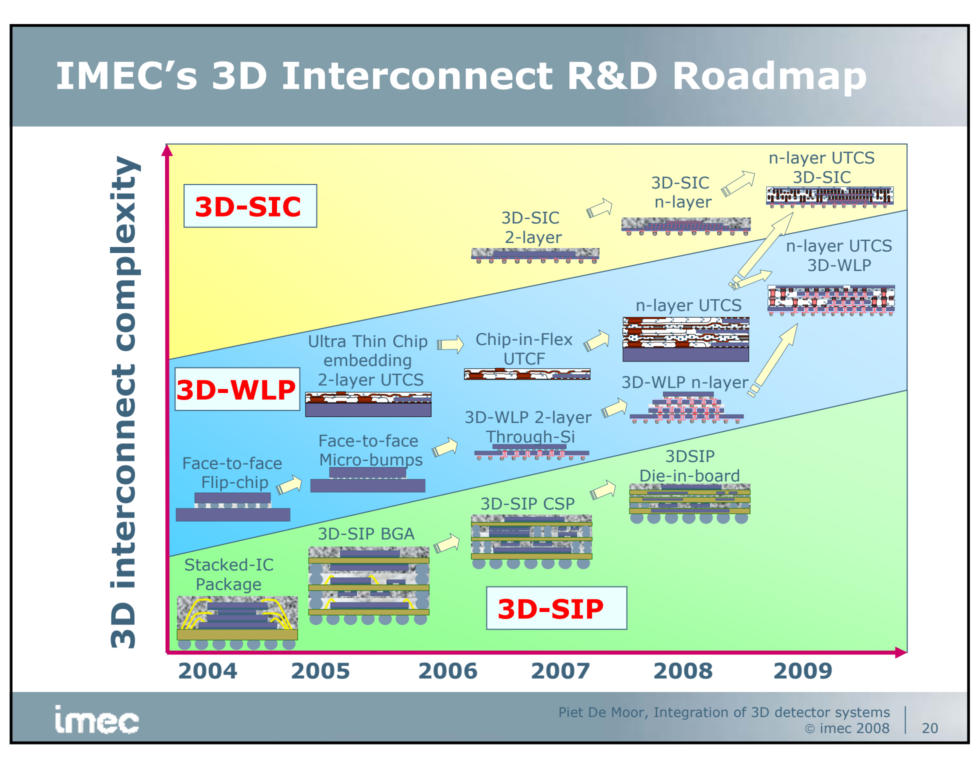

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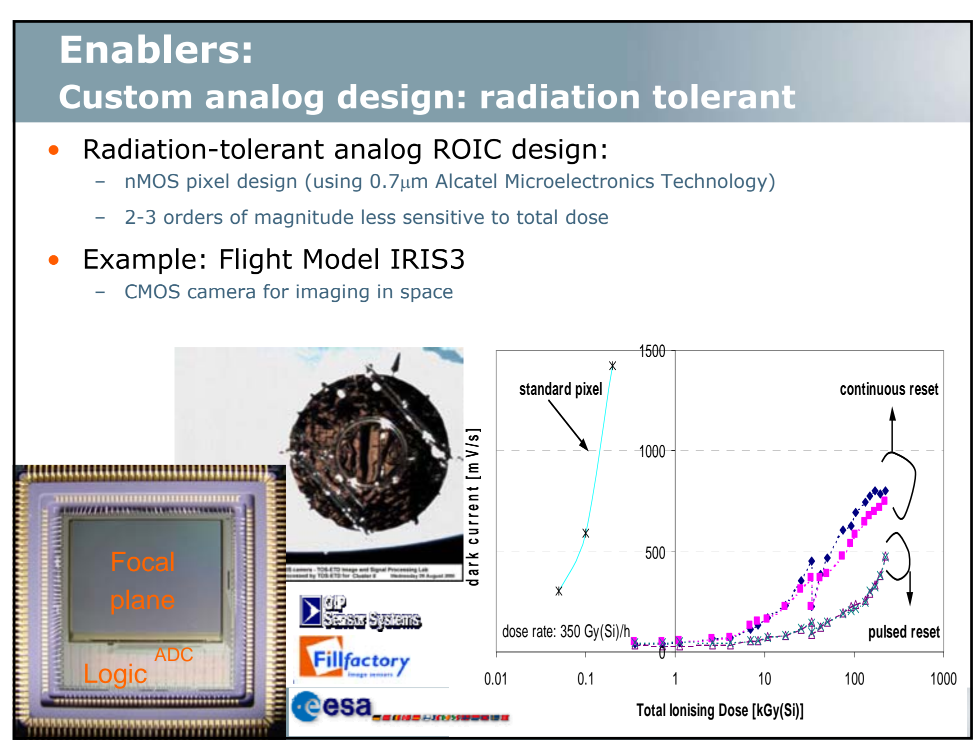
Positioning different 3D approaches

	3D-SIP	3D-WLP		3D-SIC
Technology	Package interposer	WLP, Post-passivation		Si-foundry, Post FEOL
3D interconnect	Package I/O	UTCS Embedded die	Si-through vias	Si-through "Cu nail" vias
Intercon. Density	'package-to-package'	'around' die	'through' die	'through' die
Peripheral	2 - 3 /mm	10 - 50 /mm	10 - 25 /mm	25 -100 /mm
Area-array	4 - 11/mm^2	100 -2.5k/mm^2	16 - 100/mm^2	400-10k/mm^2
3D Si Via pitch	-	-	40 – 100 µm	< 10 µm
3D interconnect pitch	300 – 500 µm	20 – 100 µm	-	-
3D Si Via diameter	-	-	25 - 100 µm	1 - 5 µm
Die thickness	> 50 µm	10 - <u>20</u> µm	<u>50</u> - 100 µm	<u>10</u> - 20 µm

Enablers:
Custom analog design: radiation tolerant

- Radiation-tolerant analog ROIC design:
  - nMOS pixel design (using 0.7µm Alcatel Microelectronics Technology)
  - 2-3 orders of magnitude less sensitive to total dose
- Example: Flight Model IRIS3
  - CMOS camera for imaging in space



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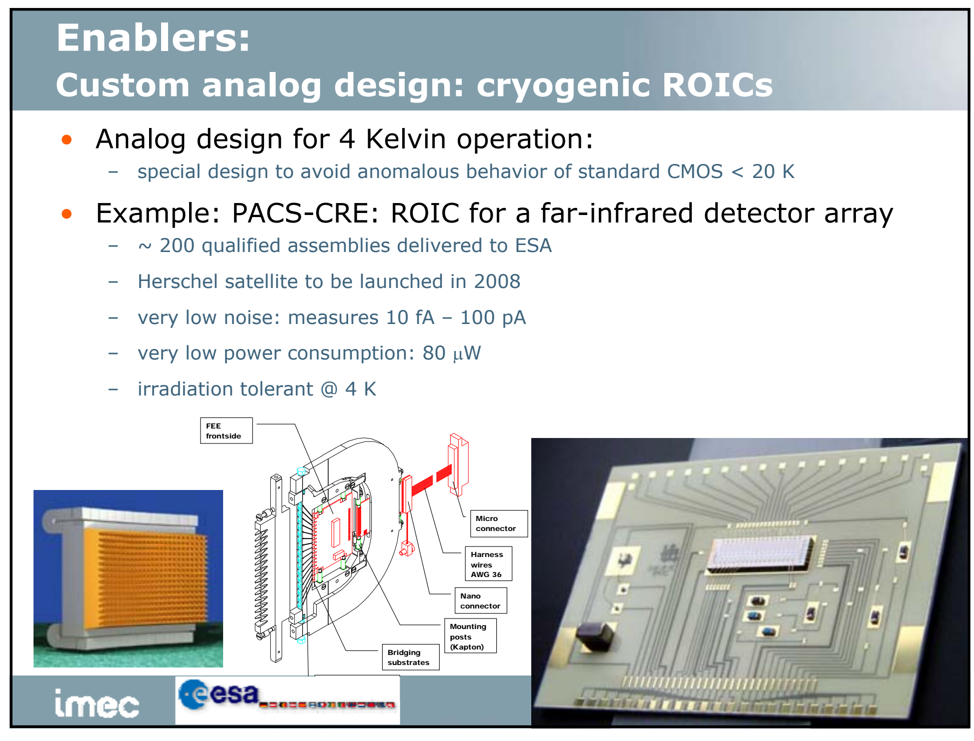

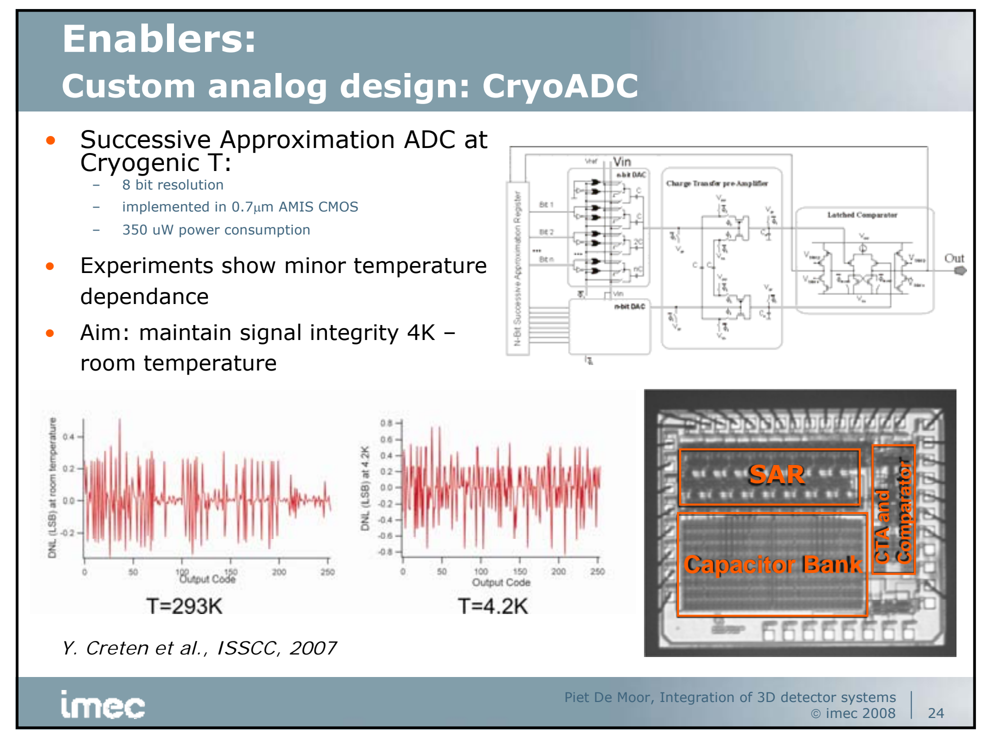

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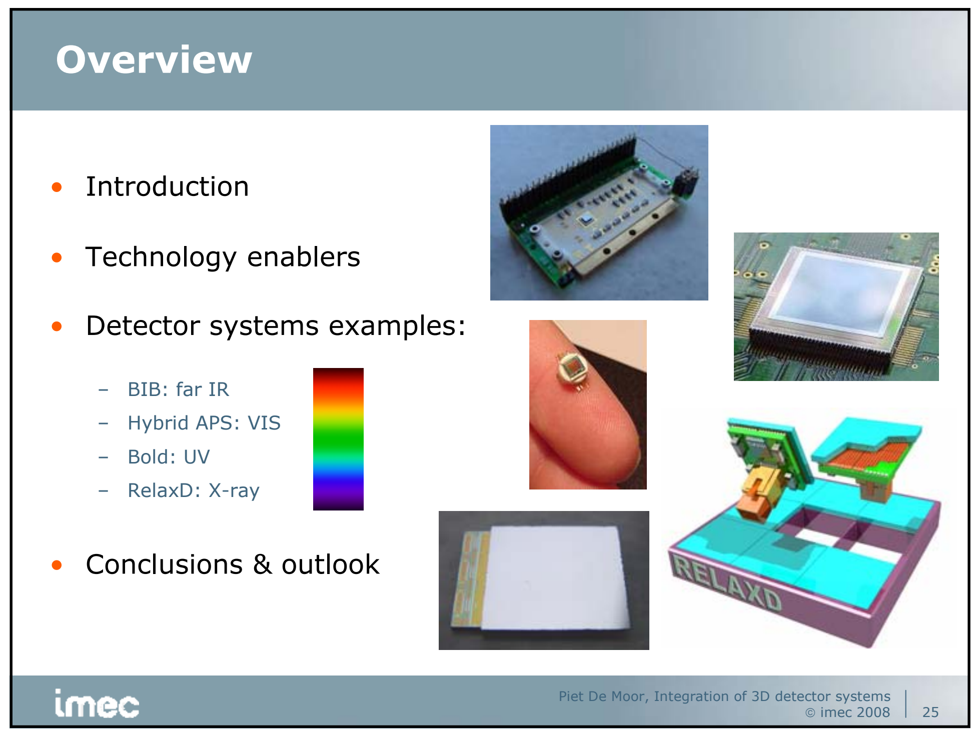

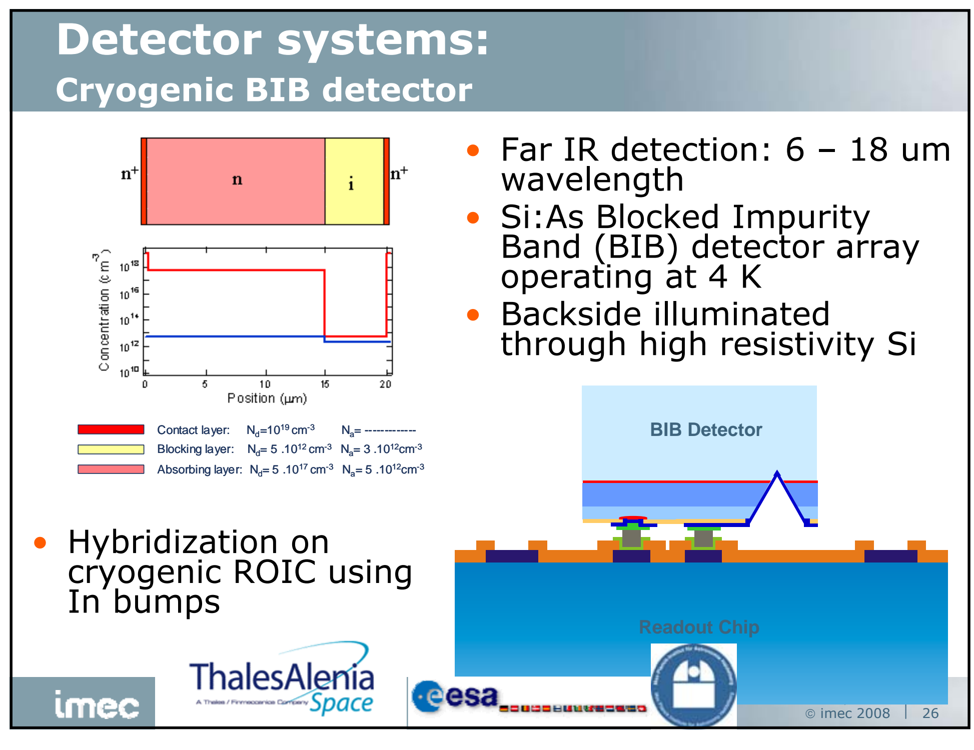

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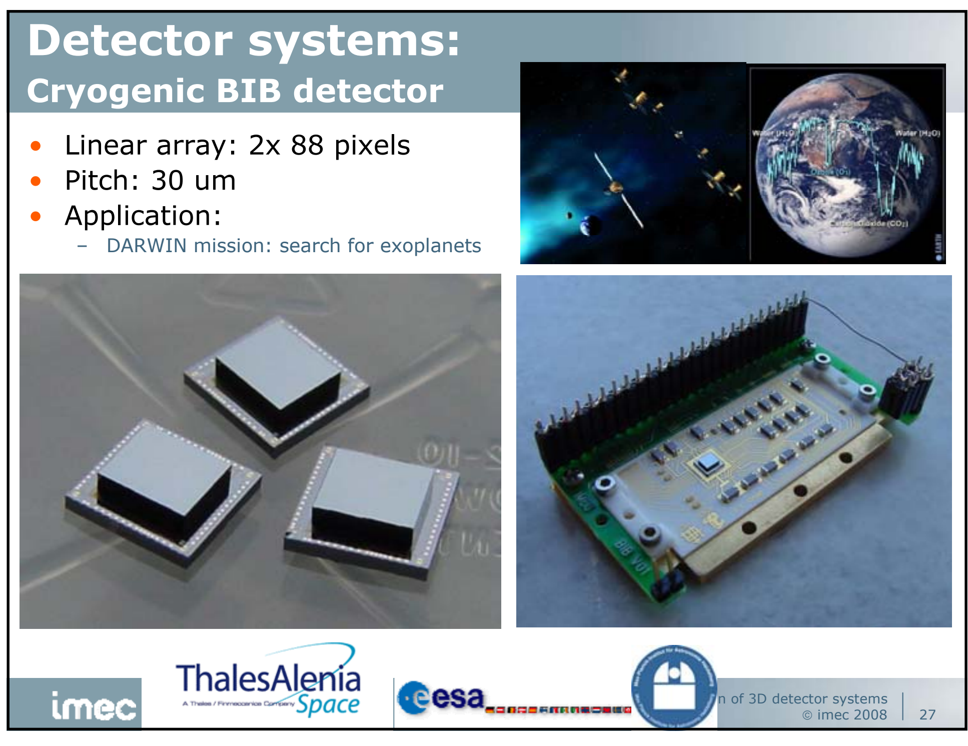

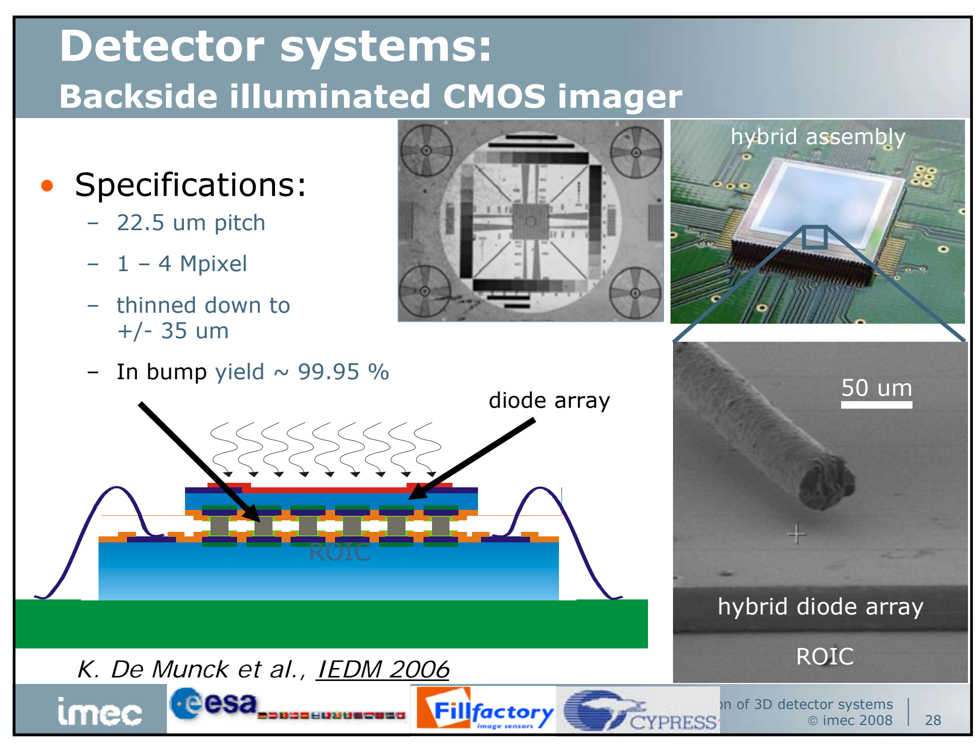

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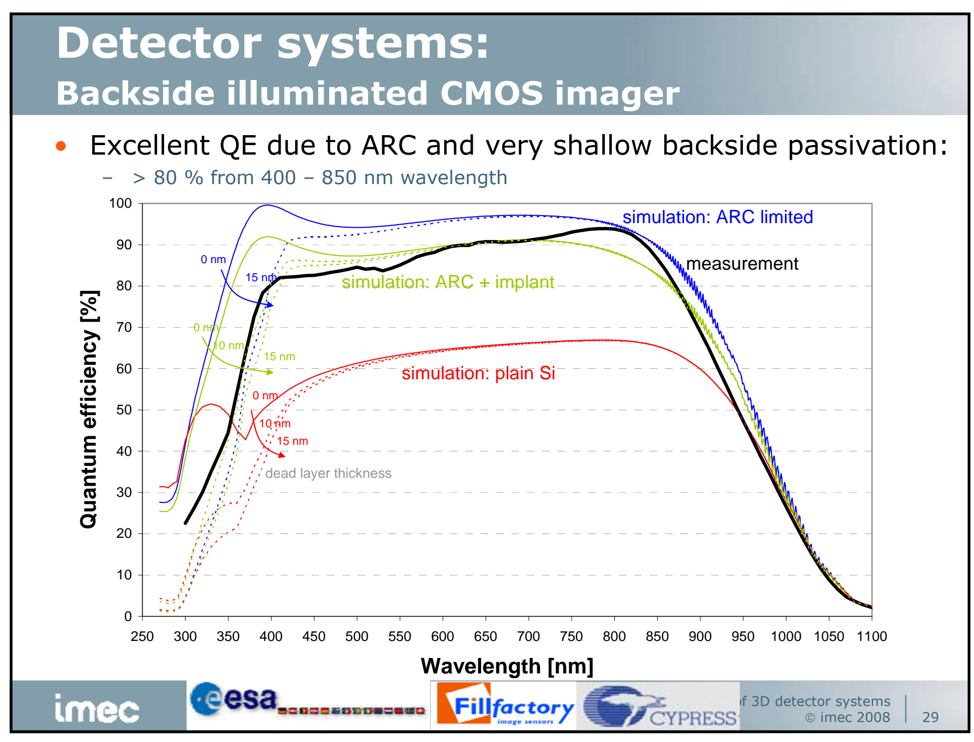

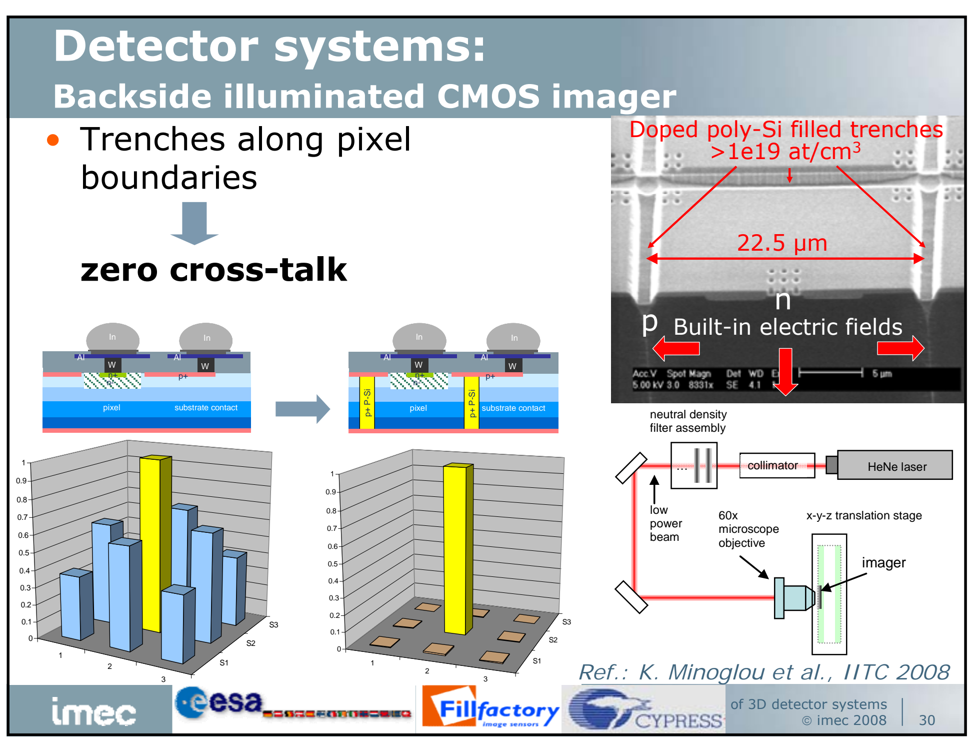

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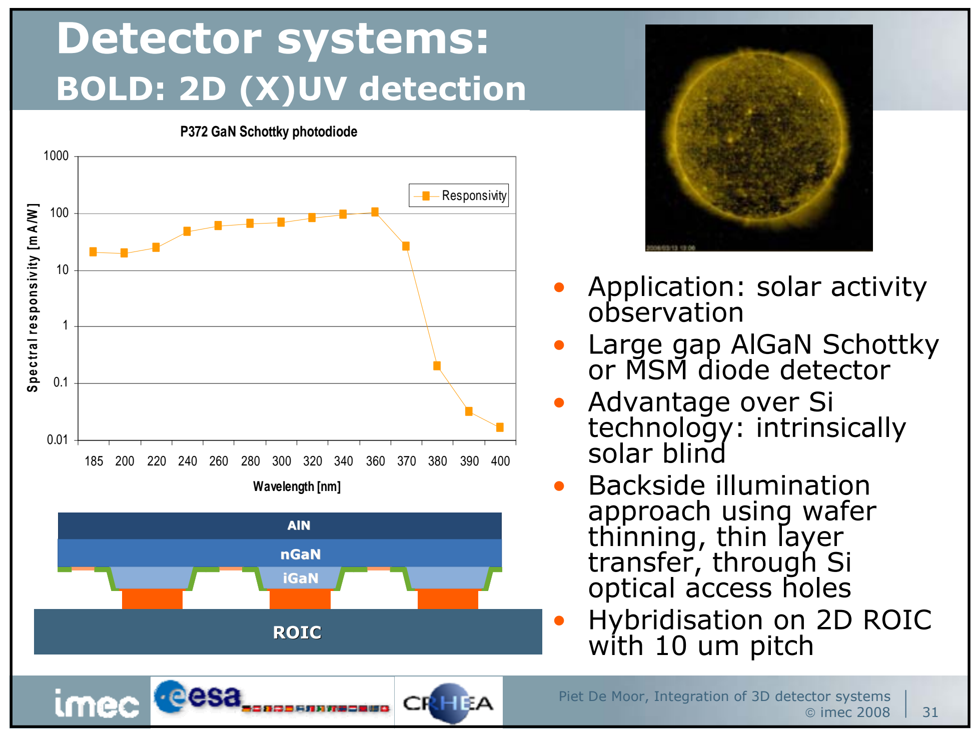

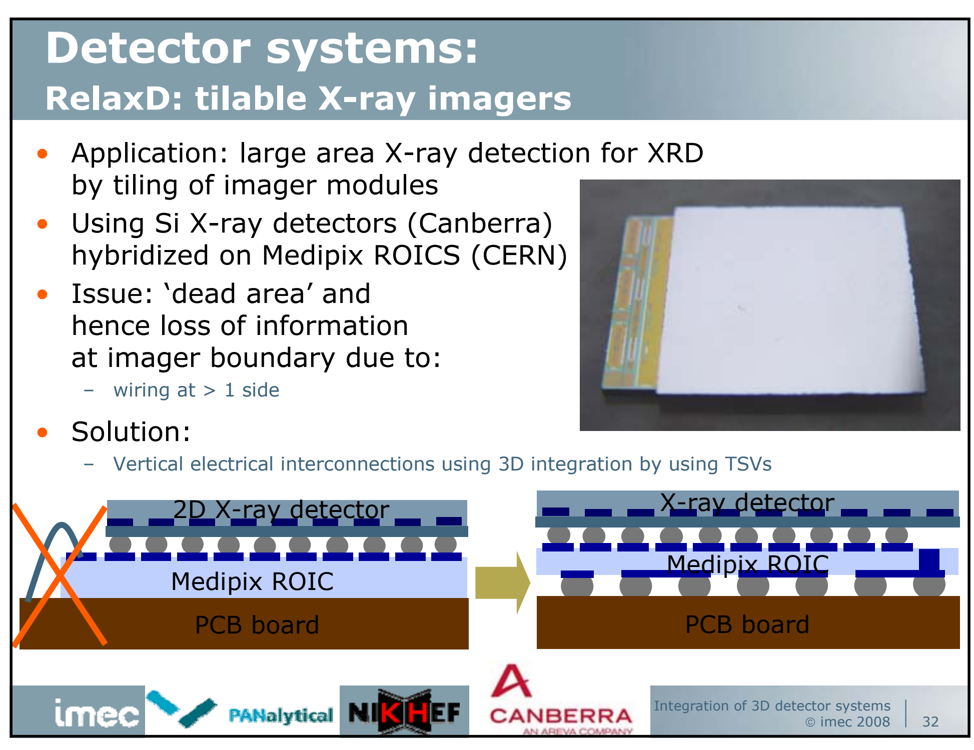

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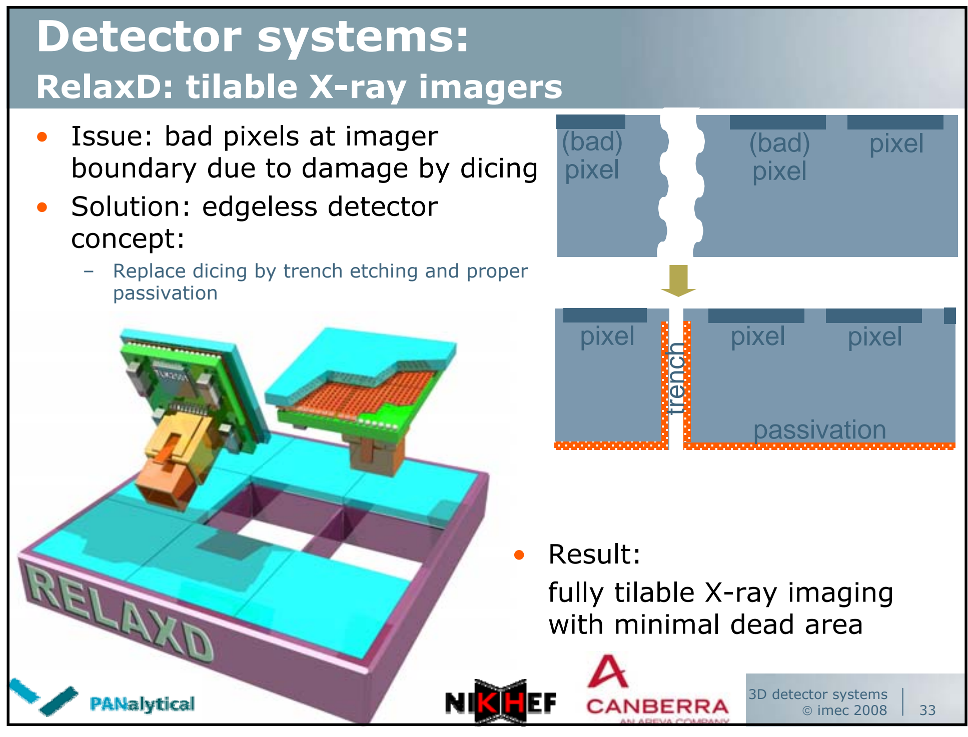

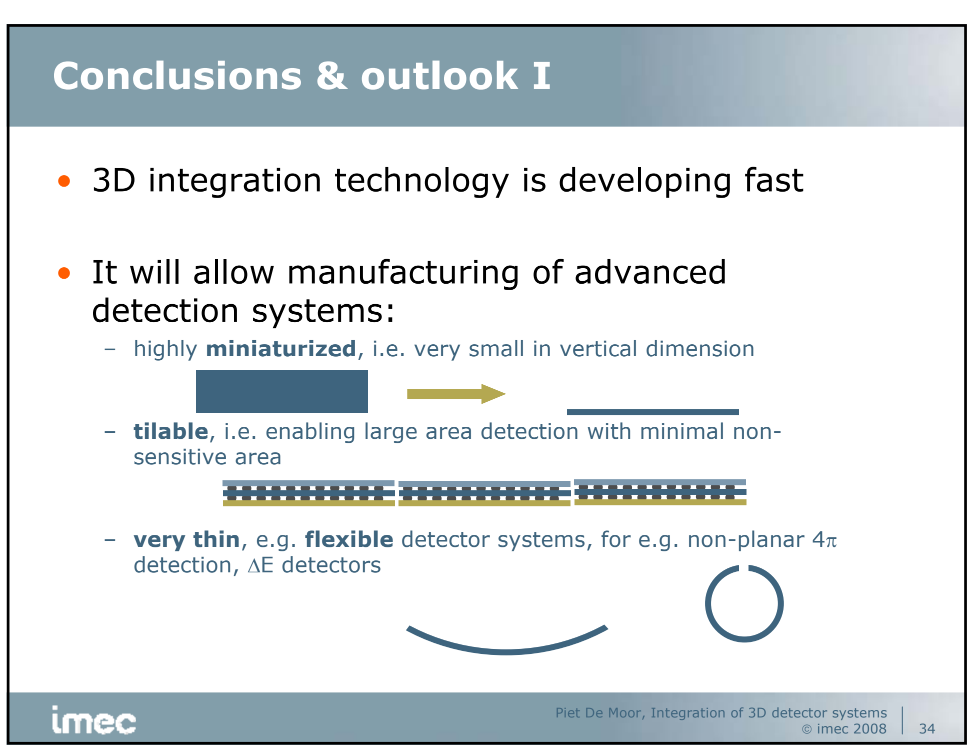

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