

Integration of 3D detector systems

Piet De Moor

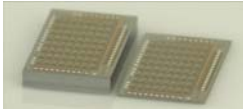
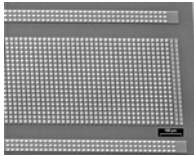

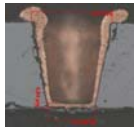
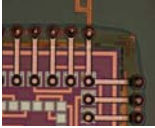

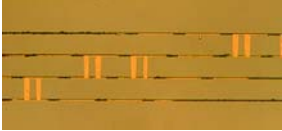



Introduction

- Evolution in radiation detection/imaging:
 - single pixel → linear array → 2D array
 - increase in resolution = decrease in pitch (down to few μm)
- = thanks to development in **microelectronics fabrication technology**:
 - CMOS scaling
 - hybridisation using solder bumps
- Question: what's next ?
 - which new technologies become available ?
 - what are the benefits ?
- Answer:
 - advanced packaging including flex and/or 3D integration

Overview

- Introduction
- Technology enablers:
 - Thinning
 - Assembly
 - Bumping
 - 3D integration:
 - 3D-“System-in-Package” (3D-SiP)
 - 3D-“Wafer-Level-Packaging” (3D-WLP):
 - die stacking
 - thin chip embedding
 - 3D-“Stacked-IC” (3D-SiC)
 - Analog ROIC design
- Detector systems examples
- Conclusions & outlook

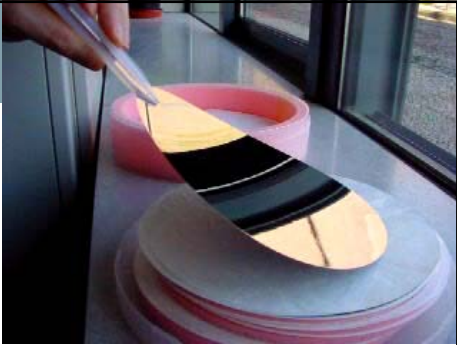
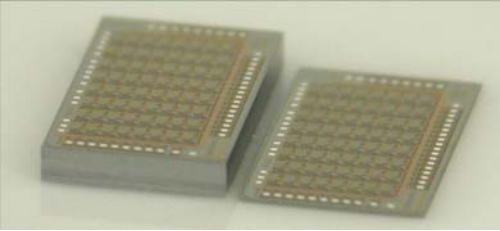



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Technology enablers: Wafer thinning

- Technology:
 - rough/fine grinding, dry/wet etch
 - Si, glass, GaAs, ...
 - critical: thinning damage, impact on devices
 - very thin wafers (< 100 um): use of carrier wafers and temporary (de-)bonding technology
- Features:
 - thinning down to 15 um
 - total thickness variation < 1 um
- Applications:
 - 3D stacking, enabling through Si interconnects
 - ultra thin chip embedding
 - thin substrates: backside illuminated imagers, ΔE detectors, ...





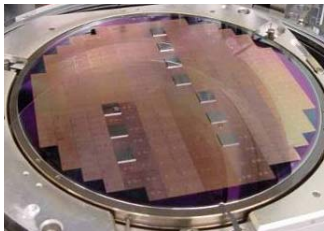
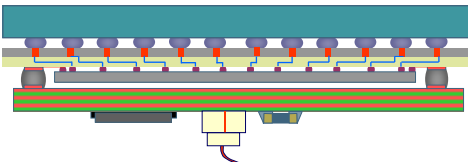


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Technology enablers: Assembly

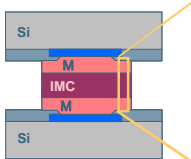
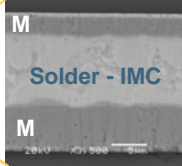
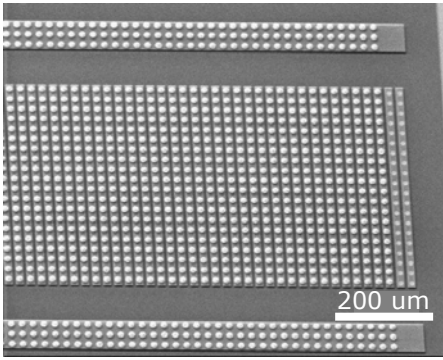
- Assembly at:**
 - PCB or package level
 - (thin) wafer level
 - (thin) die level
- Using:**
 - Solder
 - (temporary) dielectric
- Multiple layers/components:**
 - Embedding in flex
 - Die stacking, e.g. using interposer die

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Technology enablers: (Micro-)bumping

- Technology:**
 - (post-)processing Si, CMOS
 - under bump metallization (UBM)
 - solder (e.g. In, Sn, ...) deposition using electroplating or evaporation
 - flip-chip bumping
 - Ev. intermetallic compound formation allowing multiple staking
- Features:**
 - bump size ~ 10 μm
 - pitch ~ 20 μm
 - 1 Mpixel 2D arrays
- Applications:**
 - hybrid interconnect between substrates of different technologies with low parasitics/microphonics
 - high density interconnect between imagers and ROIC

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Technology enablers: Self-assembly

The diagram illustrates the three stages of capillary self-assembly:

- Approaching:** A part is placed on a substrate with a lubricant layer. Fluid is introduced between the part and the substrate.
- Energy minimization:** The fluid spreads, pulling the part towards the substrate.
- Self-alignment:** The part is fully aligned and adhered to the substrate.

The process results in a self-assembled microfluidic chip, shown in two micrographs: one showing the individual components and another showing the fully assembled chip.

- Capillary self-assembly
- Advantages:
 - Parallel process = fast
 - Auto-alignment = sub-micron accuracy
- **LOW COST**
- Challenge:
 - Electrical interconnect

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Technology enablers: 3D micro-fluidics

The schematic shows a 200mm wafer with a complex network of channels. Key features include:

- Supply channels:** The main flow paths.
- Through wafer holes:** Connections between the top and bottom layers.
- Liquid phase chromatograph:** The central functional area.

The SEM image shows the physical structure with **Pillars in separation channels**. The device is built on a **Si** substrate with a **glass** layer.

Deniz S. Tezcan et al., IEDM 2007

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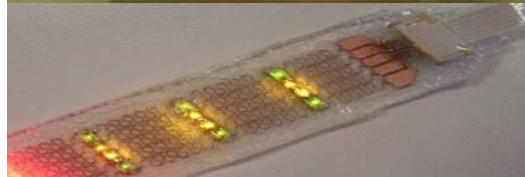
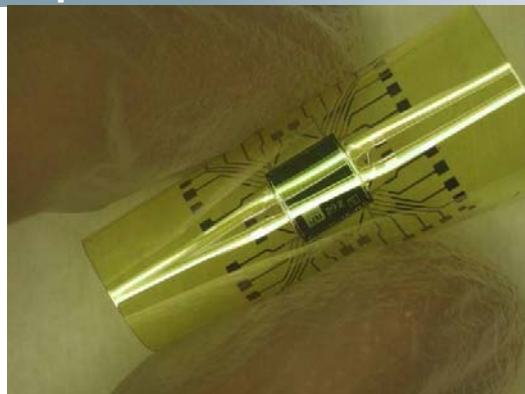
3D-SIP approach: Traditional packaging & interconnection

- **Stacking of 2D-SIP "sub-systems"**
 - each layer is an SIP PCB
 - different assembly technologies can be used
 - interconnect density: 2-3/mm, 4-11/mm²
- **Advantages:**
 - generic 3D technology
 - each layer is fully tested before final assembly
 - best yield and manufacturability
- **Limitations :**
 - relatively low 3D interconnectivity
 - lack of standardization of package sizes
- **Application:**
 - intelligent/autonomous wireless sensor nodes
 - miniaturized detector systems



3D-SiP: Example: embedded components

- **Technology:**
 - embedding of a thin dies and/or components by lamination or overmolding
 - materials: PCB, Polyimide and Silicone
 - interconnects made using PCB technology
- **Limitations:**
 - Interconnect density
- **Applications:**
 - Thin flexible & stretchable systems
 - Medical applications



3D-WLP approach: Wafer-level-packaging technology

- **3D interconnects:**
 - realized at wafer level
 - Post-processing on fully processed wafers
- **Interconnect density:**
 - 10-50/mm, 100-2.5k/mm²
- **Advantages:**
 - no interference with process of individual layers
- **Limitations:**
 - not the highest interconnect density
- **2 technology approaches:**
 - die stacking
 - ultra thin chip embedding

- **Applications:**
 - 3D sensor/imager systems allowing tiling/full buttability
 - thin flexible/stretchable systems

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3D-WLP approach: Via 1

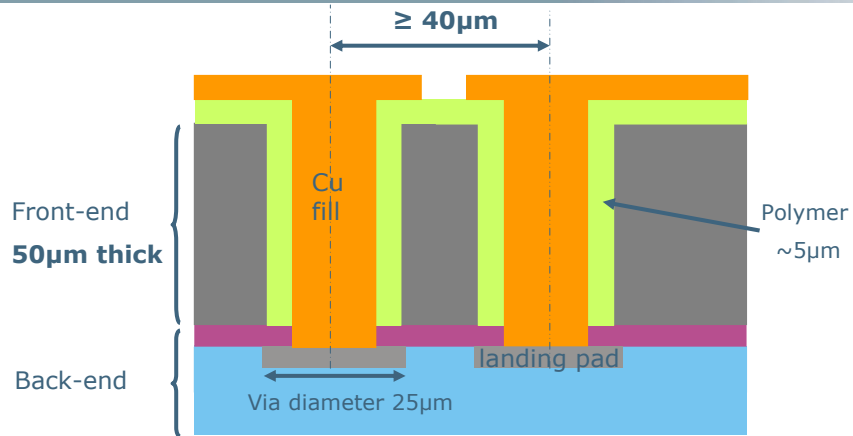
- **Through wafer via:**
 - pitch: 100-150 μm
 - diameter: 50-100 μm
 - Wafer thickness: 50-100 μm
 - resistance \leq bond wire resistance

	3D-WLP via	1mm wirebond
R	20-30m Ω	~40m Ω <i>(25μm wire)</i>

D. Sabuncuoglu et al., *ECTC 2007* Integration of 3D detector systems
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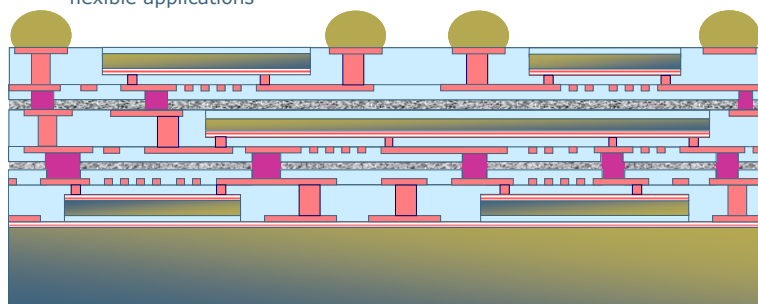
3D-WLP approach: Via 2



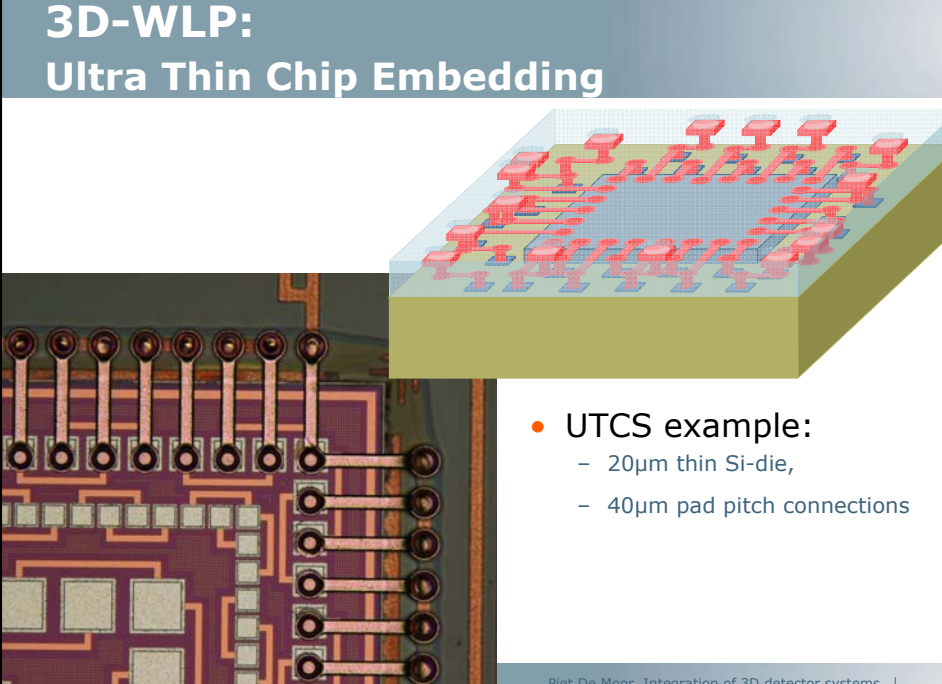
- New via process:
 - Smaller pitch
 - Better scalability

3D-WLP: Ultra Thin Chip Embedding

- Approach:
 - ultra thin 10 to 20 µm thick die
 - embedded in a multilayer thin film build-up
- Advantages:
 - allows different die size
 - flexible applications



3D-WLP: Ultra Thin Chip Embedding

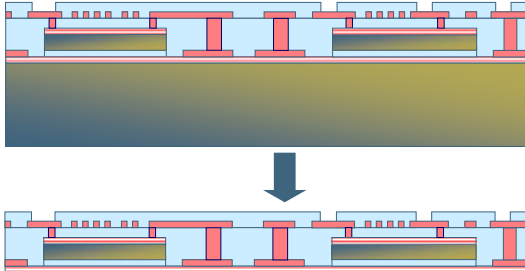


- UTCS example:
 - 20µm thin Si-die,
 - 40µm pad pitch connections

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3D-WLP: Ultra Thin Chip Embedding: Flexible electronic systems



- Technology:
 - thin chip embedding on sacrificial layer
 - release of sacrificial layer: chip-in-flex
- Result:
 - flexible/stretchable embedded electronics using e.g. Silicone dielectric
- Applications: medical

M. Vanden Bulcke et al., *IEEE-EMBC 2006*



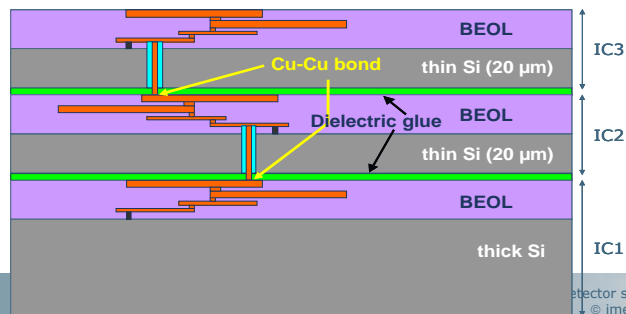
"chip-in-wire"

500 µm

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3D-SiC approach: Introduction

- **Technology:**
 - fabrication at device level, i.e. as a part of (CMOS) flow
- **Specifications:**
 - Si thickness: 10 – 20 μm
 - via diameter: 3 – 5 μm
 - via pitch: 10 μm
- **Applications:**
 - CMOS/memory/imager stacking

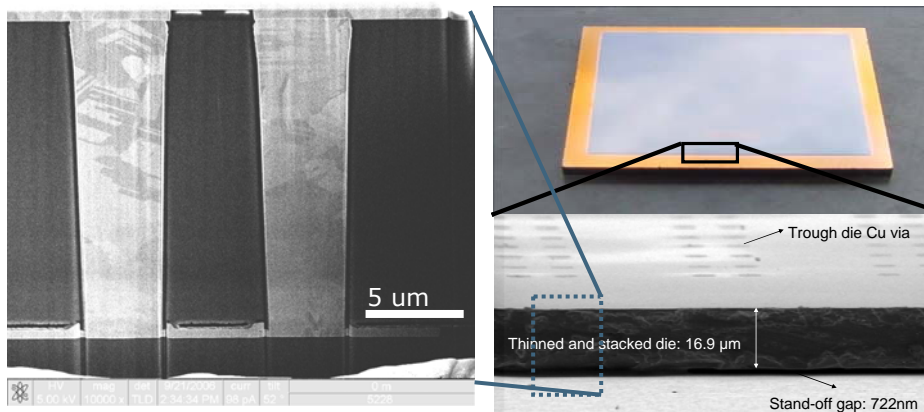


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3D-SiC approach: Results

- **Through Si vias:**
 - Pitch 10 micron, via diameter: 5 micron



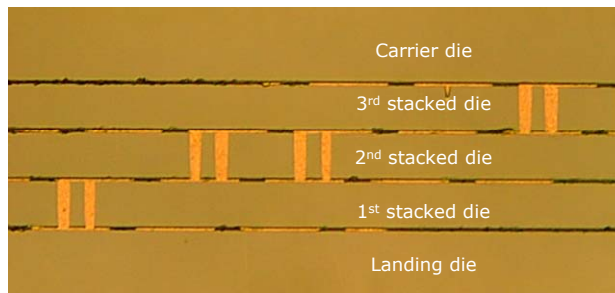
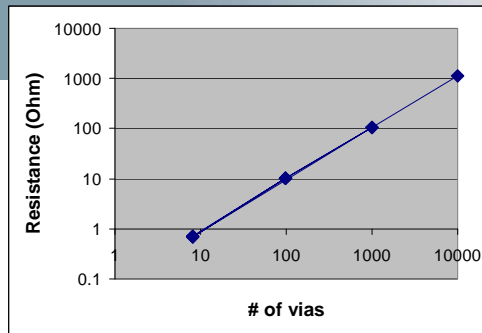
B. Swinnen et al., *IEDM 2006*

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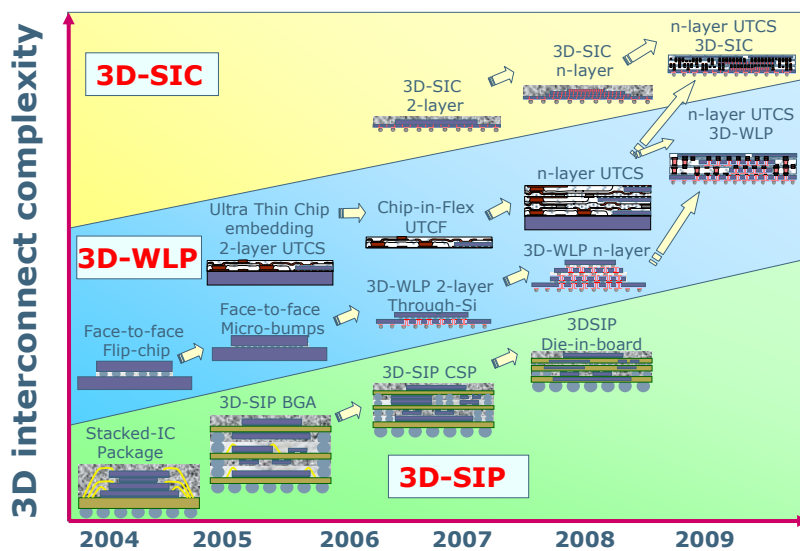
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3D-SiC approach: Results

- 10000 Cu vias in series yielding
- linear I-V curve
- via resistance ~ 30 mOhm
- 4-layer demonstrator realized



IMEC's 3D Interconnect R&D Roadmap


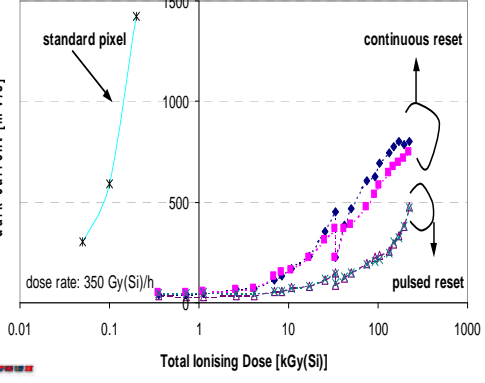


Positioning different 3D approaches				
	3D-SIP	3D-WLP		3D-SIC
Technology	Package interposer	WLP, Post-passivation		Si-foundry, Post FEOL
3D interconnect	Package I/O	UTCS Embedded die	Si-through vias	Si-through "Cu nail" vias
Intercon. Density	'package-to-package' 2 - 3 /mm	'around' die 10 - 50 /mm	'through' die 10 - 25 /mm	'through' die 25 -100 /mm
Peripheral				
Area-array	4 - 11/mm ²	100 -2.5k/mm ²	16 - 100/mm ²	400-10k/mm ²
3D Si Via pitch	-	-	40 – 100 μm	< 10 μm
3D interconnect pitch	300 – 500 μm	20 – 100 μm	-	-
3D Si Via diameter	-	-	25 - 100 μm	1 - 5 μm
Die thickness	> 50 μm	10 - <u>20</u> μm	<u>50</u> - 100 μm	<u>10</u> - 20 μm

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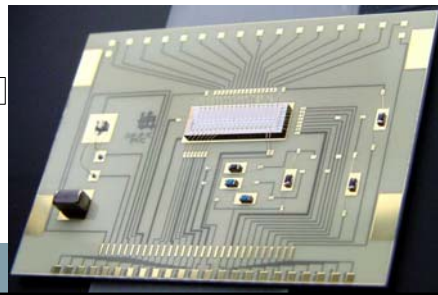
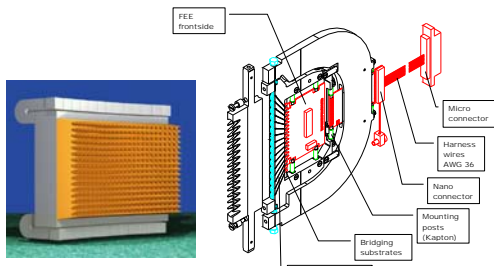
Enablers: Custom analog design: radiation tolerant

- Radiation-tolerant analog ROIC design:
 - nMOS pixel design (using 0.7μm Alcatel Microelectronics Technology)
 - 2-3 orders of magnitude less sensitive to total dose
- Example: Flight Model IRIS3
 - CMOS camera for imaging in space

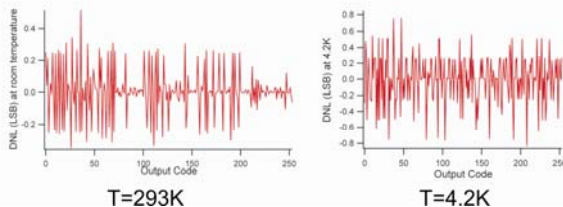
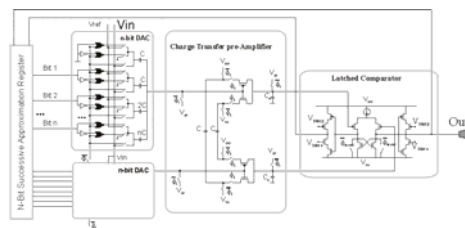
Enablers: Custom analog design: cryogenic ROICs

- Analog design for 4 Kelvin operation:
 - special design to avoid anomalous behavior of standard CMOS < 20 K
- Example: PACS-CRE: ROIC for a far-infrared detector array
 - ~ 200 qualified assemblies delivered to ESA
 - Herschel satellite to be launched in 2008
 - very low noise: measures 10 fA – 100 pA
 - very low power consumption: 80 μ W
 - irradiation tolerant @ 4 K

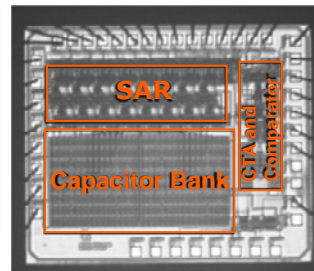


Enablers: Custom analog design: CryoADC

- Successive Approximation ADC at Cryogenic T:
 - 8 bit resolution
 - implemented in 0.7 μ m AMIS CMOS
 - 350 μ W power consumption
- Experiments show minor temperature dependence
- Aim: maintain signal integrity 4K – room temperature


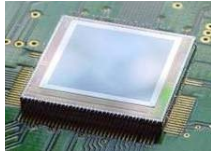
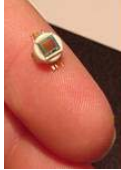





Y. Creten et al., ISSCC, 2007



Overview

- Introduction
- Technology enablers
- Detector systems examples:
 - BIB: far IR
 - Hybrid APS: VIS
 - Bold: UV
 - RelaxD: X-ray
- Conclusions & outlook

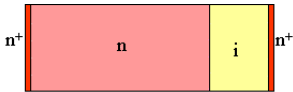
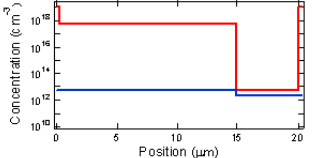








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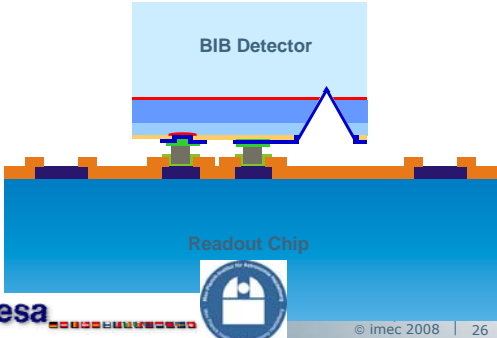
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Detector systems: Cryogenic BIB detector








	Contact layer: $N_D=10^{19} \text{ cm}^{-3}$ $N_A=$ -----
	Blocking layer: $N_D=5 \cdot 10^{12} \text{ cm}^{-3}$ $N_A=3 \cdot 10^{12} \text{ cm}^{-3}$
	Absorbing layer: $N_D=5 \cdot 10^{17} \text{ cm}^{-3}$ $N_A=5 \cdot 10^{12} \text{ cm}^{-3}$

- Far IR detection: 6 – 18 μm wavelength
- Si:As Blocked Impurity Band (BIB) detector array operating at 4 K
- Backside illuminated through high resistivity Si



- Hybridization on cryogenic ROIC using In bumps



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Detector systems: Cryogenic BIB detector

- Linear array: 2x 88 pixels
- Pitch: 30 μm
- Application:
 - DARWIN mission: search for exoplanets

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Detector systems: Backside illuminated CMOS imager

- Specifications:
 - 22.5 μm pitch
 - 1 - 4 Mpixel
 - thinned down to +/- 35 μm
 - In bump yield $\sim 99.95\%$

hybrid assembly

50 μm

diode array

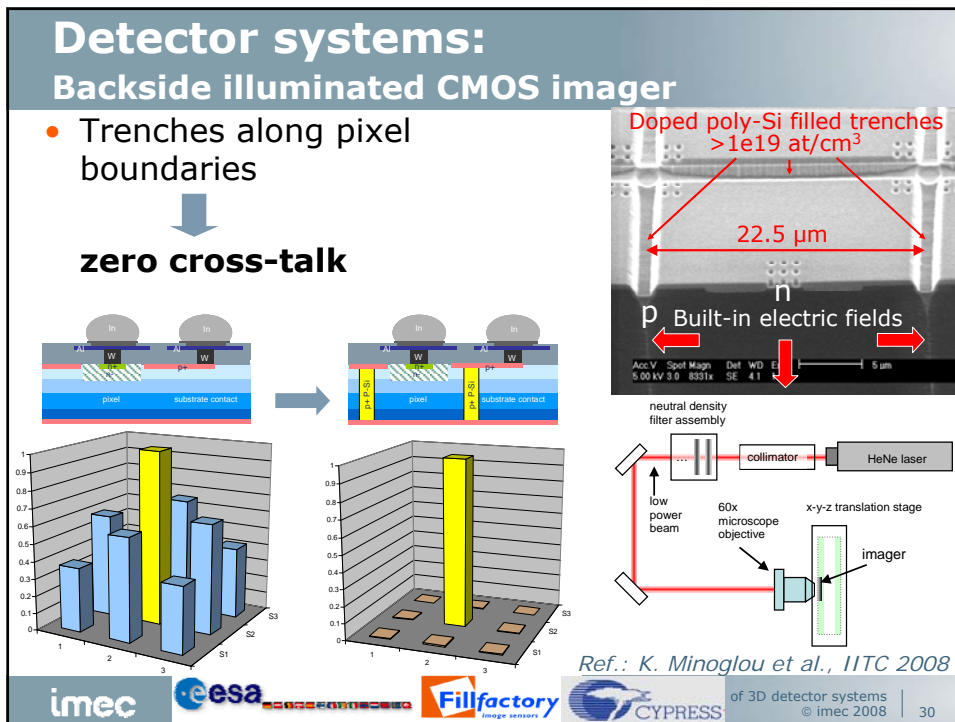
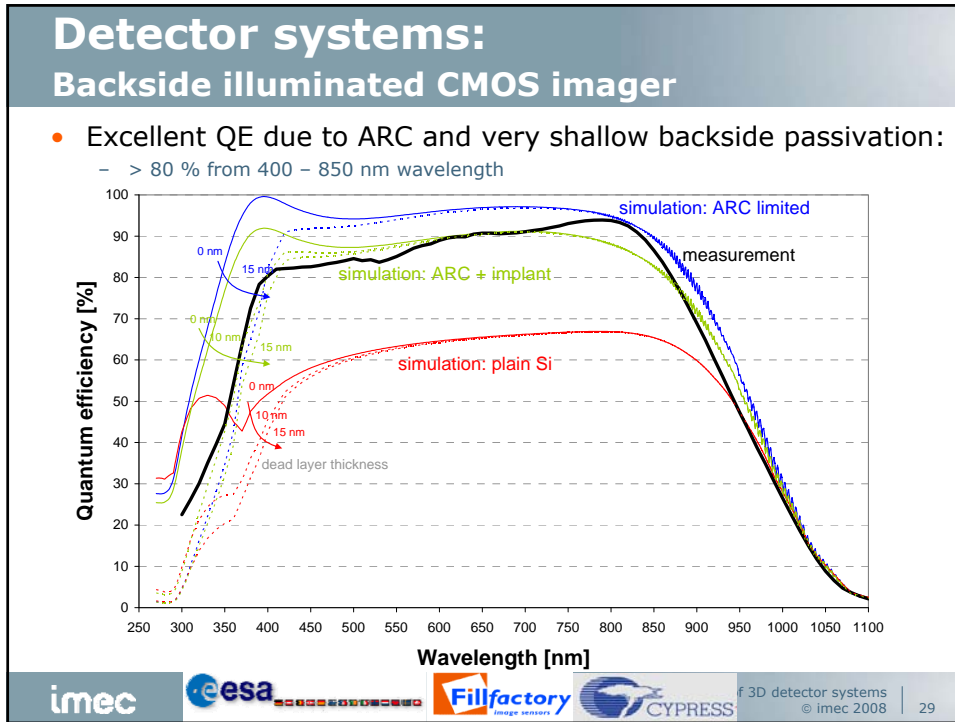
ROIC

hybrid diode array

ROIC

K. De Munck et al., IEDM 2006

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Detector systems: BOLD: 2D (X)UV detection

P372 GaN Schottky photodiode

Wavelength [nm]	Spectral responsivity [m A/W]
185	20
200	20
220	25
240	40
260	60
280	70
300	80
320	90
340	100
360	100
370	30
380	0.2
390	0.05
400	0.02

- Application: solar activity observation
- Large gap AlGaN Schottky or MSM diode detector
- Advantage over Si technology: intrinsically solar blind
- Backside illumination approach using wafer thinning, thin layer transfer, through Si optical access holes
- Hybridisation on 2D ROIC with 10 μm pitch

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Detector systems: RelaxD: tilable X-ray imagers

- Application: large area X-ray detection for XRD by tiling of imager modules
- Using Si X-ray detectors (Canberra) hybridized on Medipix ROICs (CERN)
- Issue: 'dead area' and hence loss of information at imager boundary due to:
 - wiring at > 1 side
- Solution:
 - Vertical electrical interconnections using 3D integration by using TSVs

2D X-ray detector
Medipix ROIC
PCB board

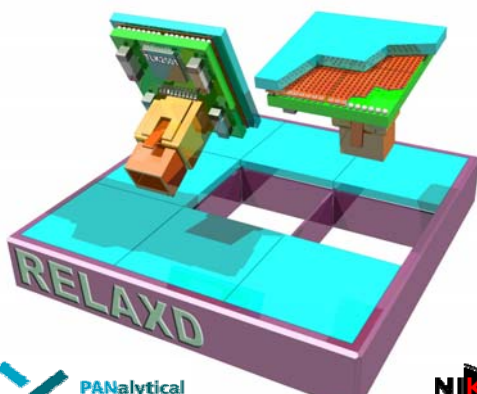
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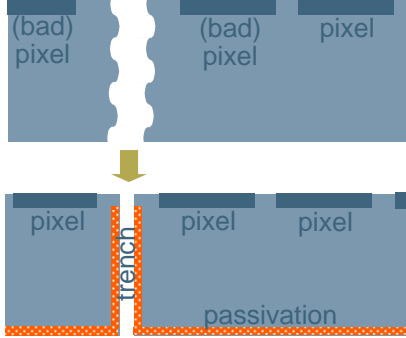
X-ray detector
Medipix ROIC
PCB board

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Detector systems: RelaxD: tilable X-ray imagers

- Issue: bad pixels at imager boundary due to damage by dicing
- Solution: edgeless detector concept:
 - Replace dicing by trench etching and proper passivation





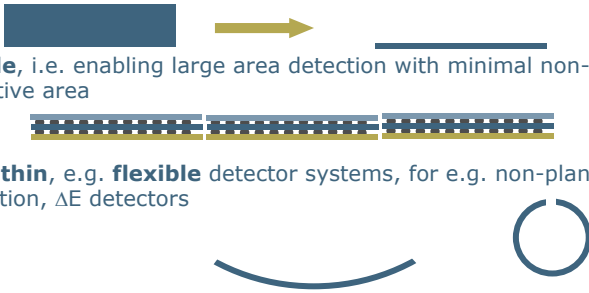
- Result: fully tilable X-ray imaging with minimal dead area






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Conclusions & outlook I

- 3D integration technology is developing fast
- It will allow manufacturing of advanced detection systems:
 - highly **miniaturized**, i.e. very small in vertical dimension
 - **tilable**, i.e. enabling large area detection with minimal non-sensitive area
 - **very thin**, e.g. **flexible** detector systems, for e.g. non-planar 4π detection, ΔE detectors

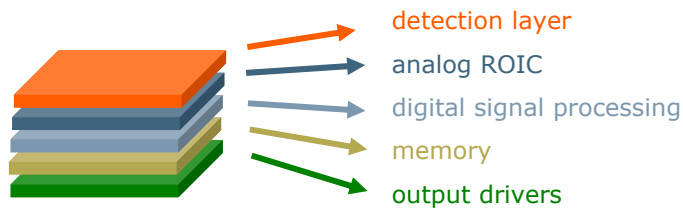




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Conclusions & outlook II

- 3D integration technology will allow manufacturing of advanced detection systems:
 - **complex** imaging detectors using high density 3D interconnects (≥ 1 per pixel) between different intelligent layers:



- Economical aspects:
 - (large) commercial foundries will offer 3D in (near) future
 - But: typically large volume
 - Solution: IMEC prototyping/small scale production "CMORE"

aspire invent achieve

