Three-Dimensionnal Pixel Sensors for an ILC Micro-Vertex Detector

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▷ **More information on ILC Web site: http://www.linearcollider.org/cms/**

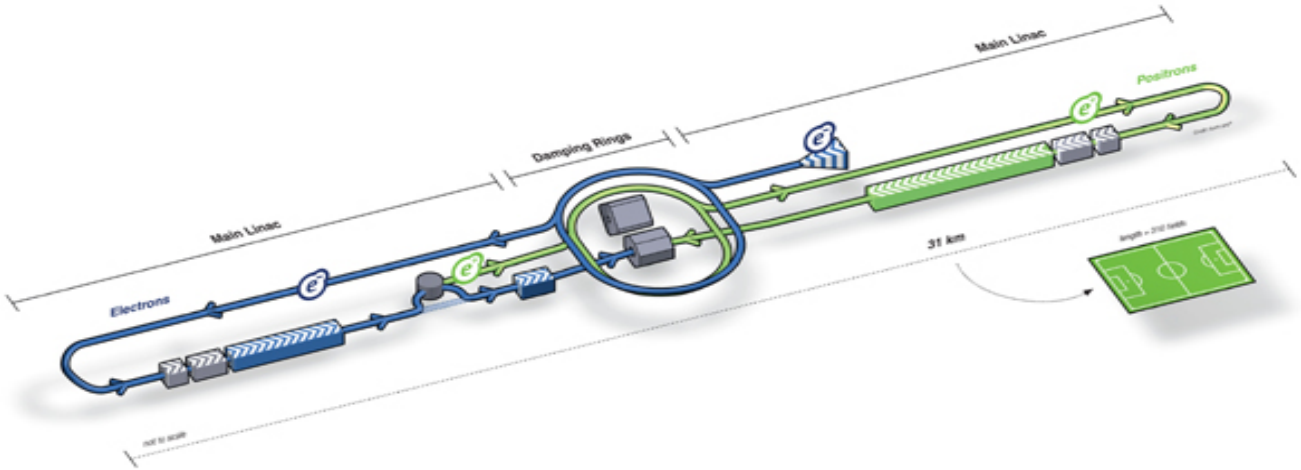
OUTLINE

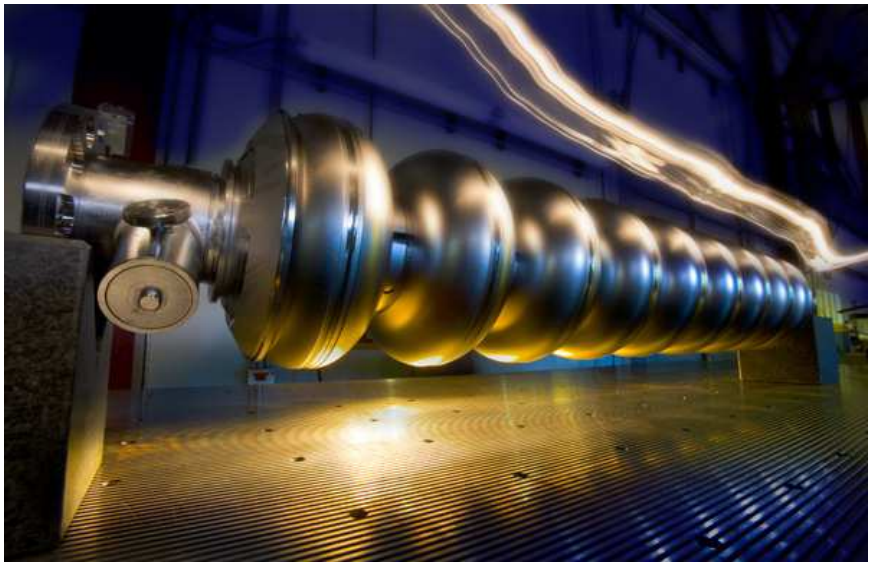
- **Requirements for a Vertex Detector at ILC**
  - *Constraints from physics goals*
  - *Constraints and Benefits from running conditions*
  - *Example of vertex detector geometry*
  - *Pixel technologies under development*
- **Expected evolution triggered by 3DIT**
  - *Signal processing functionnalities*
  - *Material budget*
  - *Concerns : power consumption, material budget*
  - *Common and complementary activities with sLHC*
- **Summary**

- **ILC $\equiv$ next large scale accelerator after LHC $\triangleright\triangleright\triangleright$ Physics $\gtrsim$ 2020**

  $\triangleright$ *it is an electron - positron linear collider : c.m. energy up to $\sim$ 1 TeV ; 31 km long site;*

  $\triangleright$ *it will* **deepen discoveries made at LHC** *and* **extend the experimental sensitivity to new phenomena** *underlying the history of Universe (laws of Nature) and its present mysteries (Dark Matter, Dark Energy)*





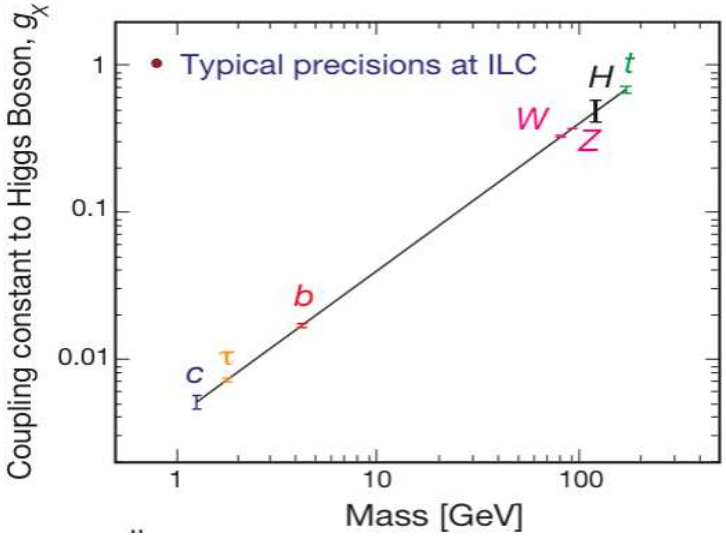
- **ILC design expected to be technically ready for construction $\gtrsim$ 2012 (... R&D started $\gtrsim$ 10 years ago ...)**

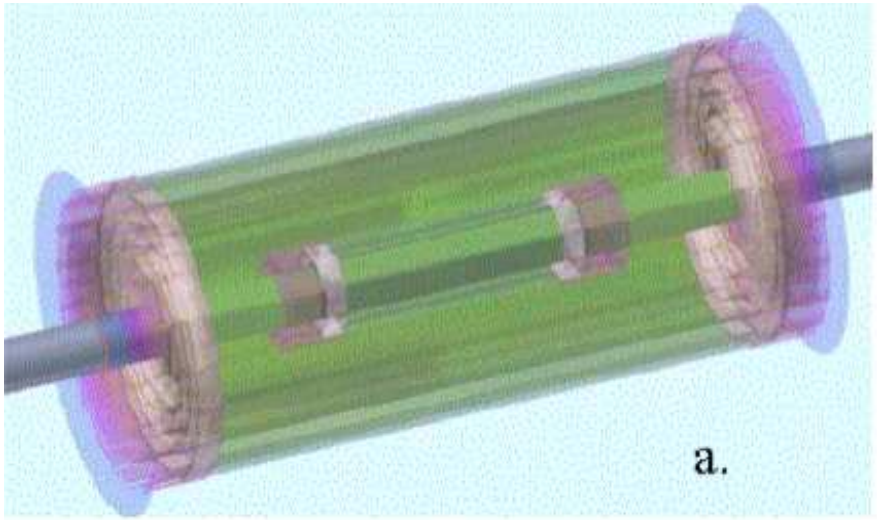
  $\hookrightarrow$ **Detector concept should mature synchronously** **(time scale less tight as LHC)**

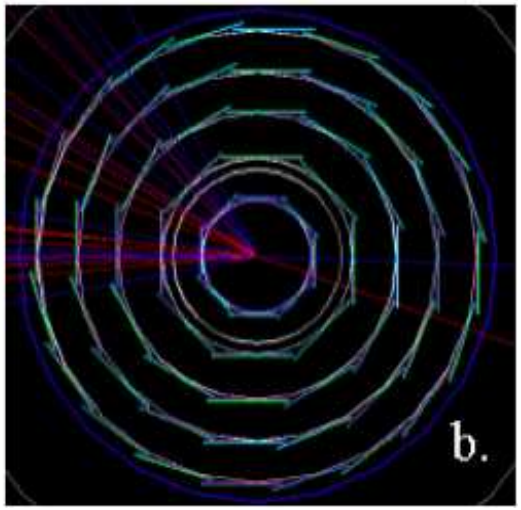
- **ILC is a high precision machine :**
  - ▷ *electron - positron collisions are relatively (compared to LHC) background free*
  - ▷ *physics conditions of elementary interactions are particularly well defined and tunable*

⇛ **Very high precision/sensitivity studies accessible if detectors are extremely sensitive**

⇛ **Vertex Detector with unprecedented performances**







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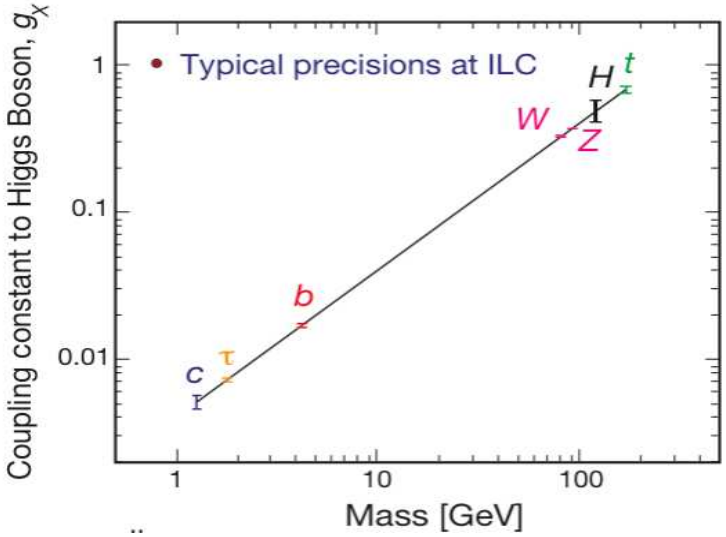
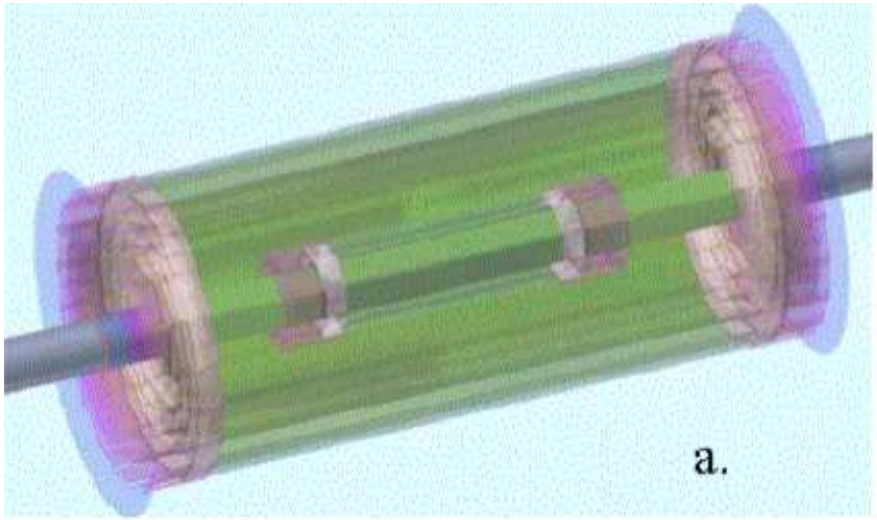
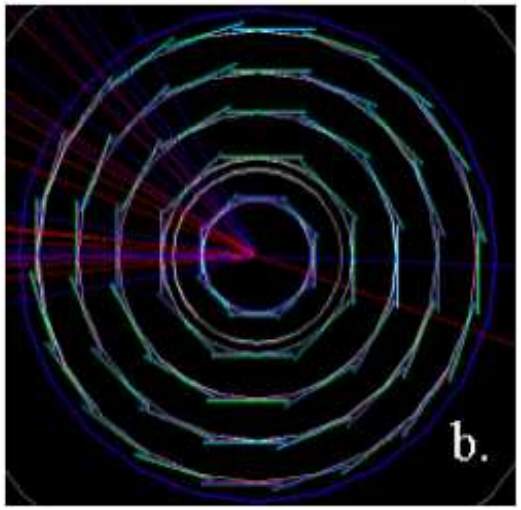






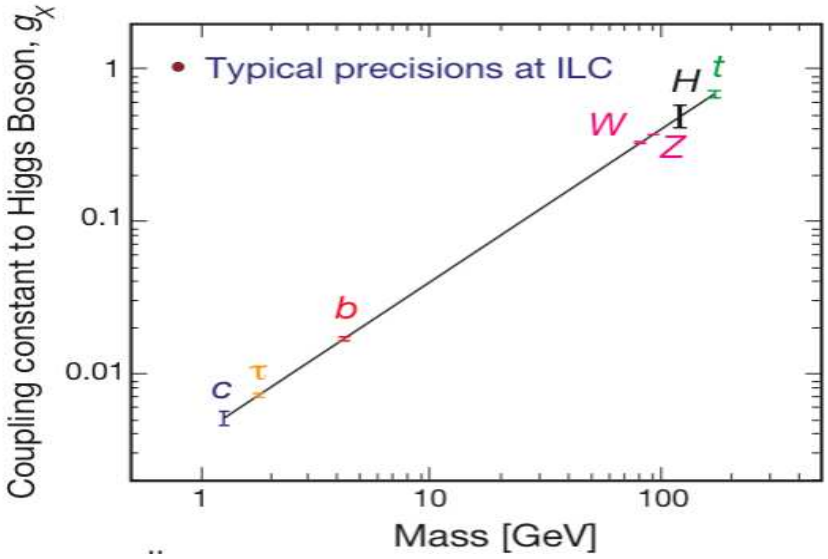
► 3D Integrated Technologies are expected to boost the access to the ultimate limit in precision and sensitivity

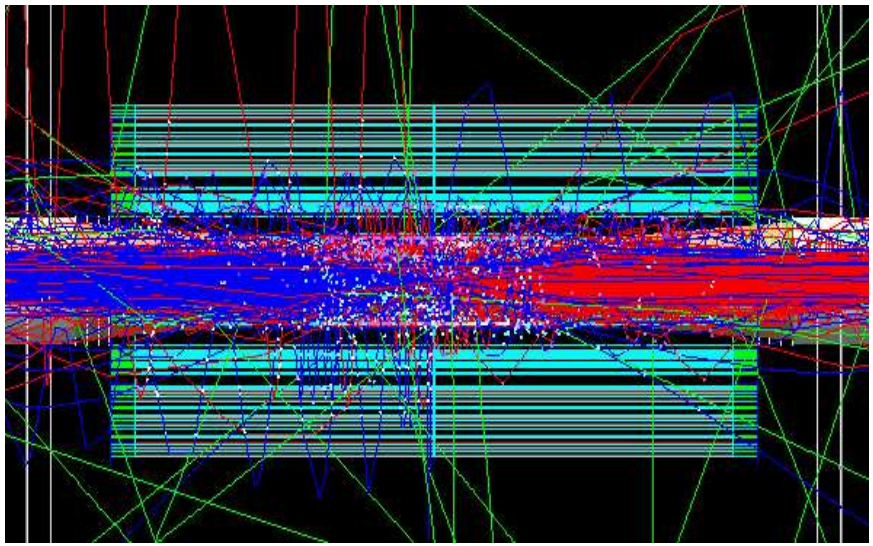
- **Vertex Detector requirements include 2 major antagonistic trends :**
  - **Physics goals :**
    - ▷ *high granularity ⟼ single point resolution*
    - ▷ *low material budget ⟼ thin detectors*
    - ▷ *small distance to vertex ⟼ inner most layer very close to Interaction Point*
    - ▷ *large number of events of interest ⟼ high interaction rate ⟼ high beam intensity*
  - **Running conditions :**
    - ▷ *high beam intensity ⇛ high particle rate*
      - ⇛ *occupancy and radiation dose increase when approaching the IP*
        - ⇛ *prevents from approaching the IP as close as desired .....*
          - ▷ *situation will worsen when collision energy ⟼ 1 TeV*
            - ⇛ **3DIT are expected to allow reducing the VD inner radius and keeping high precision vertexing at the highest collision energy**

- **Optimum between physics related requirements and limitations due to running conditions ?**
  - ⇛ **Substantially different for ILC and LHC: different pixel technologies to develop ⟼ 3DIT**
    - ↪ **Identify common and complementary ILC-LHC objectives**

- **ILC physics requires finding evidence of very short lived particles which decay $\gtrsim$ 100 μm away from the Interaction Point (e.g. Higgs $\rightarrowtail$ charmed mesons) , inside the vacuum beam pipe (R $\sim$ 15 mm)**

  $\hookrightarrow$ *reconstruct trajectories of electrically charged daughter particles with high resolution pixel detectors installed as close as possible to the Interaction Point*





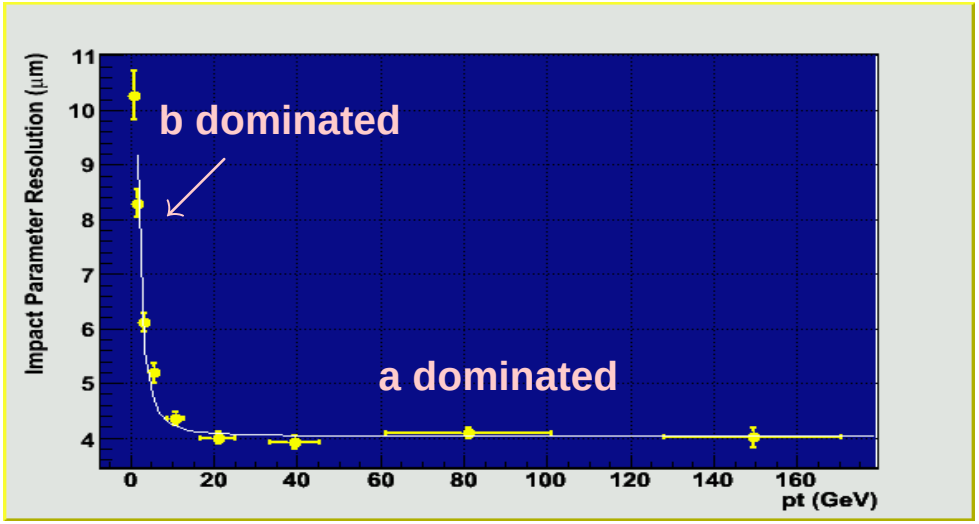
- **Major requirements :**
  - ◇ *Resolution on vertex position $\sim$ O(10) μm*
  - ◇ *Ionising radiation : O(100) kRad / yr*
  - ◇ *O(10^3) pixels /cm^2/10 μs (inner layer)*
  - ◇ *Non-ionising radiation $\lesssim$ O(10^{11})n_{eq}/cm^2/yr from $e^{\pm}_{BS}$ and $\lesssim$ O(10^{10})n_{eq}/cm^2/yr from neutron gas*

- **How to achieve high spatial resolution : small pixels (pitch) and reduced material ($\equiv$ weight)**

$\hookrightarrow$ *Figure of merit :* $\sigma_{ip} = a \oplus b/p_t$ $\rightarrowtail$ b *governs low momentum (*$\sim$ *30 % particles* $<$ *1 GeV/c)*

a *governs high momentum*

Accelerator	a (μm)	b ($\mu m \cdot GeV$)
LEP	*25*	*70*
SLD	*8*	*33*
LHC	*12*	*70*
RHIC-II	13	19
ILC	< 5	< 10



- **Expectations from 3DIT :**
  - ◇ *high degree of functionnality integration in very small pixels* $\rightarrowtail a \searrow$
  - ◇ *thinning and connection technologies allowing very low material budget* $\rightarrowtail b \searrow$

Beam time structure : *∼ 1 ms train (∼ 3000 BX) every 200 ms ⇛ duty cycle ∼ 1/200*

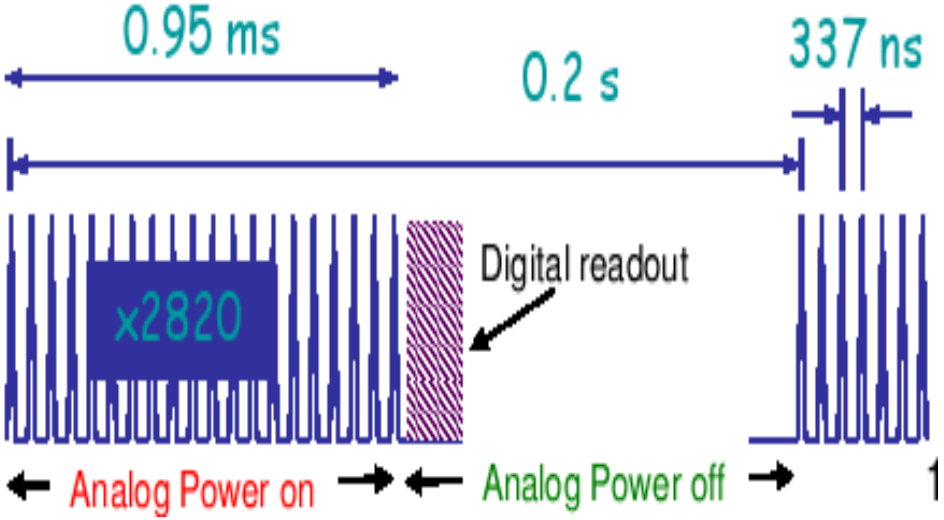
▷ **2 consequences :**

1) Switching off the sensors between trains may allow
average power reduction by factor of ∼ 100

⇛ essential for material budget (modest cooling)
also: room for high density functionnalities
integrated inside sensitive area (pixels)

2) Only a few BX contain relevant physics info.
but all contain large amounts of beam background

↪ remove unrelevant BX !



Electro-Magnetic Interference from bunch wake field :

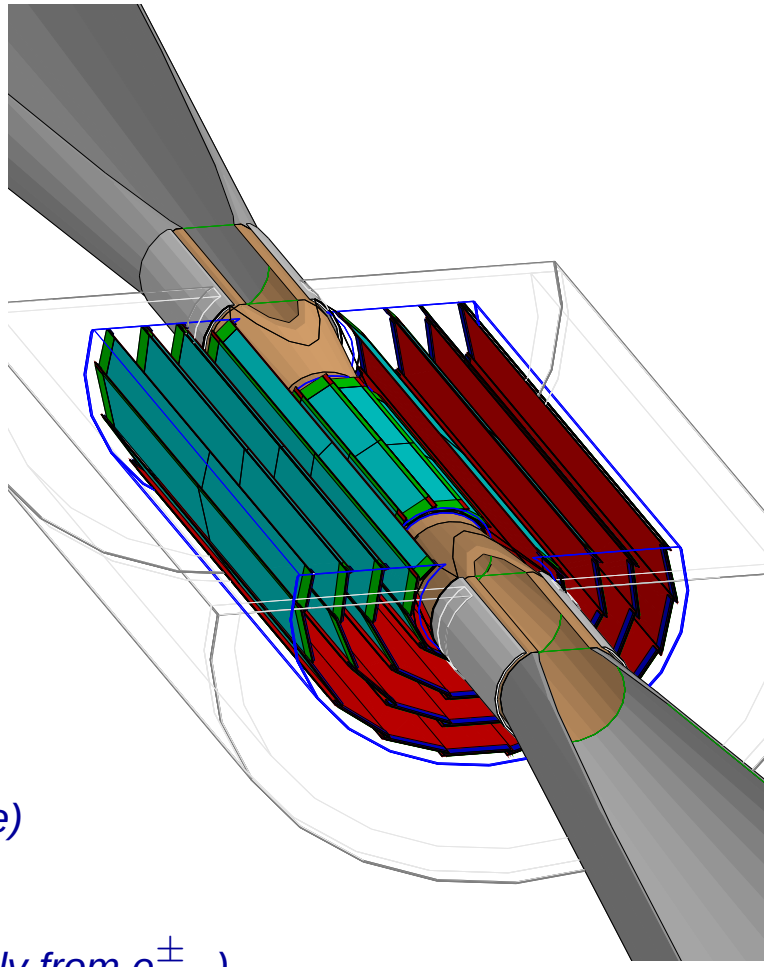
◇ *beam delivery elements may be source of very short λ EM field*

◇ *specific sensor architecture : store signal during train (∼ 1 ms) and read out after train*

⇛ large nb of memories ⇛ short time slices ⇛ better background rejection

↪ **3DIT may allow a big step towards this goal**

- **Vertex Detector geometries:**
  - ▷ *ILD : $\geq$ 5 (or 3 pairs of) long cylind. layers (R = 15–60 mm),*
  - ▷ *SiD: shorter barrel & fw/bw disks*
- **Possibly: room temperature operation**
  (modest cooling $\rightarrowtail$ minimise material)
- **Pixel pitch $\sim$ 5–25 μm (inner layer)**
  $\Rrightarrow$ *$\gtrsim$ 0.5 billion pixels equipping $\gtrsim$ 0.3 m^2*
- **Ultra thin layers: $\sim$ 0.1–0.2 % X_0/layer** *(STAR-HFT: $\lesssim$ 0.3 % X_0)*
- **Very low P_{diss}^{mean}: $<<$ 100 W** *(exact value depends on duty cycle)*
- **Fake hit rate $\lesssim 10^{-5}$** $\Rrightarrow$ *whole detector $\cong$ close to 1 GB/s (mainly from $e^{\pm}_{BS}$)*



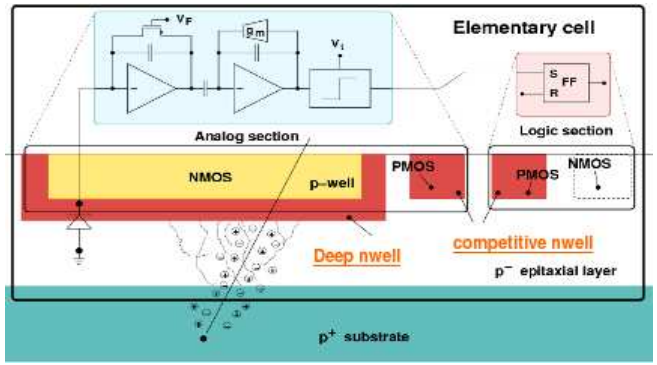
- **Mature pixel technologies (e.g. adapted to LHC or to SLD) are not adequate**

  ⇛ **several new technologies are being developed since several years**

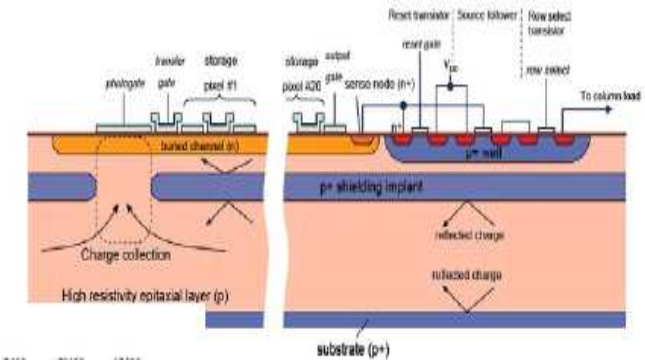
  - **DEPFETs** *(Germany)* : *continuous read-out architecture*
  - **CCDs** *(UK, Japan)* : *continuous and delayed read-out architectures*
  - **CMOS Sensors** *(France, Italy, USA)* : *continuous and delayed read-out architectures*

- **Example of pixel architectures with integrated signal processing:**

CMOS pixels with shaping + discri.



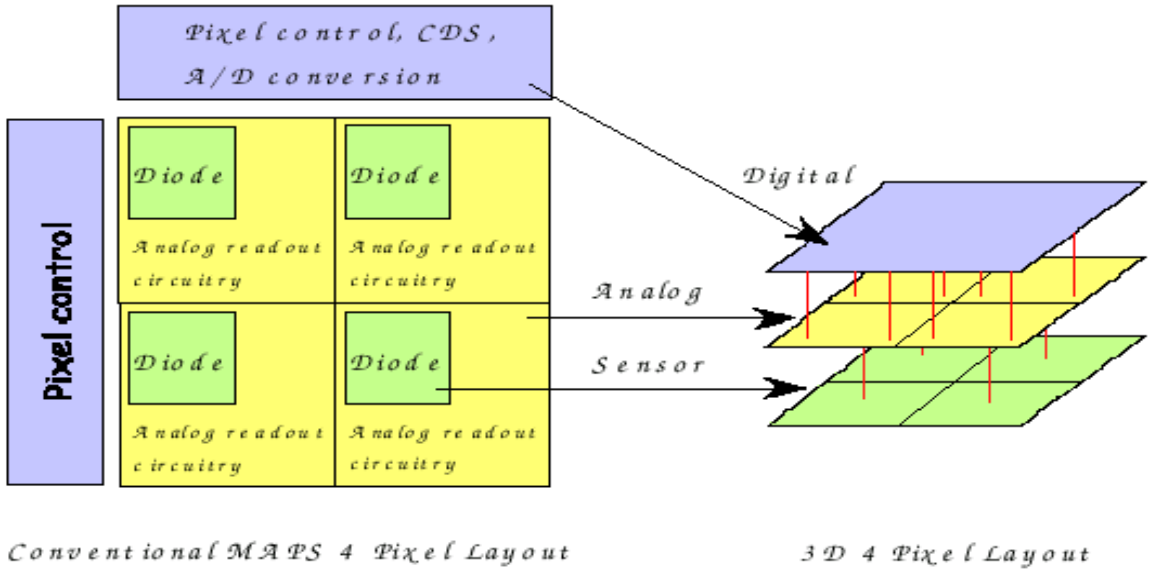
CCD pixels with memo. & delayed r.o.

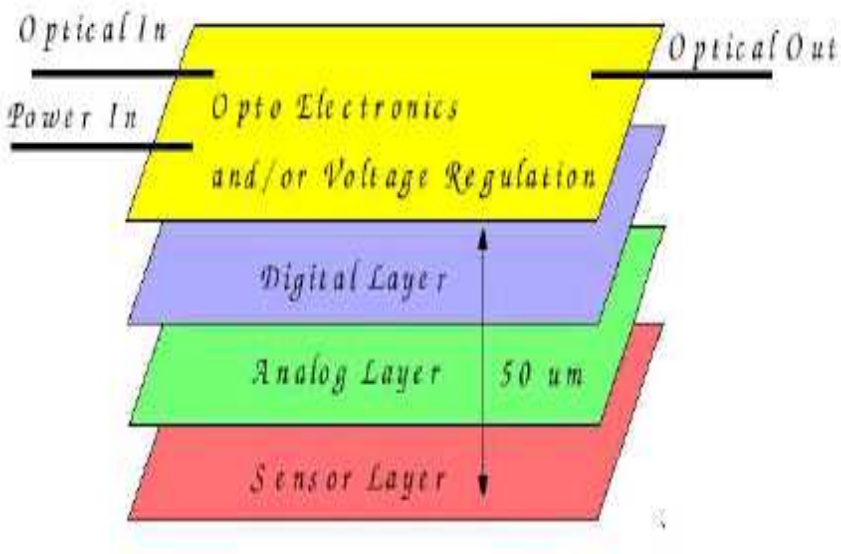


- *None of the present designs offers simultaneously desired pixel size, time resolution & data compression*

  ⟶ **Major motion to tame 3DIT and exploit their miniaturisation capabilities**

- **3DIT are expected to be particularly beneficial for CMOS sensors :**
  - *combine different fab. processes*
  - *alleviate constraints on transistor type inside pixel*
- **Split signal collection and processing functionnalities :**
  - *Tier-1: charge collection system*
  - *Tier-2: analog signal processing*
  - *Tier-3: mixed and digital signal processing*
  - *Tier-4: data formatting (electro-optical conversion ?)*
- **Use best suited technology for each Tier :**
  - *Tier-1: epitaxy, deep N-well ?*
  - *Tier-2: analog, low leakage current, process (nb of metal layers)*
  - *Tier-3 & -4 : digital process (nb of metal layers), feature size ⟼ fast laser (VOCSEL) driver, etc.*





- **Minimise multiple scattering inside detector material wherever possible ($b \searrow$)**

  $\hookrightarrow$ *thickness, amount and choice of material for mechanical support, gluing, electrical connexions, thermal conductivity, power dissipation (avoid active cooling), ...*

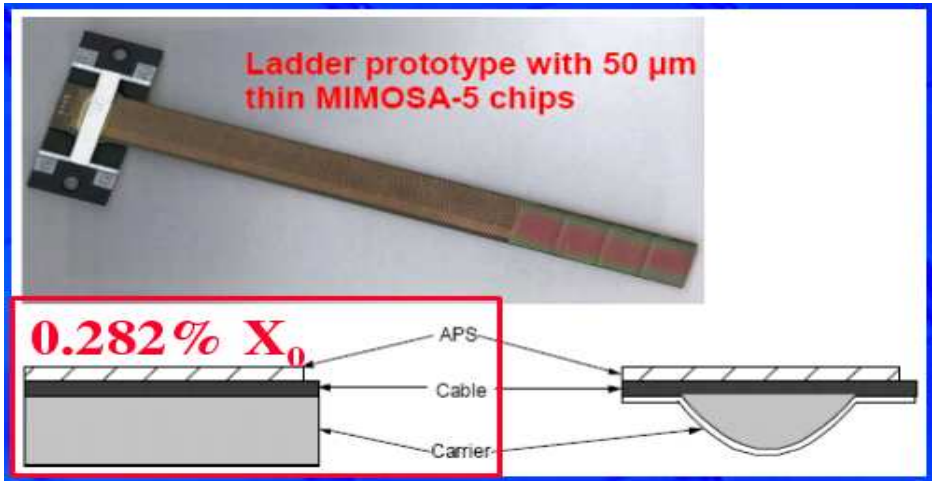
- **Goal : $<$ 0.2 % radiation length / layer** *(including chip + support + services) ($\Leftrightarrow <$ 200 μm of silicon)*

- **Presently $\lesssim$ 0.3 % seems achievable** *(STAR vertex detector)*

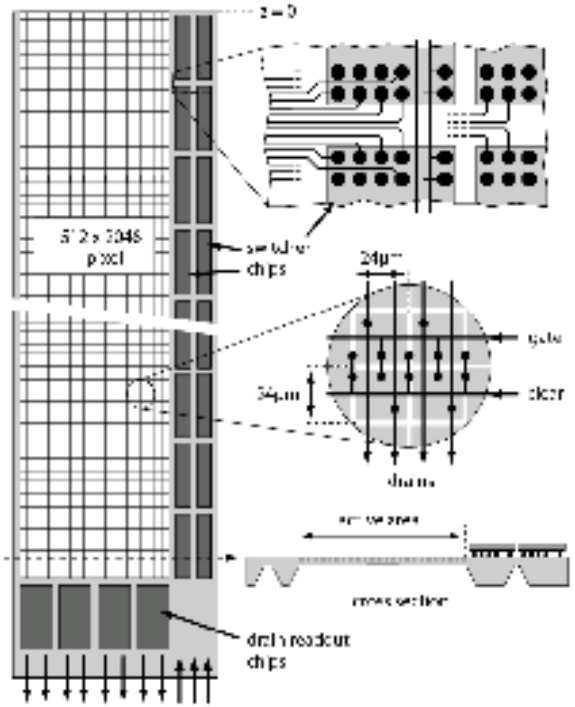
- **STAR ladder : kapton cable contributes with $\sim$ 0.1 %**
  and carrier with $\sim$ 0.1 % of radiation length

  $\Rrightarrow$ **replace them with aluminised CVD diamond ?**

  $\hookrightarrow$ *bonus in thermal transport*



- **Minimise insensitive areas inside fiducial volume**
  and extend the sensitive area to small polar angles
  - ◇ *CMOS sensors: mixed and digital μcircuits at sensor edge*
  - ◇ *DEPFETs: steering chips bonded along ladder* $\longmapsto$
  - ◇ *End of ladder electronics*

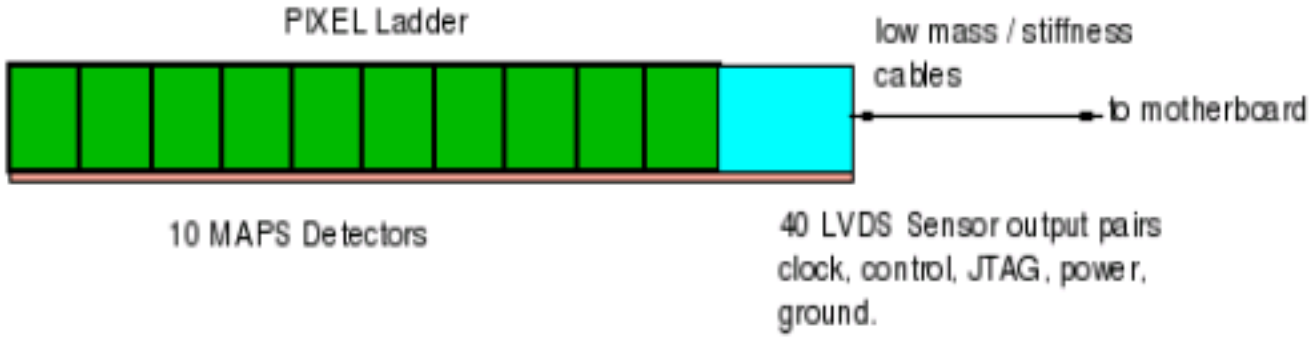


- **(CMOS) Sensor fabrication yield is a concern**

  $\Rrightarrow$ *diced sensors prefered to stitched sets of 5–10 sensors*

$\hookrightarrow$ *inactive zones (twice $\gtrsim$ 40 μm wide) at sensor edge from dicing*

$\Rrightarrow$ *can these zones be reduced to $\lesssim$ few μm with plasma etching ?*



- **Effects of vias on material budget:**
  - ◇ *Ex: 20x20 μm^2 pitch $\longmapsto$ 250,000 pixels/cm^2* ◇ *2 vias/pixel ($\emptyset$ = 2 μm, L = 20 μm)*
    - $\Rrightarrow$ *0.01 % if made of tungsten $\cong$ 10 % of full ladder material budget !!!* *(concern for ILC mainly)*
    - $\Rrightarrow$ **Sensor architecture should be guided by the necessity to minimise :**
      - $\backsimeq$ *pixel density* $\backsimeq$ *via density* $\backsimeq$ *number of tiers*

- **Effect of highly integrated signal processing functionnalities:**
  - ◇ *Ex (CMOS sensors) : present col. // design features P(pixel) $\sim$ 200 μW & P(discri) $\sim$ 300 μW*
    - ▷ *If this would propagate to 250,000 pixels/cm^2 $\Rrightarrow$ P(chip) $\gtrsim$ 100 W/cm^2 during train !!!*
    - $\Rrightarrow$ *$\sim$ O(1) W/cm^2 in average (chip off between trains)* $\Rrightarrow$ *several kW fro the full detector !!!!*
    - $\Rrightarrow$ **Sensor architecture should be guided by the necessity to minimise power consumption:**
      - $\backsimeq$ *pixel and signal processing architecture* $\backsimeq$ *power cycling capability (essential for ILC)*

- **2008 : explore, and exploit some of the, possibilites offered by industry and semi-academic labs**
  - ◇ *Commercial multi-tier chip design and packaging, e.g. 2-tier device for sensing & signal proc. (see R.Y.)*
    - ↪ *Learn designing in CMOS technologies involved ⟼ "new" fab. processes (e.g. IBM 130 nm)*
      Concern: substrate characteristics (sensitive volume)
  - ◇ *Investigate technology : via characteristics, parasitic couplings, radiation tolerance, power cycling, ...*
  - ◇ *Investigate system integration aspects : edgeless dicing, CMOS sensors / diamond, sensor thinning, ...*
  - ◇ *Explore possibilties to combine wafers from different fab. processes (e.g. AMS-0.35 OPTO with IBM-0.13)*
  - ◇ *Others ???*

- **2009: start developing architectures adapted to ILC vertex detector**
  - ◇ *Step 1: combine tier adapted to charged particle detection with tier hosting signal processing μcircuits*
  - ◇ *Step 2: design a 2-tier chip with integrated signal storage (1 ms) and delayed (low power) read-out*
  - ◇ *Step 3: design a 3-tier chip with integrated data formatting*
  - ◇ *Develop system integration aspects for an ILC ladder*
  - ◇ *Investigate radiation tolerance and power cycling*

- **ILC vertex detector provides a very demanding framework for pixel detector R&D**

  $\Rrightarrow$ *unprecedented performances ambitionned* $\rightarrowtail$ *different from sLHC target values and time line*

- **The R&D addresses two areas: Pixel array &System integration performances**

- **Natural choice for ILC sensor architecture exploits beam time structure** $\rightarrowtail$ **power saving, no EMI :**

  ▷ *thin sensitive volume* $\rightarrowtail$ *Tier-1*

  ▷ *signal storage during 1 ms with 10* μs *resolution* $\rightarrowtail$ *Tier-2*

  ▷ *delayed read-out and data formatting* $\rightarrowtail$ *Tier-3 (+ 4 ?)*

- **ILC specific concerns:**

  ▷ *power cycling* $\rightarrowtail$ *reduce (time averaged) power by factor of* $O(100)$ $\rightarrowtail$ *mechanical stress ????*

  ▷ *material budget* $\rightarrowtail$ *full ladder* $\cong$ *0.1–0.2 %* X_0 *(nb of vias ...)*

- **Several common issues with sLHC** $\Rrightarrow$ **common or complementary actions:**

  ▷ *3D technological aspects: via characteristics, parasitic couplings, rad. tolerance, design tricks/rules/kits*

  ▷ *design in dedicated CMOS fab. technologies : e.g. IBM-0.13* $\rightarrowtail$ *"building blocks" ???*

  ▷ *explore the (fast moving) "3DIT landscape"* $\rightarrowtail$ *network for common knowledge building*

  $\Rrightarrow$ *Optimise complementarity against redundancy*