3D activities and plans in Italian HEP labs

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Vertical integration technologies in Italian R&D programs

- In Italy, so far interest for 3D vertical integration of sensors and readout electronics mainly comes from people involved in MAPS developments and in tracking and vertexing systems in ILC and SuperB

- 3D could address needs to operate pixel detectors at high rate with low material budget to optimize position and momentum resolution; information from the tracking system could be used in a Level 1 trigger system

- Vertical integration would offer solutions for a higher functional density and a better signal-to-noise ratio and charge collection efficiency as compared to 2-D MAPS

CMOS MAPS R&D: the Italian way

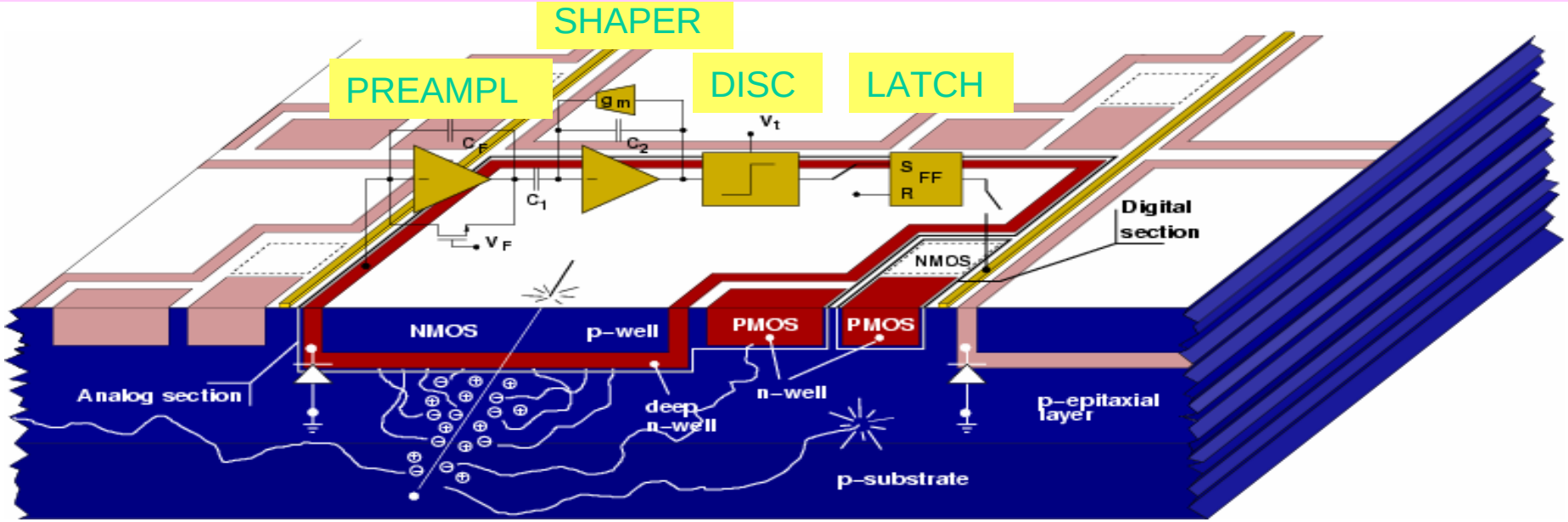
- 130nm Deep NWell MAPS design for SuperB
  - → the APSEL series chips with sparsified readout and time stamping (see talk on SuperB Vertex Detector)
  - → Funding by INFN (SLIM5 collaboration) and Italian Ministry of University and Research (PRIN)

- 130nm DNW CMOS MAPS for the ILC Vertex Detector
  - → smaller pitch and power dissipation, different readout architecture
  - → funding by INFN (P-ILC collaboration)

- 180nm and 130nm bulk CMOS MAPS
  - → Various readout architectures, small pixels
  - → funding by INFN (Perugia and Roma3 groups)

Deep N-Well (DNW) sensor concept

New approach in CMOS MAPS design compatible with data sparsification architecture to improve the readout speed potential



Classical optimum signal processing chain for capacitive detector can be implemented at pixel level:

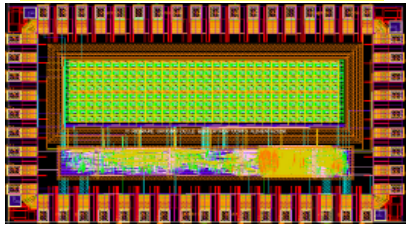
- Charge-to-Voltage conversion done by the charge preamplifier
- The collecting electrode (Deep N-Well) can be extended to obtain higher single pixel collected charge (the gain does NOT depend on the sensor capacitance), reducing charge loss to competitive N-wells where PMOSFETs are located
- Fill factor = DNW/total n-well area ~90% in the prototype test structures

Why hybrid-pixel-like MAPS

- Modern VLSI CMOS processes (130 nm and below) could be exploited to increase the functionality in the elementary cell → sparsified readout of the pixel matrix.
- Data sparsification could be an important asset at future particle physics experiments (ILC, Super B-Factory) where detectors will have to manage a large data flow
- A readout architecture with data sparsification will be a new feature which could give some advantages with respect to existing MAPS implementations → flexibility in dealing with possible luminosity and background changes during the experiment lifespan, decouple modularity from readout speed
- An ambitious goal is to design a monolithic pixel sensor with similar readout functionalities as in hybrid pixels (sparsification, time stamping)

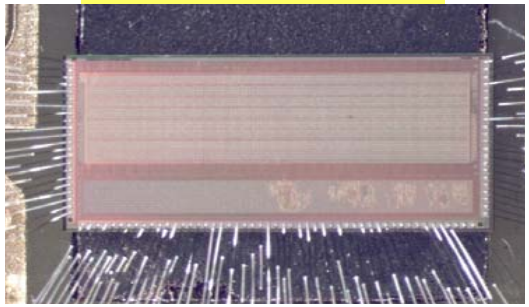
130 nm DNW MAPS: first generation of CMOS sensors with in-pixel sparsification and time stamping (to be tested in a beam quite soon)

APSEL3D



8x32 matrix.
Shielded pixel
Data Driven
sparsified readout

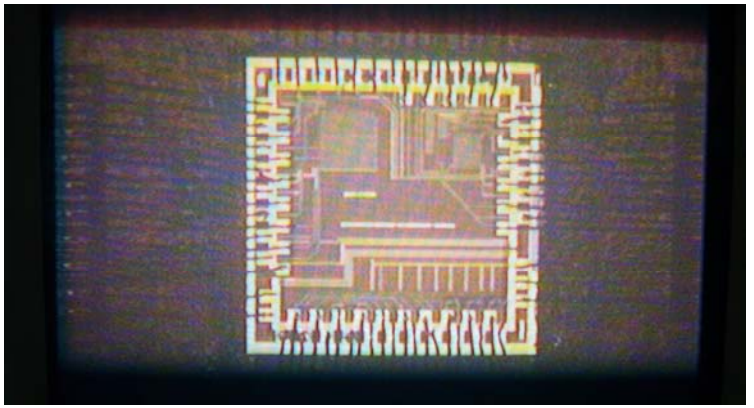
APSEL4D



32x128 matrix.
Data Driven,
continuously operating
sparsified readout
Beam test Sep. 2008

50x50 um pitch

SDR0



16x16 matrix + smaller test structures.
Intertrain sparsified readout

25x25 um pitch

130nm CMOS DNW MAPS for the ILC vertex detector

- INFN program started in 2006; design DNW MAPS according to ILC specifications

  (INFN Milano, Pavia, Roma III; University of Bergamo, University of Insubria, University of Pavia)
- Same concept as in the APSEL chips, but reduced pixel pitch and power dissipation
- Digital readout architecture with in-pixel sparsification logic and time stamping, taking into account the beam structure of ILC
- A pipeline with a depth of one in each cell should be sufficient to record > 99% of events without ambiguity
- Data can be readout in the intertrain interval → system EMI insensitive

Sparsified readout architecture

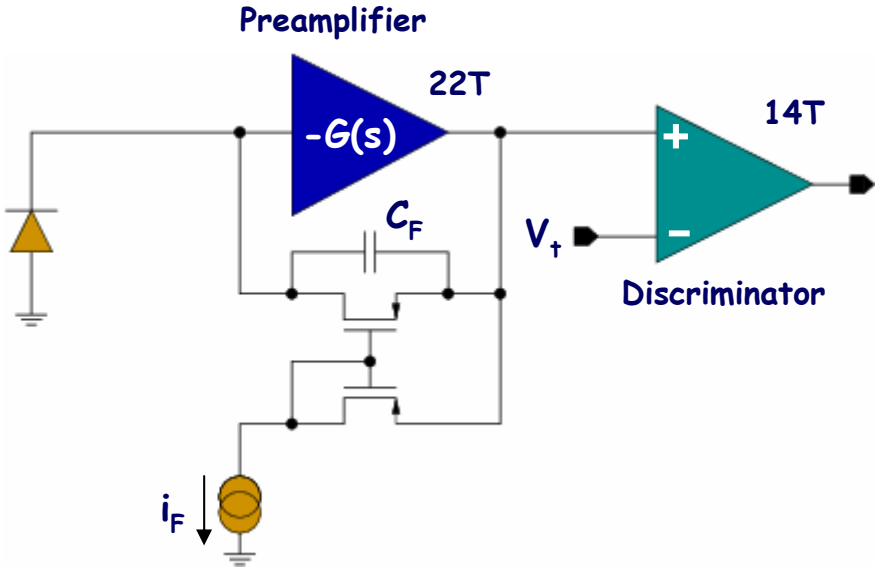
- In DNW MAPS sensors for ILC sparsification is based on a token passing readout scheme suggested by R. Yarema (FNAL)

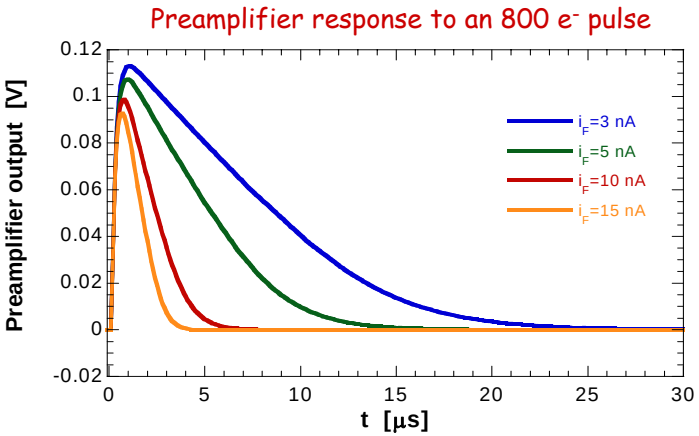
  (R. Yarema, "Fermilab Initiatives in 3D Integrated Circuits and SOI Design for HEP", *ILC VTX Workshop at Ringberg*, May 2006)

- This architecture was first implemented by Fermilab ASIC designers Jim Hoff, Tom Zimmerman and Gregory Deptuch in the VIP1 chip (3-D MIT LL technology, see Fermilab presentation on Wednesday)

- MAPS sensor operation is tailored on the structure of ILC beam
  - Detection phase (corresponding to the bunch train interval)
  - Readout phase (corresponding to the intertrain interval)

Pixel level processor





- C_F obtained from the source-drain capacitance
- High frequency noise contribution has been reduced limiting the PA bandwidth

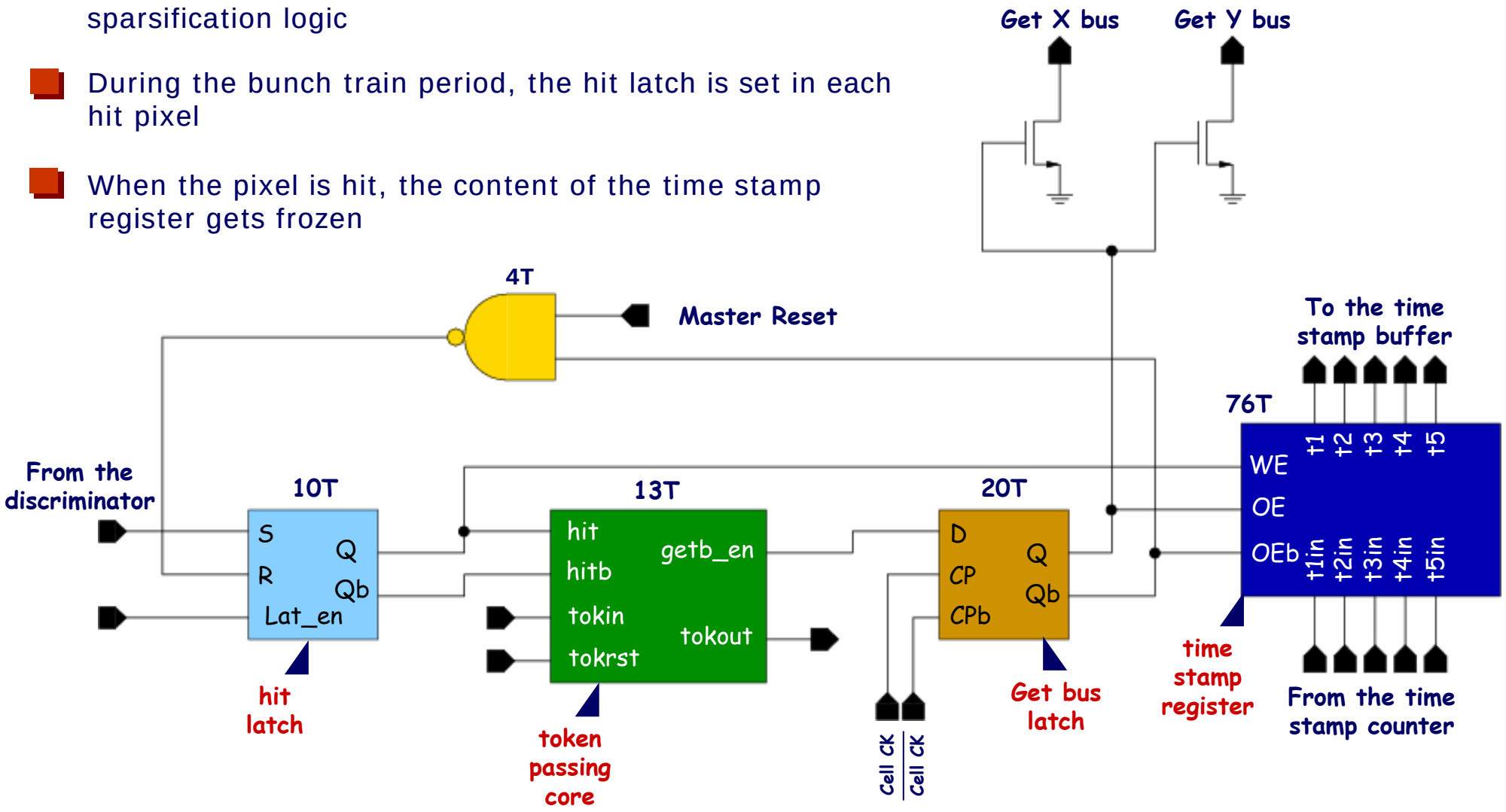
From simulations:

- ENC = **25 e⁻ rms@C_D=100 fF**
- Threshold dispersion ≈ **30 e⁻ rms**
- Power consumption ≈ **5 µW**
- Features power-down capabilities for power saving: the analog section cell can be switched off during the intertrain interval in order to save power

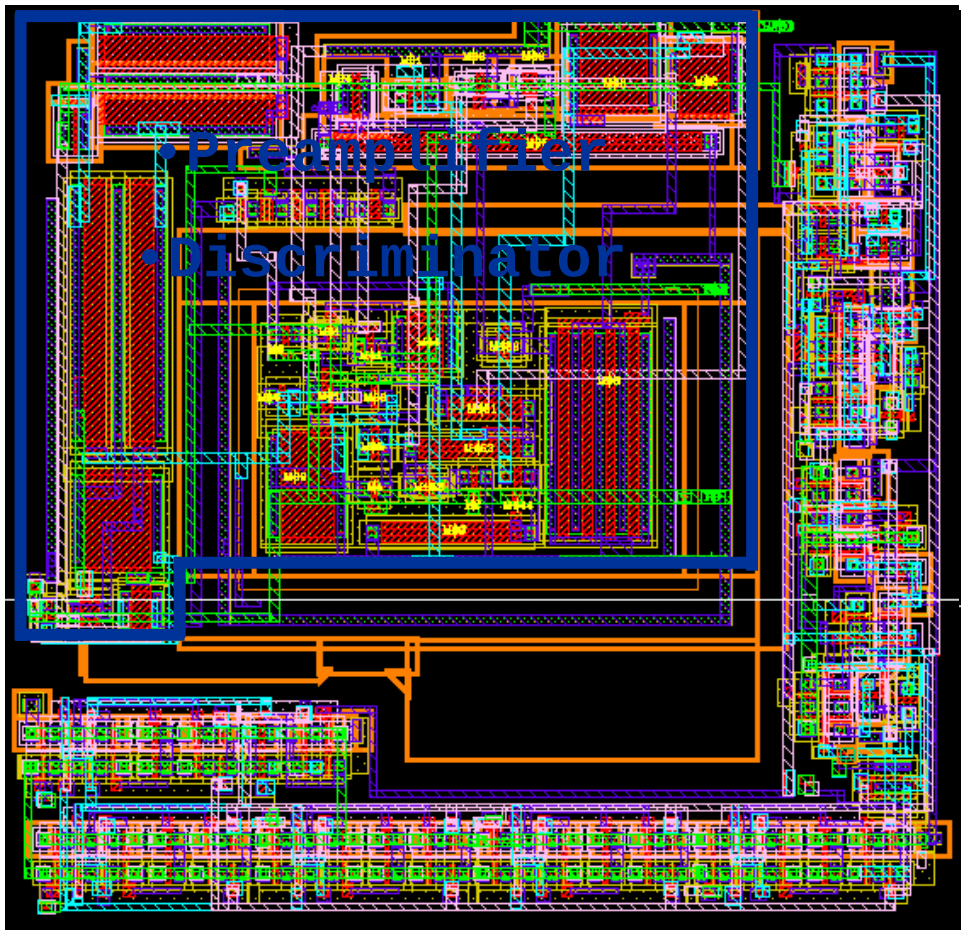
  (**1% duty-cycle** seems feasible)

Cell digital section

- Includes a 5 bit time stamp register and the data sparsification logic
- During the bunch train period, the hit latch is set in each hit pixel
- When the pixel is hit, the content of the time stamp register gets frozen



ILC DNW elementary cell



analog front-end

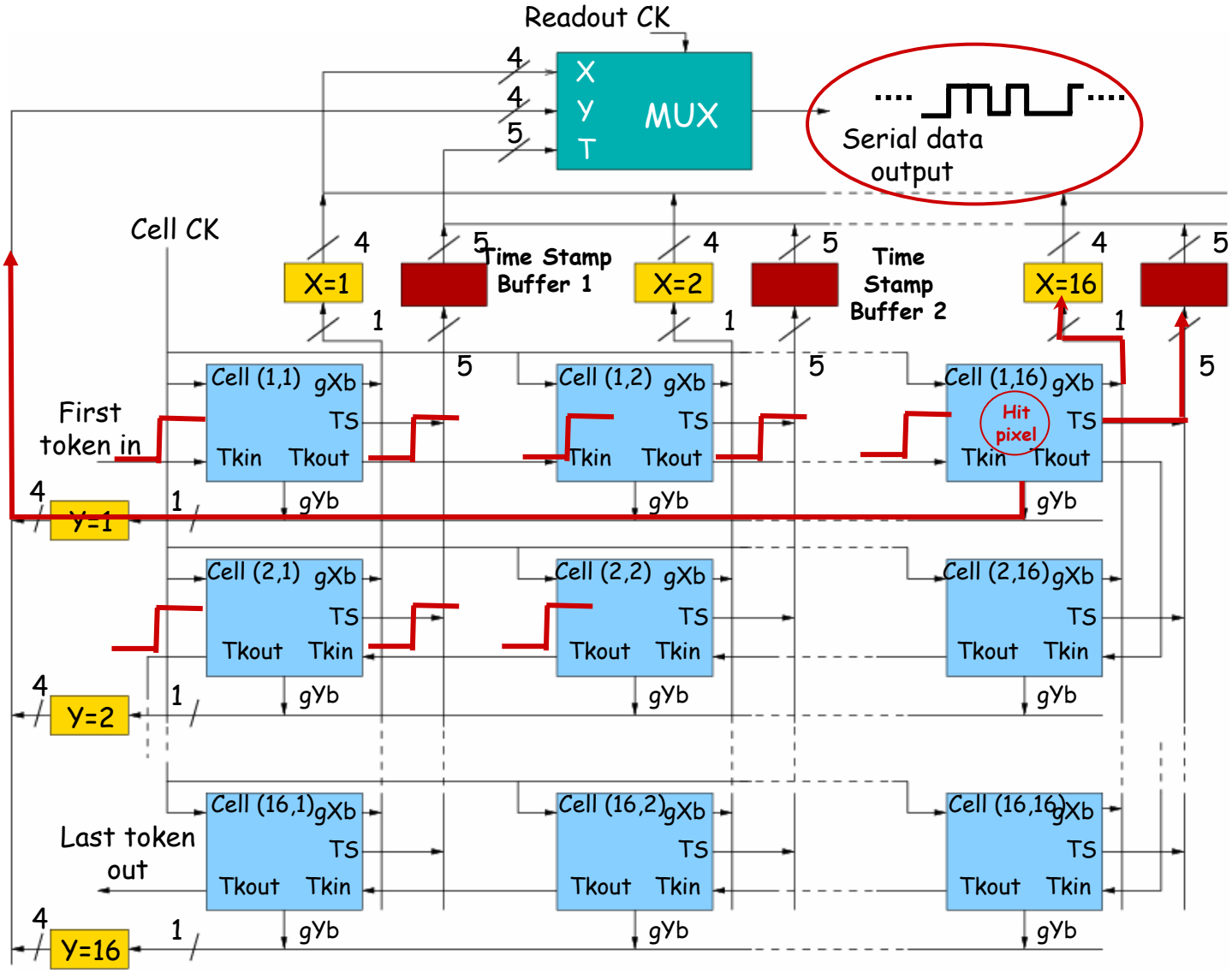
+

digital section

↓

164 transistors

Digital readout scheme



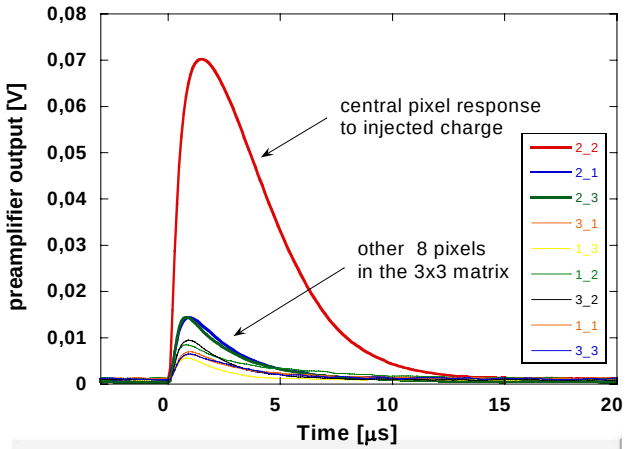
Readout phase:

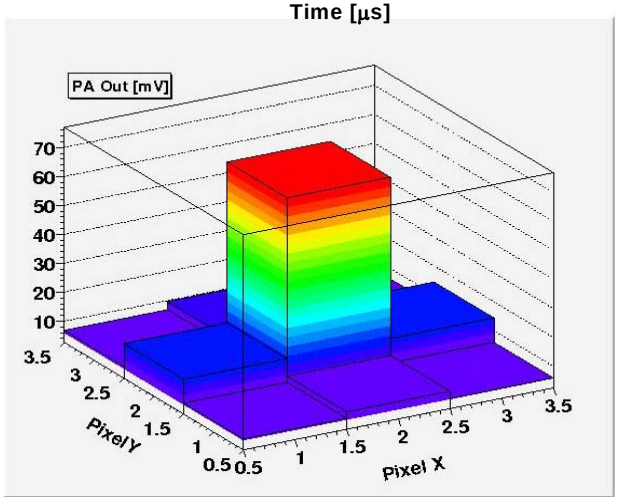
- token is sent
- token scans the matrix and
- gets caught by the first hit pixel
- the pixel points to the X and Y registers at the periphery and
- sends off the time stamp register content
- data are serialized and token scans ahead

The number of elements may be increased without changing the pixel logic (just larger X- and Y-registers and serializer will be required)

SDR0 experimental results

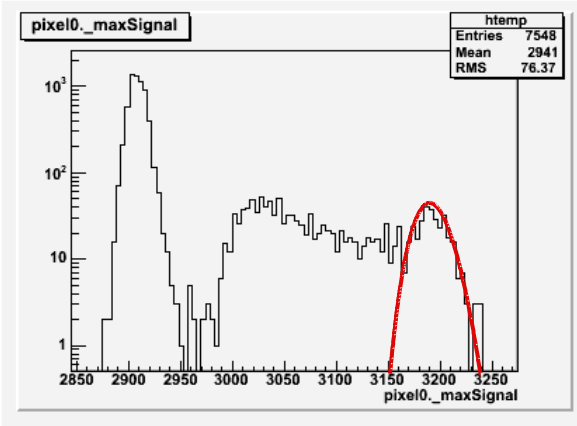
Matrix response to infrared laser





- Average **charge sensitivity ≈ 0.7 V/fC**
- ENC = **40 e rms @ C_D=120 fF**
  (preamplifier input device: I_D = 1 µA, W/L = 22/0.25)
- **Threshold dispersion ≈ 60 e** (in 8x8 matrix)

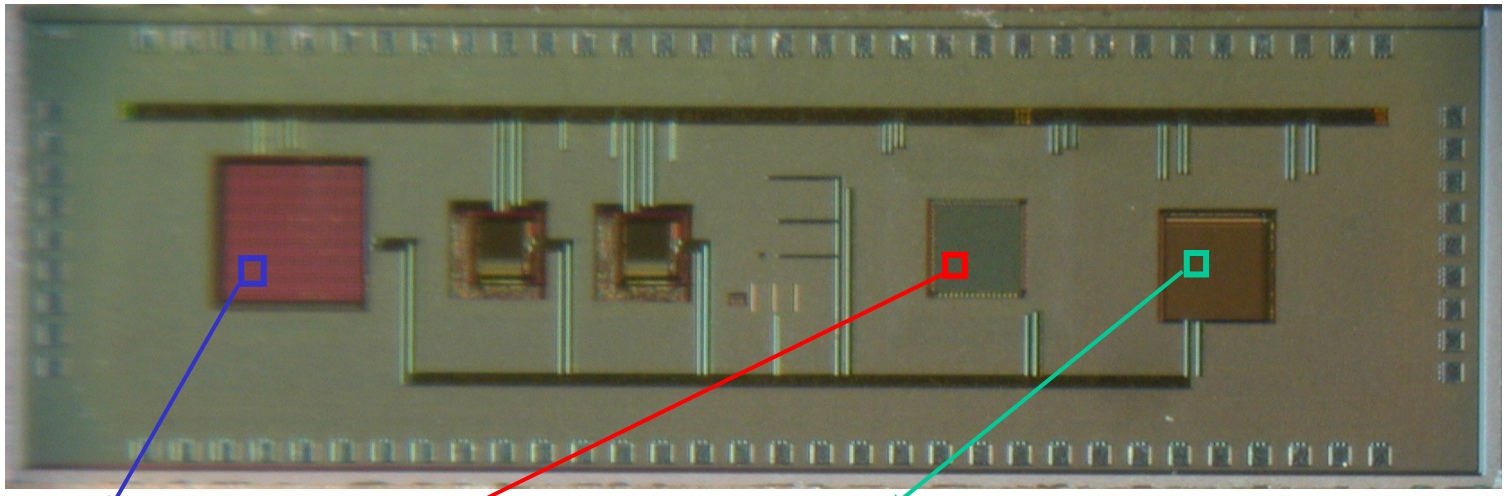
Test with ^{55}Fe



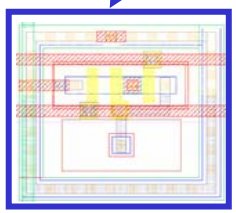
Digital readout is working fine

CMOS APS: RAPS/SHARPS Perugia

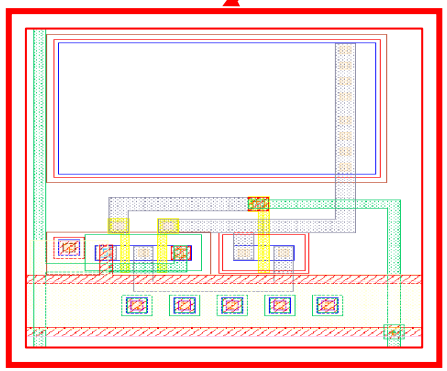
UMC 0.18μm MM 1P6M bulk CMOS technology (twin-tub, no-epi)



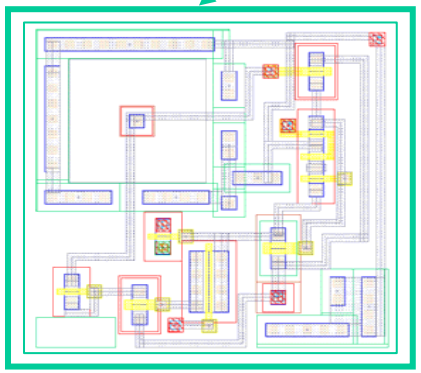
RAPS02



APS



WIPS



SHARPS

- 3T/... architecture (nMOS & pMOS);
- from 4x4μm² to 10x10μm² pixel size;
- sparse read-out;
- high-gain, in-pixel amplification;
- self-reset mode (event-triggered).

Explore more advanced technological solutions: Vertical Integration

- R&D proposal submitted to MUR (Oct. 2007):
  "Pixel systems for thin charged particle trackers based on high density microelectronic technologies"
  (Universities of Pisa, Pavia, Bergamo, Bologna)

The problem of thin pixel detectors is tackled from various sides:

  - "Develop a 128x128 DNW pixel matrix that can be used in an experiment (ILC or SuperB)"
  - "Develop a readout architecture allowing operation in high rate environments"
  - "Explore innovative cooling technologies where microchannels are integrated directly in the silicon substrate"
  - "Explore Vertical Integration Technology"

- Hopefully start R&D in summer 2008 (PRIN Project submitted, pending approval …)
- These technologies might not be ready when the SuperB construction starts but could be mature for an upgrade of Layer 0 (we need to design an interaction region with easier access & replacement).

Explore more advanced technological solutions: Vertical Integration

- R&D aiming at ASIC/pixel sensor interconnection for ILC (15-20 μm pitch) and Super B-Factory (50 μm pitch) vertex detectors with in-pixel data sparsification

- Overcome limitations typically associated to "conventional" and DNW CMOS MAPS:

  Fully depleted thick substrate, 100 % fill factor, better S/N vs power dissipation performance, pixel pitch, possible analog-to-digital interferences,...

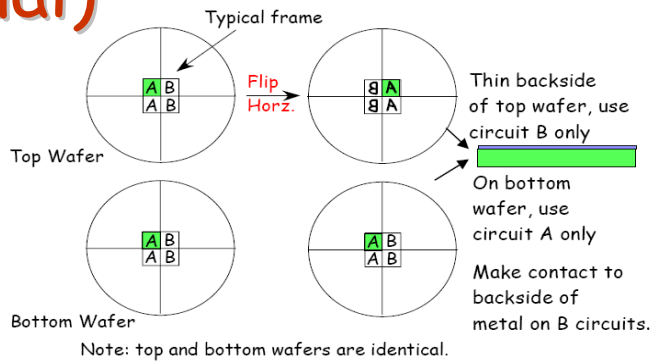
Ideas for Vertical Integration of Pixel Sensors

- Three possible implementations:
  - Vertical integration of a 130nm CMOS readout chip with a high resistivity fully-depleted pixel sensor
    100 μm total thickness
  - Vertical integration between two layers of 130nm CMOS chips.
    The first layer may include a MAPS device with analog readout, and the second layer the digital readout circuits
    (from an idea of Ray Yarema)
  - Vertical integration of multiple, thinned and stacked CMOS MAPS improve the spatial/angular ionizing particle trajectory resolution
    (Perugia group)

3D vertical integration based on DNW MAPS (conceptual)

Use vertical integration technology to interconnect two 130nm CMOS layers

(R. Yarema)

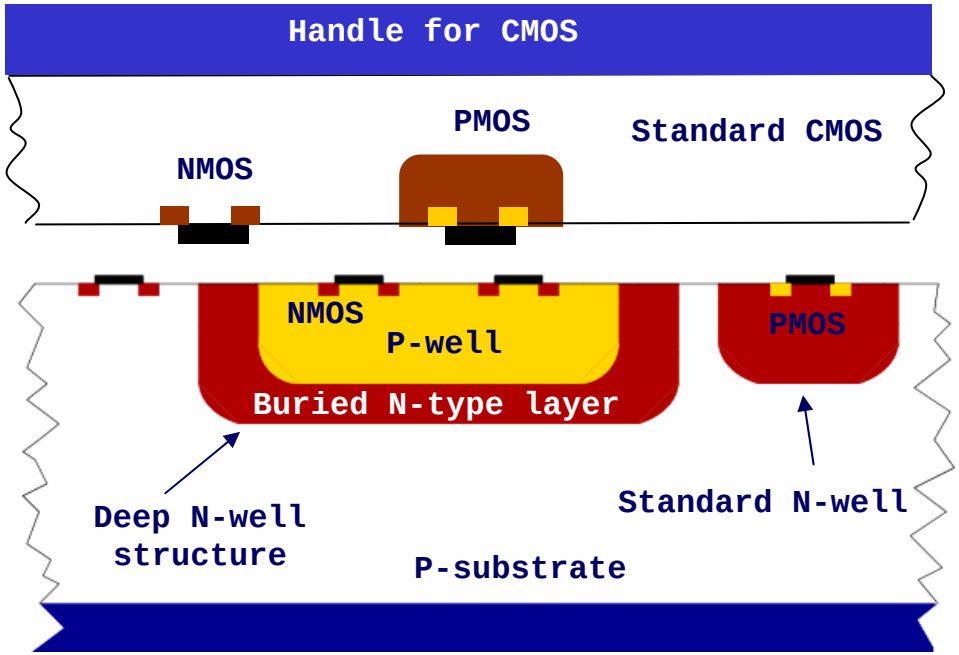


Face to Face Bonding

Mostly digital CMOS tier

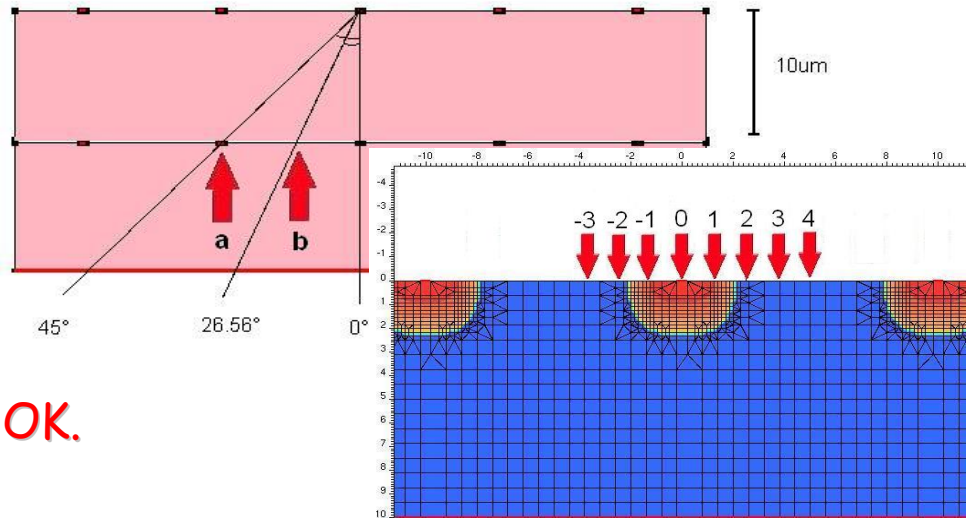
Tier interconnection and vias with industrial technique

Analog and sensor CMOS (mostly NMOS) tier



3D CMOS APS Perugia

- 3D approach to vertexing issues: adoption of multiple thinned, stacked, fully functional CMOS APS detectors.
- Aim:
  - to reduce the multiple scattering / material problems (especially in high magnetic field regions);
  - to improve the spatial/angular ionizing particle trajectory resolution.
- Proof of concept:
  - 2D device-level simulation;
  - spatial/angular resolution enhancement.
- Requirements:
  - Vertical alignment 1 micron;
  - pitch 10 microns;
  - tier depth 15/20 microns;
  - Through-Silicon Vias technology OK.



To sum up

- In Italy R&D activity on 3D vertical integration technology is presently in a conceptual stage
- Italian groups are looking to different ideas and technologies using vertical integration to improve the performance of CMOS MAPS
- In the DevDet FP7 project, Italian groups are taking part in the Task on 3D interconnection of microelectronics and semiconductor detectors