Development of thin pixel sensors and a novel interconnection technology for the ATLAS pixel upgrade at SLHC

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on behalf of

MPI Munich SLHC Upgrade Group

✓*Upgrade of the ATLAS pixel system at Super-LHC*

✓ *Properties of thin planar sensors*

✓ *New pixel module concept using the 3D integration approach developed by Fraunhofer-IZM*

Solid Liquid Inter Diffusion (SLID)

Inter Chip Vias (ICV)

✓*Production of metal dummies for SLID characterization and thin pixels sensors at MPI-HLL*

✓ *Studies of the effect of the SLID post-processing on detector properties*

The Challenge

Expected conditions at LHC and Super-LHC

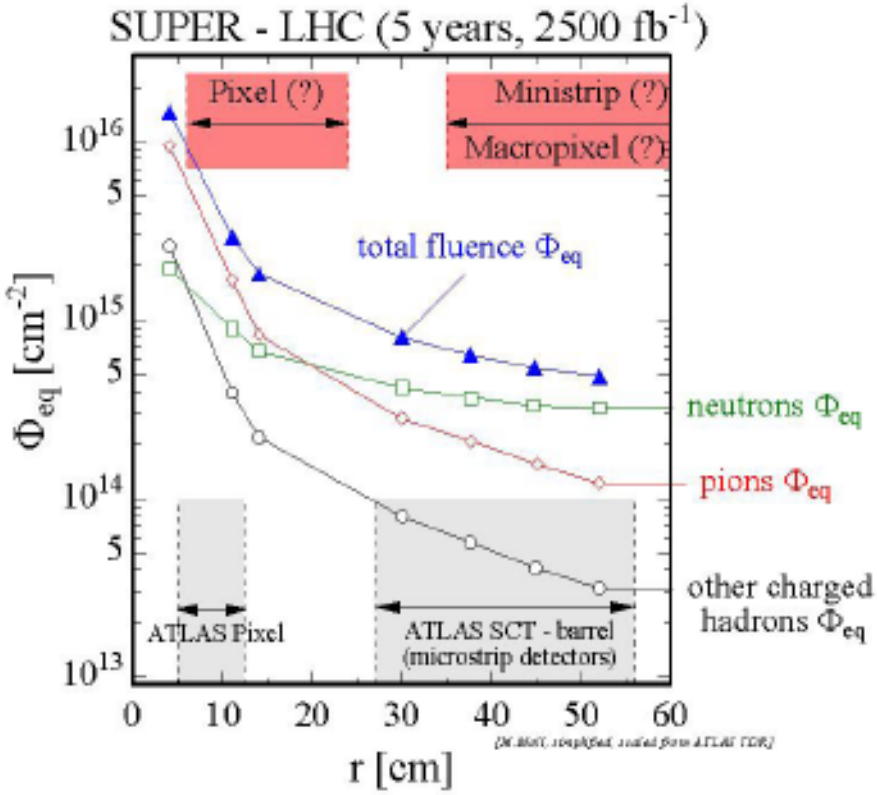
LHC:

- *Start 2008*
- *L = $10^{34}cm^{-2}s^{-1}$*
- *Integrated Luminosity: 500 fb^{-1} (10y)*
- *Φ= $3x10^{15}cm^{-2}$ 1 MeV eq. n at r=4cm*
- *Multiplicity: 0.5-1 k tracks / bunch cross.*

Super-LHC:

- *Start 2014-2018*
- *L = $10^{35}cm^{-2}s^{-1}$*
- *Integrated Luminosity: 2500 fb^{-1} (5y)*
- *Φ= $1.6x10^{16}cm^{-2}$ 1 MeV eq. n at r= 4cm*
- *Multiplicity: 5-10 k tracks/ bunch cross.*

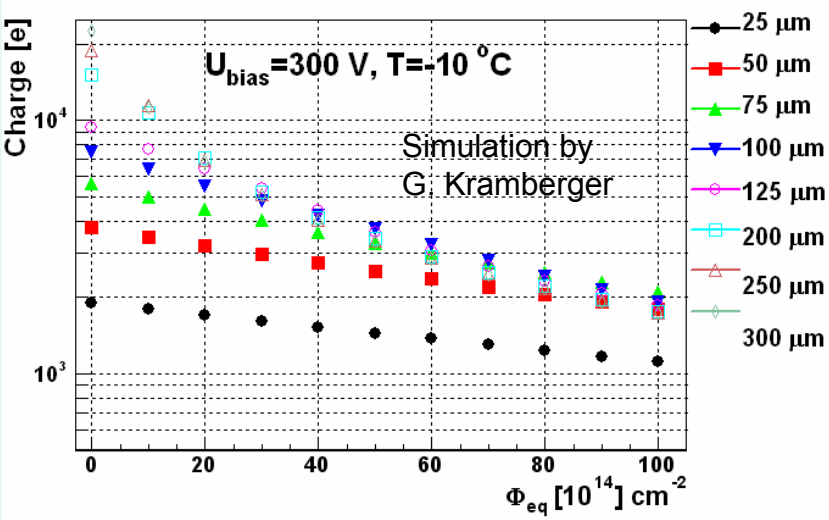
New detector concepts needed!



Thin planar pixel detectors for SLHC - Motivation

Two thicknesses in the on-going MPI production: 75 and 150 μm

- good radiation-hardness properties at SLHC fluences ($\Phi \sim 10^{16}$ n_{eq} cm^{-2})
- $V_{depl} \propto d^2$, $I_{leak} \propto$ Depleted Volume
- collection distance equalized among different thicknesses by trapping;



At the same voltage thin (=over depleted) detectors have a higher electric field than thick (= partially depleted) detectors in the area adjacent to the read-out electrode

- lower radiation length: 250 + 180 μm → 150 + 50 μm (sensor + chip)

0.46% X_0 → 0.21% X_0

n-on-n pixels: present and proven technology

n-on-p pixels: don't undergo type inversion and don't need double-side processing. They introduce some problems in the module design that must be addressed

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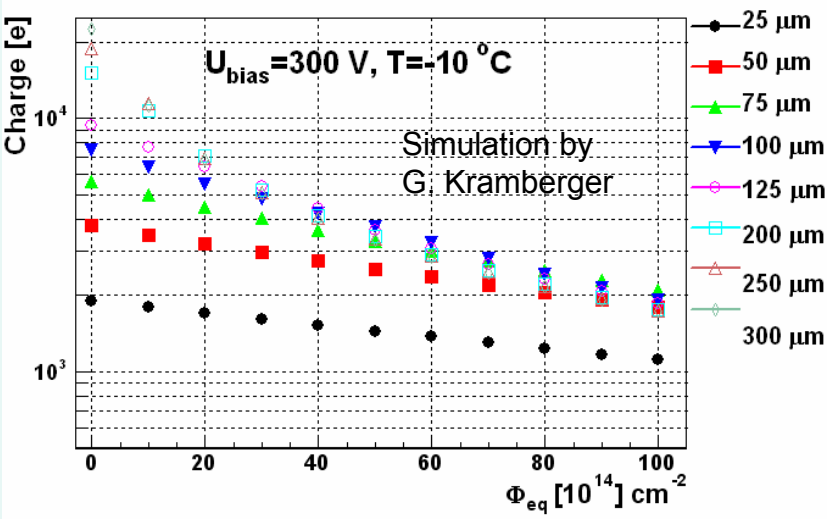

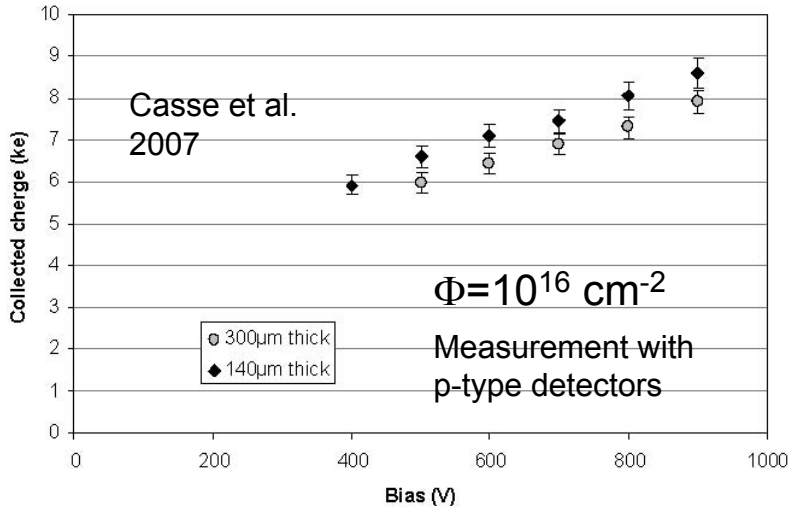

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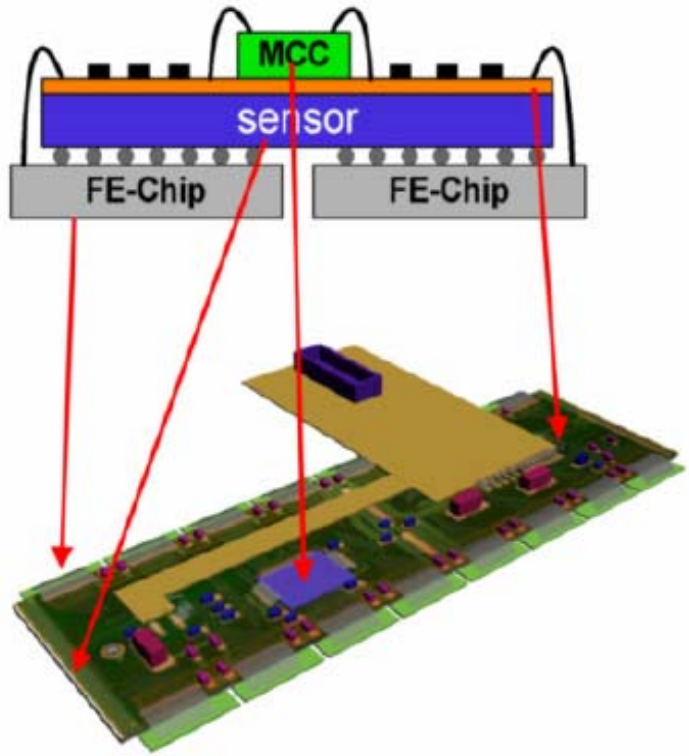
The ATLAS Pixel Detector

Present Layout:

-250 μm thick n-in-n pixel sensor
-50 x 400 μm^2 pixels
-0.25 μm rad hard ASIC
-rad hard till $\Phi=10^{15}$ n/cm^2



-Live fraction ~71%
-Cantilever for readout
-Large material overhead

New FE-I4 for B-layer upgrade

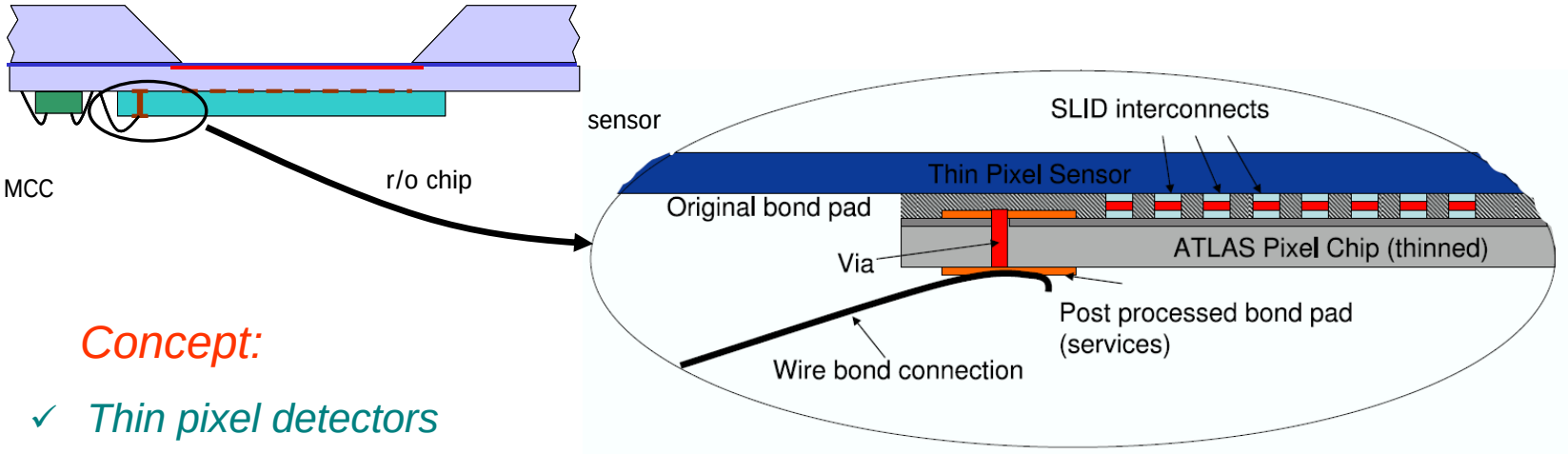
- 130 nm ASIC
- New pixel size 50 x 250 μm^2
-Target chip total size ~ 4 times FE-I3
- reduced amount of circuitry at the bottom of the chip to decrease the area of the cantilever
- Chip will be submitted around the end of 2008

MPI R&D for the Atlas Pixel Upgrade

MPI R&D aims to use 3D integration technology developed by Fraunhofer IZM (Munich) to develop a new module concept:

✓ *Thinned pixel sensors*	→ *Improved radiation hardness, reduced radiation length*
✓*SLID connection between thin pixel sensors and front-end (or different ASIC layers)*	→ *smaller pitches possible, depending on the pick and place precision,* → *allow the stacking of different ASIC layers (next bonding process does not affect previous SLID bond).*
✓*Stacked layers of electronics, for example digital read-out on top of the analogue layer*	→ *different technologies can be used and singularly optimized*
✓*Route signals through vias across the Si layers*	→ *avoid need of cantilever* → *four side buttable*

Demonstrator Module



Concept:

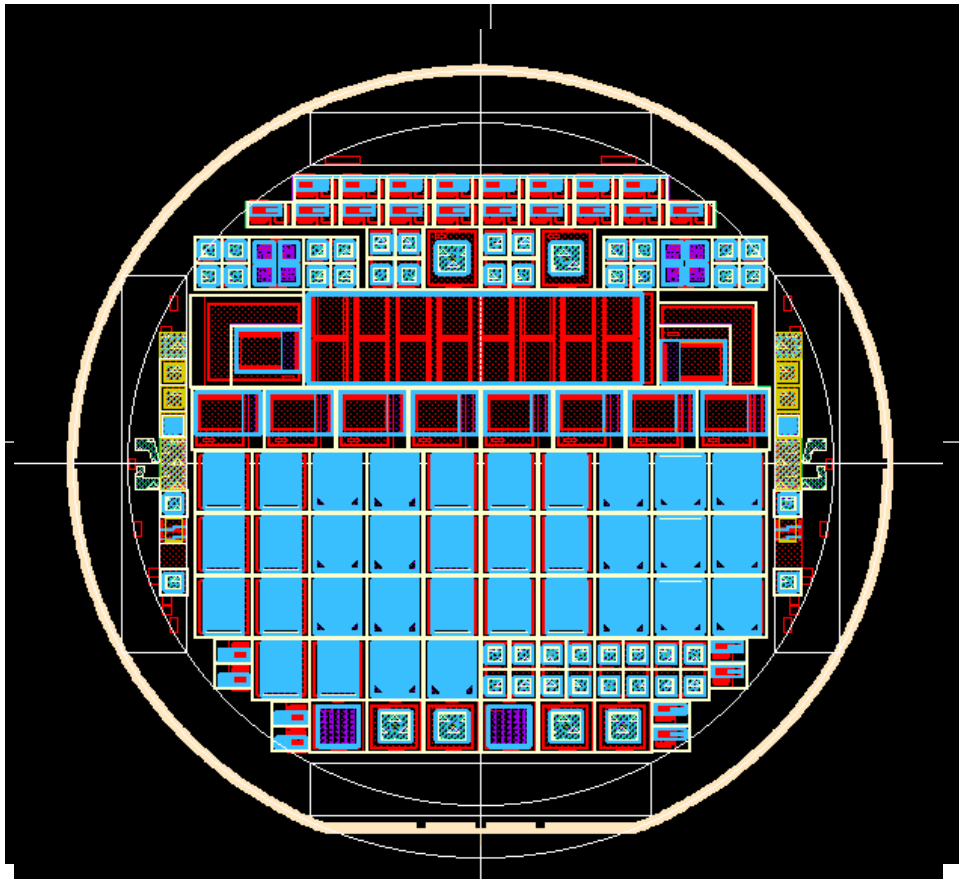
- ✓ *Thin pixel detectors*
- ✓ *SLID connection between pixel sensors and ASIC (FE-I2), placed face to face → "chip to wafer" technique with the ASIC mounted on a handle-wafer*
- ✓ *Thinning of the readout chip wafer down to 50 μm*
- ✓ *drilling of vias to route signal and services out from the ASIC wafer backside*

Status:

- ✓ *Production of thin pixel sensors: already implanted in the backside, thinned, topside process is on-going*
- ✓ *ASIC wafers tested in Bonn to produce "good dies" map*
- ✓ *Optimization of the present Atlas pixel read-out system to cope with smaller signals*

Pixel wafer design

6” wafer

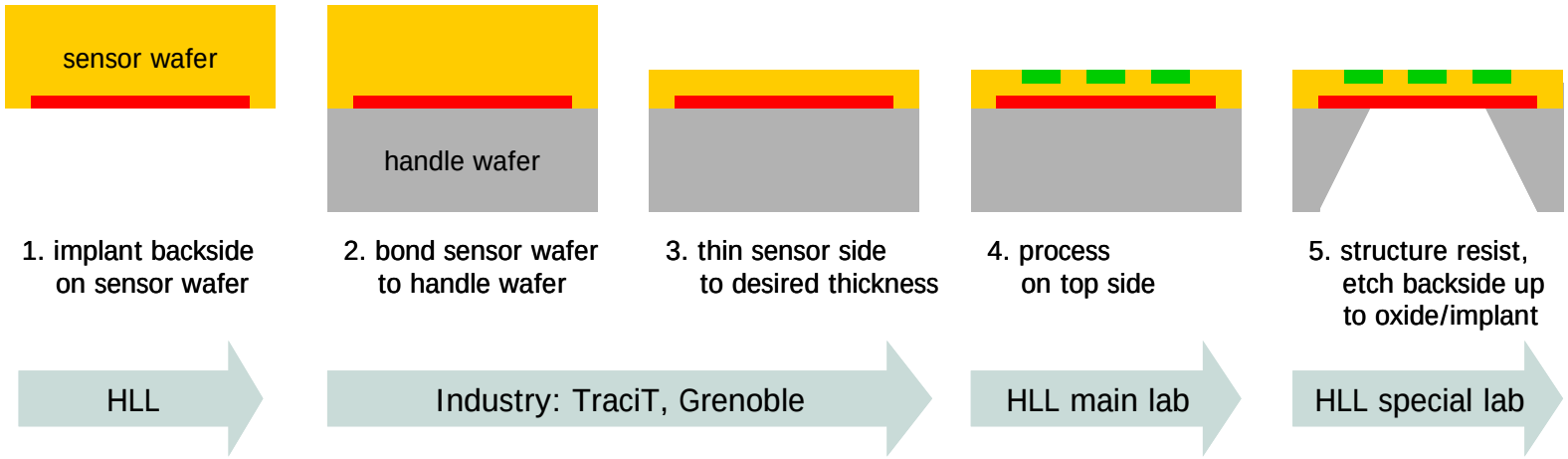


- 42 cells 10.5 x 11.9 mm^2
  10 different micro-strips versions + test-structures
- 12 diode cells
  10.0 x 10.0 mm^2
- 8 pixel cells – ATLAS geometry to be read out by a single FE chip – designed for SLID interconnection
- ATLAS module, to be connected to the FE with bump-bonding
- Pixel cells to be read out by a FE chip by INTERON (Norway)

- *Pixels follow ATLAS layout, 160 x 18 pixel 50 x 400 μm^2 for FEI-2 chip*
- *10 x 10 pixel arrays with smaller pitch (50x200, 100, 50) for special simple readout chip*
- *Ministrips to be read by ATLAS SCT128 chip*

Thinning Technology

✓ *Handle wafer of the same material as the top wafer, n- or p-type Fz*



✓*Deep anisotropic wet etching leaves rough surfaces → the process has been optimized to open the contacts and apply the metallization after etching of the handle wafer.*

✓ *Thin (50 μm) silicon already successfully produced at MPI.:*

- *MOS diodes.*
- *Small strip detectors.*
- *Mechanical dummies.*

-No deterioration of detector properties, keep I_{leak} *<100pA/cm*^{2}

Processing of the SOI wafers

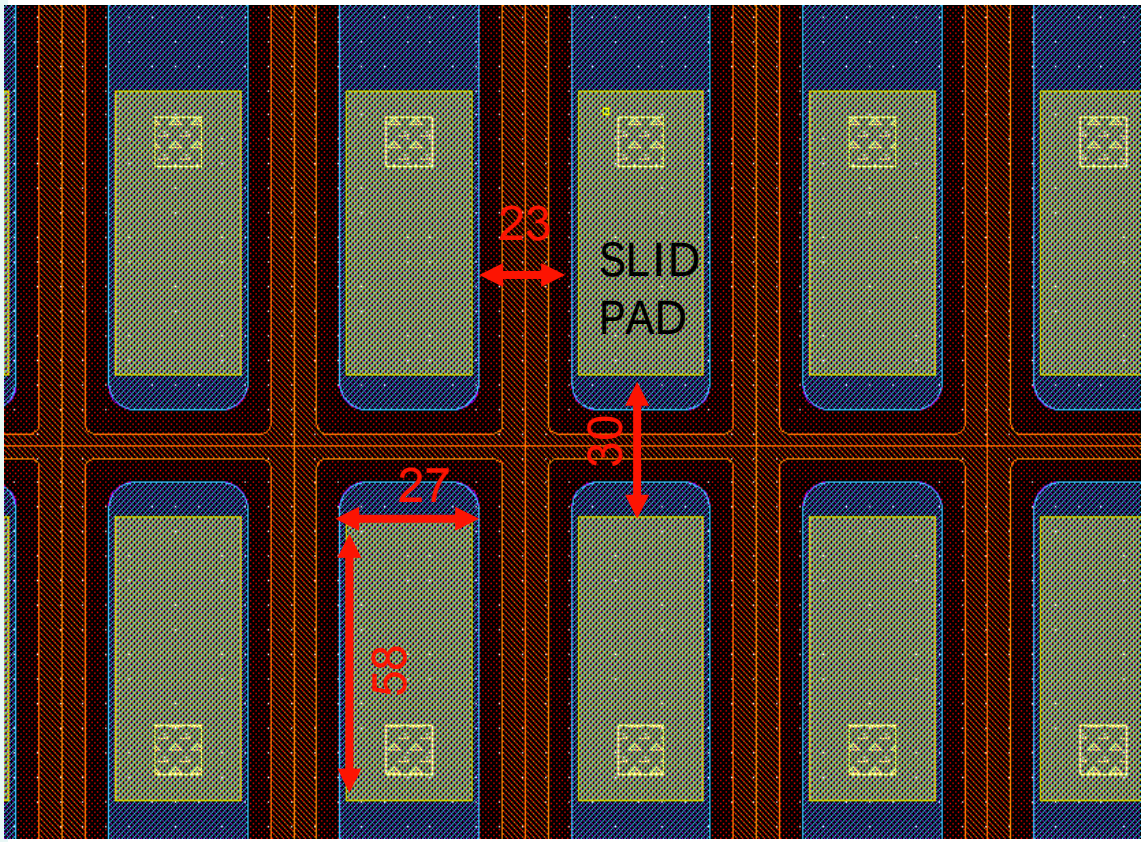
SOI wafer (Tracit/Soitec): 6” (backside processed, bonded, thinned and delivered)

Nr	Type	thickness	P-spray	Planned use
1	N	75	high	Irrad
2	N	75	high	SLID/irrad
3	N	75	high	SLID/irrad
4	N	75	high	SLID/irrad
5	P	75	Low	Irrad
6	P	75	Low	SLID/irrad
7	P	75	High	Irrad
8	P	75	High	SLID/irrad
9	P	150	Low	SLID/irrad
10	P	150	Low	Bump/irrad
11	P	150	High	Irrad
12	p	150	High	Bump/irrad

Irrad: can be used immediately for irradiations
SLID/irrad: first processed for interconnection, irradiation later
Bump/irrad: first processed for bump bonding, irradiation later

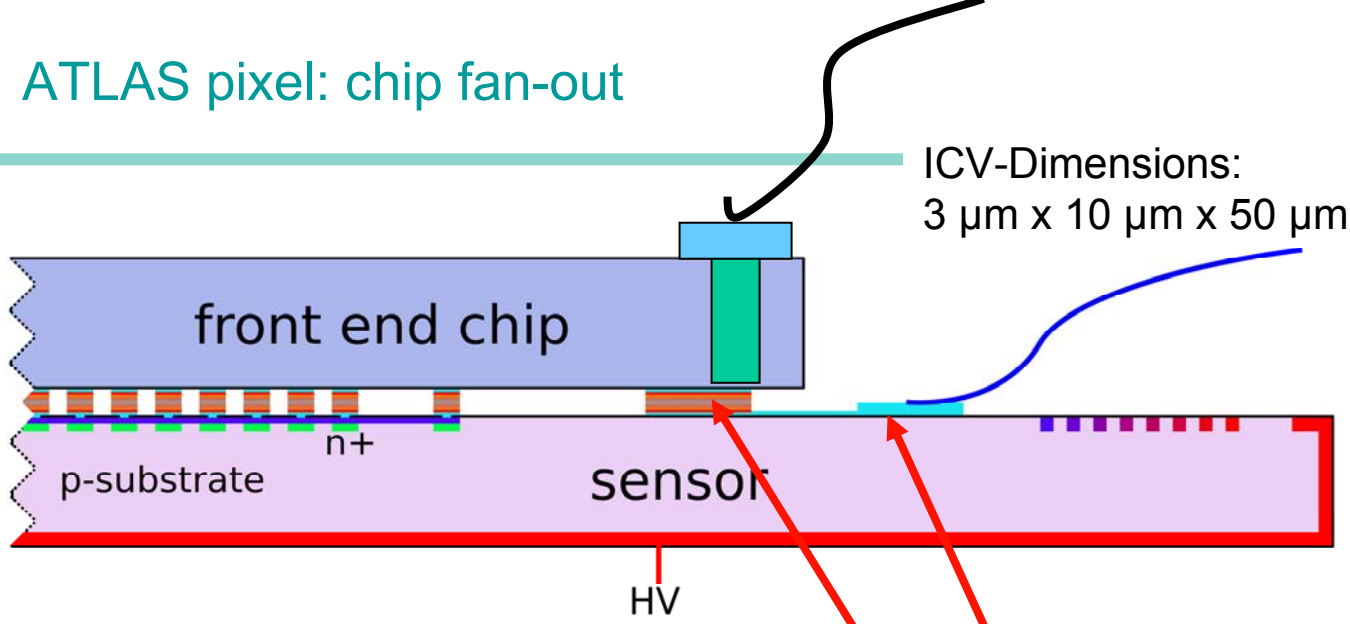
ATLAS pixels: active area

- *Pixel cells to be read out by a single FE chip*
- *The active area is unchanged with respect to the standard design of the Atlas pixels: DC coupled pixels, isolation achieved through moderated p-spray, punch-through biasing*
- *Added a guard-ring structure on the front side needed in the case of the n-in-p detectors*



- *width and distance between the SLID pads along the x-axis most critical parameter for the interconnection → IZM specs for SLID "chip to wafer" require slightly larger spacing to allow for possible misalignment of the chip in the handle wafer*

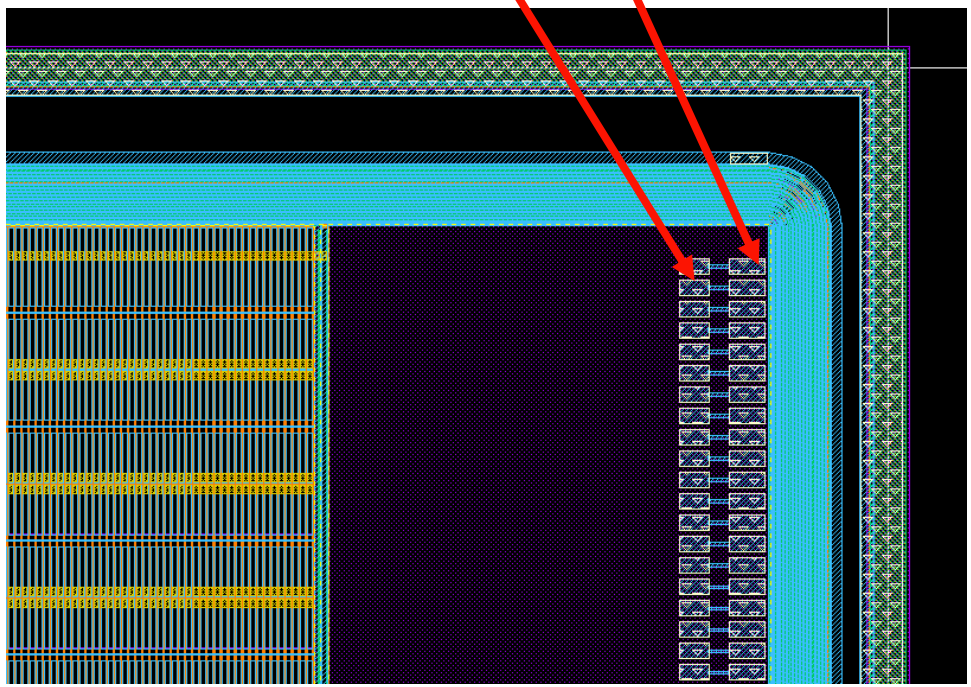
ATLAS pixel: chip fan-out



- *n-in-n: sensor edge at ground*
- *n-in-p: sensor edge at HV*
- *service area within guard ring: in future productions the GR extension can be avoided if BCB isolation is proved to stand the potential difference between detector and chip surfaces*

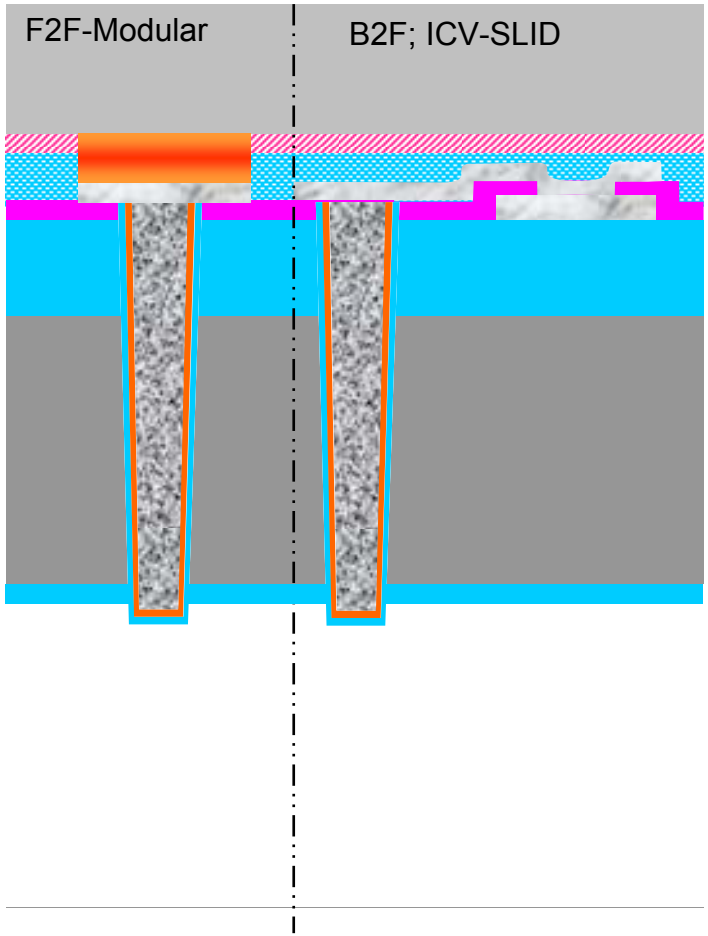
Chip can be serviced:

-using ICV (vias)
-fan-out (redundant)



Process steps for ICV-SLID at IZM

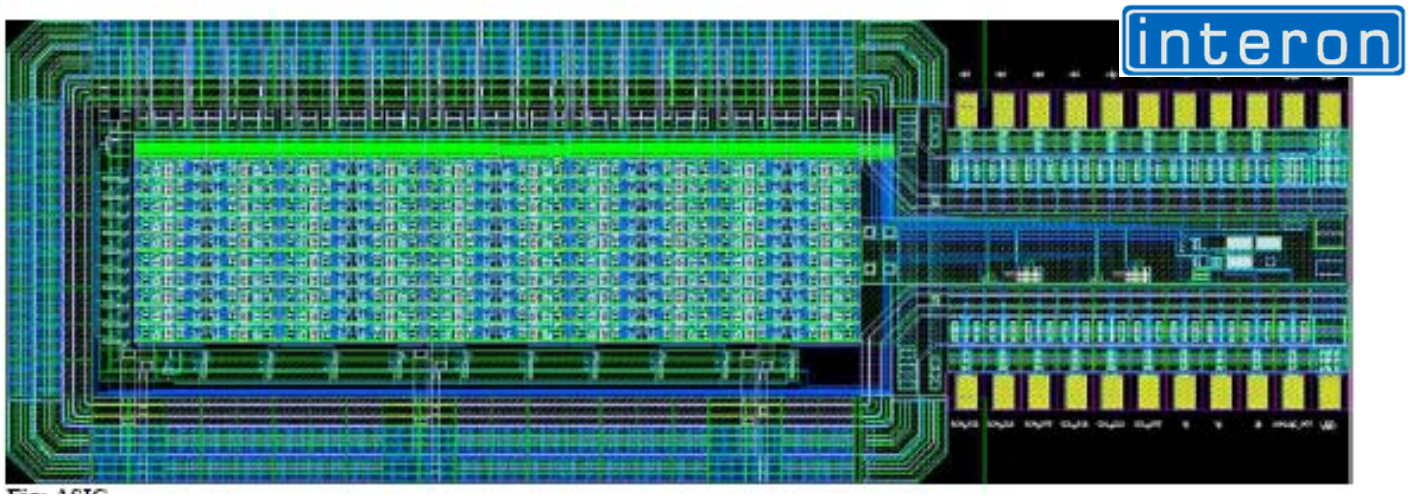
Fraunhofer Institut Zuverlässigkeit und Mikrointegration



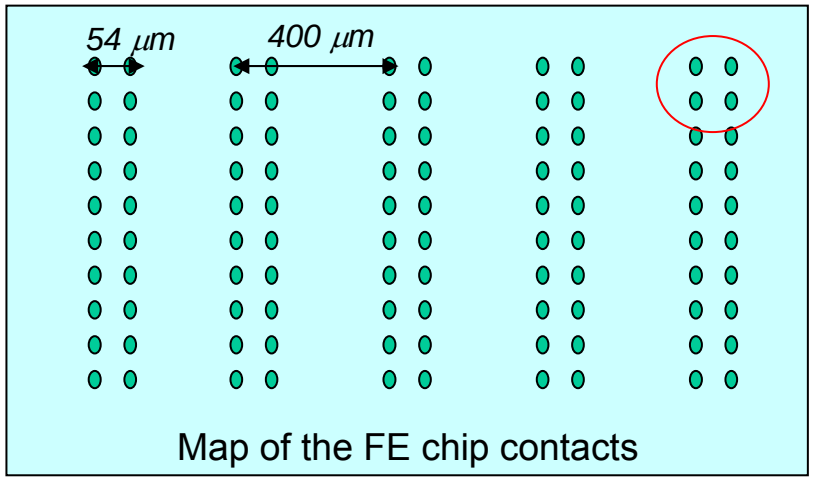
- *Atlas pixels and FE will be interconnected F2F*
- *Fabrication of Tungsten-filled InterChip Vias on chip → Via Opening and Metallization from front side*
  - *Chip are diced and placed on a Handling wafer needed for the SLID interconnection. SLID performed between detector wafer and chips. Handling wafer is removed.*
  - *Thinning the ASIC to 50 μm & Backside Metallization.*

Special Test Chip from Interon (Oslo)

- *Test chip for small pixel array: 10 x 10 pixels*
- *Preamp, Shaper followed by Simple track/hold & multiplexing*
- *Pitch: 50 x 200 μm^2 (can be used with 50 x 50 μm^2 and 50x100 μm^2 pixels skipping intermediate pixels)*
- *Noise: < 200 e^- at 50 ns shaping and 1 mW power/pixel*
- *Prepared for SLID and ICV (wire bond pads **AND** pixel pads)*
- *AMS 0.35 μm CMOS*
- *Already produced and ready for testing (Oslo University)*



Pixel arrays to be read by the Interon chip

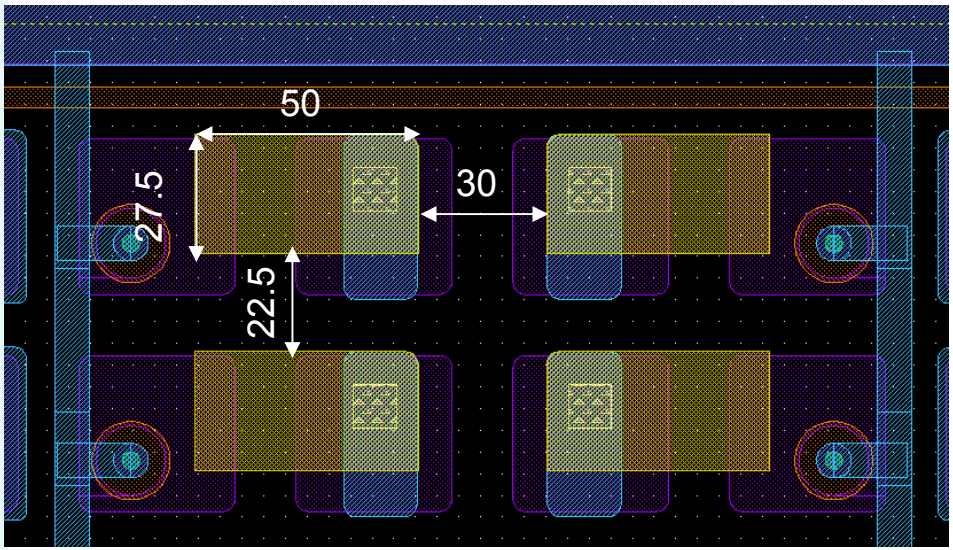


Four pixel arrays with same external size but different segmentation:

- *50 x 50 μm^2*
- *50 x 100 μm^2*
- *50 x 200 μm^2*
- *50 x 400 μm^2*

As for the ATLAS pixel structure:

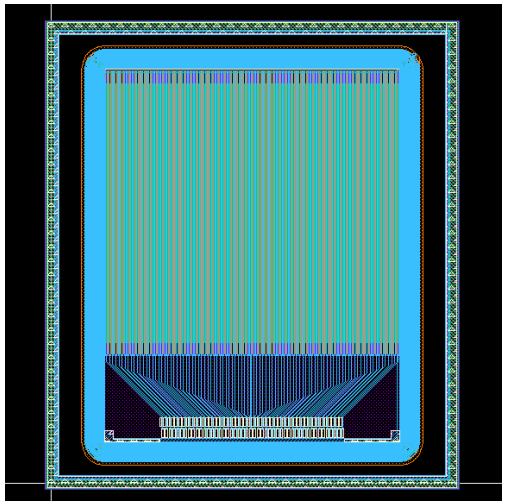
- *Guard Ring encloses the fan-out structure*
- *Alternative solutions to read out the chip: wire bonding pads, via from the chip pads*



50 x 50 μm pixel array

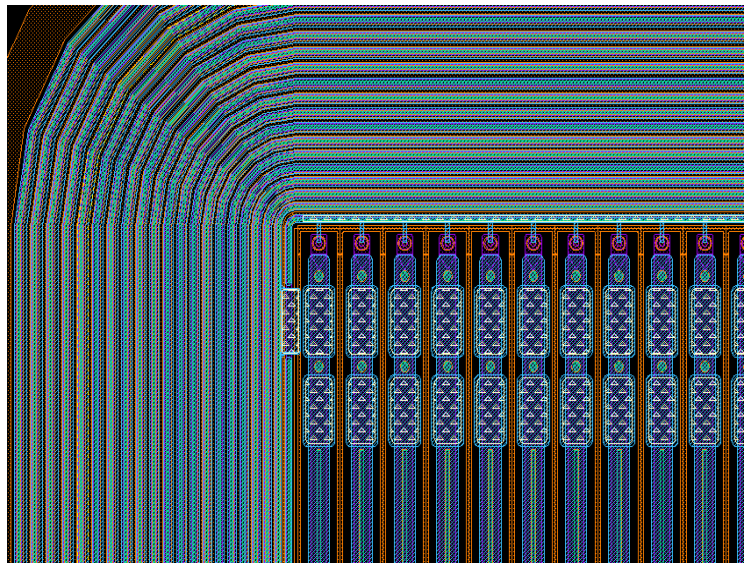
- *Most challenging geometry to accommodate the SLID pads*
- *Only a subset of pixels are attached to the FE chip → the SLID pads could be enlarged beyond the cell boundaries*

Micro-strip devices for isolation studies



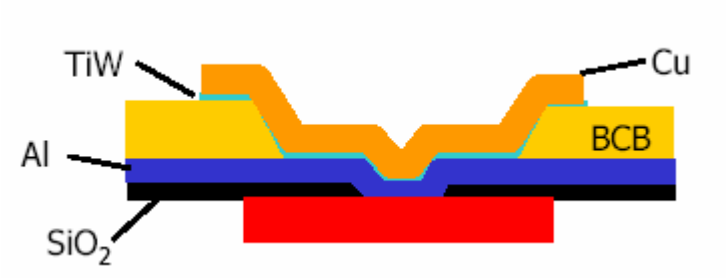
- *The micro-strip devices will be read out by ATLAS SCT 128 chip.*
- *An optimization of the strip and pixel isolation technique is needed, especially for p-type detectors.*
- *The micro-strip detectors represent an easy tool to investigate strip (pixel) isolation and inter-strip (inter-pixel) capacitance as a function of the pitch, the implantation width and the p-spray method.*

Nr	Strip pitch	N+ impl. width	P-spray
1	50	30	10
2	50	30	No mod.
3	80	30	10
4	80	30	No mod.
5	50	24	10
6	50	30	6
7	50	36	6
8	80	20	No mod.
9	80	20	24
10	80	30	24



Ancillary productions at MPI-HLL (I)

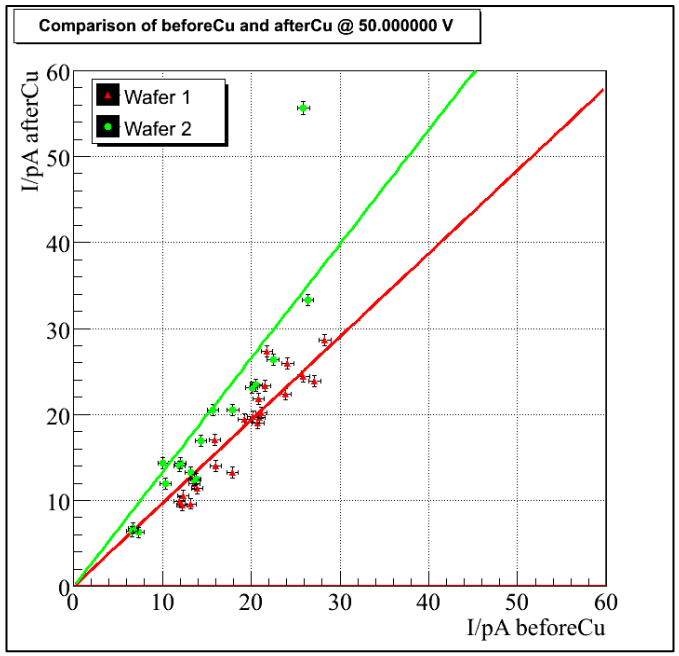
1) *Diodes processed on SOI wafers to investigate how post-processing influences sensor characteristics*



Metal system added at IZM → simulation of SLID process without a real soldering of the two wafers :

Wafer 1: TiW sputtering + Cu through mask electroplated + SLID temperature treatment

Wafer 2: TiW sputtering + Cu and Sn through mask electroplated + SLID temperature treatment



Correlation of the reverse current at full depletion (50 V) before and after Cu metallization

→ No significant effect noticeable, both before and after the temperature treatment

Ancillary productions at MPI-HLL (II)

2) Test of “chip on wafer” SLID interconnection with metal dummies.

Status: production started

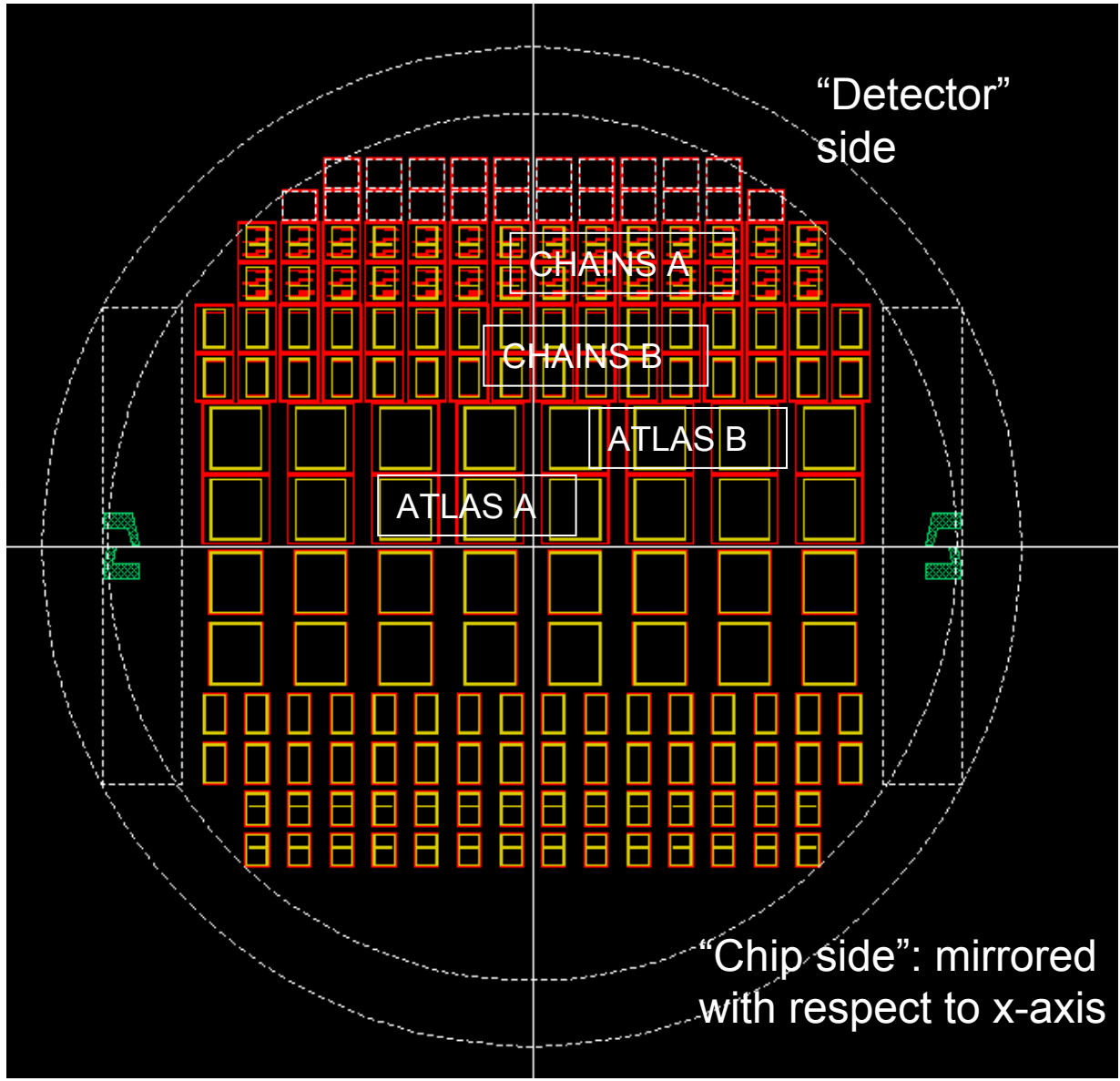
- *Aim: determine the feasibility of the SLID inter-connection within the parameters we need for the ATLAS pixels.*
- *Test of the mechanical strength as a function of different area coverage by the SLID pads*
- *Test the SLID efficiency varying the dimensions of the SLID pads*
- *Study the SLID efficiency when degrading the planarity of the structure underneath the pads*
- *Determine the alignment precision between single “chip” and “detector” wafer*
- *Investigate the BCB isolation capability between the detector and chip surfaces*

Basic test device: chain arrays

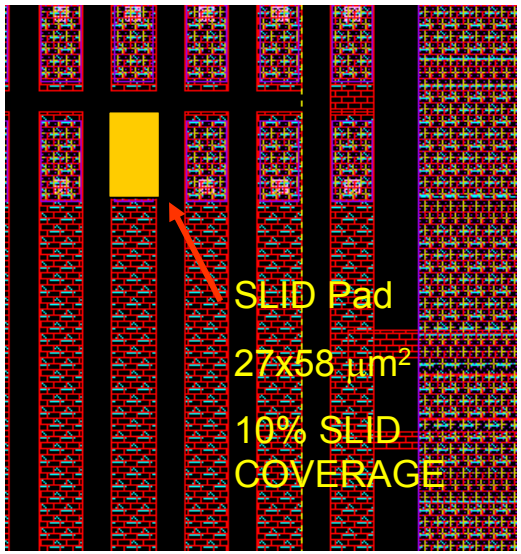
Design of the of 6” wafer with metal dummies

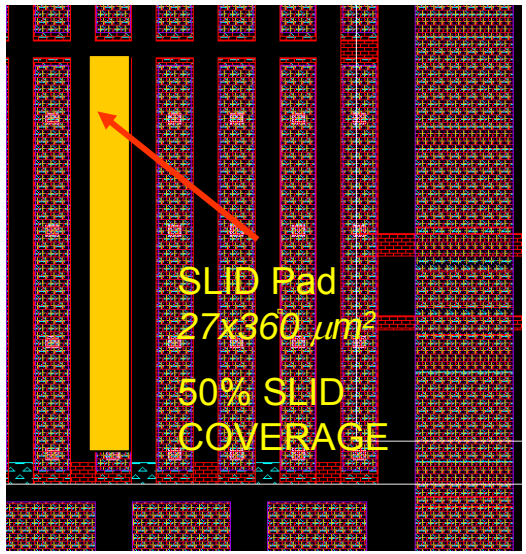
Single mask for the detector and chip wafers

- *The “detector” structures are on the top half of the wafer*
- *The “chip” structures to be cut and be placed on the handle wafer on the bottom half of the wafer*
- *Post-processing on full wafers: every single wafer fully dedicated either to “detector” or to “chip” production*
- *Process in HLL up to BCB deposition and contact opening*
- *Preparation for SLID, cutting of the “chip” structures, SLID interconnection at IZM*

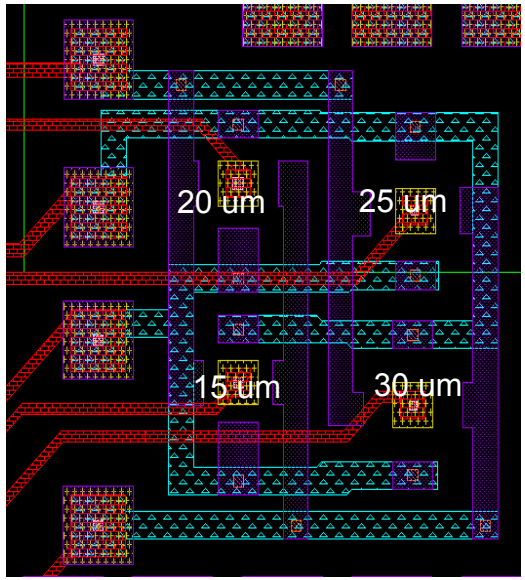


Test structures - ATLAS pixel geometry





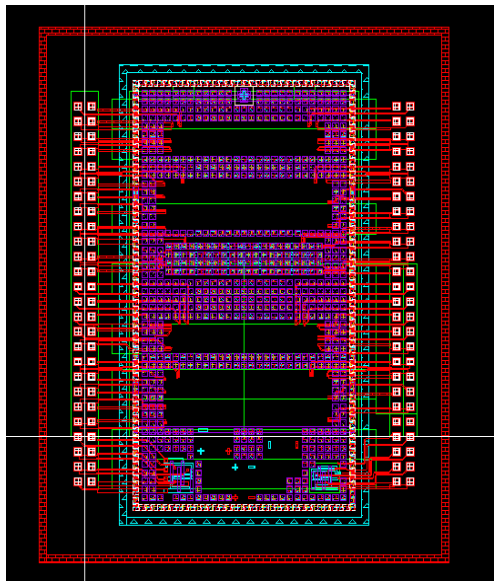
Chains with ATLAS pixel geometry: test SLID efficiency with ATLAS pixel parameters and mechanical stability with different area coverages



Structures to measure the alignment precision of the "chips" with respect to the detector wafer

- *The alignment precision of the chips with respect to the detector wafer can vary due to the possible displacement of the single chips in the handle wafer.*
- *In each device three different structures allow to measure the direction and the value of the misalignment in the range from 2 to 30 μm*

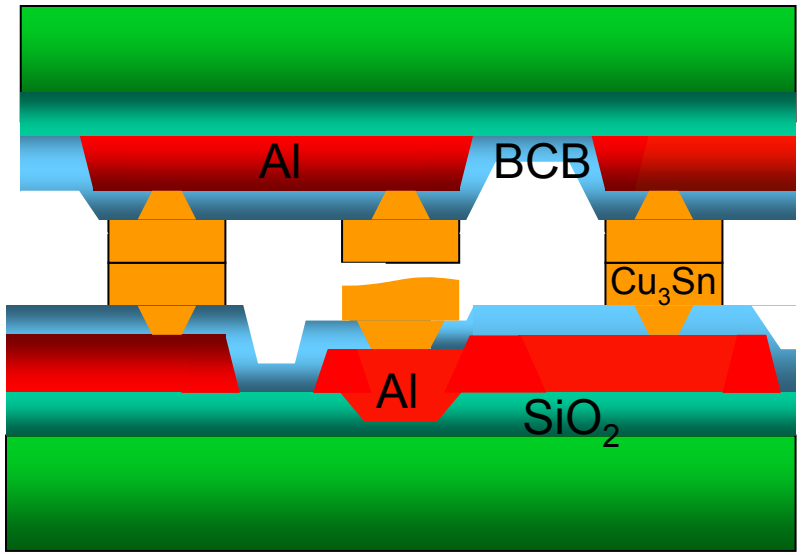
Test structures - Chains with different SLID pads parameters



Set of chains with different SLID pad sizes, pitches

- *W_{pad}= 30, 40, 50, 80 μm*
- *Distance between pads = 20, 30, 35 μm*
- *Aim: test feasibility of the interconnection down to the minimum SLID dimensions implemented in the production wafer*

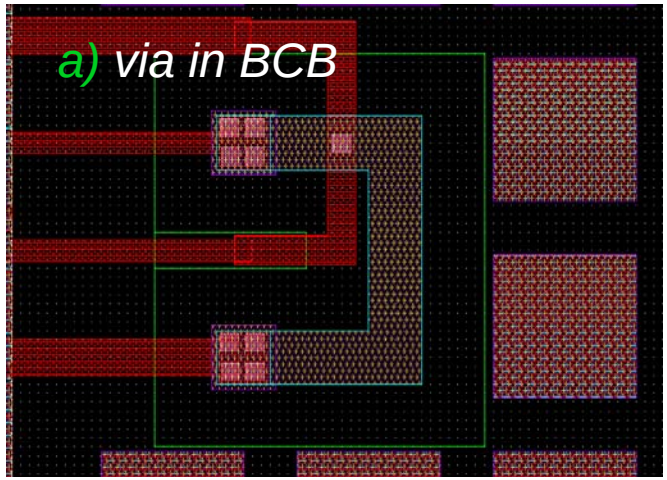
… and variations on the planarity of the layers beneath the SLID pads

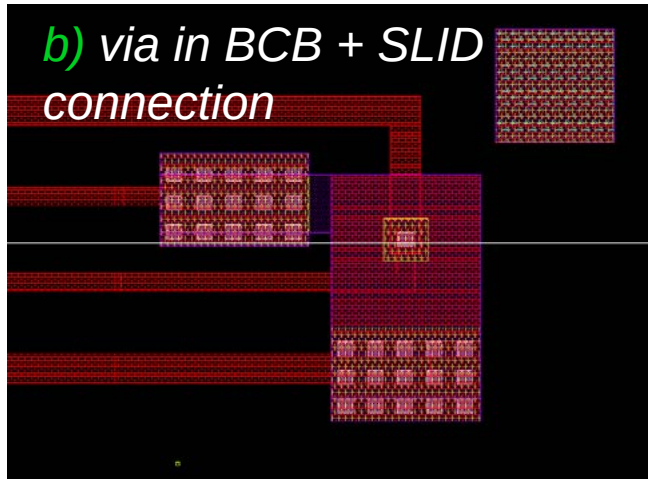


- *etch in the oxide underneath every second pad (~ 100 nm) on the detector side.*
- *The corresponding pad (Al+BCB+SLID metal system) sits at a lower height with respect to the neighbouring ones → possible SLID inefficiencies*

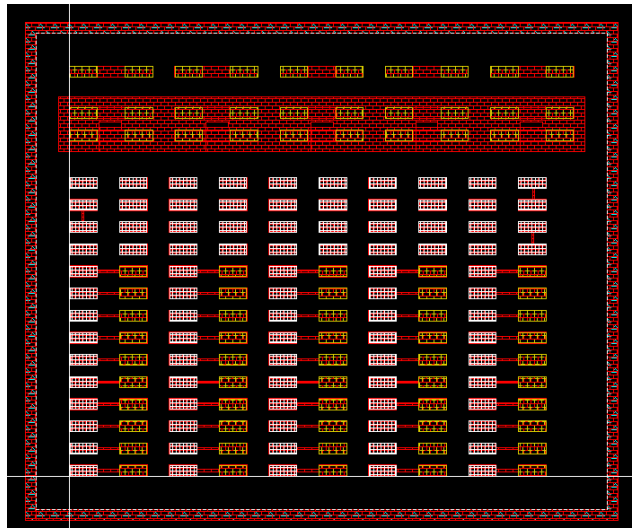
Test structures - Kelvin structures and BCB isolation

Kelvin structures to measure with the four probe method the resistivity of:





Test structures (on detector wafer only) to measure the capabilities of the BCB layer in terms of electrical isolation.



Conclusions and Outlook

On-going R&D program at MPI for the upgrade of the ATLAS pixel system in view of SLHC:

✓*Two parallel productions: thin pixel detectors designed for 3D integration and metal dummies for SLID studies are being processed*

✓ *Measurements results on diodes with SLID metal system showed no influence of the post-processing on the sensor characteristics*

Outlook:

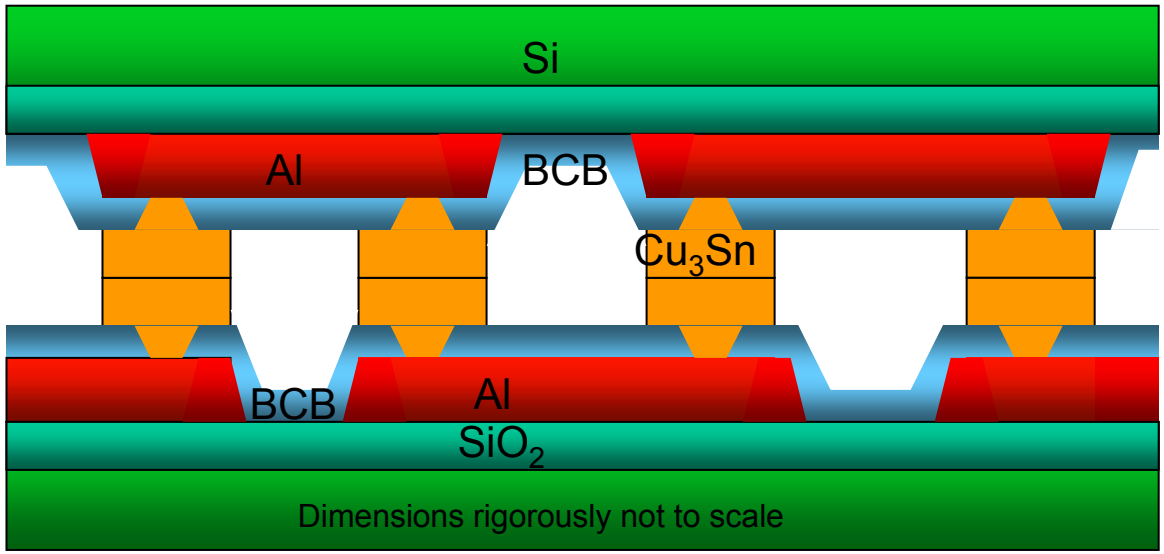
✓ *Production of a demonstrator module in 2008-2009 as proof of principle for:*
- *thin planar pixel sensors*
- *SLID interconnections*
- *Inter Chip Vias*

✓ *Collaboration started with the IN2P3 R&D on 3D integration:*

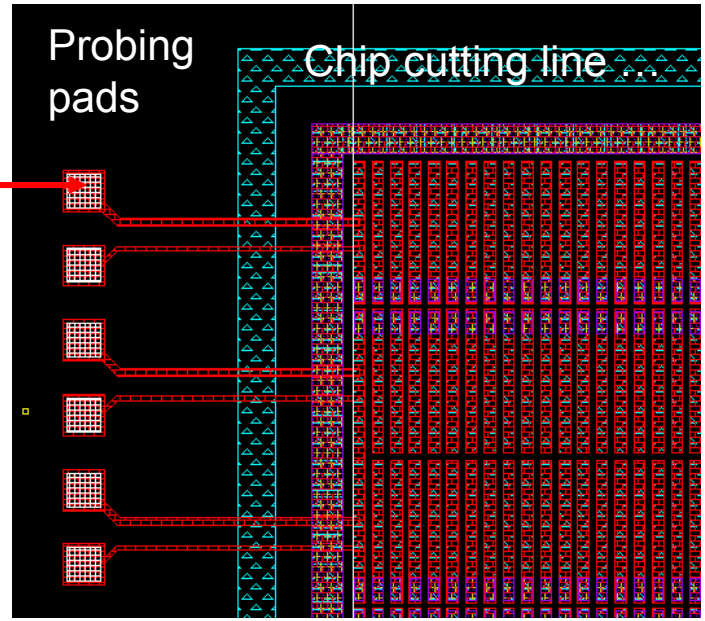
✓ *Future production of pixels with a geometry suited for FE-I4 and/or 3D versions of FE-I4*

Schematic cross-section of a chain array

- *The SLID pads are connected to their neighbors trough the Al layer alternatively on the bottom and on the top side*



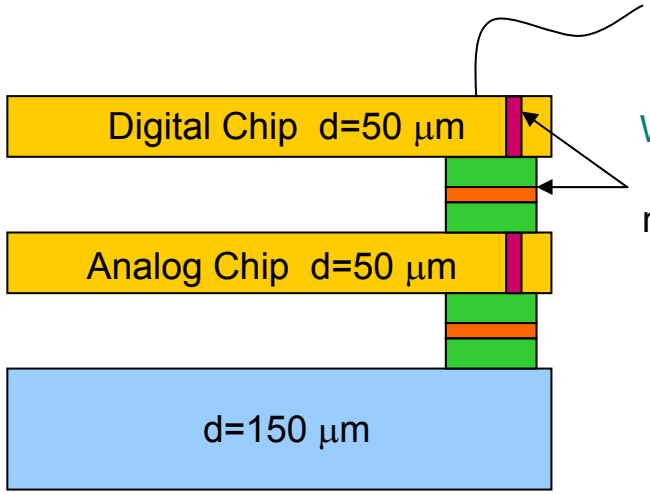
to the probing pads on the detector side



- *The electrical continuity of the chain can be tested contacting the probing pads on the detector side at the beginning and the end of the chain*

Radiation length – SLID + ICV

	Total thickeness	Area	Length/ X_0	Area weighted L/X_0
Silicon (sensor + 2 chips)	**150+50+50**	**50x125 (100%)**	**0.27%**	**0.27%**
Copper (SLID pads)	**5x4**	**27x27 (11.7 %)**	**0.14%**	**0.02%**
W (filling of VIAS)	**50x2**	**3x10 (0.5%)**	**2.86%**	**0.015%**



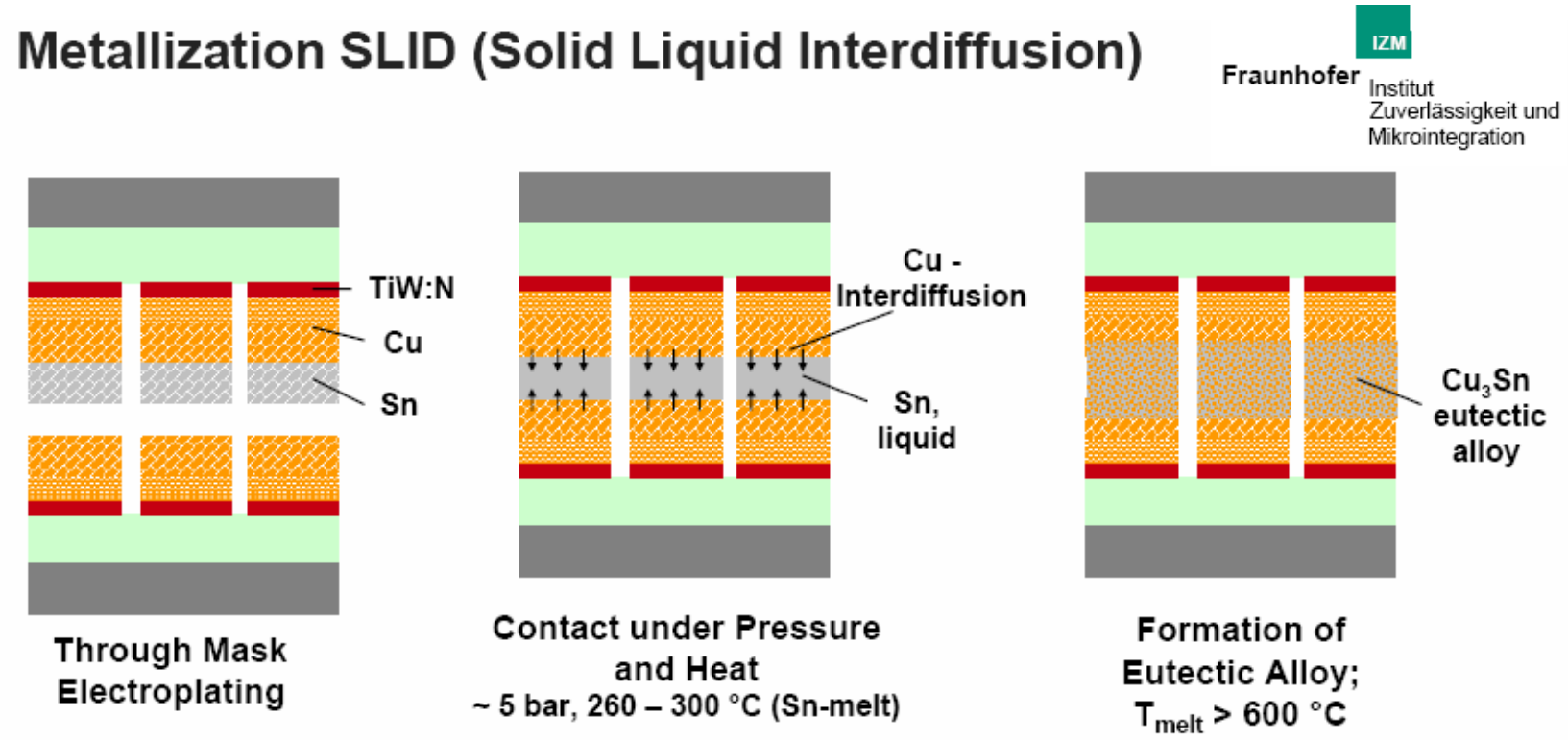
Worst case: probably a SLID connection + via is not needed between analog and digital layer for each pixel

Pixel with area 50x125 μm^2

Possible 3D FE-I4 version

X_0
Si: 9.36cm,
W: 0.35cm,
Cu: 1.43 cm,
Sn: 1.21 cm

IZM SLID Process



- *Alternative to bump bonding (less process steps "potentially lower cost" (IZM)).*
- *Small pitch possible (< 20 μm, depending on pick & place precision).*
- *Stacking possible (next bonding process does not affect previous bond).*
- *Wafer to wafer and chip to wafer possible.*