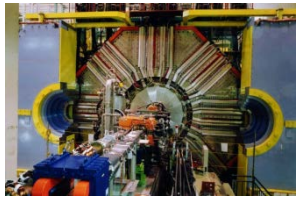
The MPI Semiconductor Laboratory

Projects - Devices - Technology

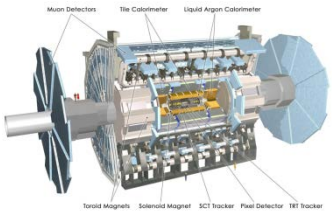
BepiColombo, eRosita

MAGIC, CTA

XFEL, FLASH, LCLS



Belle II



ATLAS

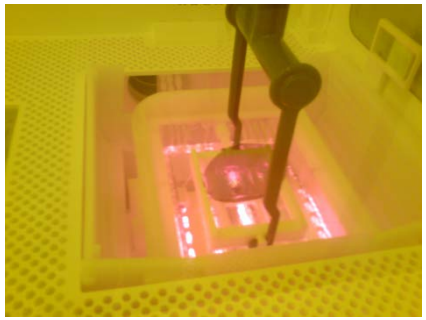
***The MPP HLL Team**:*
L. Andricek, Z. Albrechtskirchinger, G.Fuchs, C. Jendrysik, C. Koffmane, G.Liemann, H.-G.Moser, P. Müller, J. Ninkovic, A.Plis, R.Richter, A. Ritter, A.Ritter, F. Müller, S. Petrovics, M. Schnecke, A.Wassatsch, M.Tesar

***from ATLAS/SCT**:*
M. Beimforde, A.Macchiolo, M. Ellenburg, R.Nisius, S.Terzo, P.Weigell

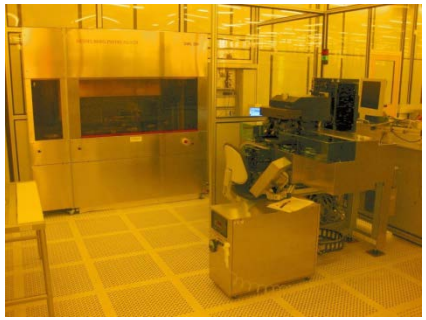
& many colleagues from MPE and PNS

Inside HLL – Sensor Development and Fabrication

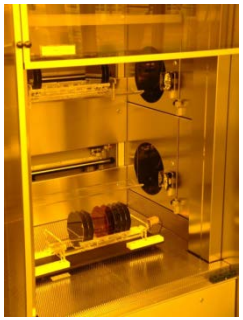
cleaning



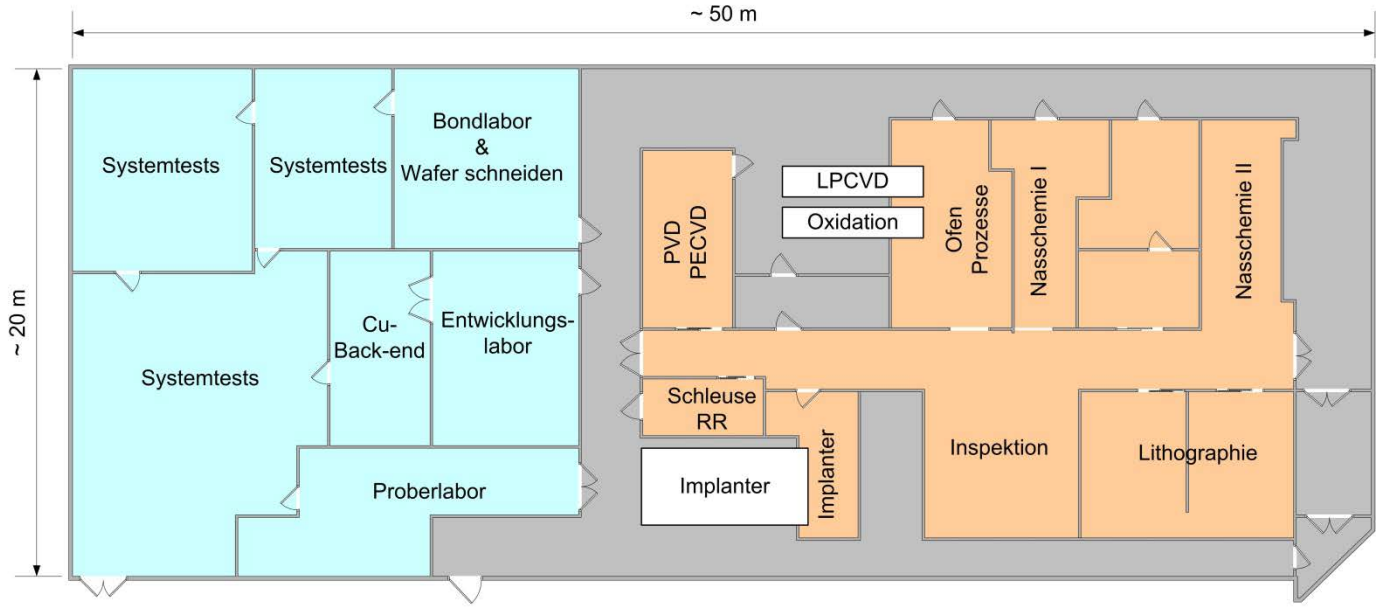
lithography



thermal



inspection



plasma and sputter

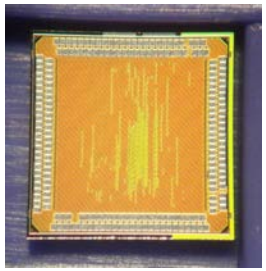
Cu and flip chip

MPI HLL is the only lab worldwide doing fully depleted silicon radiation sensors with integrated electronics

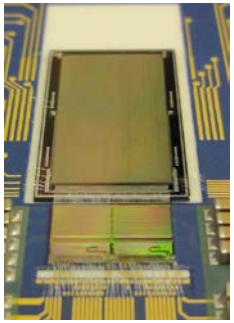
Inside HLL – ASIC and System Design&Test

ASIC	Filter	Filter architecture	pnCCD	DEPFET Source follower	DEPFET Drain r/o
VELA[1]	Trapezoidal	unipolar, single-ended, two stages			✓
ASTEROID[1]	Trapezoidal	unipolar, single-ended, two stages		✓	
VERITAS 1.0	Trapezoidal	unipolar, single-ended, two stages	✓	✓	
VERITAS 2.0	Trapezoidal	bipolar, fully differential, single stage	✓	✓	✓
DCE3	Data Clustering Engine, digital chip, TSMC 65nm, novel real time clustering → Belle II System				

[1] *In collaboration with Politecnico di Milano*



DCE3



pnCCD with Veritas read-out

at HLL:

- sensor design and fabrication
- r/o ASIC development
- interconnection
- system/camera design and test

HLL inside – (simplified) project overview

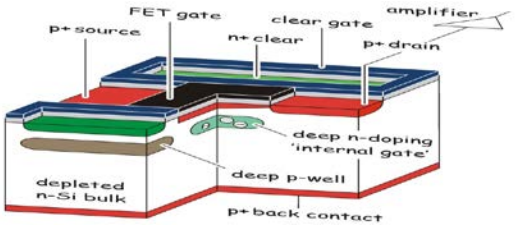
	Passive Pixels	Active Pixels DEPFETs	pnCCD	SiPM Simpl
MPP	ATLAS upgrade[2]	Belle II - PXD[3] ILC - VXD[2]		MAGIC, CTA[1/2] ILC calorimetry[1/2] CLIC tracking[1/2]
MPE		BepiColombo[4] SVOM[1] XTP-Gravitas[1] ATHENA[1]	eRosita[4]	
CFEL/ASG/(MPE) MPSD		XFEL-DSSC[3] lowE e- detectors[1]	CAMP[5] → LAMP	

[1] proposal phase, [2] R&D, sensor and system, [3] sensor production phase, [4] system assembly and calibration
[5] system in operation, improved version of CAMP (→ LAMP) planned

Common requirements for present-day and future detector systems:

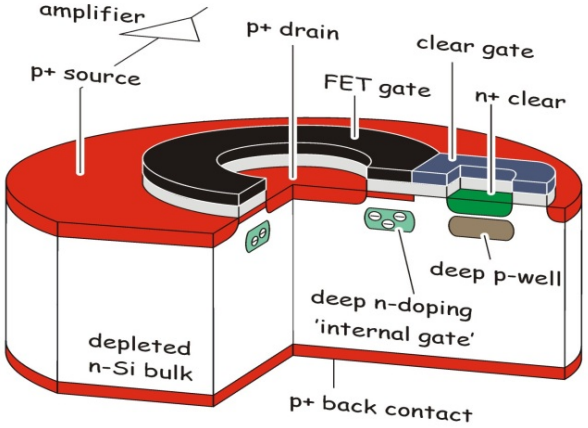
high S/N → sensor integrated first amplification stage (DEPFETs, first-FET in pnCCDs)
thin → sensors on SOI wafers (Belle II, ILC, lowE e- detectors, ATLAS upgrade, Simpl)
fast r/o
"intelligent" → new sensor/ASIC interconnection techniques, (ATLAS, XFEL-DSSC, Belle II..)
compact

DEPFET Types and Applications



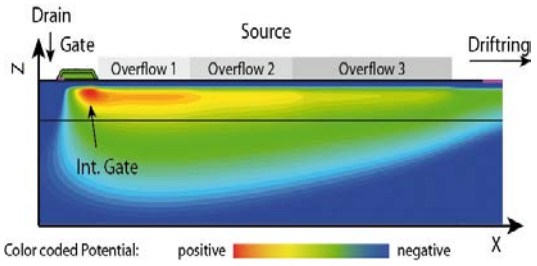
Particle tracking → vertex detector at **Belle II and ILC**

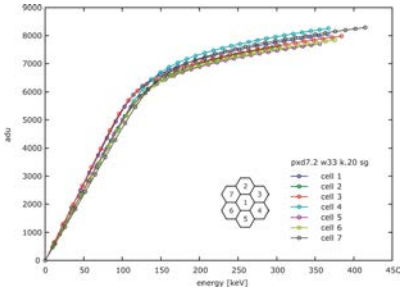
- pixel size: 20µm...75µm
- r/o time per row: 25ns-100ns
- Noise: ≈100 el ENC
- thin detectors: 50µm...75µm → still large signal: 40nA/µm for mip



X-ray imaging spectroscopy → **X-ray satellite missions**

- pixel size: 100µm, with SDD around 100s of µm
- r/o time per row: 2.5 µs
- Noise: ≈4 el ENC
- fully depleted thick detectors better → large QE for higher E

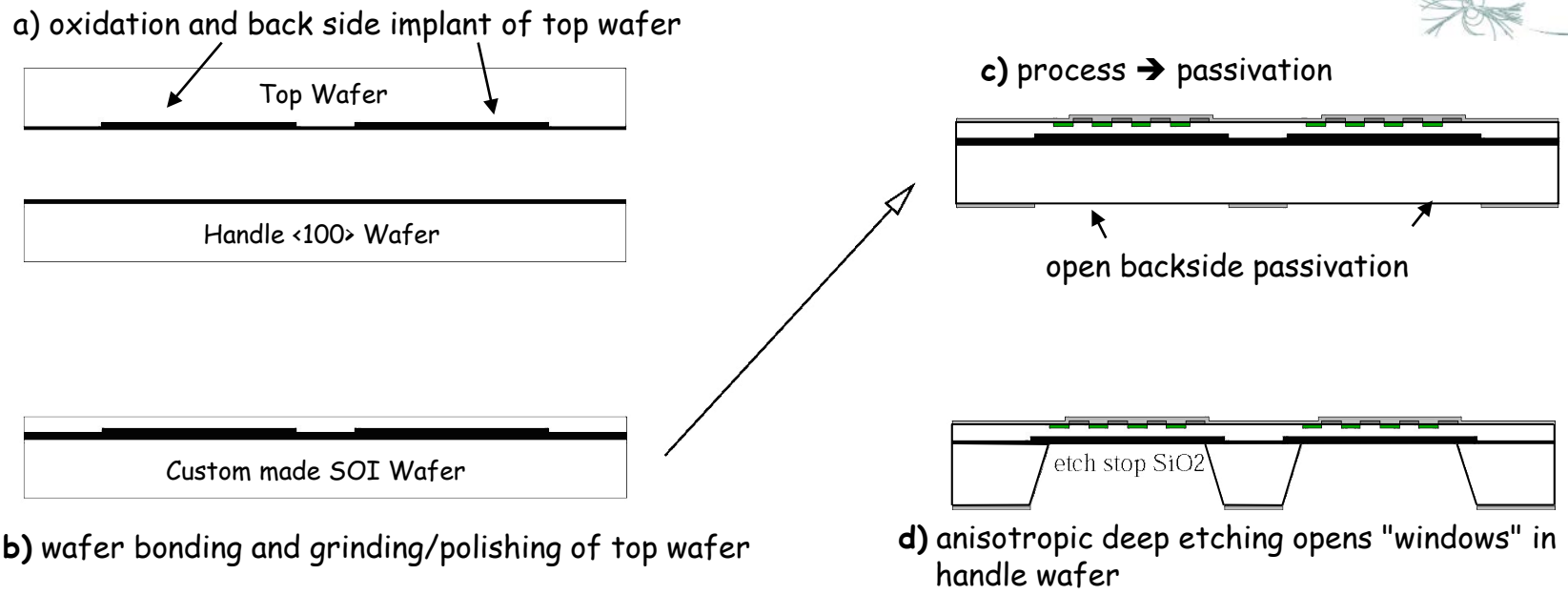




High Dynamic range: **XFEL-DSSC**

- DEPFET → DSSC
  DEPFET **S**ensor with **S**ignal **C**ompression
- pixel size: ~200 µm

Processing thin detectors - the SOI approach



The sensor thickness becomes a free parameter, adjustable to the needs of the experiment!

Key Process Modules:

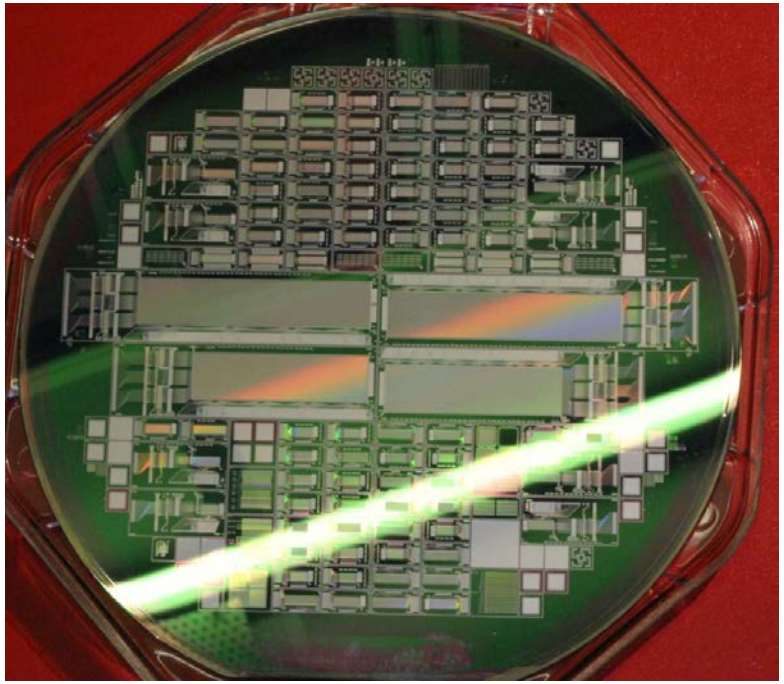
▷ Wafer Bonding and thinning of top layer → Custom made SOI Wafers (thick top, buried implant, HiRes FZ Silicon...)
↳ initial industrial partner Soitec (market leader for SOI wafer)

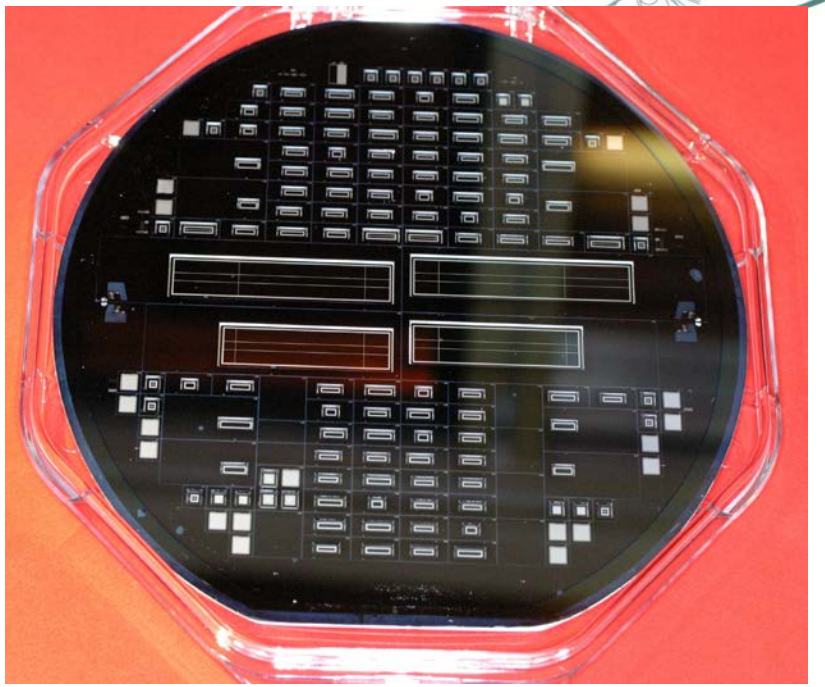
▷ Sensor fabrication on SOI
▷ Etching of the Handle Wafer
▷ Litho on extreme topographies

Developed for ILC VXD, the technology found its way into other projects:

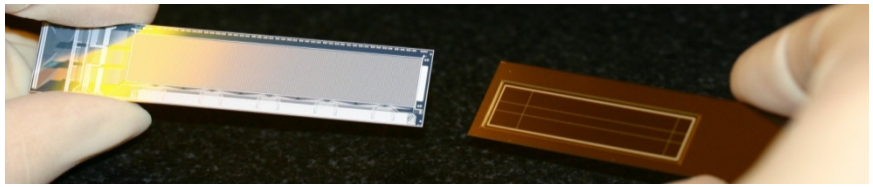
▷ 50 µm thin **DEPFETs** for Belle II PXD (will be 75 µm)
▷ production of thin (75 and 150 µm) ATLAS **pixel sensors** upgrade
▷ first production of **Geiger-mode APDs** on 70 µm top layer

PXD6: first thin DEPFETs on SOI



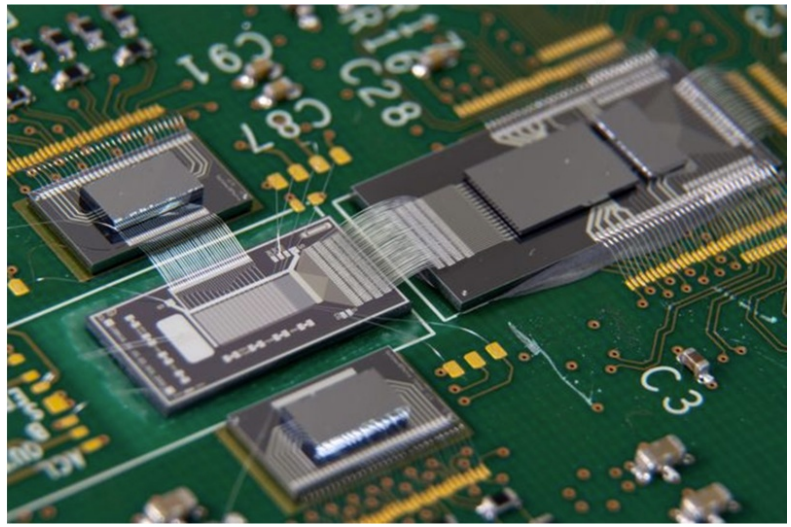


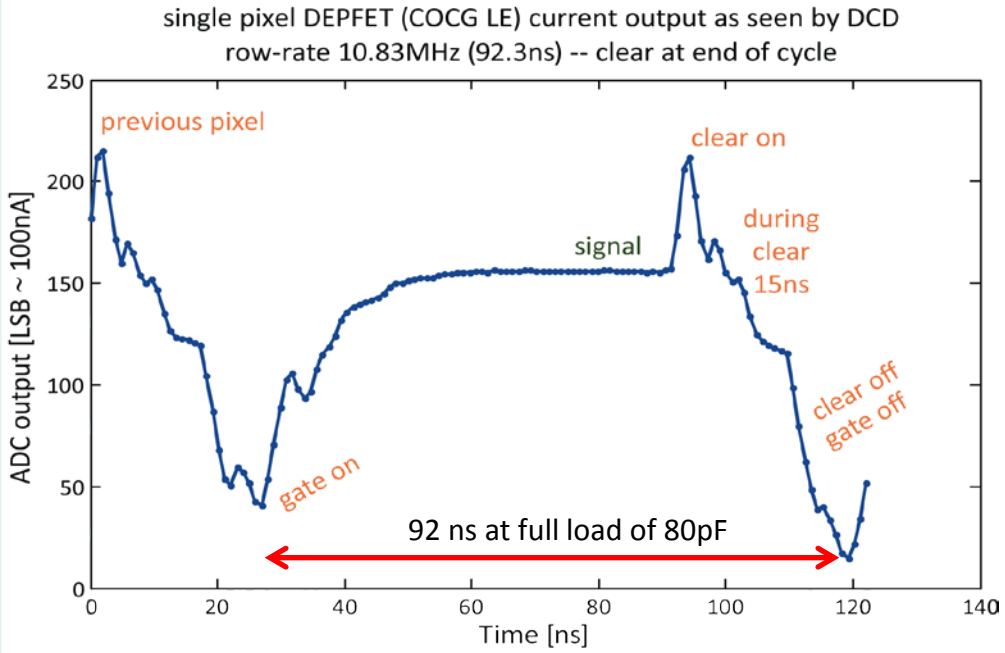
- 8 SOI wafers (50 µm top layer, 400 µm handle)
- 9 impl., 19 litho., 2 poly Si, 2 Al (.... & 3rd metal Cu later)
  - ↳ 3m (SOI) + 16m (main process incl. thinning)
- About 100 test matrices in different variations
  - ↳ pixel sizes from 20 µm to 200 µm
  - ↳ shorter gate length, improved clear structures ...
  - ↳ various drift region and pixel designs ...
- 4 large half-ladders with the most promising options

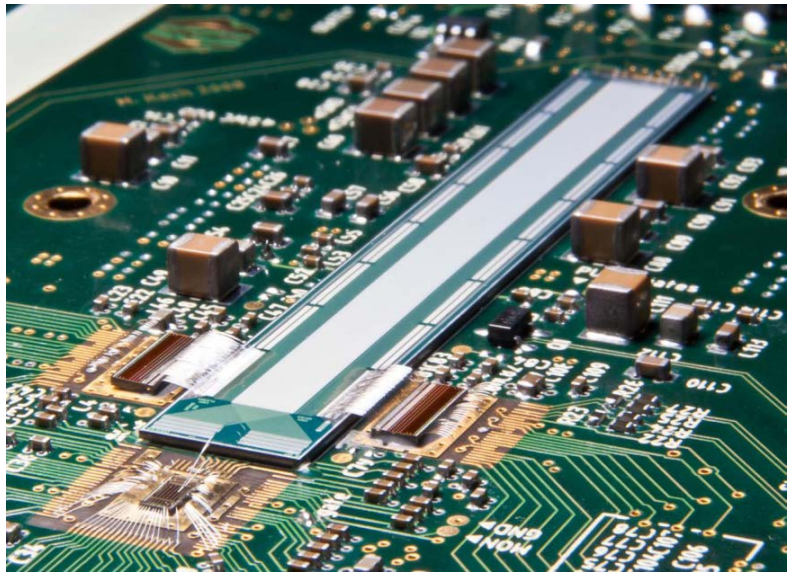


PXD6 testing in the lab

- bench tests in the lab
  - ↳ determine best operating point (Clear, ClearGate, Drift..)
  - ↳ in-pixel studies with laser
  - ↳ radioactive source tests
  - ↳ **read-out speed...**
- goal @Belle II
  - ↳ 320 MHz system clock
  - ↳ 50 kHz frame rate (20µs r/o time per frame)
  - ↳ 768 rows, 4-fold r/o → **~100 ns per row**

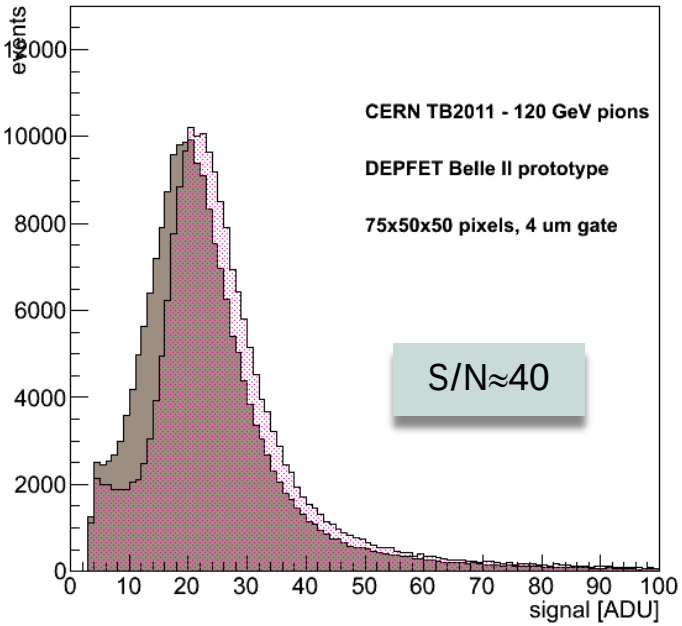


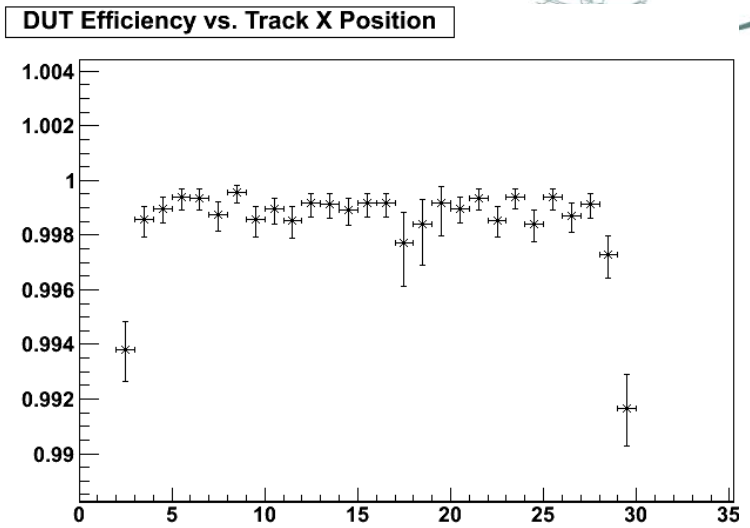


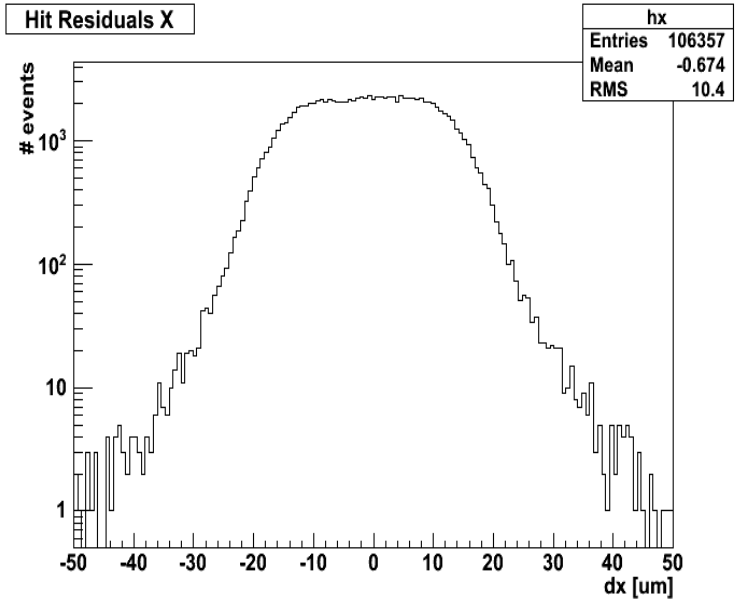


120 GeV pions beam test results

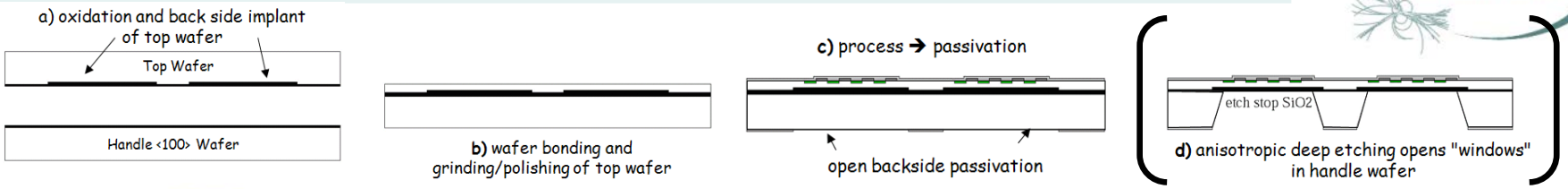
- latest beam test Oct. 2011, CERN SPS, 120GeV pions
  - PXD6 matrices, thickness 50µm
  - L=4µm, 75x50µm^2 pixel
- very good S/N
- efficiency >99.5%, both in X and y
- single point resolution ~10 µm (binary 14.4µm)



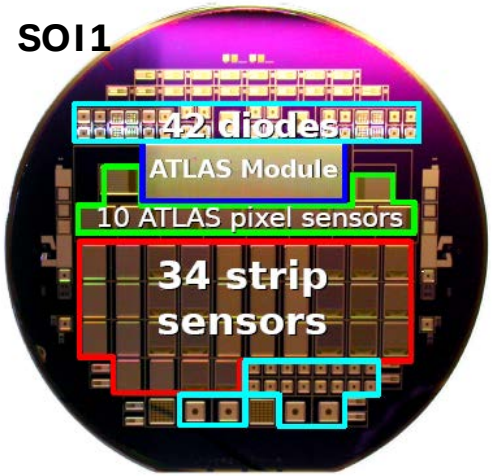




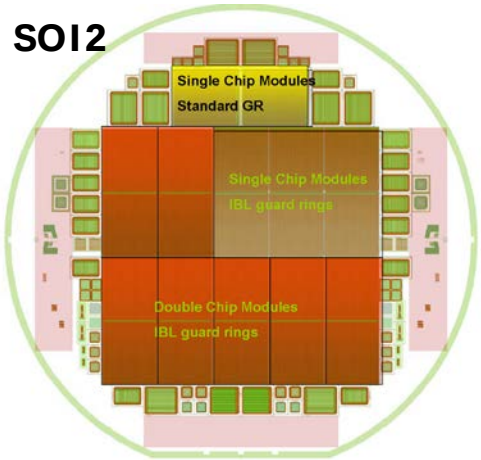
Thin sensors for the ATLAS pixel upgrade



SOI1



SOI2



SOI1:

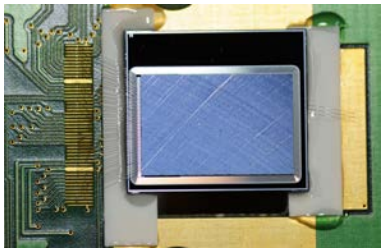
- 150mm, p-type top wafer, **75 µm** thin, HLL
- FE-I3 type pixel sensors (50x400 µm²)
- bump-less sensor and f/e interconnect (SLID, EMFT Munich)

SOI2:

- 150mm, p-type top wafer, **150 µm** thin, HLL
- FE-I4 type pixel sensors (50x250 µm²)
- sensor and f/e interconnect by conv. bump-bonding (IZM Berlin)

Reference:

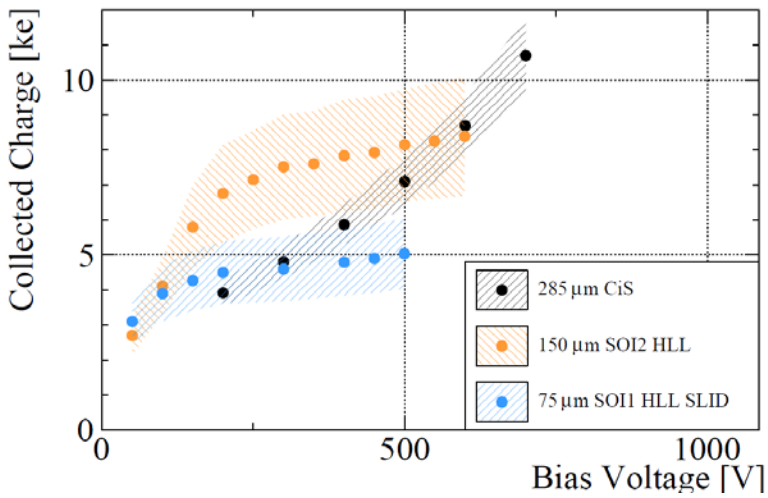
- 100mm, p-type std., **285 µm** thick, CiS
- FE-I3 type pixel sensors (50x400 µm²)



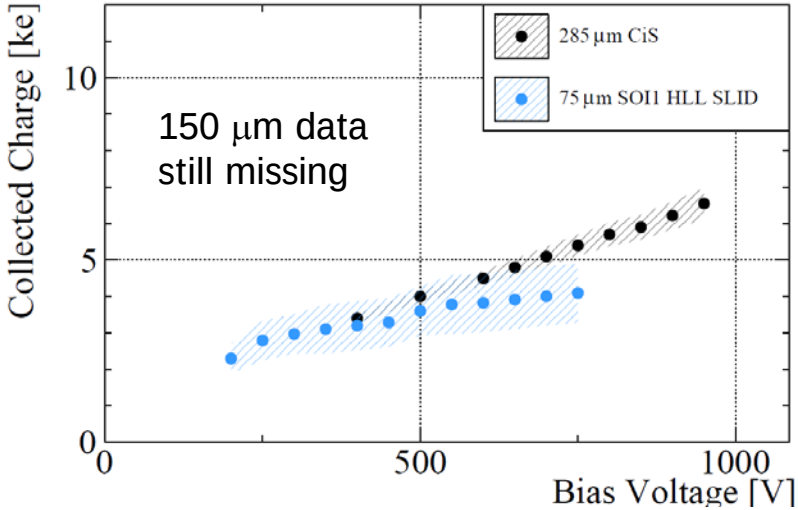
- Single chip modules irradiated up to 1e16 n_{eq}/cm^2
- Tests in lab and beam the charge collection and tracking efficiency

Charge collection in comparison

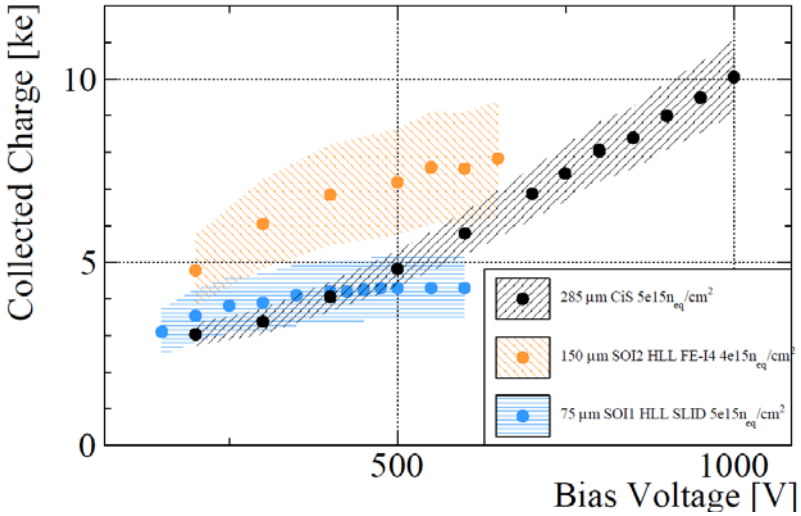
Φ= 2 x10^{15} n_{eq} cm^{-2}



Φ= 10^{16} n_{eq} cm^{-2}



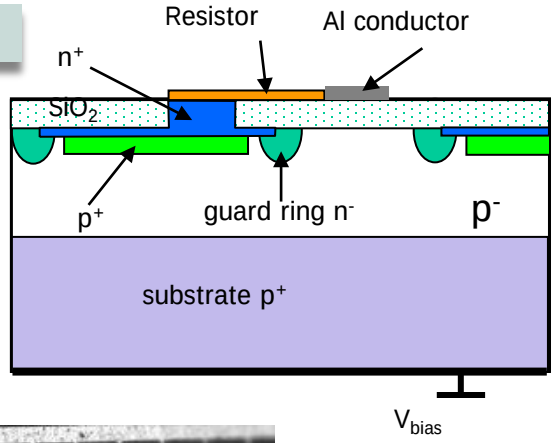
Φ=(4-5) x10^{15} n_{eq} cm^{-2}



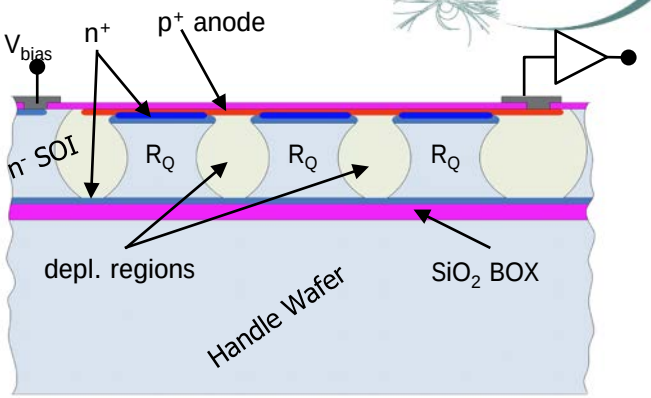
- Higher signal with 150 µm thick sensors up to Φ=(4-5)x10^{15} n_{eq} cm^{-2}
- At higher fluences the signal of thin and thicker sensors tends to equalize

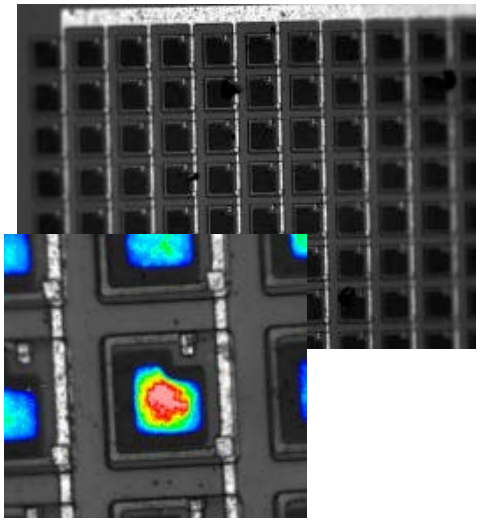
SOI III: Array of Geiger-mode APDs → SiPM → SiMPL

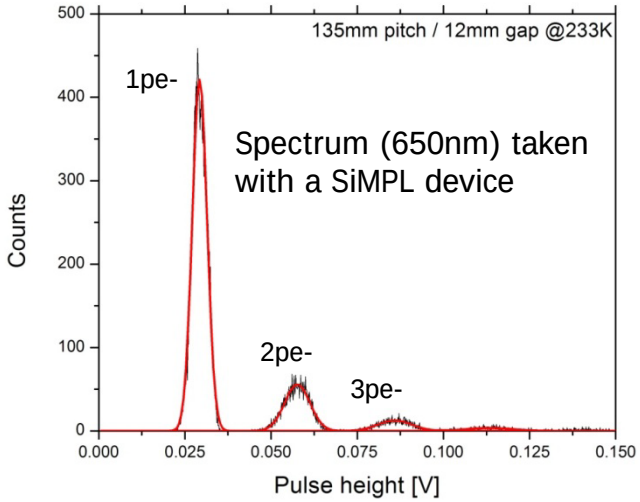
Conv. SiPM

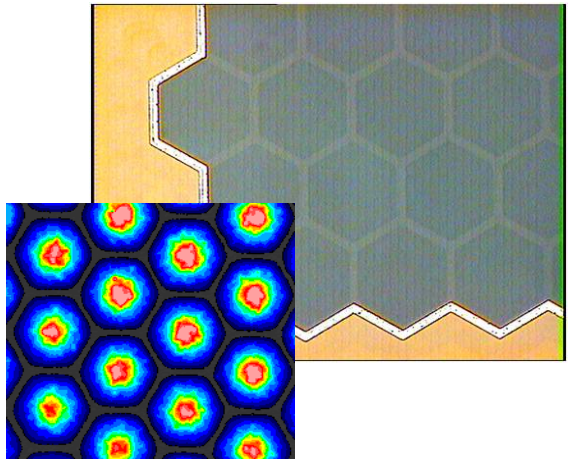


SiMPL



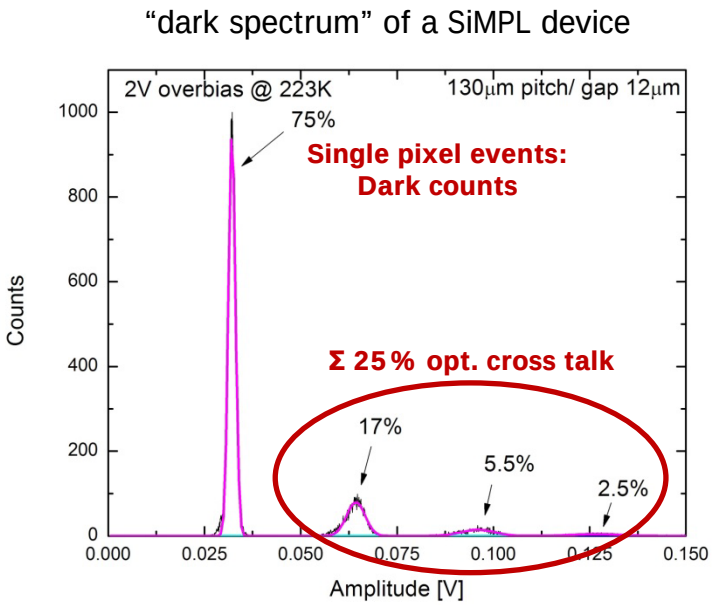


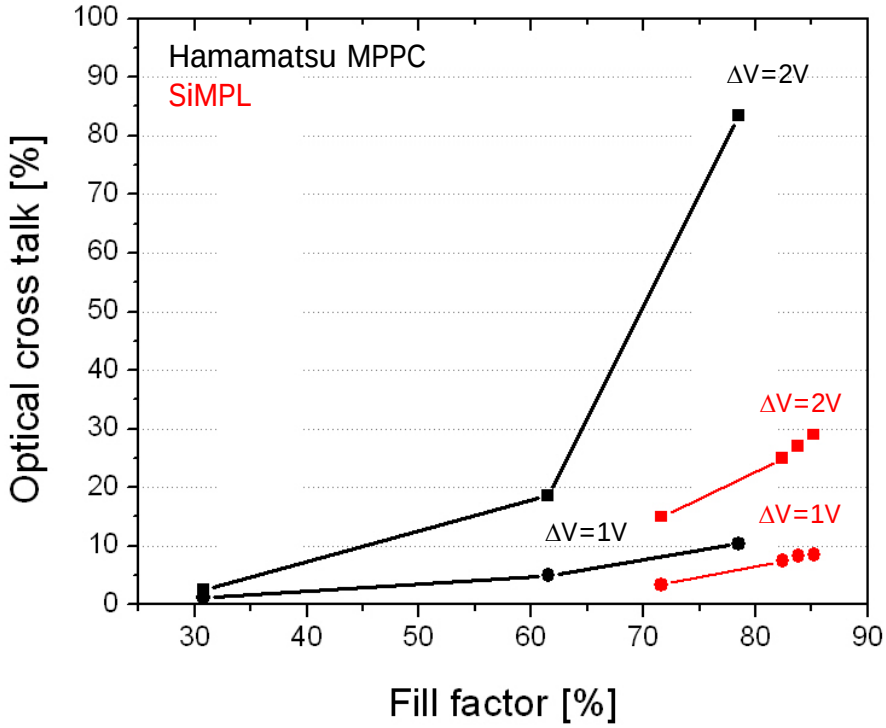




- New concept for an array of Geiger-mode APDs
- Bulk integrated quench resistors open the way to build arrays with very high fill factors
- Technology much simpler: Two prod. runs on SOI wafers with 70 µm top layer on R&D line

SiMPL – status





- Proof of principle is shown: quenching works and dynamical measurements show expected behavior
- In addition to the simplified process the devices have the advantage of
  - a lower optical cross talk at
  - high geometrical fill factors
- studies of the produced sensors (geometry dependent performance, PDE, ...) are still ongoing
- some process details still need optimization, mainly to reduce dark count rate

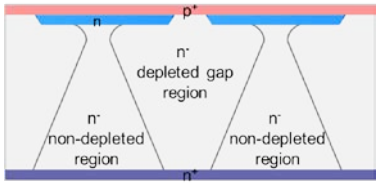
SiMPL – the future

Based on the promising results from the prototyping:

▷ foundation of a new Minerva group under the leadership of Jelena Ninikovic

↳ Jelana's postion, one post-doc, one PhD student, one technician: all positions filled, ready to start..

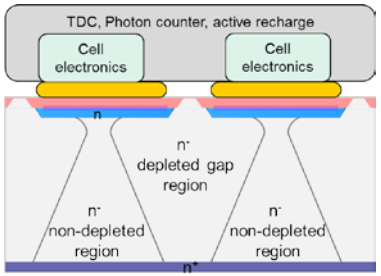
Roadmap of the project



▷ Optimize technology and produce improved SiMPL SiPMs for photon detection

▷ Optimized radiation entrance for various applications

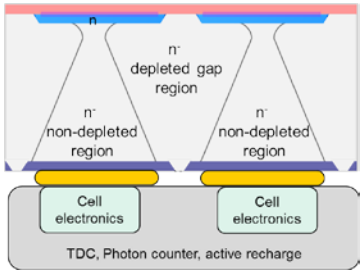
▷ Target experiments: Magic, CTA, Scintillator read-out for ILC Calorimetry



▷ SiMPL for particle tracking

▷ Segmentation of the anode, one r/o node per APD, bump bonded

▷ Target experiment: fast time stamping (few ns) for CLIC tracker



▷ SiMPL for particle tracking AND photons

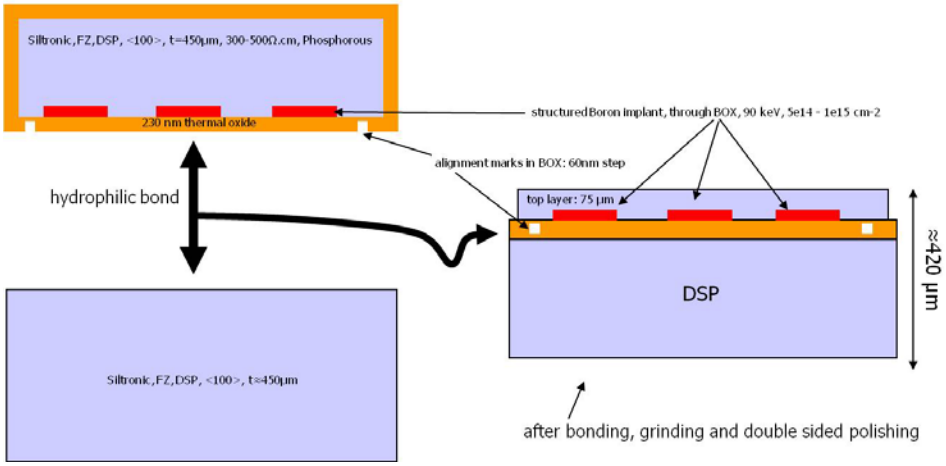
▷ Segmentation of the cathode, one r/o node per APD, bump bonded to thin Silicon

▷ Fast detection with more intelligence per pixel cell

SOI wafer supply

▷ all current MPP projects rely on high quality SOI wafers!

Raw wafer supply → pre-processing → SOI → HLL process → thinning…

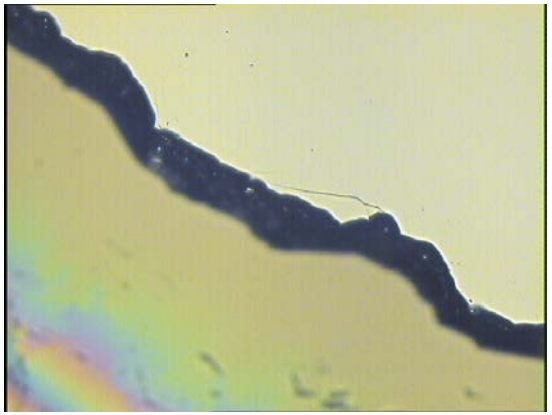


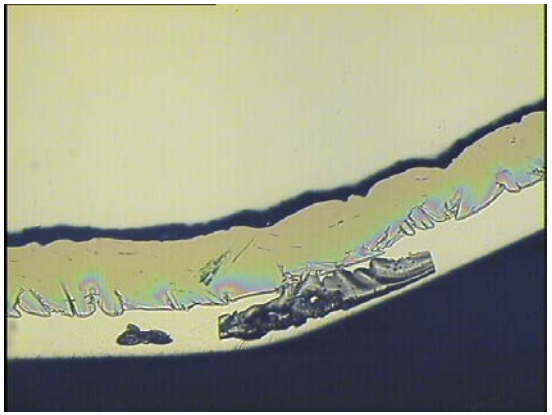
- ▷ Non-standard SOI, done externally
- ▷ Industrial partner Soitec stopped co-operation end 2010
- ▷ Urgent need to find and qualify other SOI supplier
- ▷ Need for external technology development

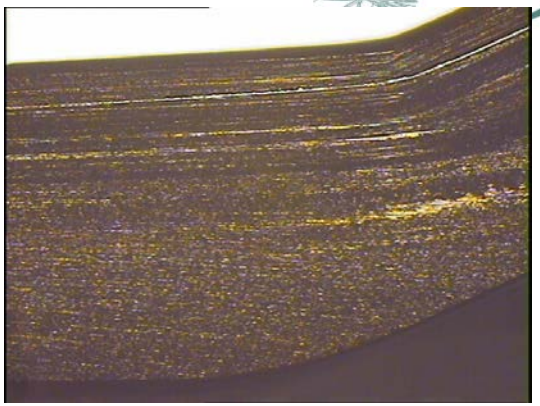
▷ SOI process modules

↳ Wafer bonding	→ Somewhat special due to our implanted back
↳ Edge treatment of the top wafer	→ turned out to be the most tricky part
↳ grinding and polishing	→ basically standard processes

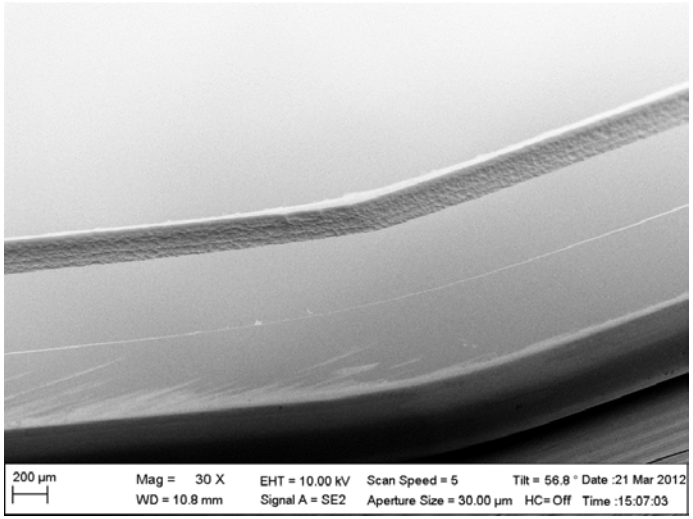
Technology development at Icemos





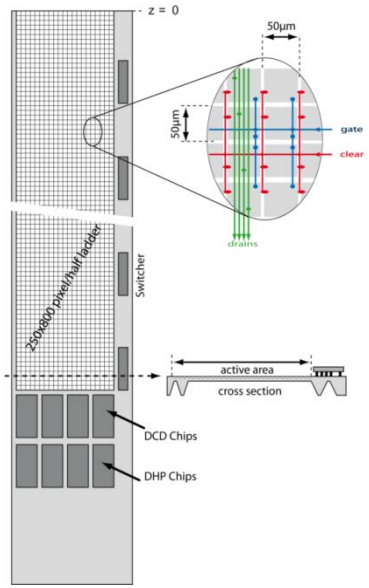


Proposed new process sequence



- Result of ~18 month development time
- Icemos now qualified as SOI supplier for Belle II, SiMPL …
  - ↳ bonding, edge treatment..
- In parallel qualify 2nd source Shin Etsu, Japan
  - ↳ Only possible due to Japanese contacts at KEK!!
  - ↳ Almost the same process →same quality
- **Belle II DEPFET production started with Icemos wafers!**
- **2nd batch Shin Etsu**

interconnection Sensor - ASICs

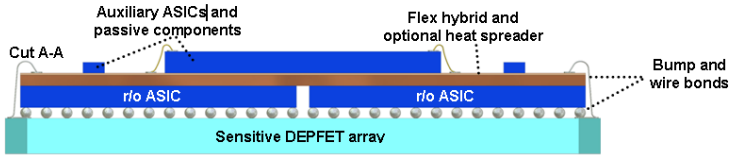


1. Belle II (and ILC):

- MCM – ASICs in different technologies on sensor as substrate
- bump bonds only on insensitive edge
- ~ 250 bumps/chip, 150 - 200 µm pitch
- frame rate: 50 kHz

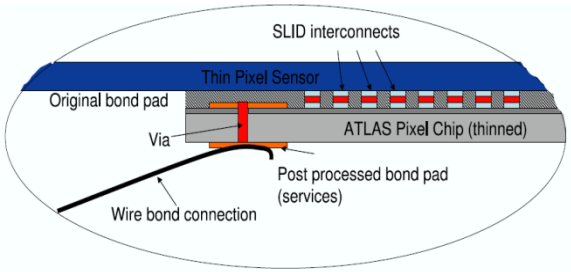
2. XFEL-DSSC:

- 1-on-1 connection DEPFET ←→ front-end
- ~4000 bumps / r/o-chip and 8 chips per module
- ~200 µm pitch
- frame rate 4.5 MHz for a 1Mpix camera



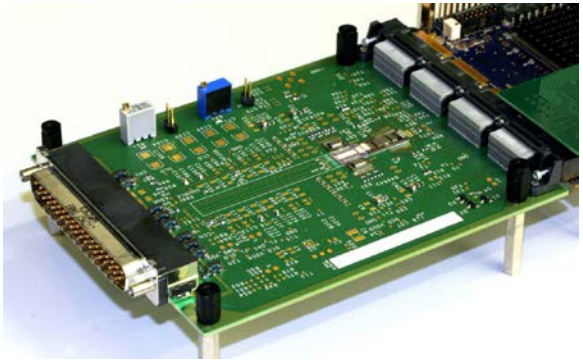
3. ATLAS Pixel upgrade:

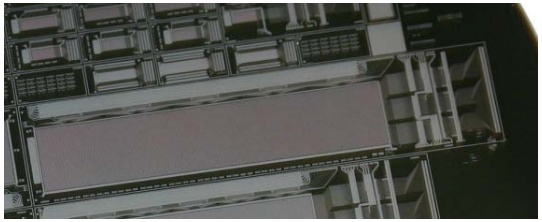
- 1-on-1 connection Thin pad detector ←→ front-end
- Vertical integration project with Fraunhofer EMFT Munich
- 50 µm pitch
- frame rate 40 MHz

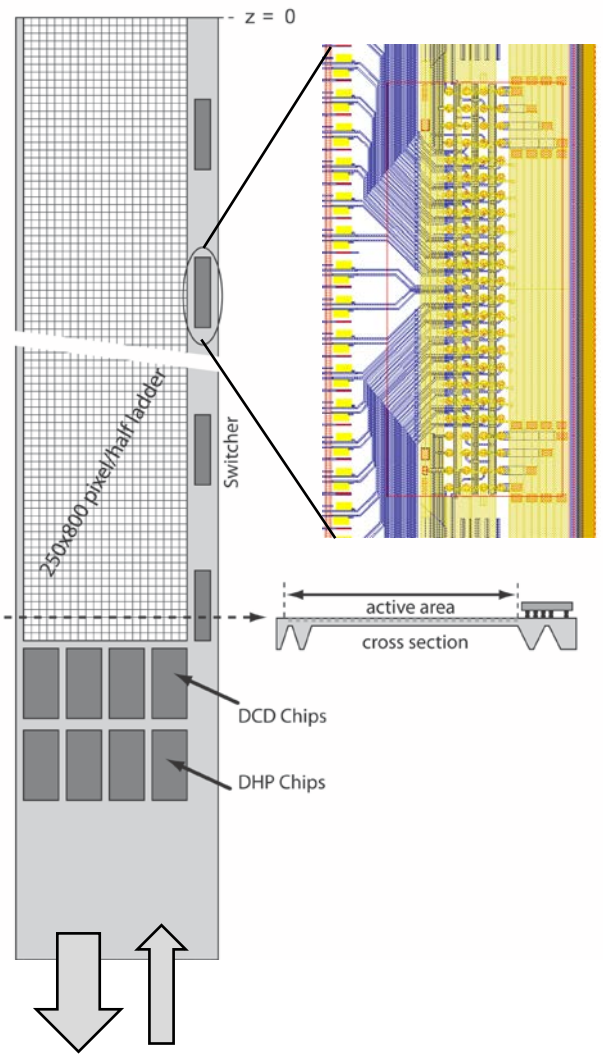


- Three important projects demand fine-pitch high-density interconnections → bump and bump-less flip-chipping
- We have to prepare our sensors for conv. bump bonding → solderable third metal layer
- We work with semi-industrial partners on novel vertical integration technologies

Belle II - towards a real ladder



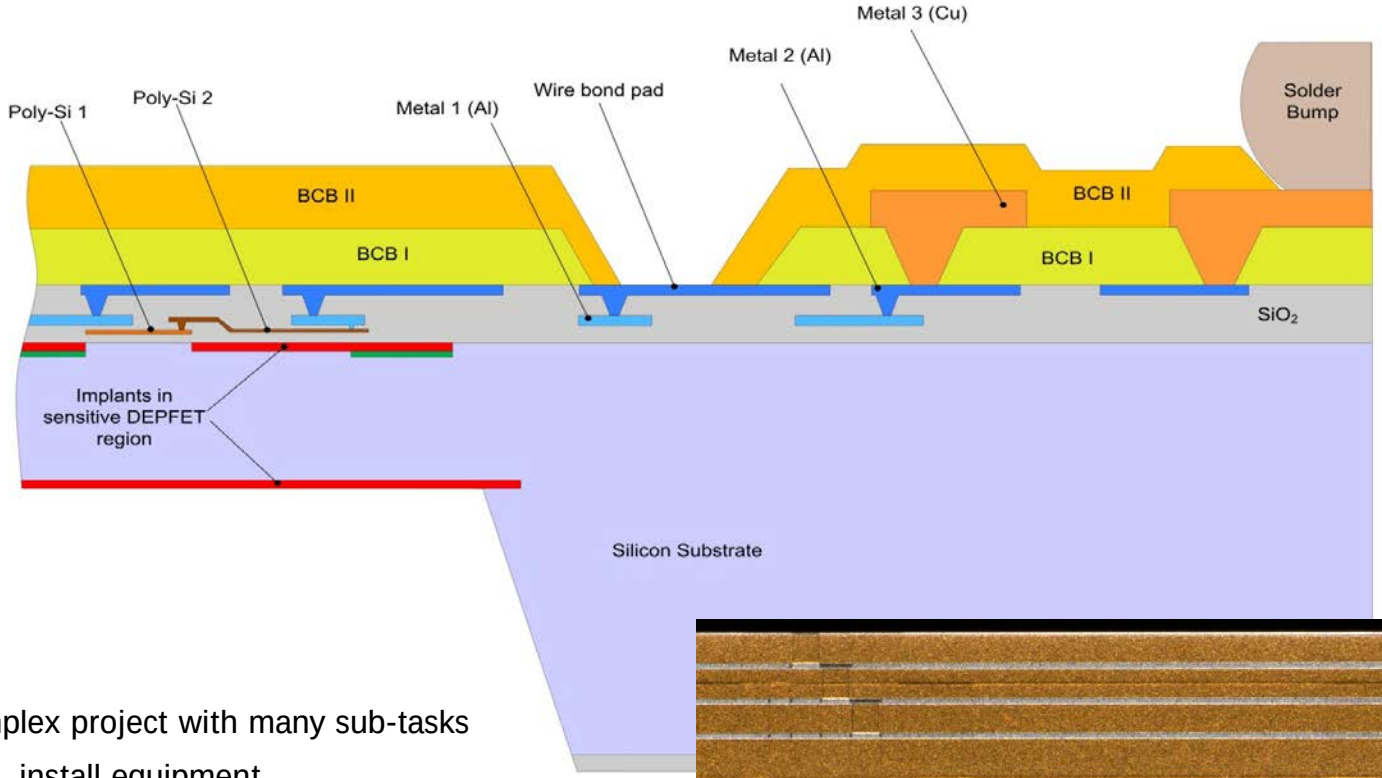


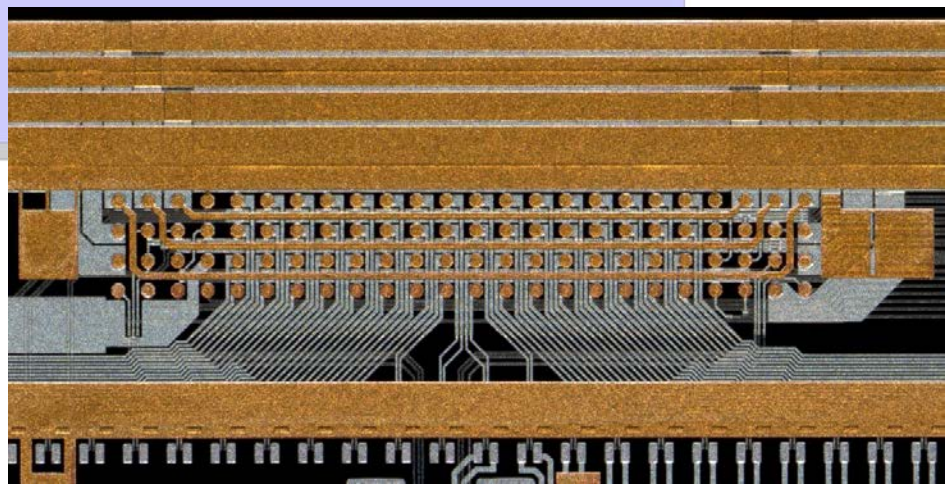


Transition from test systems to integrated modules

- PCB for the various matrices ….. “hybrids”
- first bump bonded chip on PXD6 matrices
  - 2 metal layers, not the final geometry, simple 3rd metal later
  - need still support PCB for I/O
  - not perforated balcony, Au studs as UBM
- Belle-II PXD Module (two modules form a ladder)
  - **three metal layers, Cu as LM only on periphery**
  - 4 DCD, 4 DHP, 6 Switchers → ~3000 bonds/module
  - **Cu as UBM, bumps partly on thinned perforated frame**
  - passive components soldered to substrate
  - I/O and power over Kapton cable

introducing a Cu layer on the DEPFET module





- complex project with many sub-tasks
  - ↳ install equipment
  - ↳ qualify various process modules
  - ↳ many(!!) test runs
    - ↳ electrical test samples and test diodes

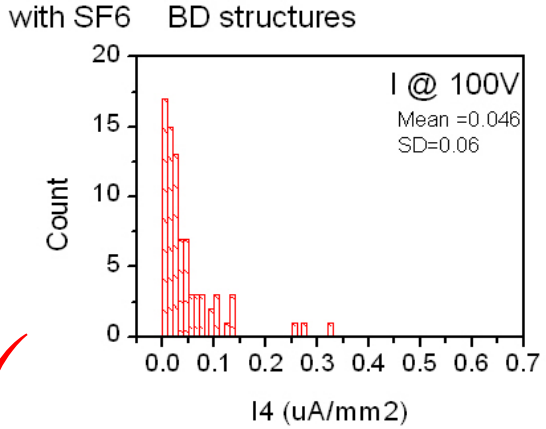
Cu Layer – status in summary

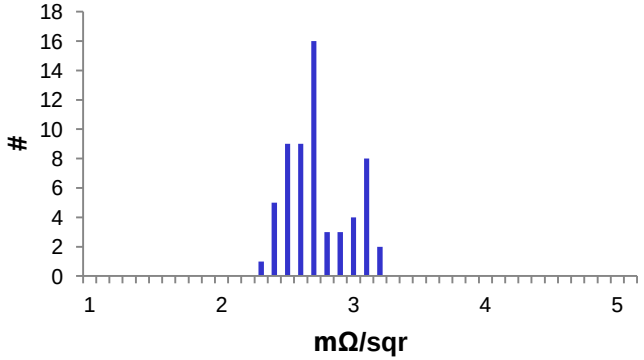
▷ BCB isolation layer to last Al: **stands 100 V with negligible current** ✓

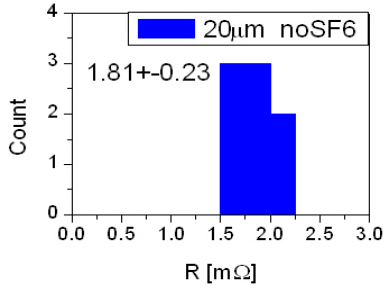
▷ 6µm Cu layer: **sheet resistance ~3 mΩ/sq.** ✓

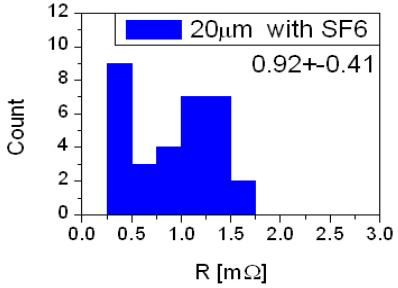
▷ contacts to Al through BCB isolation: **diameter 20 µm → 1 .. 2 mΩ/contact** ✓

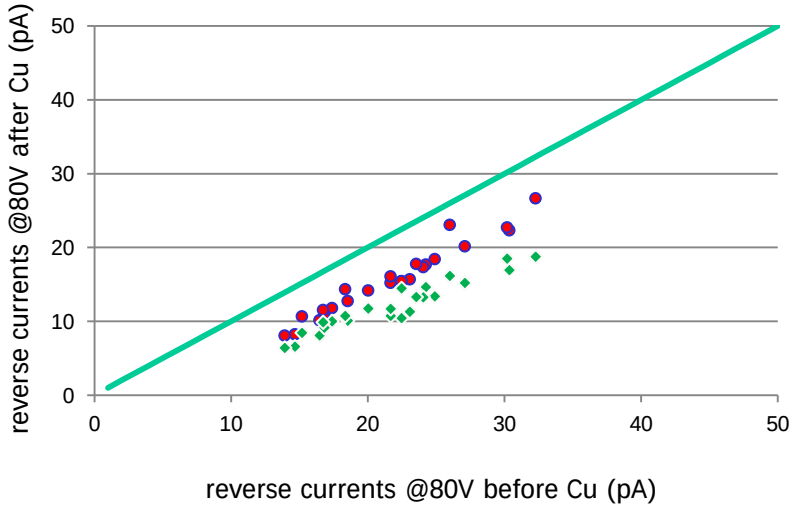
▷ basic properties of **test diodes and MOS caps not affected** by copper process ✓



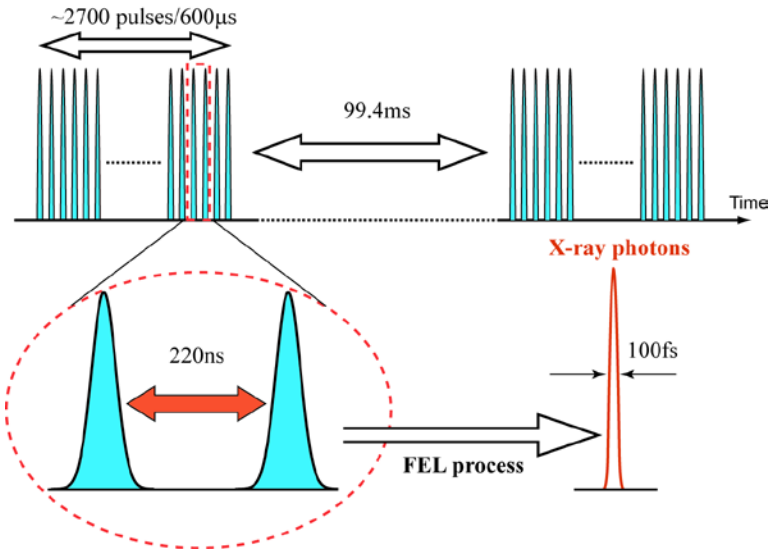


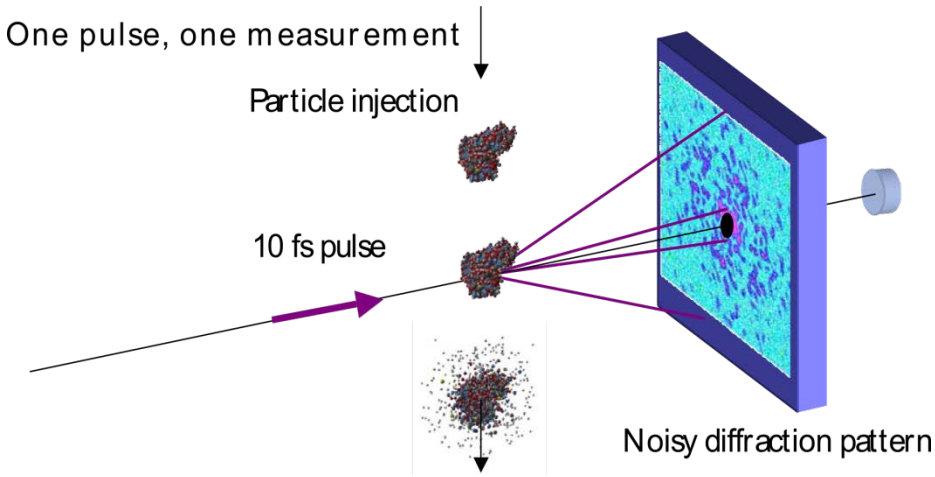






a camera for the European XFEL at DESY



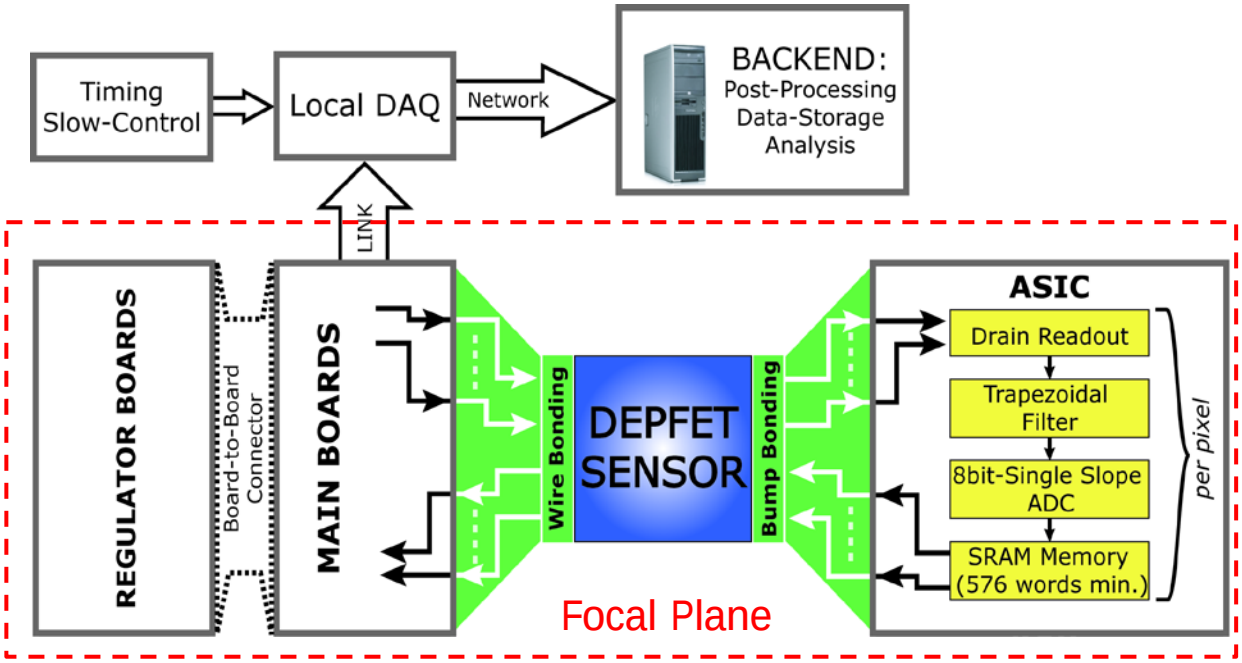


- ▷ e^- come in “trains”, ~2700 bunches/train, 600 µs long, 10 Hz train rate
- ▷ bunch spacing 220ns (4.5 MHz)
- ▷ each bunch gives an intense x-ray flash of ~100 fs duration

Key Requirements for the camera:

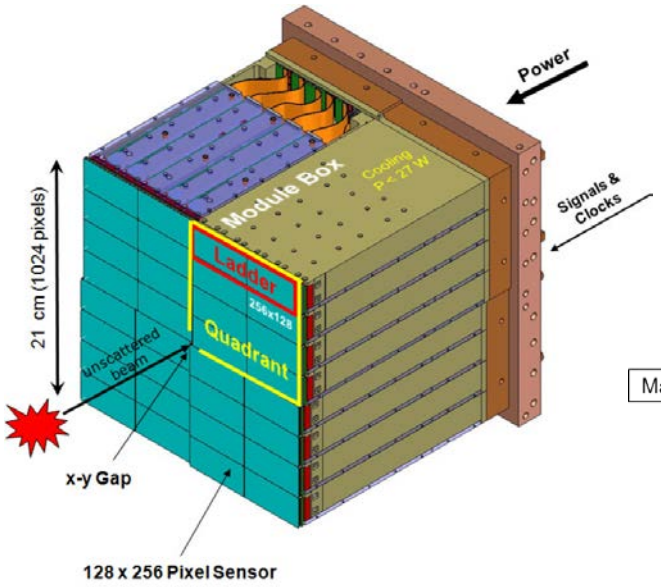
- ▷ Take “snap shot” with a 1Mpix camera with every flash
- ▷ Detect single low energy X-rays (≥0.5 keV → 140 e-h+ pairs in Si)
- ▷ Detect up to 10^4 X-rays with resolution better than Poisson limit
- ▷ Possibility to process ≥500 pulses in each burst

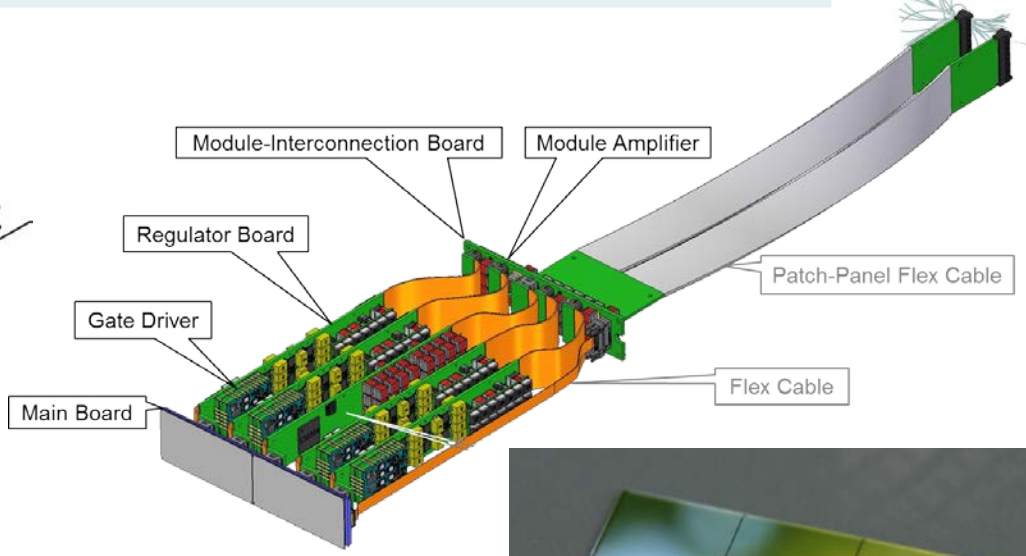
system block diagram

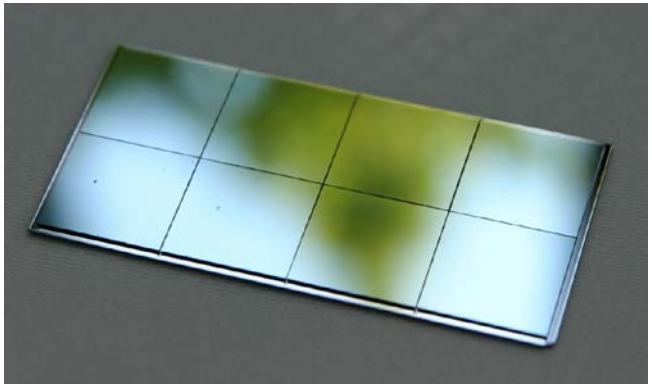


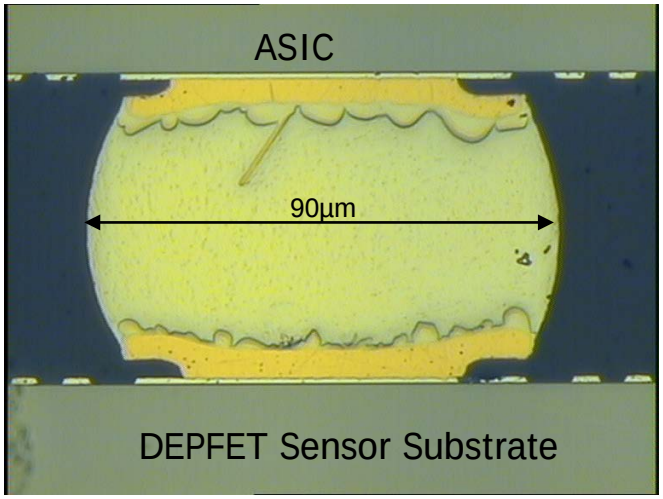
- Hybrid pixel detector with non-linear DEPFET active pixels (DSSC)
- r/o ASICs bump bonded, one bump per pixel in sensitive area
- Front- end amplifier, 8-bit ADC, and SRAM per pixel
- Digital data are sent of the focal plane during the train gap (~100ms)
- Power cycling: sensors and analog f/e in stand-by during train gap

- full parallel read-out – 1Mpix at 4.5MHz frame rate



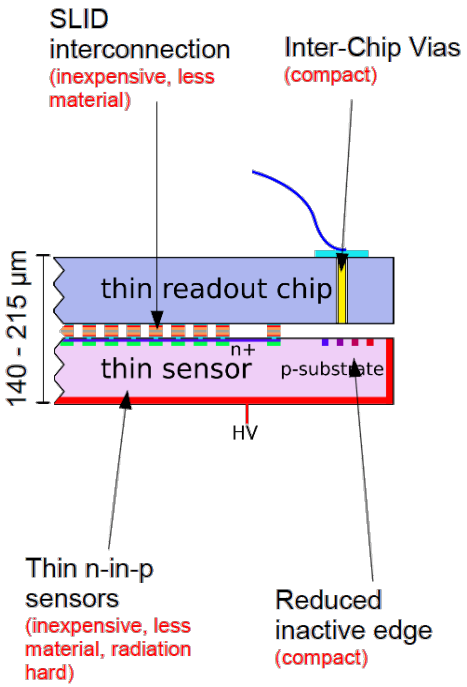


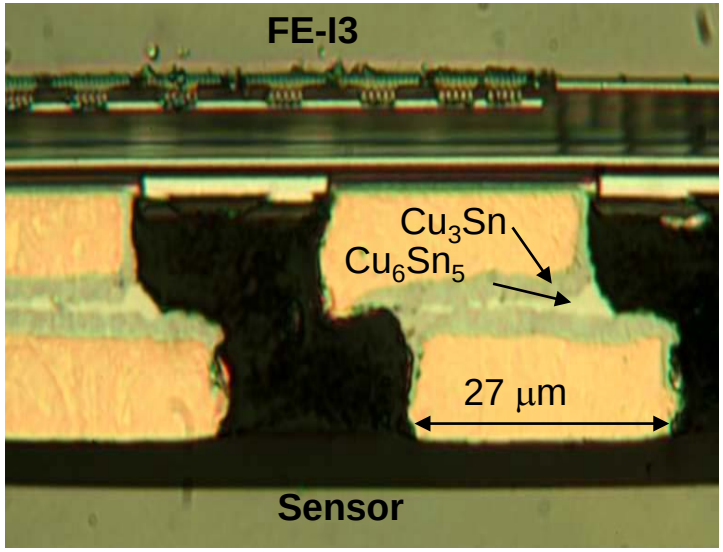


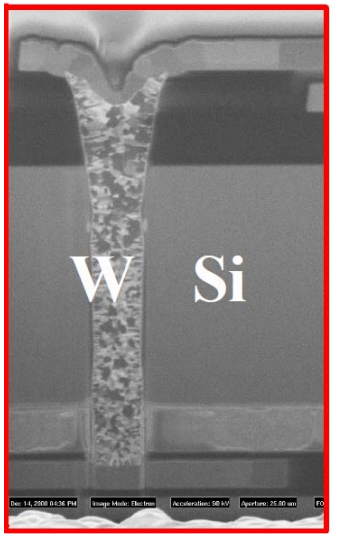


- Bump bonding installed at HLL
- 8 chips, 1.5x1.4 cm², 33000 bumps in total per half-ladder
- Low force, back side free, bump bonding on special jigs

The ATLAS Pixel Detector Upgrade







Fraunhofer EMFT

Most challenging interconnect project, in co-operation with Fraunhofer EMFT

- alternative to bump bonding → bump-less Cu-Sn eutectic bonding "SLID"
  - ↳ pitch <50µm, possibility to stack thin chips
- Through Silicon Vias (TSV) → 4-side tillable sensors

- Status
  - ↳ feasibility of SLID demonstrated: high yield, radiation tolerant up to 1e16 n_{eq}/cm^2
  - ↳ assembly of first FEI3 and thin HLL pixel sensor expected beginning of 2013

Summary

- The main MPP Projects at HLL are
  - DEPFETs for Belle II (and ILC)
    - 1st batch started and already almost half-way through, 2nd to start soon
  - Pixel detectors for the ATLAS pixel upgrade
    - vertical integration project with Fraunhofer EMFT, thin planer sensors on SOI
  - SiMPL Silicon Photomultiplier and APDs in Geiger mode
    - start of new Minerva group → CTA, Magic, ILC calorimetry and CLIC tracking

- All MPP projects use custom made SOI wafers
  - wafer supply issue resolved, two new companies qualified

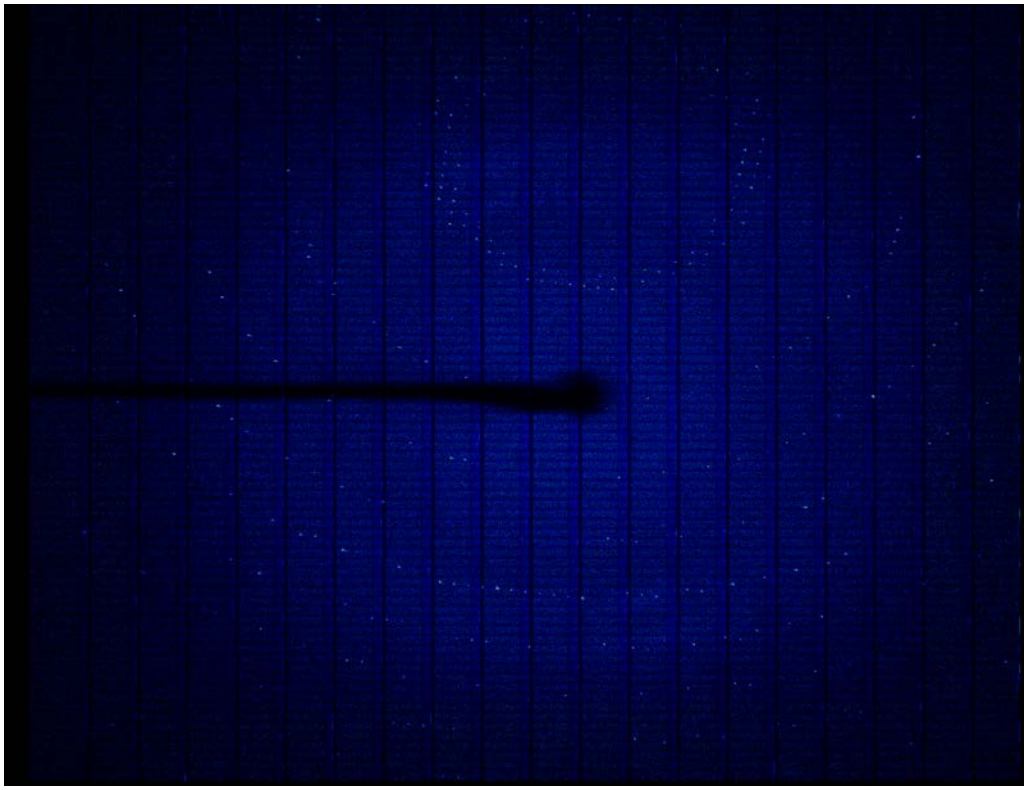
- All MPP projects (and XFEL-DSSC) need bump bonding and therefore a solderable metall layer
  - Cu technology and bump bonding installed and operational

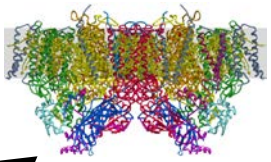
- Sorry for the biased presentation, the time is much too short!! I had to skip
  - radiation hard DEPFETs, new devices, technology improvements, spin offs ...

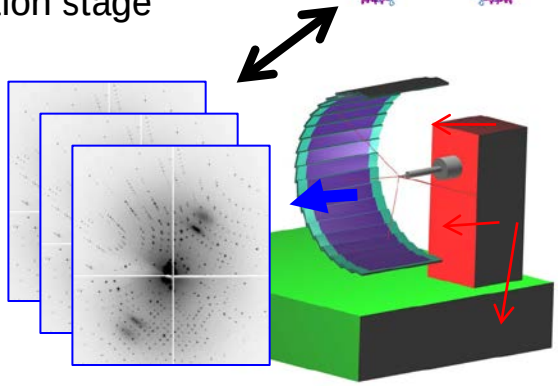
Belle II DEPFET spin-off

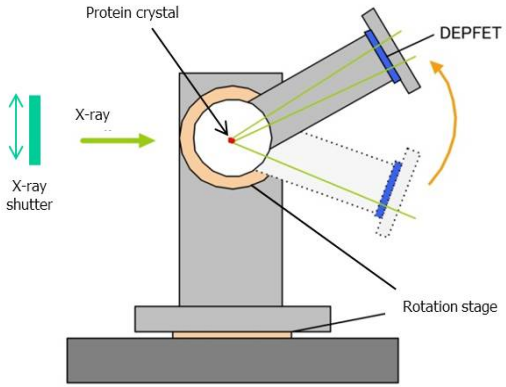
- Inquiry from KEK Photon Factory for a 8 Mpix camera based on Belle II system:
  - X-ray protein crystallography
  - time and space resolution better than commercial systems (Pilatus etc.)
  - fast read-out (50kHz frame rate) high granularity (50 µm pixel, or smaller)

- 2nd beam test 2012 with Belle II DEPFET prototype system on rotation stage
  - 12.3 keV photons on protein crystal

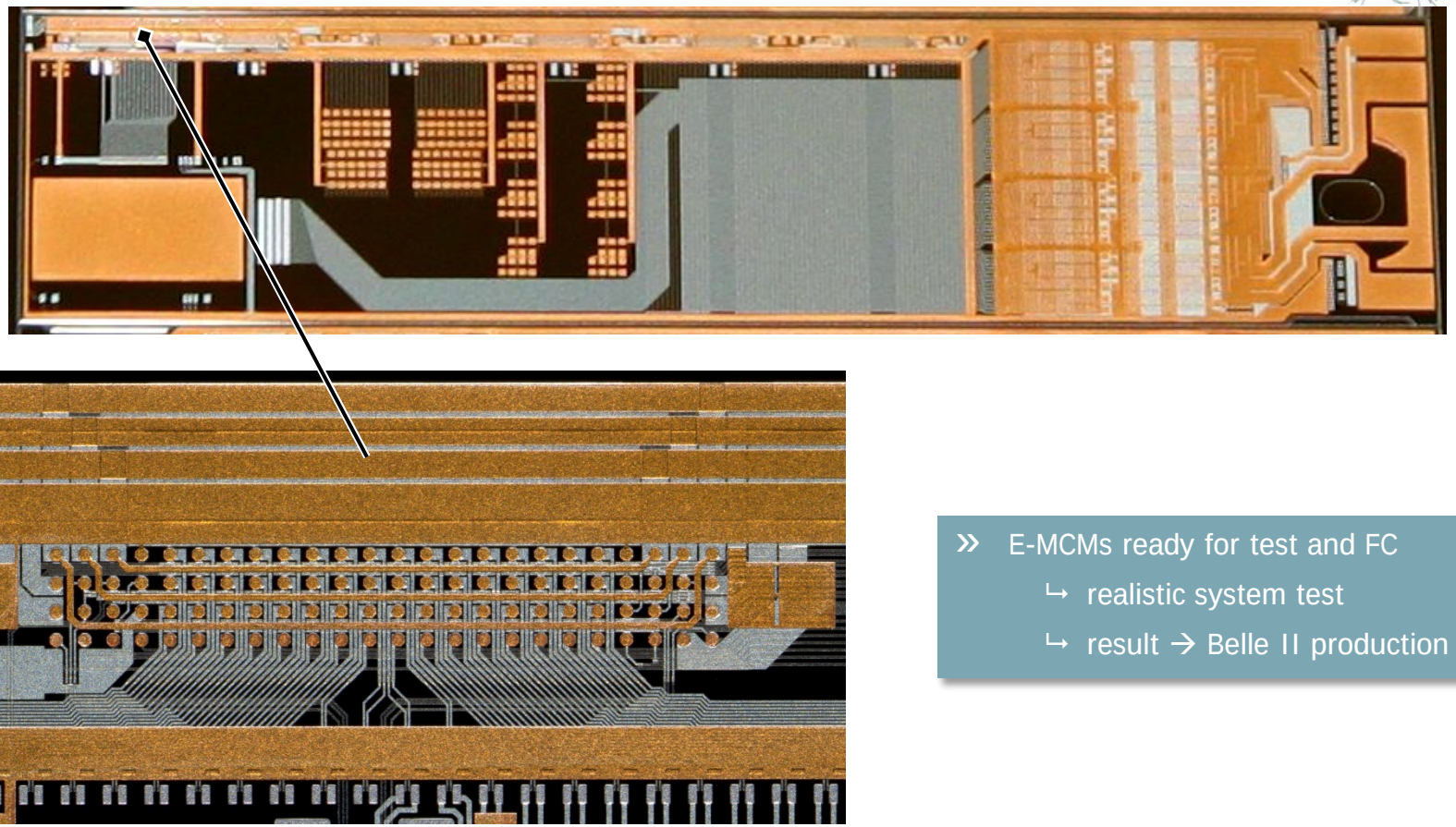








Verification of the module concept: E-MCM



- E-MCMs ready for test and FC
  - realistic system test
  - result → Belle II production

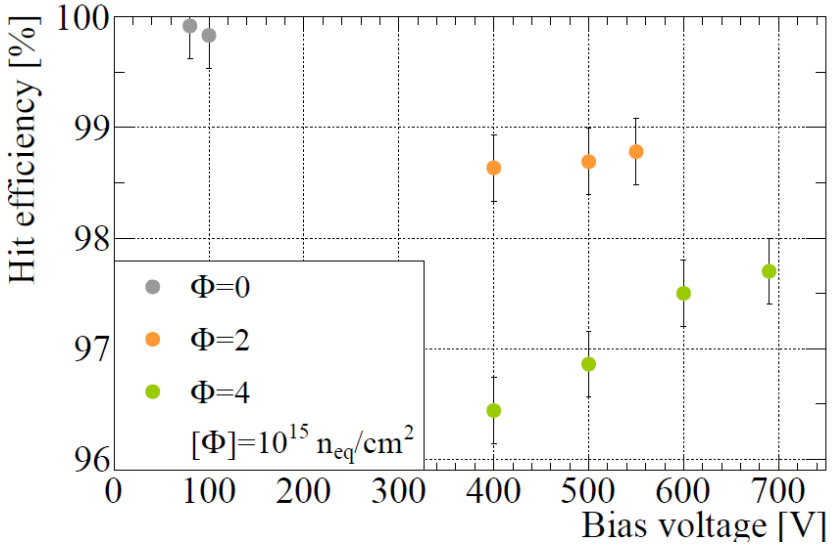
DEPFET technology with 3rd low impedance metal layer!!

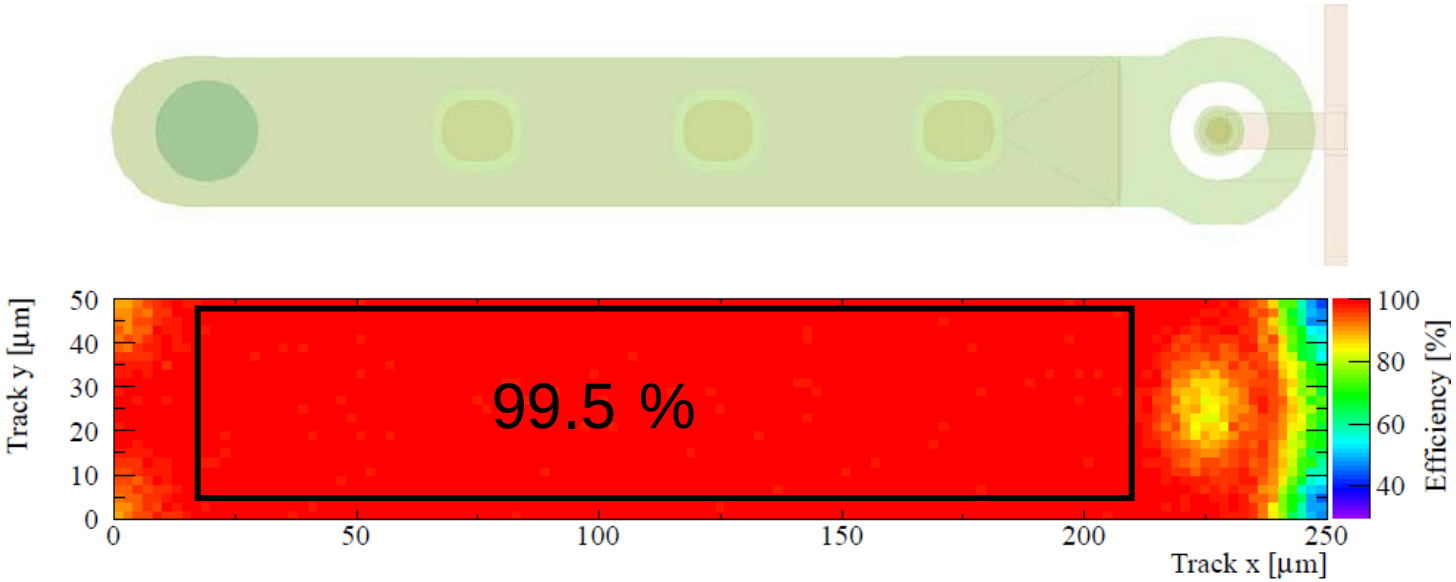
SOI2 modules: efficiency in the beam

- FE-I4 modules, SOI2, 150 µm sensor layer
- 120 GeV pions at CERN-SPS & 5-6 GeV/c e- at DESY
- non-irradiated, $2 \cdot 10^{15}$ and $4 \cdot 10^{15}$ n_{eq}/cm^2

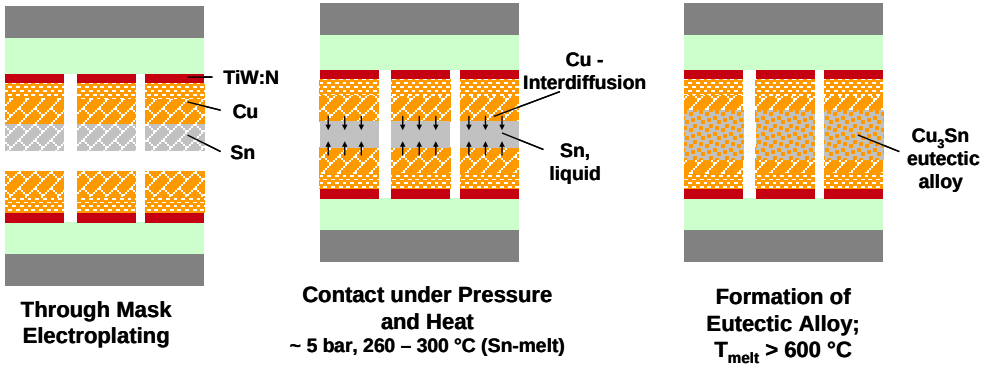
At 690 V bias, for the $4 \cdot 10^{15}$ n_{eq}/cm^2 module :

- overall CEE with a pixel (50x250µm^2): 97.7%
- excluding the PT bias structure: 99.5 %
- loss of CCE (perpendicular tracks) is a known feature of this type of sensors





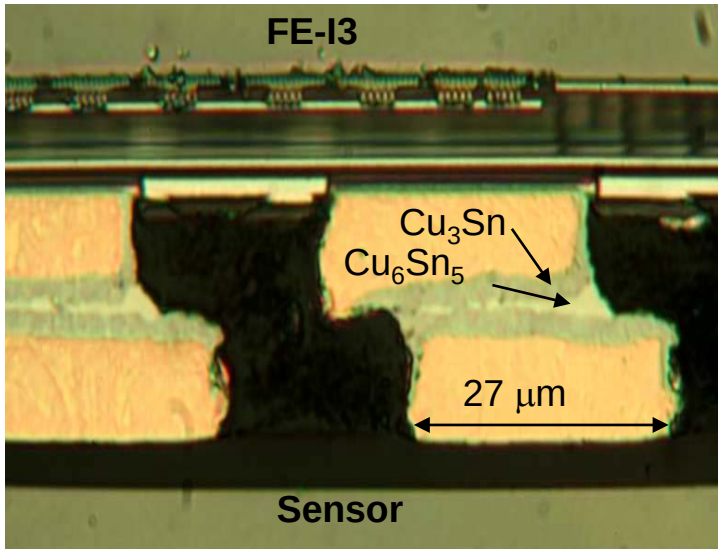
SOI1: "SLID" - "SOLID" – bump-less Cu-Sn eutectic bonding

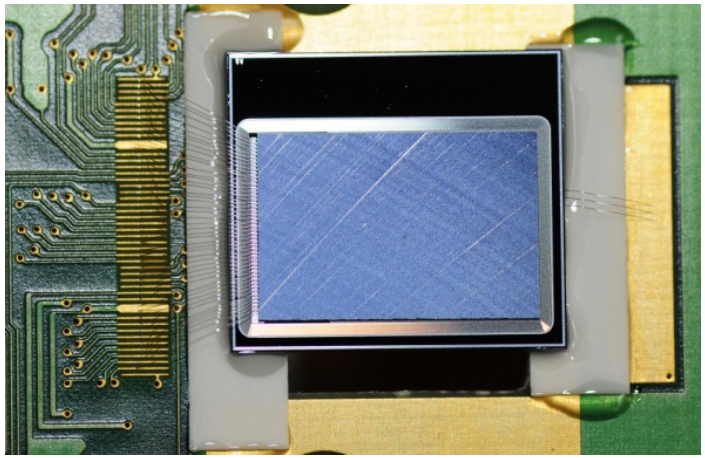


SLID: Solid Liquid Interdiffusion

- alternative to conventional bump bonding
- Cu+Sn layers → Cu_3Sn alloy
- for electrical and mechanical connection
- min. pitch given by pick and place (~20µm)
- wafer-to-wafer, chip-to-wafer, and chip-to-chip

- However: no rework possible!



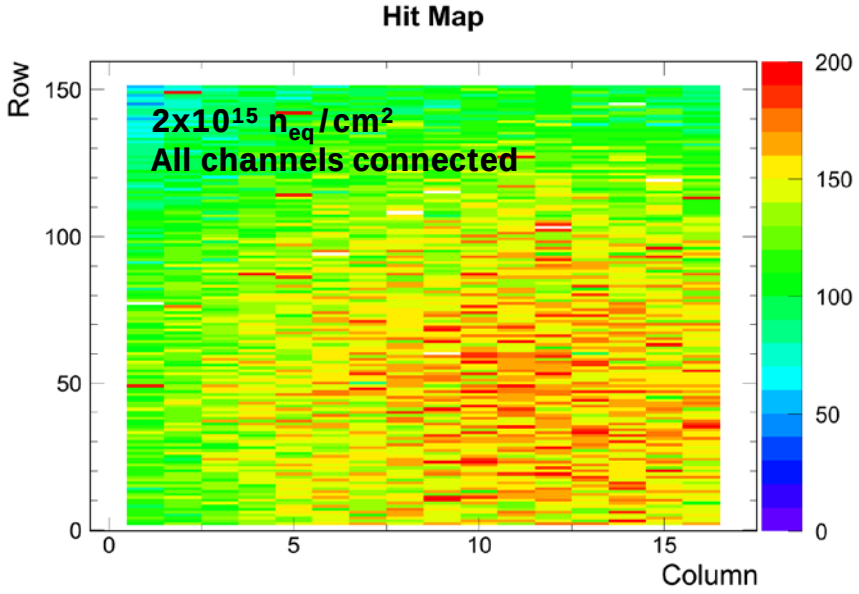


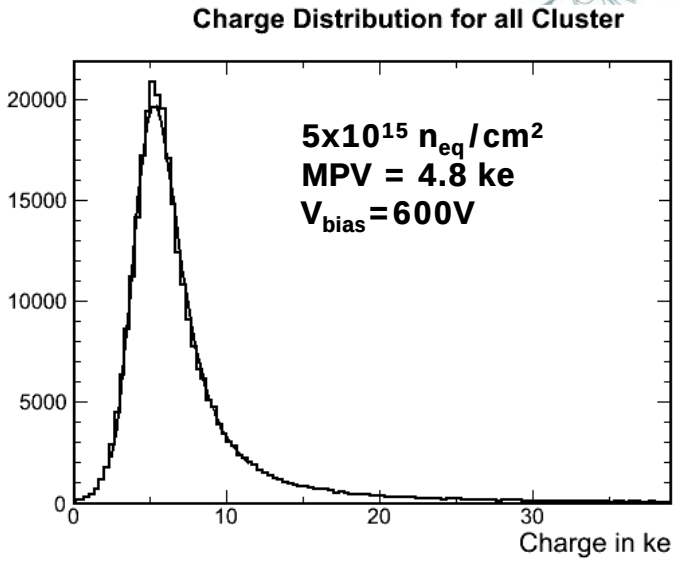
- sensor/FE-I3 stack read out with Uni Bonn read-out cards
- interconnect yield comparable with conv. bump bonding
- for more details see TIPP2012 proceedings, arXiv:1202.6497

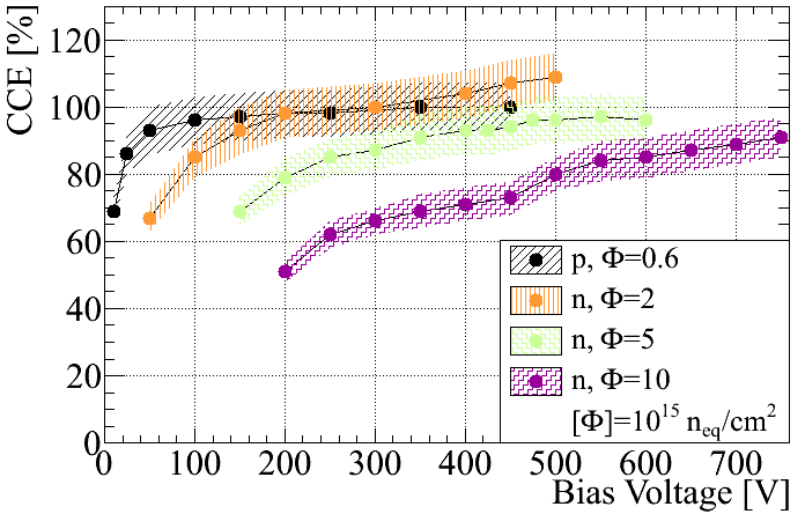
Fraunhofer EMFT

Lab tests of the SLID modules - after irradiation

- SCMs irradiated up 10^{16} n_{eq}./cm^2
- tested with a 90Sr source
- interconnection yield unchanged after irradiation and multiple thermal cycling (+20°C → -30°C)

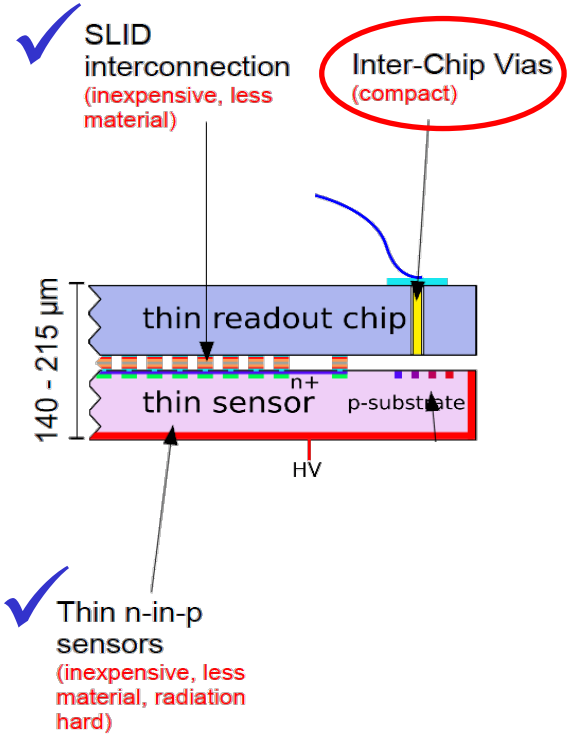


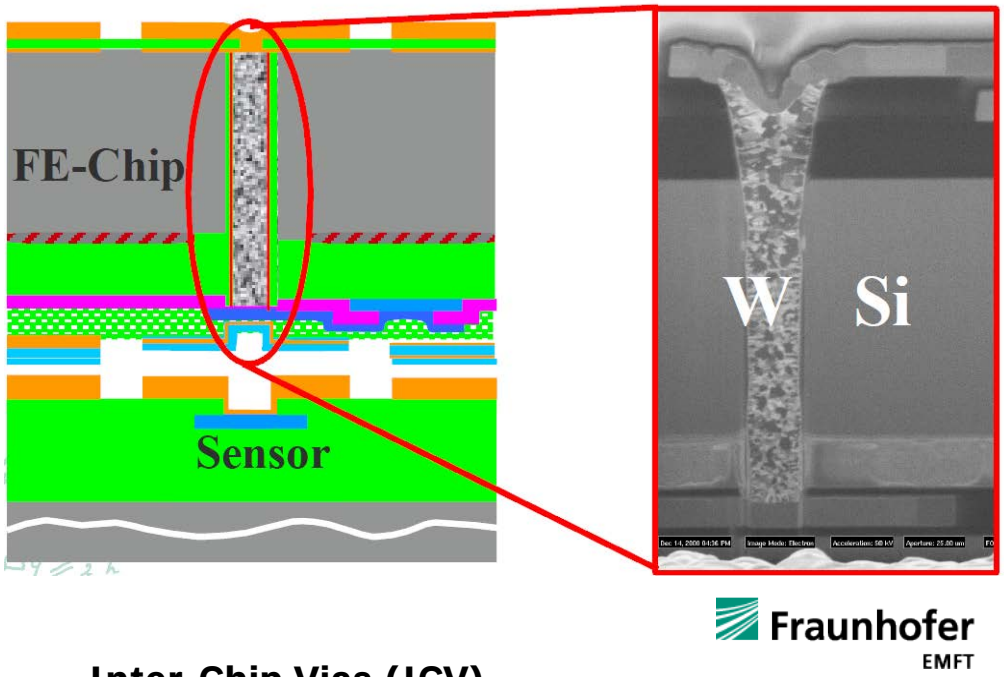




SLID interconnection is radiation hard and withstands thermal cycling

Inter-Chip Vias ICV → TSV





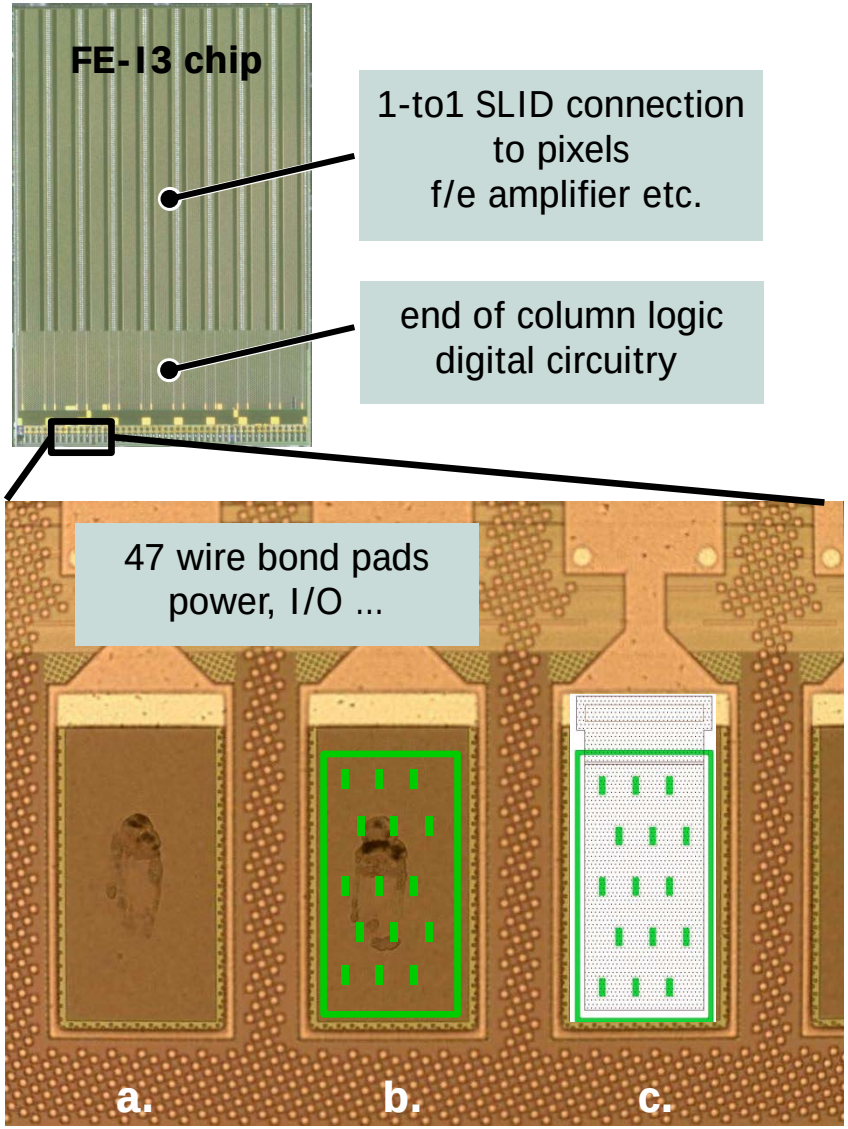
Fraunhofer EMFT

Inter-Chip Vias (ICV)

- Allow for vertical signal transport through Si structures
  → Compact pixel modules

- post-processing of the FE-I3 wafer ("via last" approach)
  - via etching on front side (Bosch-process), isolation, and tungsten filling
  - back side thinning of the wafer → ~60 µm
  - isolation and metallization for the back side contact (wire bonds)

Location of the vias



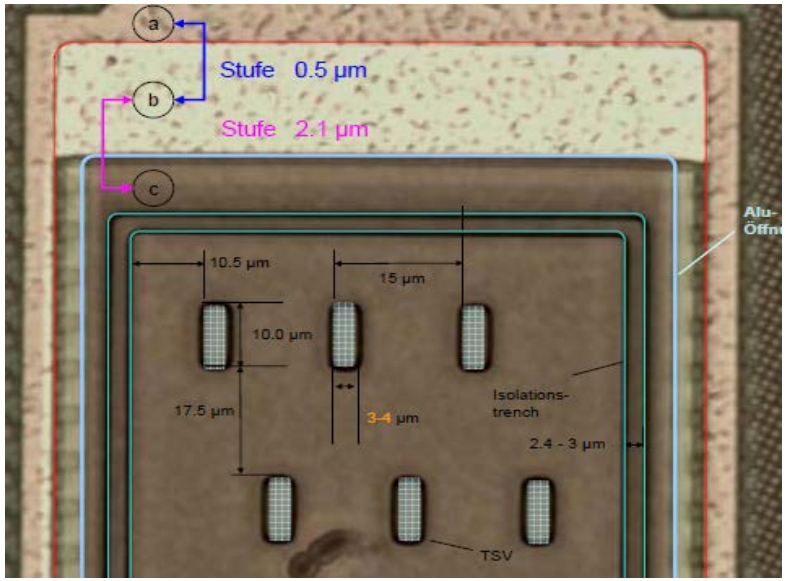
wire bond pads → back side of the chip

a.) remove pad metal (Alu)

b.) etch blind vias from the front side

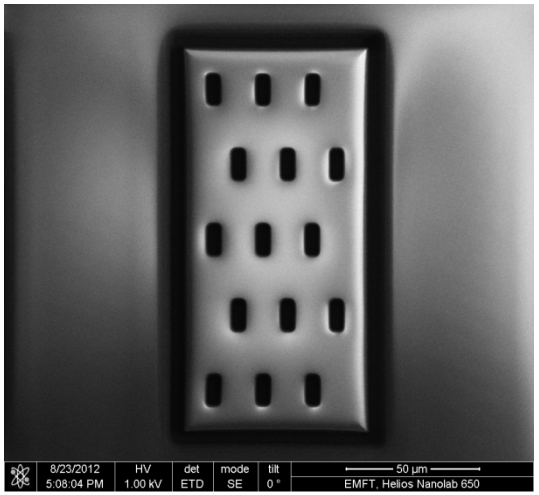
3x10 µm², ~70 µm deep

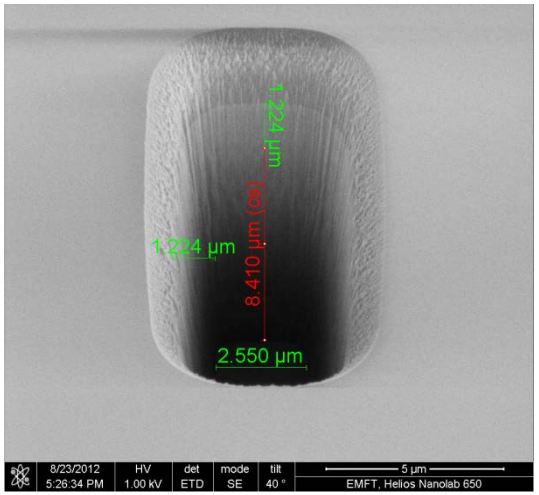
c.) connect via metal to pad metal on the front

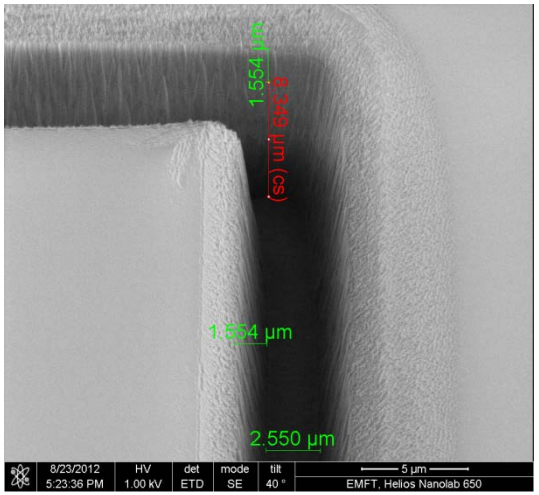


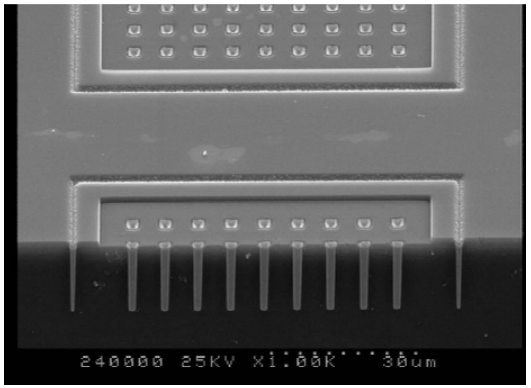
Current status

- Blind vias etched from front side of the FE-I3 Wafers









- Via isolation and Tungsten plug done
- Vias connected to I/O and Power on front side (Al)

Next steps on schedule:

- Cu electro-plating on front for SLID
- Mount to handle wafer, back-thin to expose vias from back
- Back side metallization in December

- SLID to pixel sensors in January 2013

Fraunhofer EMFT