Operation of DEPFET in gated mode for Belle II

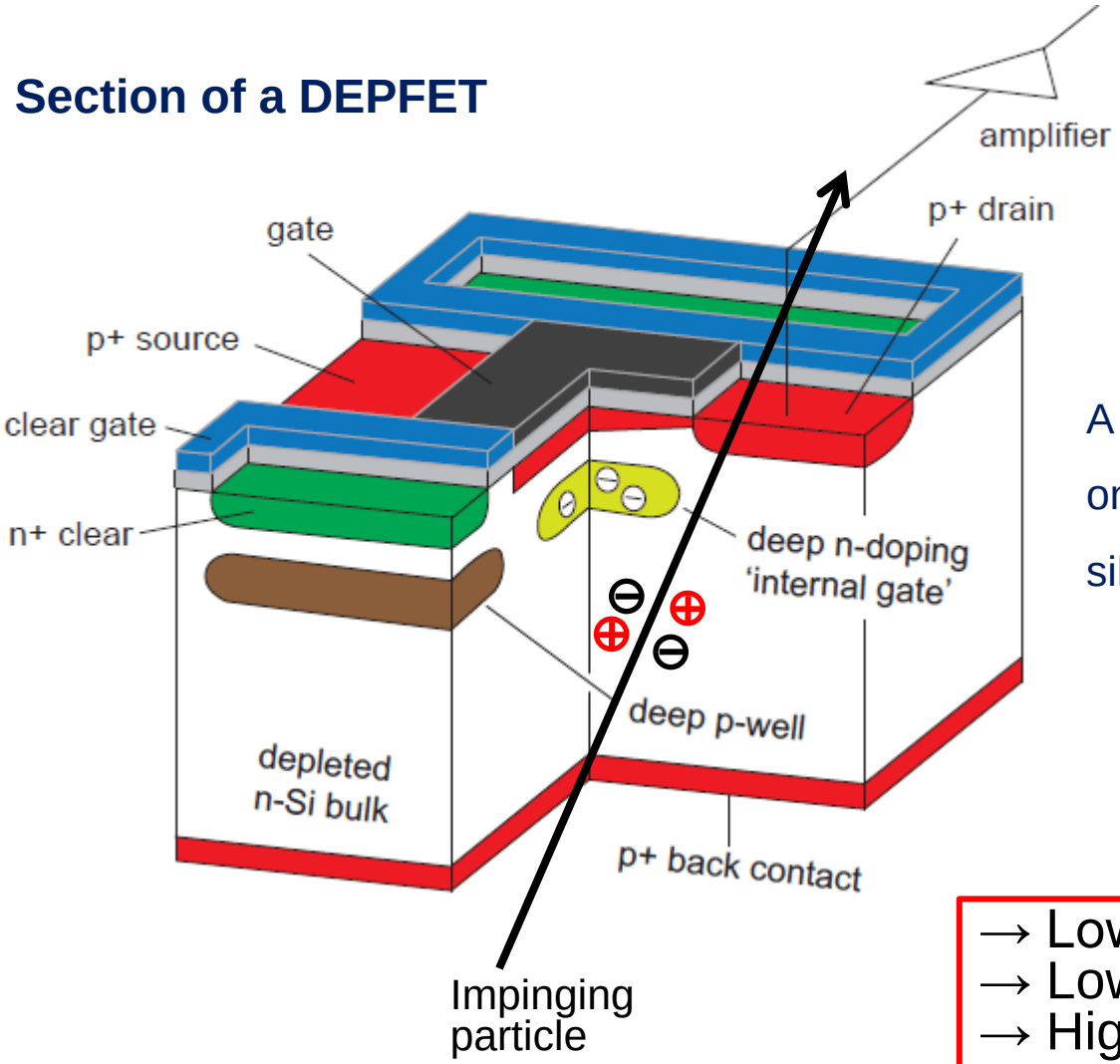
Theory and experimental results with
PXD6 matrices and the Mini-Matrix setup

Outline

1) DEPFET (DEPleted p-channel Field Effect Transistor)
   a) Signal of a single DEPFET pixel
   b) DEPFET used as a particle detector
2) Theory of gated-mode
   a) Motivation
   b) Within the sensor – what is needed?
   c) Theory & Simulations
3) Measurements
   a) Lab setup – Laser impinging onto the DEPFET matrix
   b) Operation window
   c) Junk charge generation
   d) Suppressed Clear
4) Summary

DEPFET – DEPleted p-channel Field Effect Transistor

Cross Section of a DEPFET



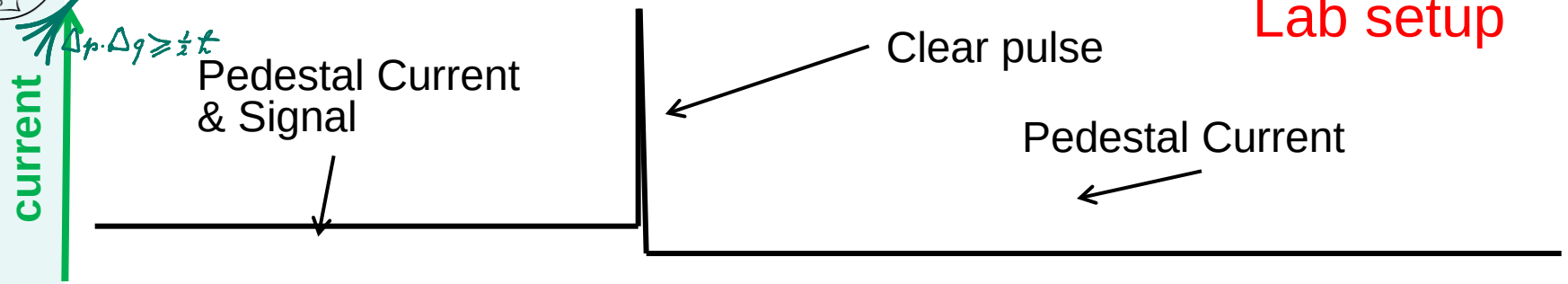
A DEPFET is a MOSFET onto a sideward depleted silicon bulk

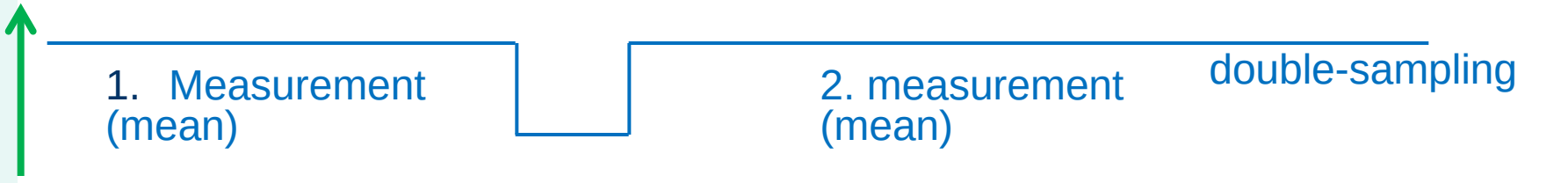
→ Low noise
→ Low power
→ High signal/noise-ratio

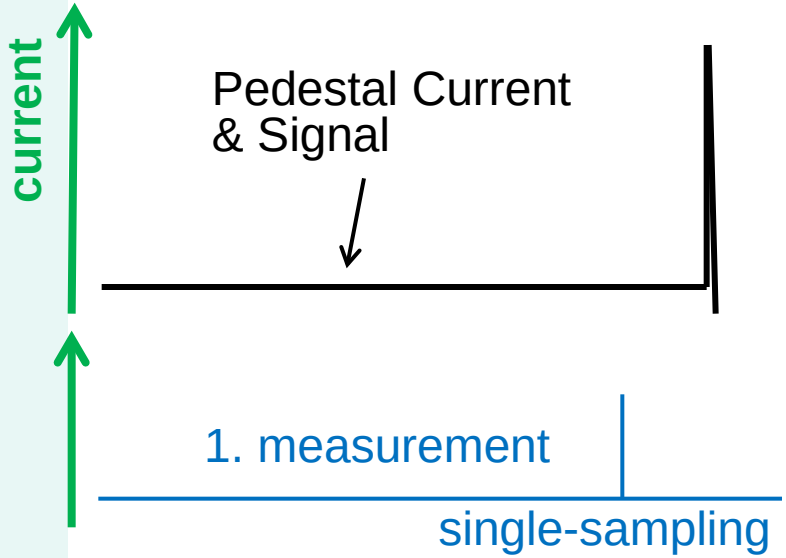
Source: Gerhard Lutz, Semiconductor Radiation Detectors

Signal of one pixel

Lab setup







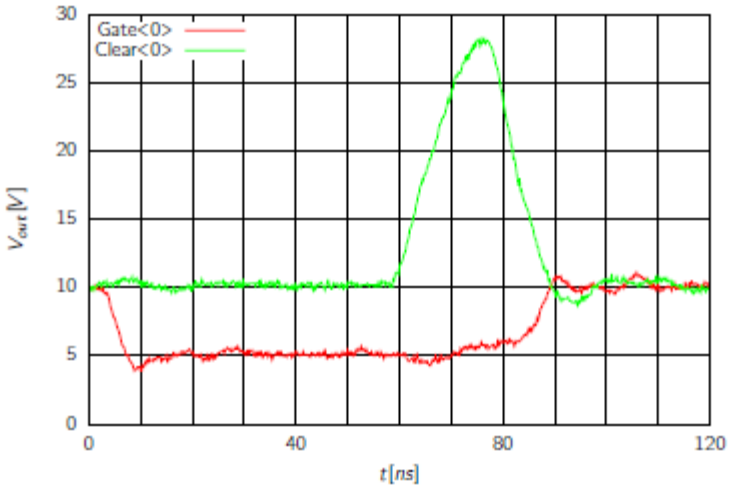
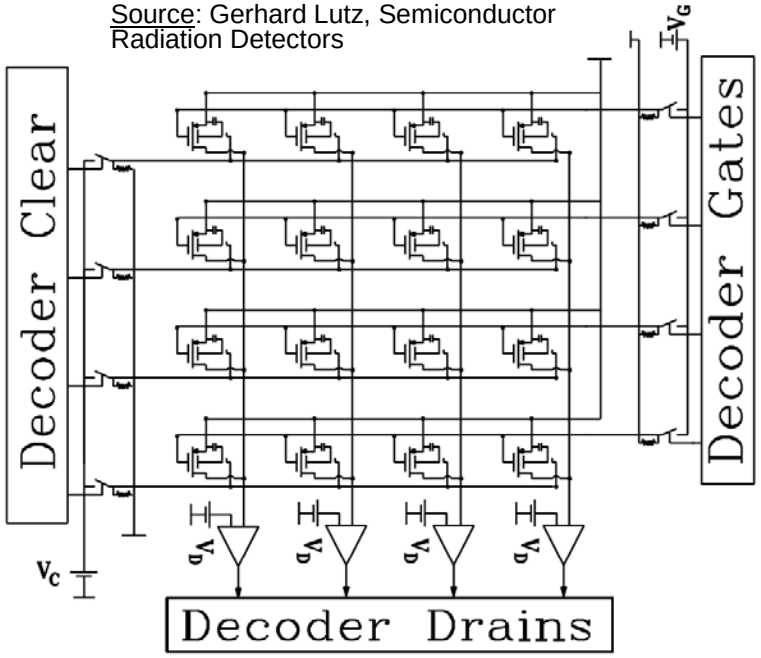
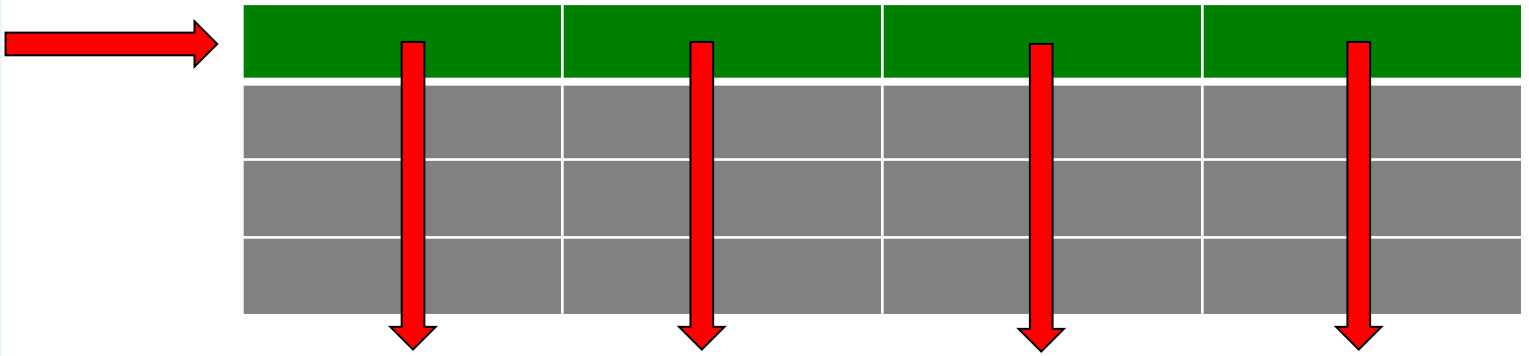


Figure 4.8: Single sampling scheme with 80ns timing 90pF load, $V_{GateHi} = 10V$, $V_{GateLo} = 5V$, $V_{ClearHi} = 27V$ and $V_{ClearLo} = 10V$. Source: SwitcherB (v2) Reference Manual

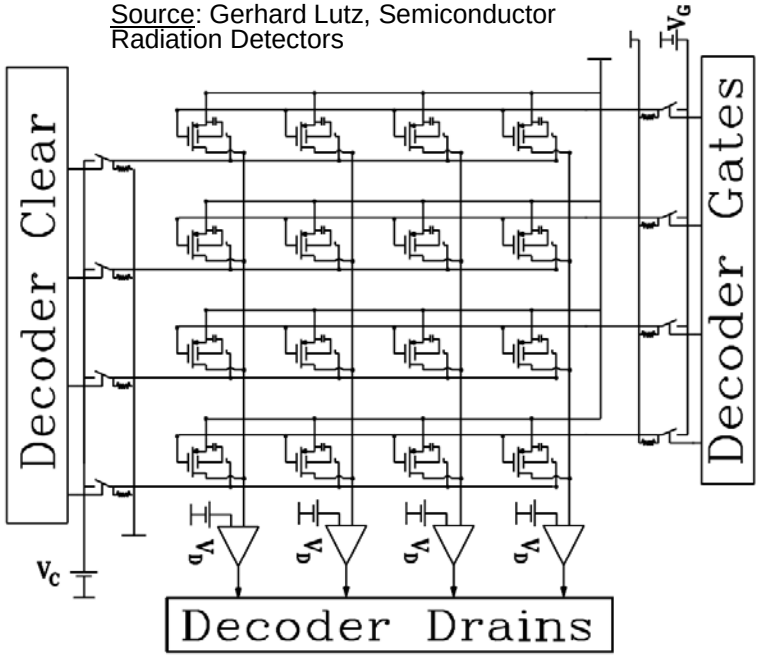
DEPFETs as detector



- DEPFETs are arranged in a matrix
- Rows are switched on successively in order to read-out the signal.



DEPFETs as detector



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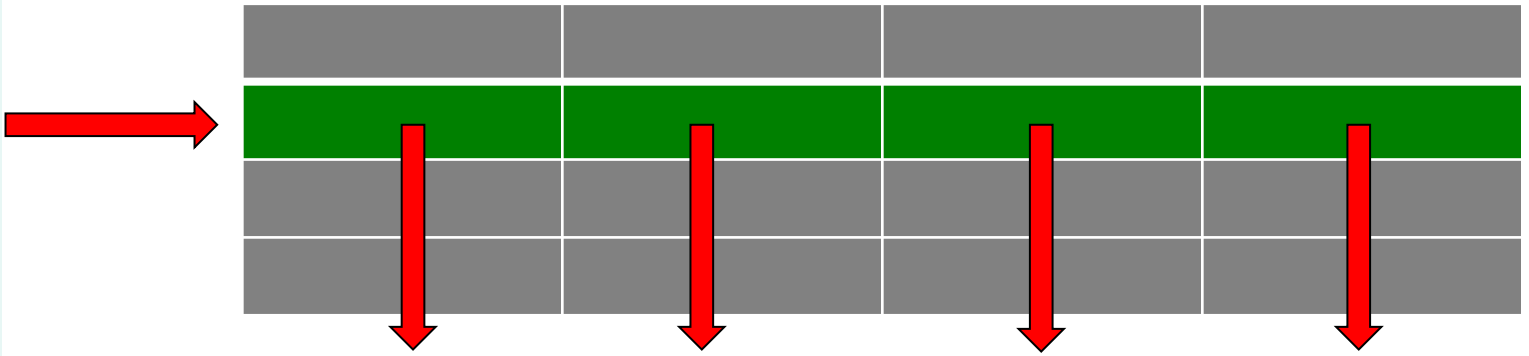
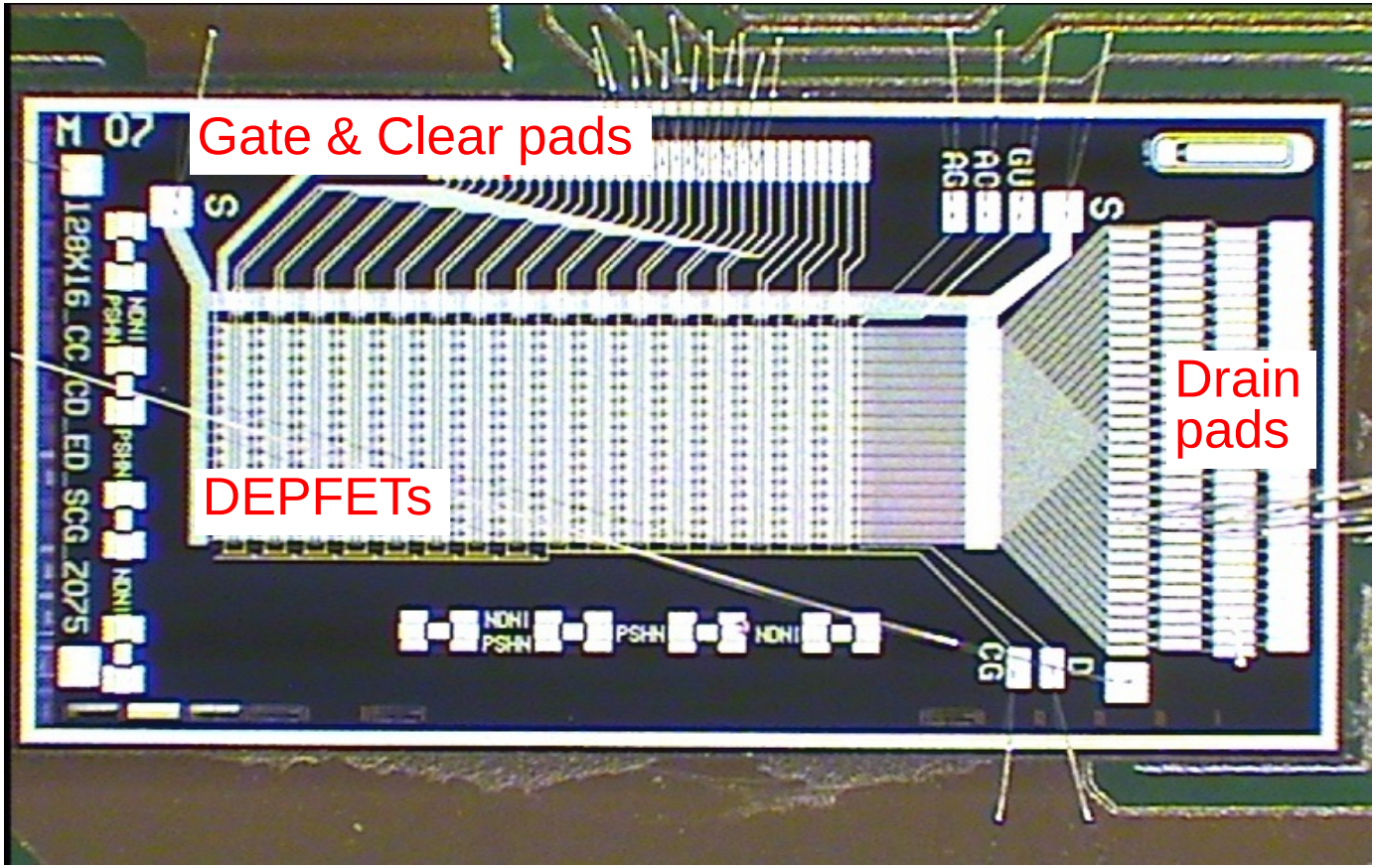
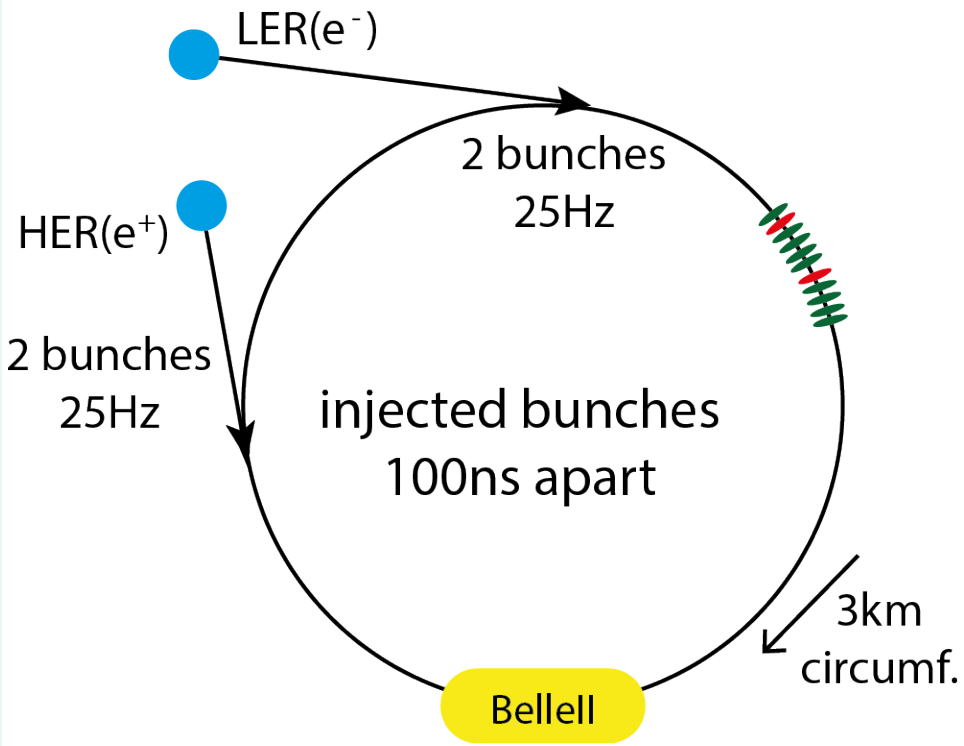


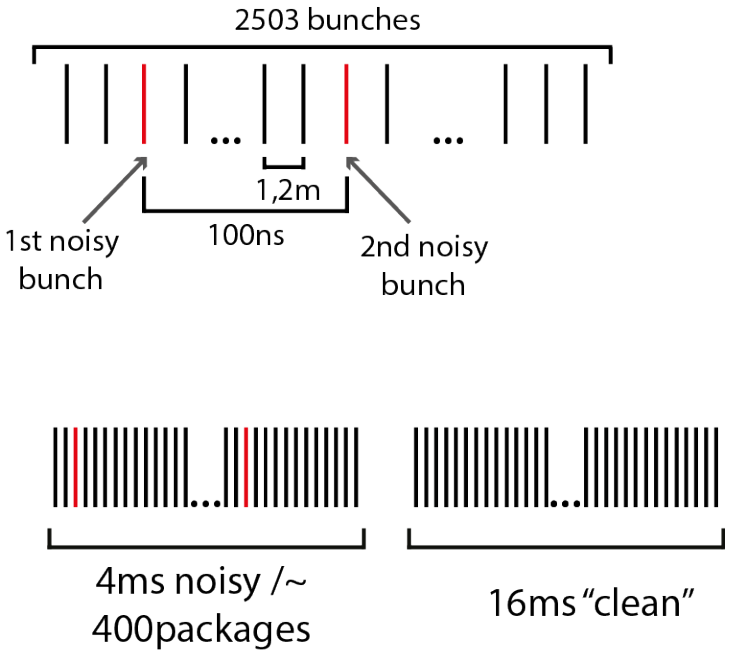
DEPFETs as detector



6 rows and 8 columns are connected (circuit design)
corresponding to
24 rows and 2 columns (geometrically design)

Motivation for gated-mode





4ms for cooling mechanism

⇒ Loss of particles (‚noisy particles')

Within the sensor - what is needed?

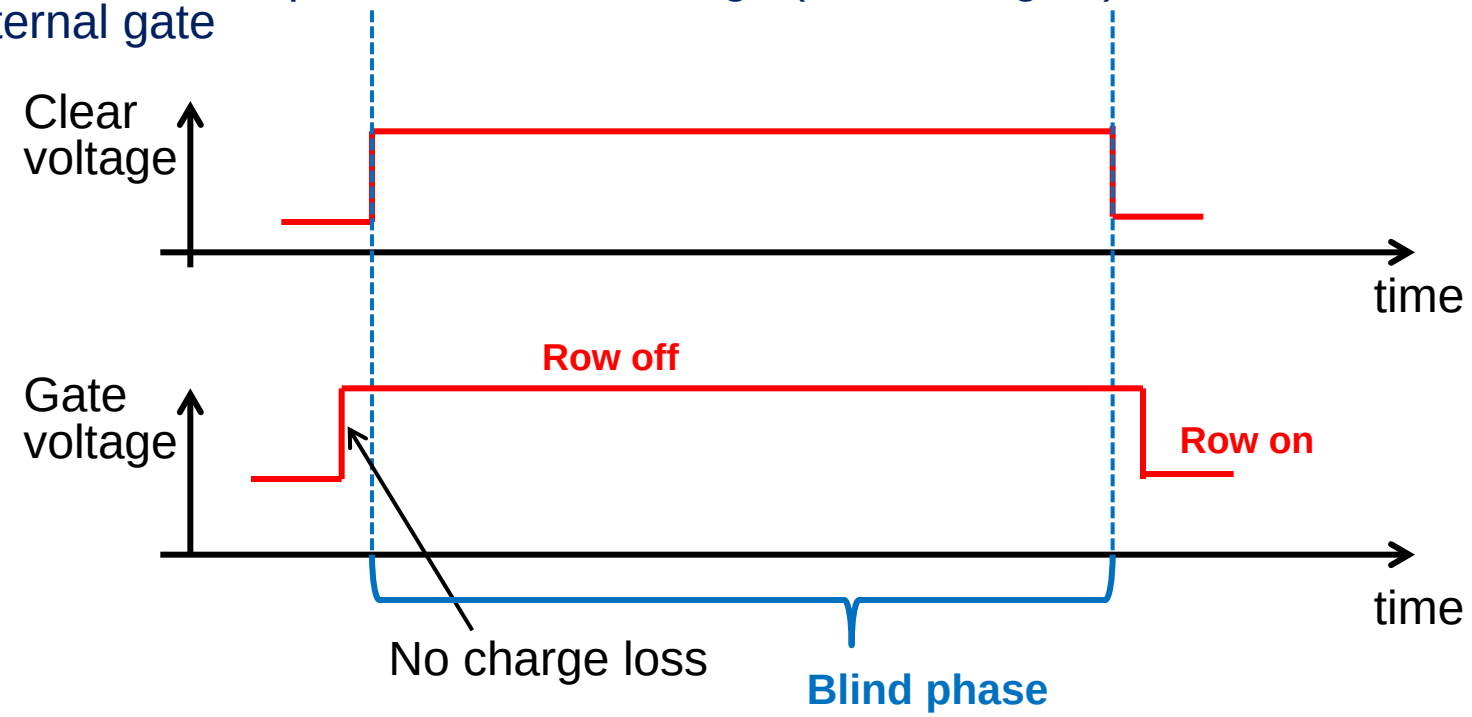
Ideal situation:

Electron-hole pairs are generated when the ‘noisy’ bunches hit the detector

⇒ These electrons should not drift to the internal gate, but should be diverted to the clear contact by applying the clear potential

Consequently, no additional charge is stored in the internal gate

Meanwhile, the previous stored charge (the real signal) should remain in the internal gate



Within the sensor - what is needed?

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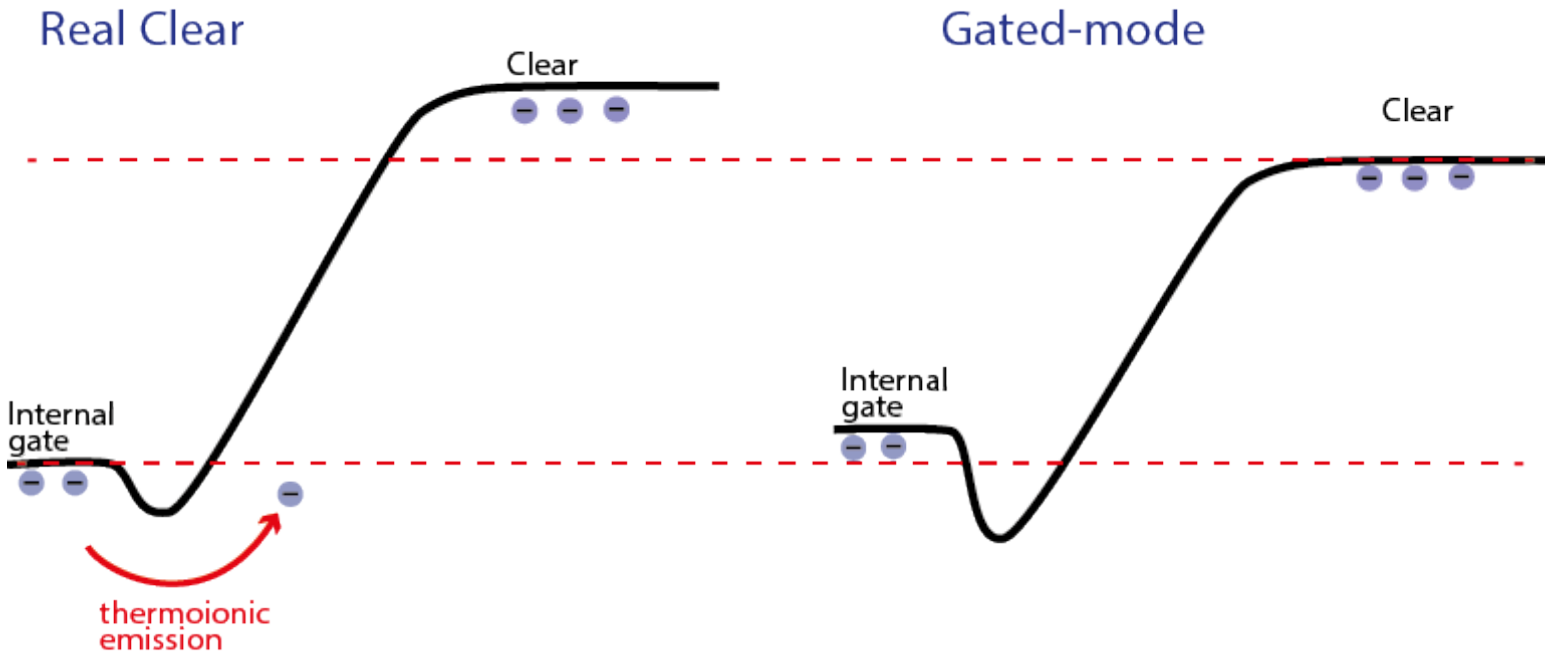
Real situation:

Two aspects (detector related) have to be considered:

1) To which degree can we protect charge in the internal gate from being cleared?

2) How much of the chunk charge will arrive in the internal gate?

‘Real Clear‘ and ‘Suppressed Clear‘ mechanism



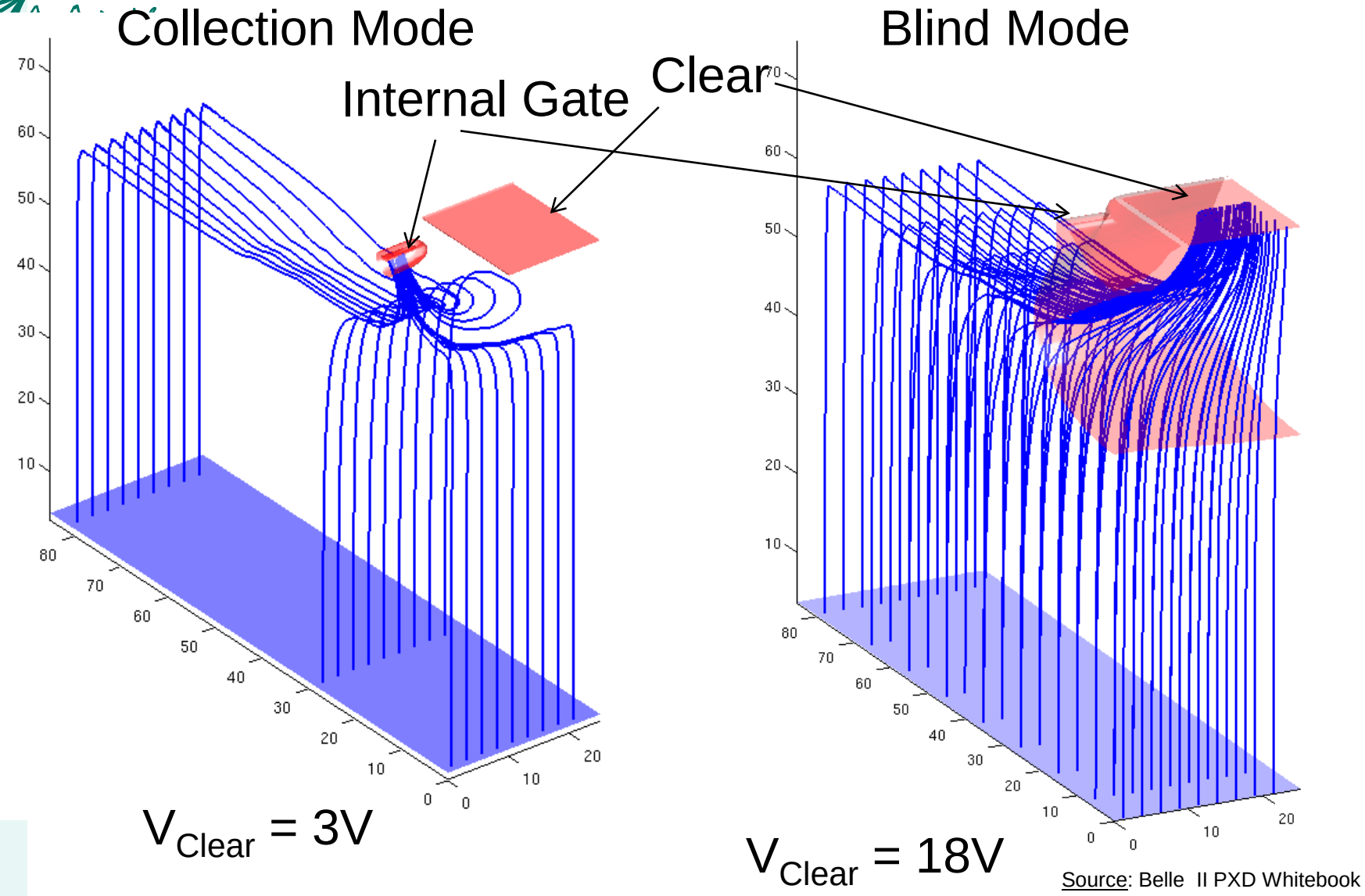
GateLow (FET on)

ClearHigh

GateHigh (FET off)

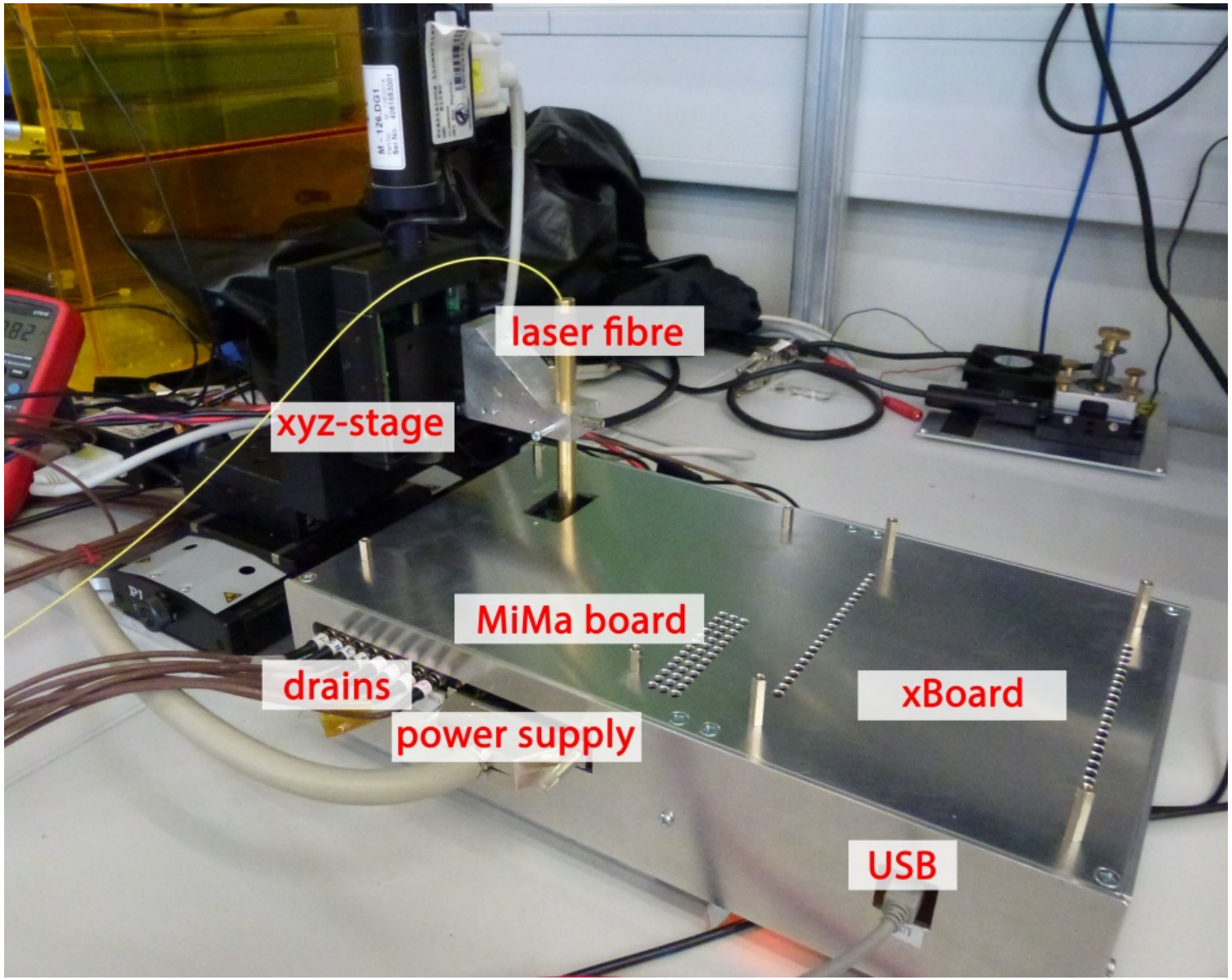
ClearHigh

Simulations – trajectories of electrons

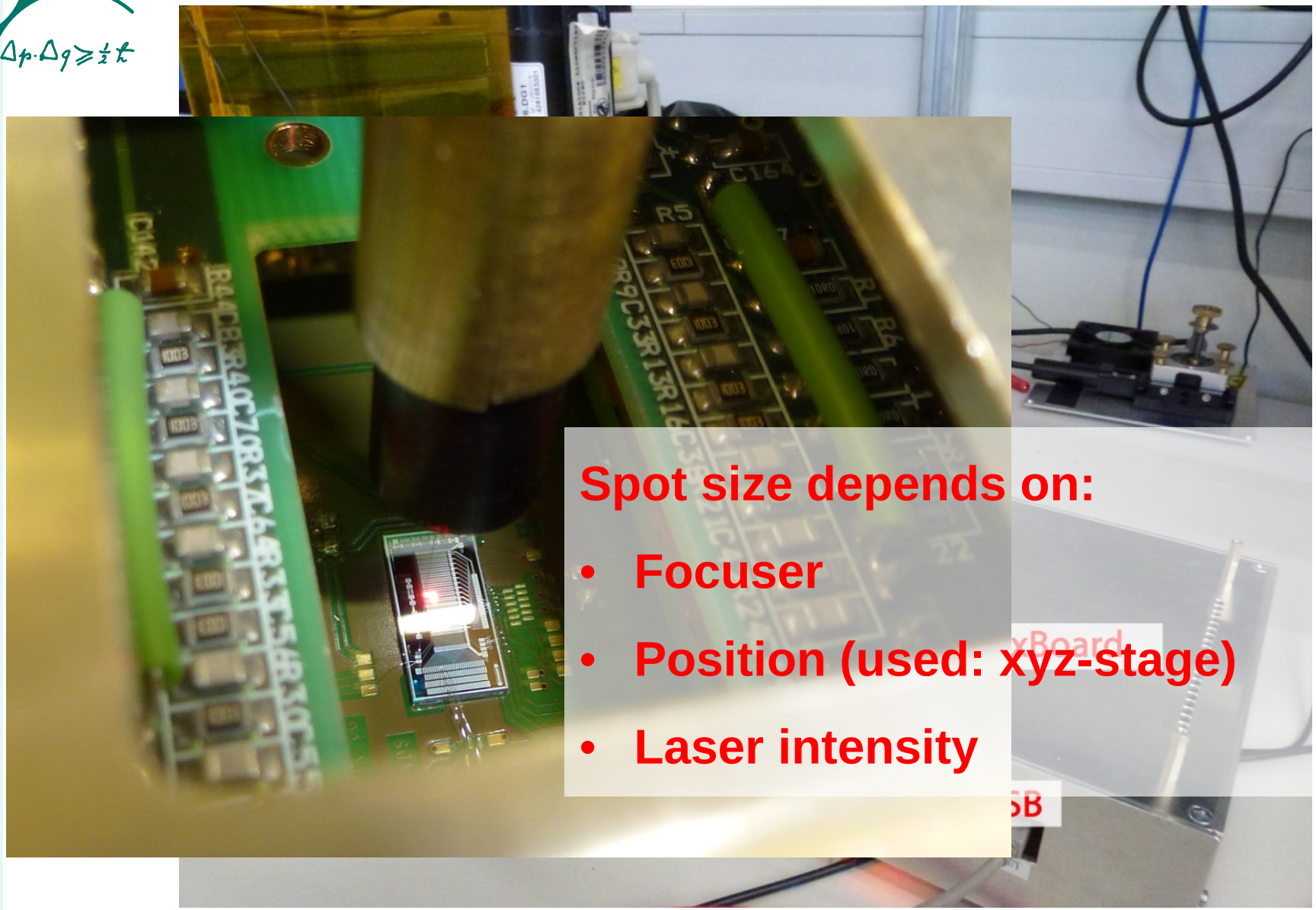


Source: Belle II PXD Whitebook

Lab setup – Laser impinging onto the DEPFETs



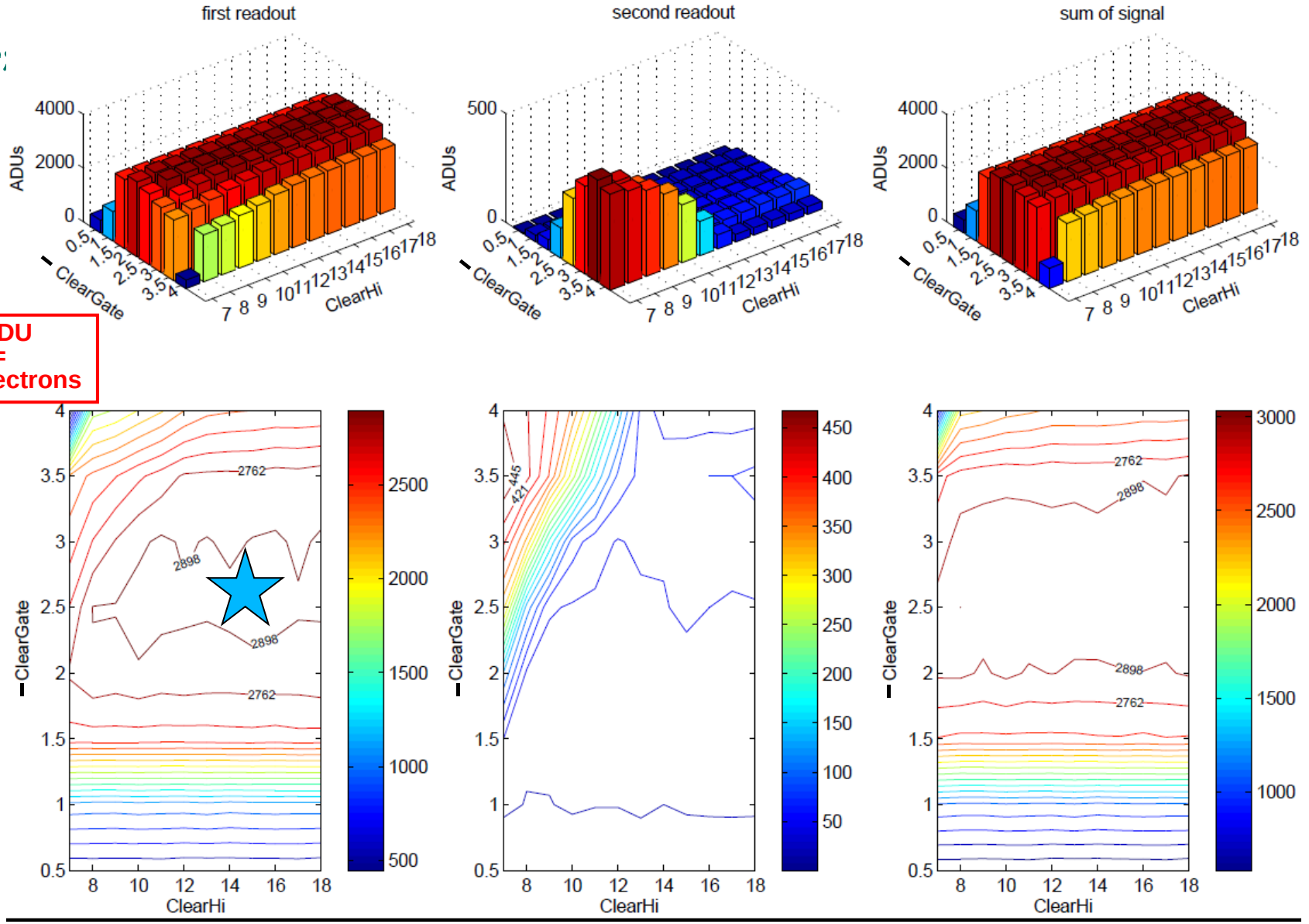
Laser impinging onto the DEPFET detector



Spot size depends on:

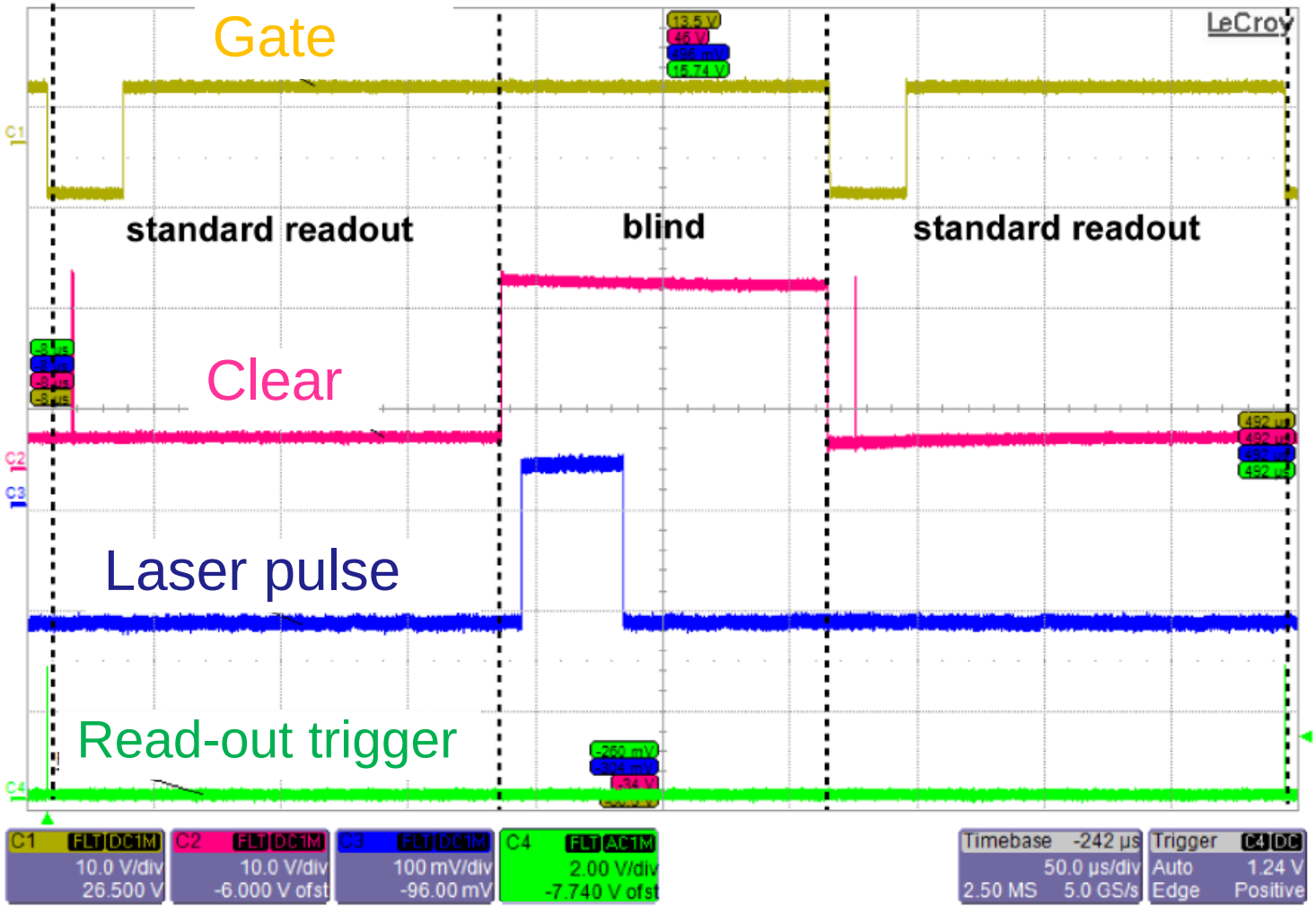
- **Focuser**
- **Position (used: xyz-stage)**
- **Laser intensity**

Determining the operation window (ClearGate & ClearHigh)

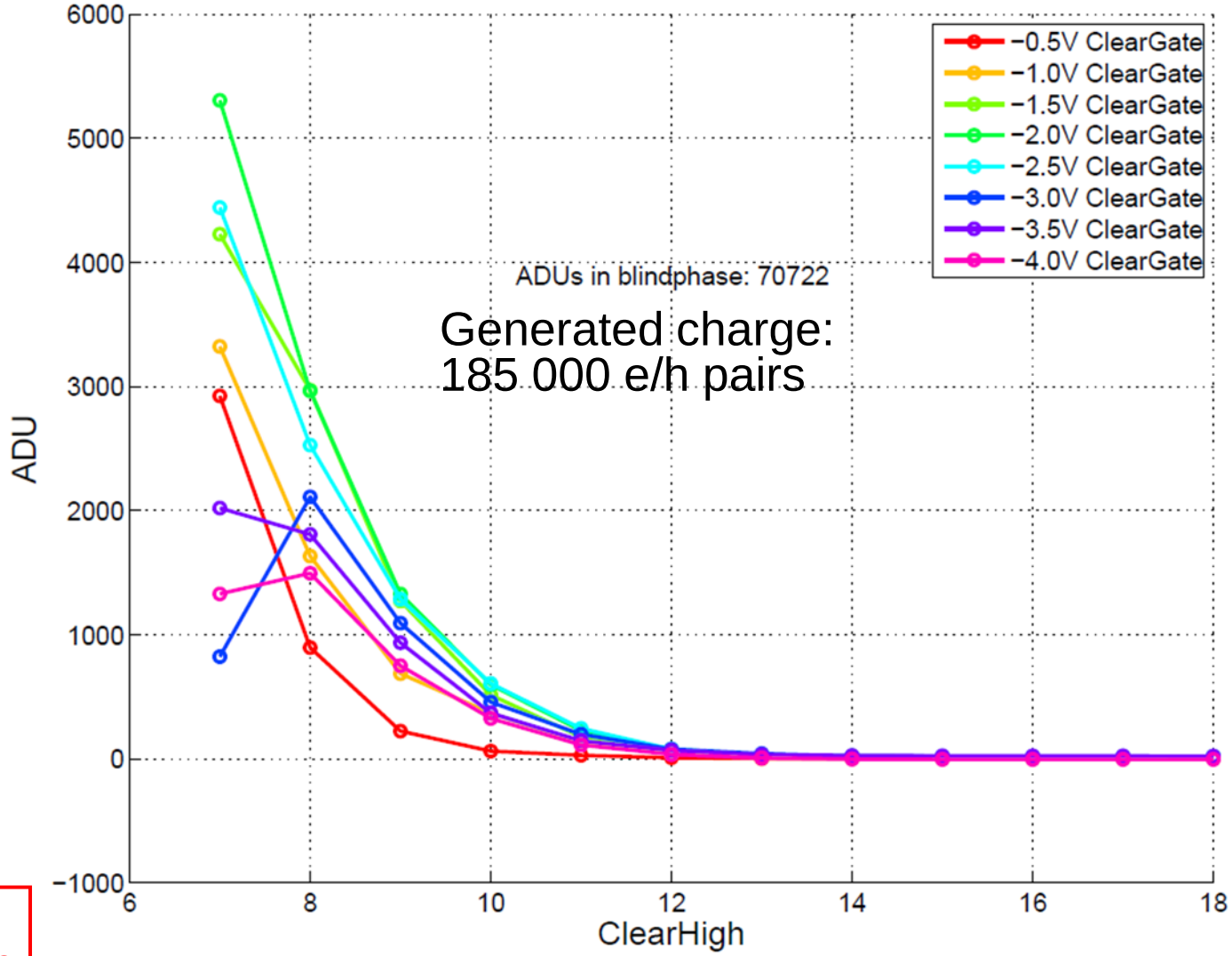


Generation of Junk Charge

Voltages for one row of the DEPFET matrix

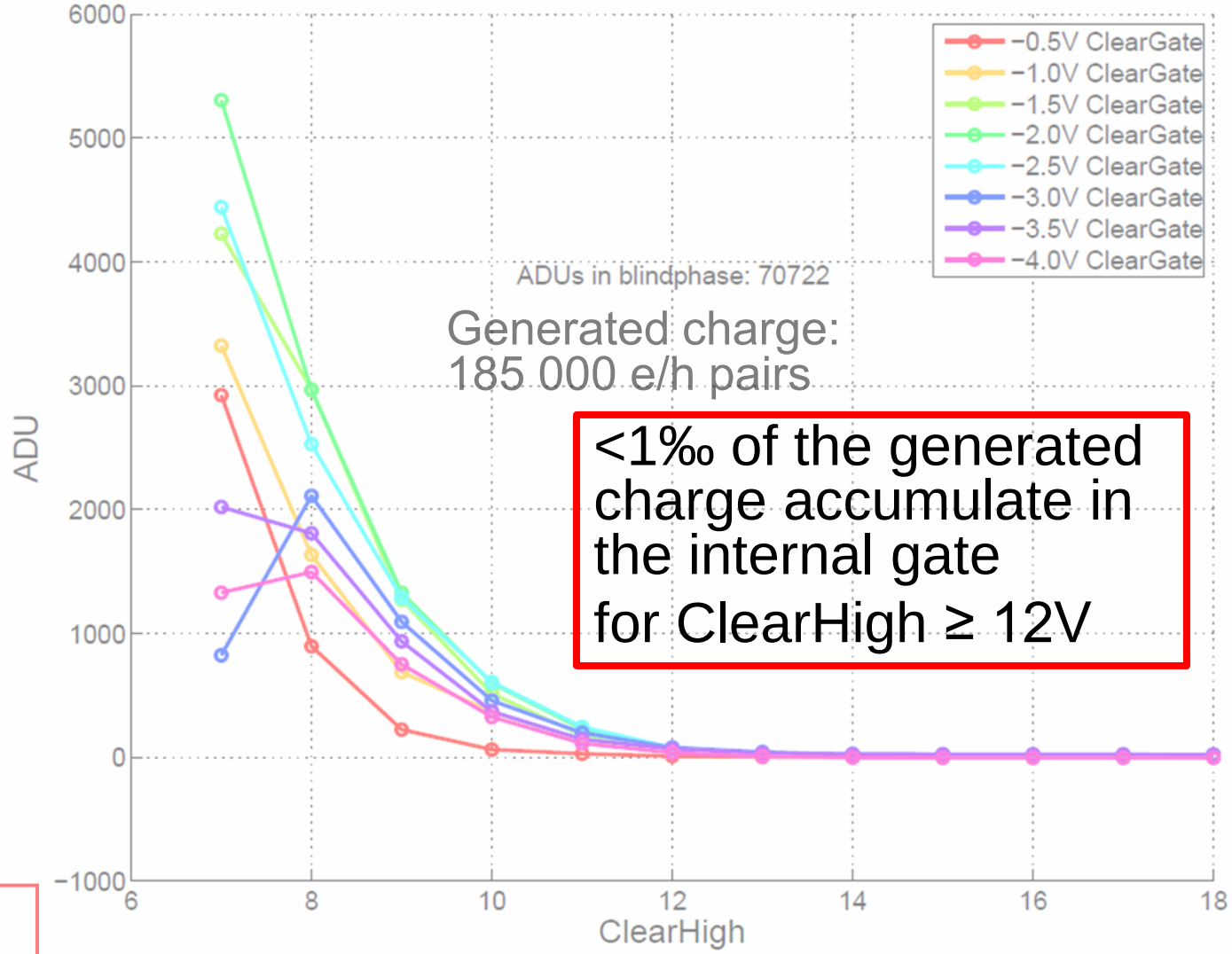


Generation of Junk Charge – ClearGate dependence



1ADU = 2.61 electrons

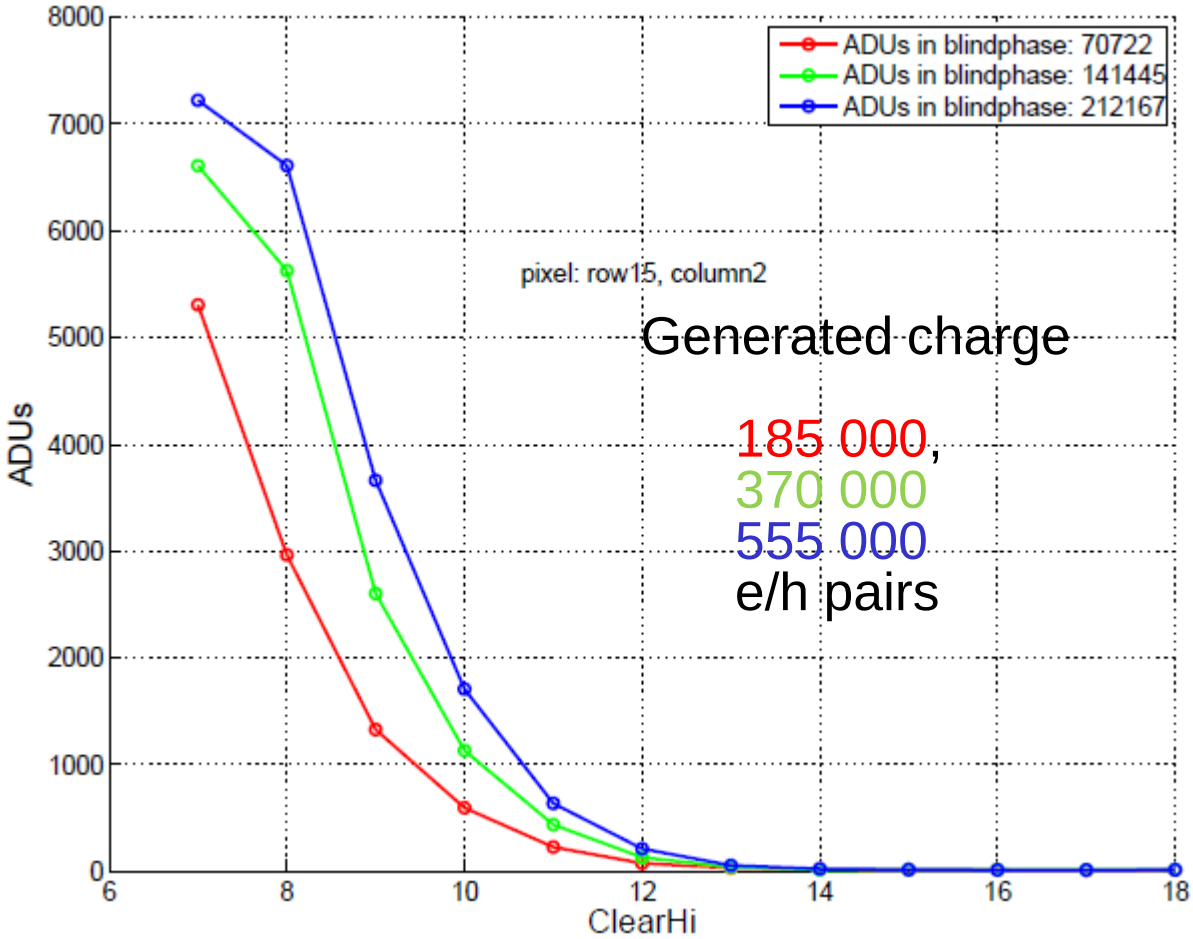
Generation of Junk Charge – ClearGate dependence



<1‰ of the generated charge accumulate in the internal gate for ClearHigh ≥ 12V

1ADU = 2.61 electrons

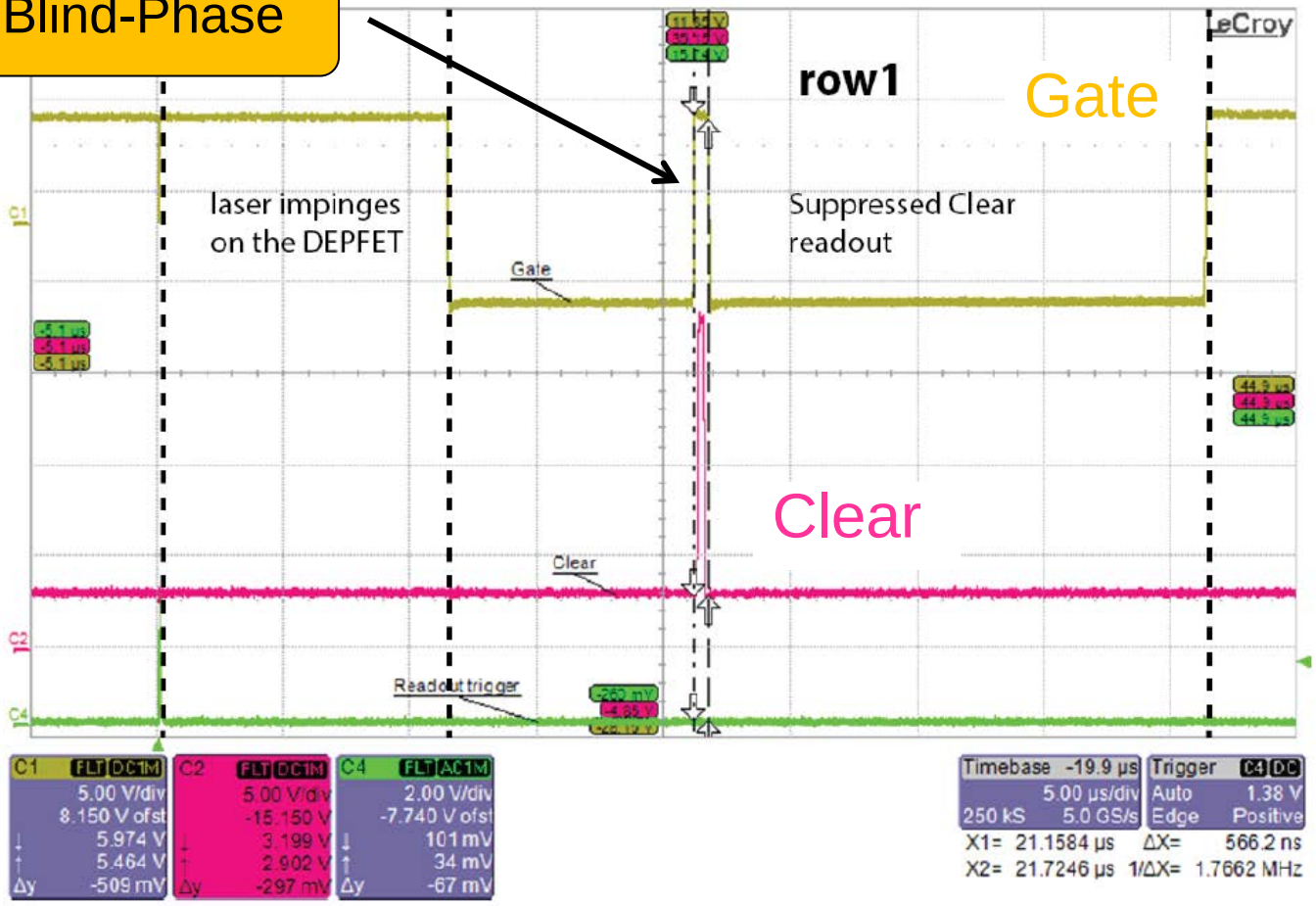
Generation of Junk Charge – Laser intensity dependence



1ADU = 2.61 electrons

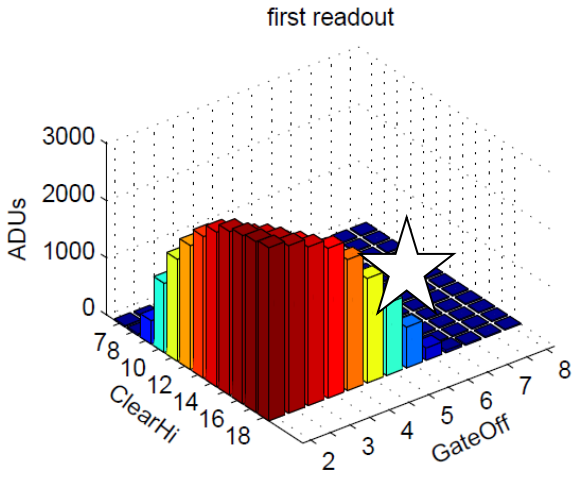
Suppressed Clear

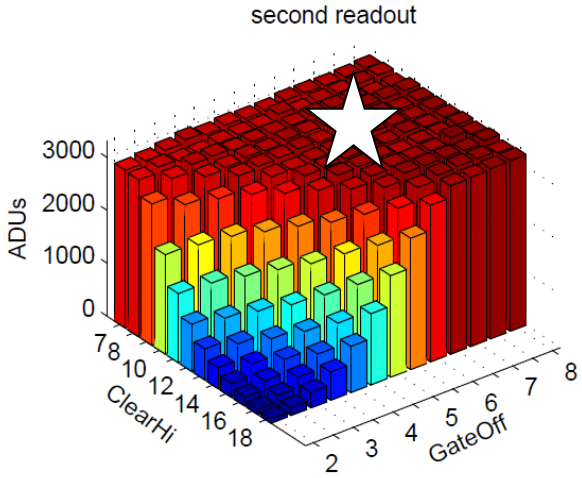
Blind-Phase

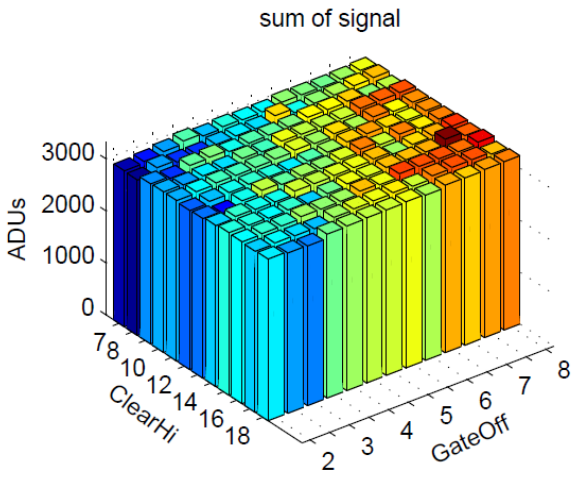


1) Laser impinges onto DEPFET
2) Gated-mode operation
3) Standard Readout

Suppressed Clear







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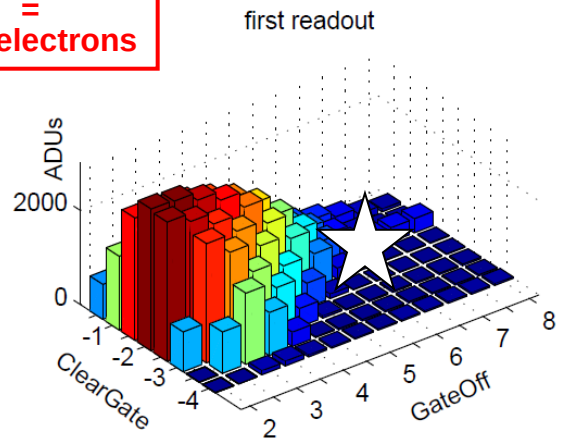
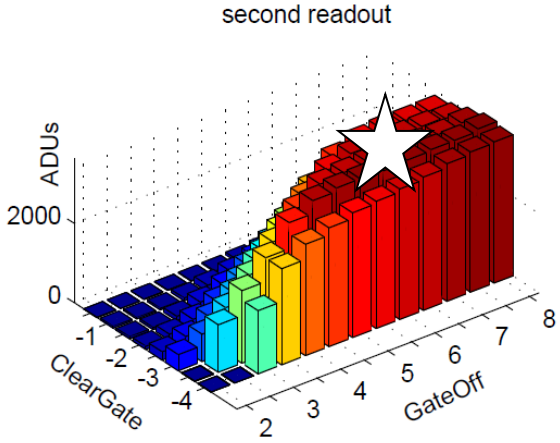
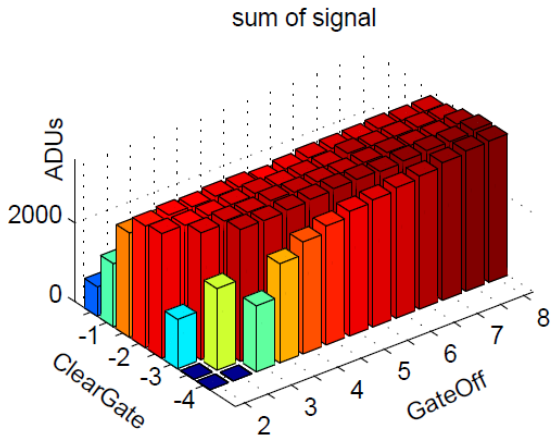
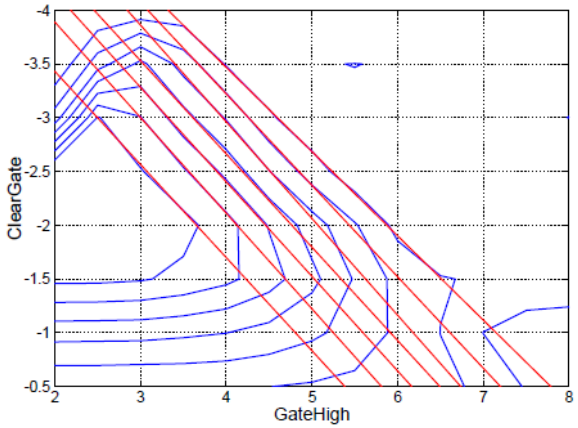




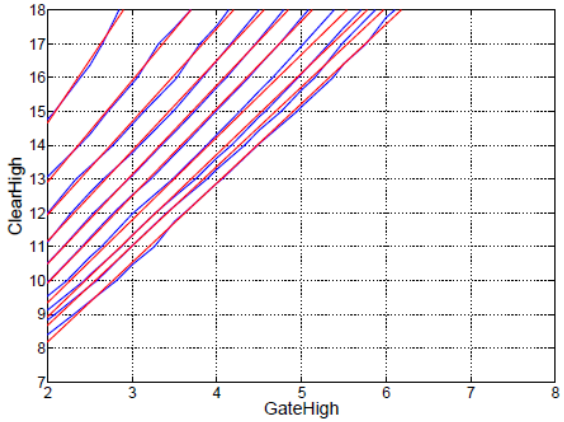


Suppressed Clear

Gated-mode

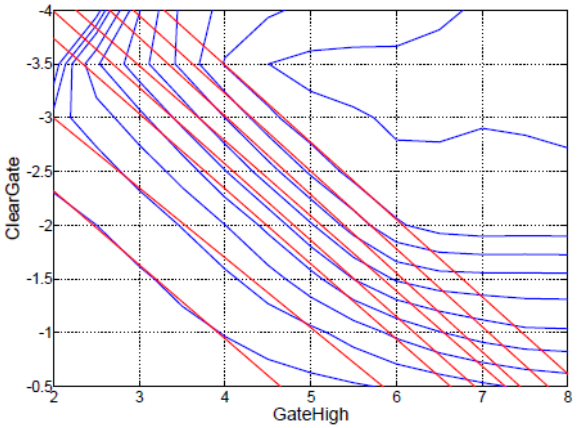


(a) Suppressed Clear: Coupling constant $0.8620 \frac{\text{ClearGate}}{\text{GateHigh}}$

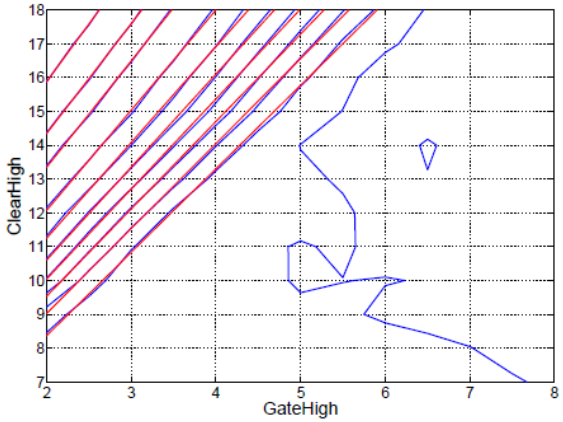


(b) Suppressed Clear: Coupling constant $2.6941 \frac{\text{ClearHigh}}{\text{GateHigh}}$

Normal operation



(c) Real Clear: Coupling constant $0.7017 \frac{\text{ClearGate}}{\text{GateHigh}}$



(d) Real Clear: Coupling constant $2.8591 \frac{\text{ClearHigh}}{\text{GateHigh}}$

Summary

- Gated mode works properly
- Results are in good agreement with simulations carried out by R. Richter (HLL) and measure-ments done by J. Scheirich (Prague) using the same setup but different analysis tools
- Another experimental setup shows similar behavior in test beams (DESY)
- ASICs for Belle II detector are modified in order to operate in the gated-mode
- Outlook: Study gated mode for long matrices (large Clear capacitance could harm)

Thank you

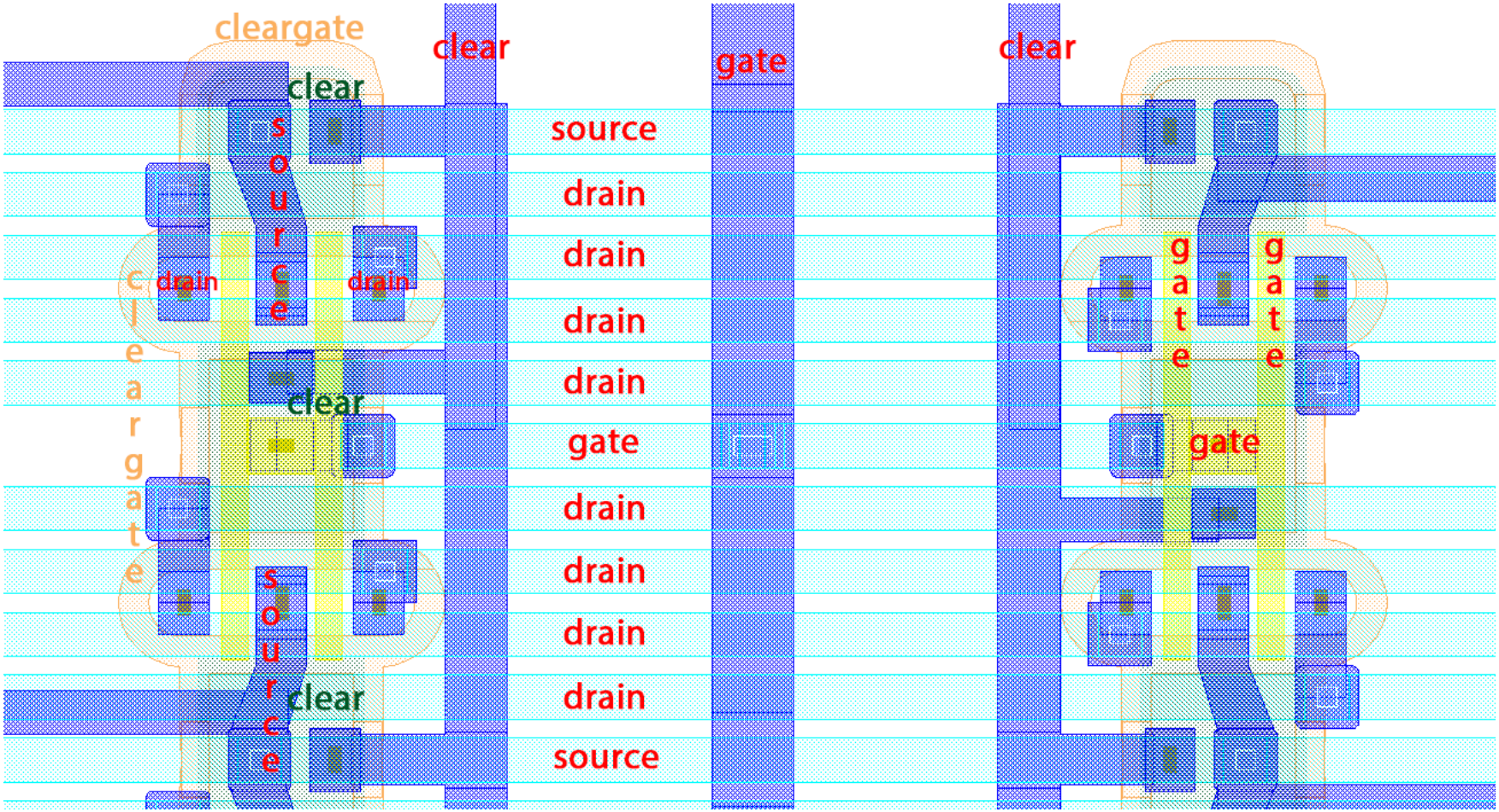
for your attention

Backup

Backup slides

- PXD6 Layout
- PXD arrangement for Belle II
- Simulations (quanitative)
- Signal of a single pixel (Gated-mode and normal operation)
- Standard Readout sequence (Rolling Shutter mode)
- Read-out signal of a single column
- Schematic lab setup
- Laser impinging onto the DEPFET (detailed picture)
- Pedestal Meaurement
- Calibration using Fe55 radioactive source
- Laser impinging onto the DEPFET detector – signal
- Measurement of signal generated by a laser
- Generation of Junk Charge – High voltage dependence
- Impact of the signal with respect to the drain voltage
- System Aspects

PXD6 Layout


cleargate
clear
clear
gate
clear
source
drain
drain
drain
drain
drain
gate
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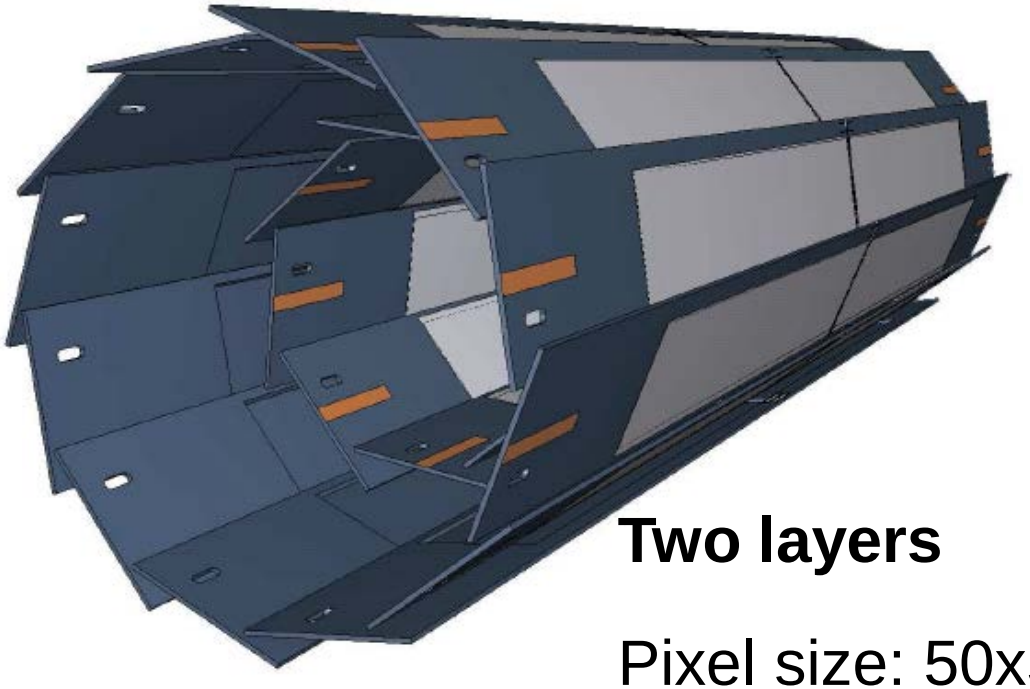
PXD arrangement for Belle II



Two layers

Pixel size: 50x50µm² and 50x75µm²
Thickness: 75µm

(for lab experiment: 50x75µm²
Thickness: 75µm)

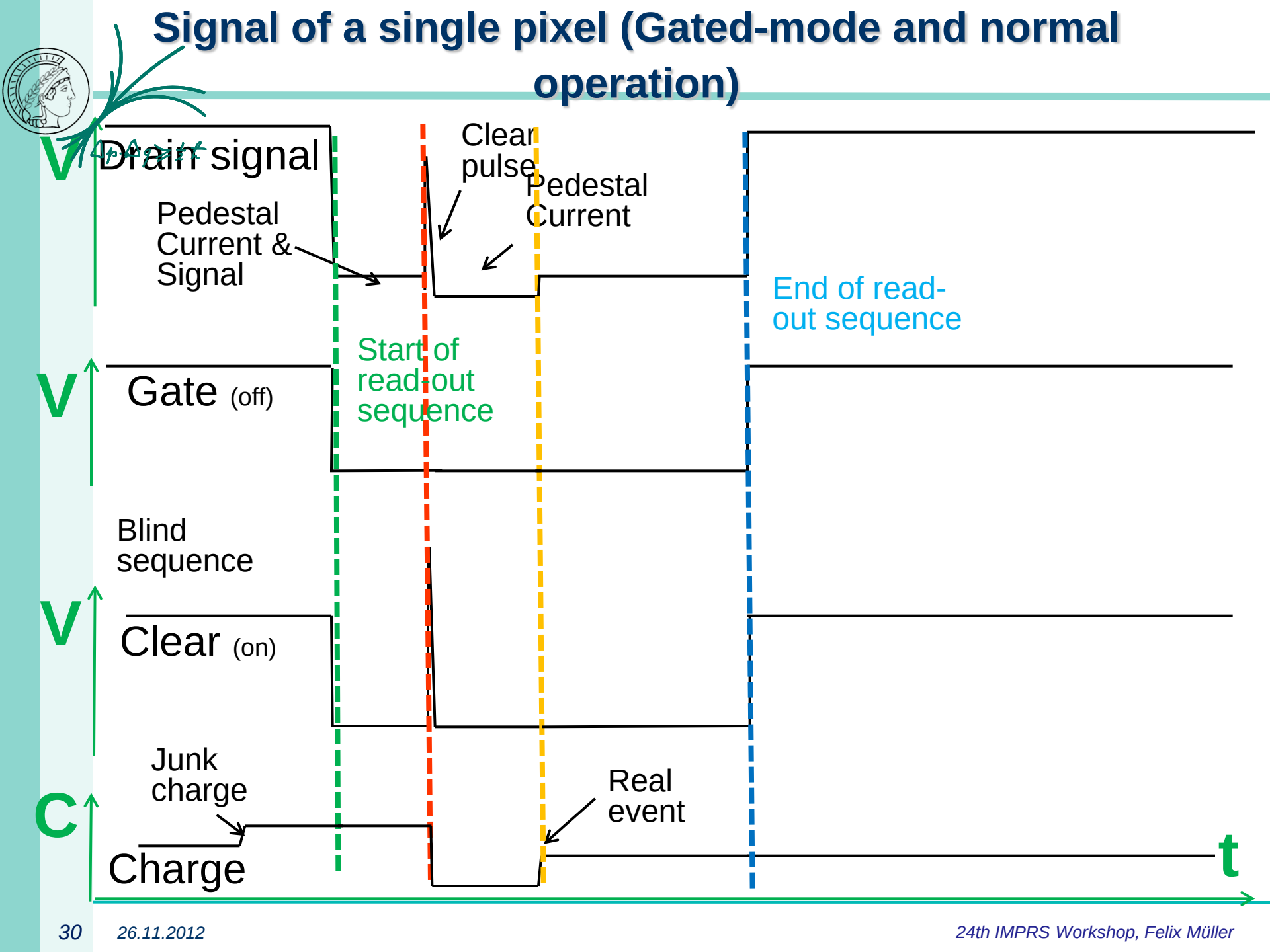
Source: Whitebook

Pixel in off state: Vgate = 5V

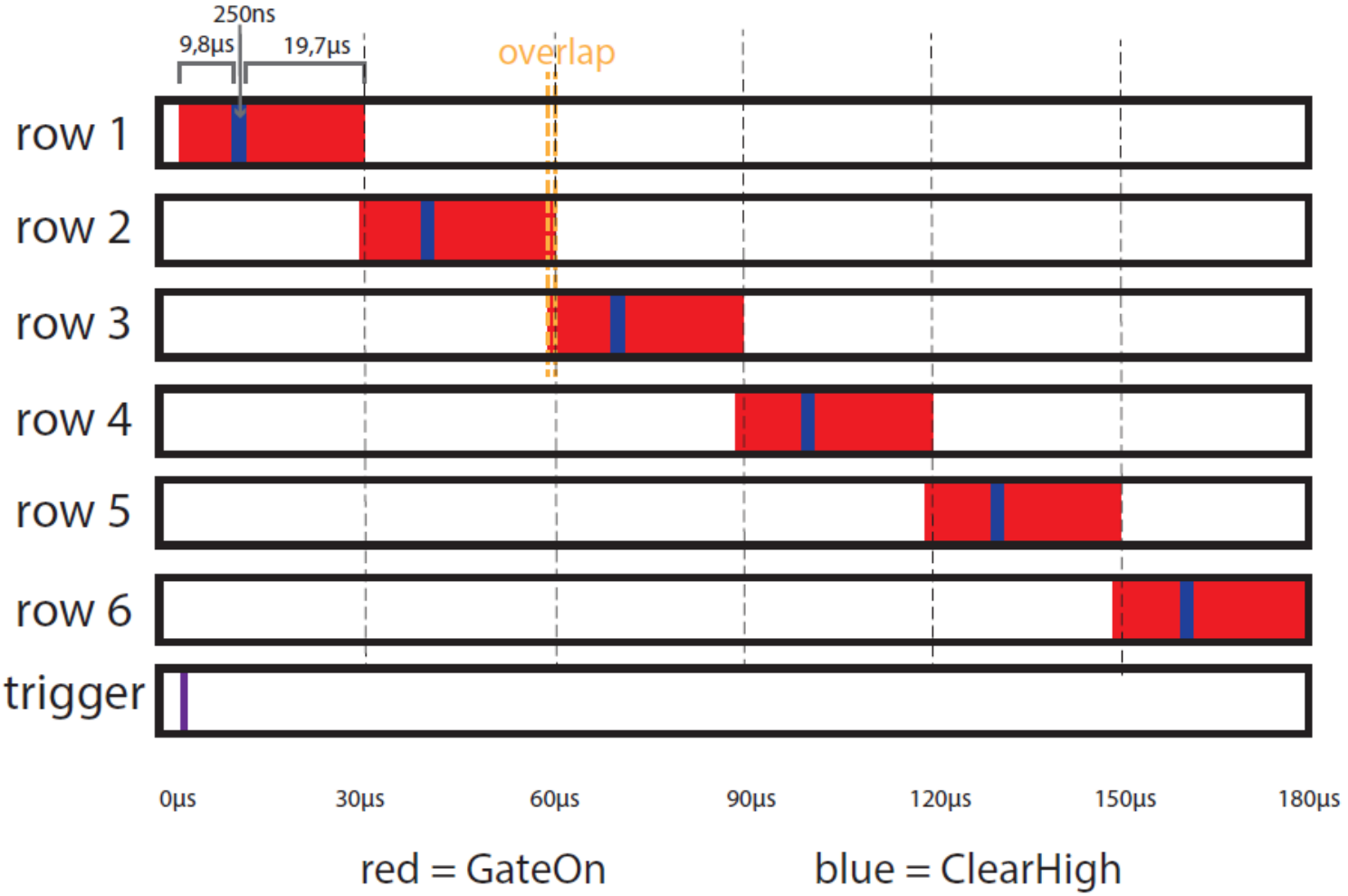
	Internal Gate protection during dump phase Number of electrons in the internal Gate if 10000 electrons are generated:			Signal Charge Protection 10000 electrons stored
Vclear	Beneath internal gate	Globally	Beneath clear	Number of signal electrons removed from the int. Gate
13V	4080	1300	120	3
16V	625	130	0	17
19V	450	90	0	64

Source: Rainer Richter

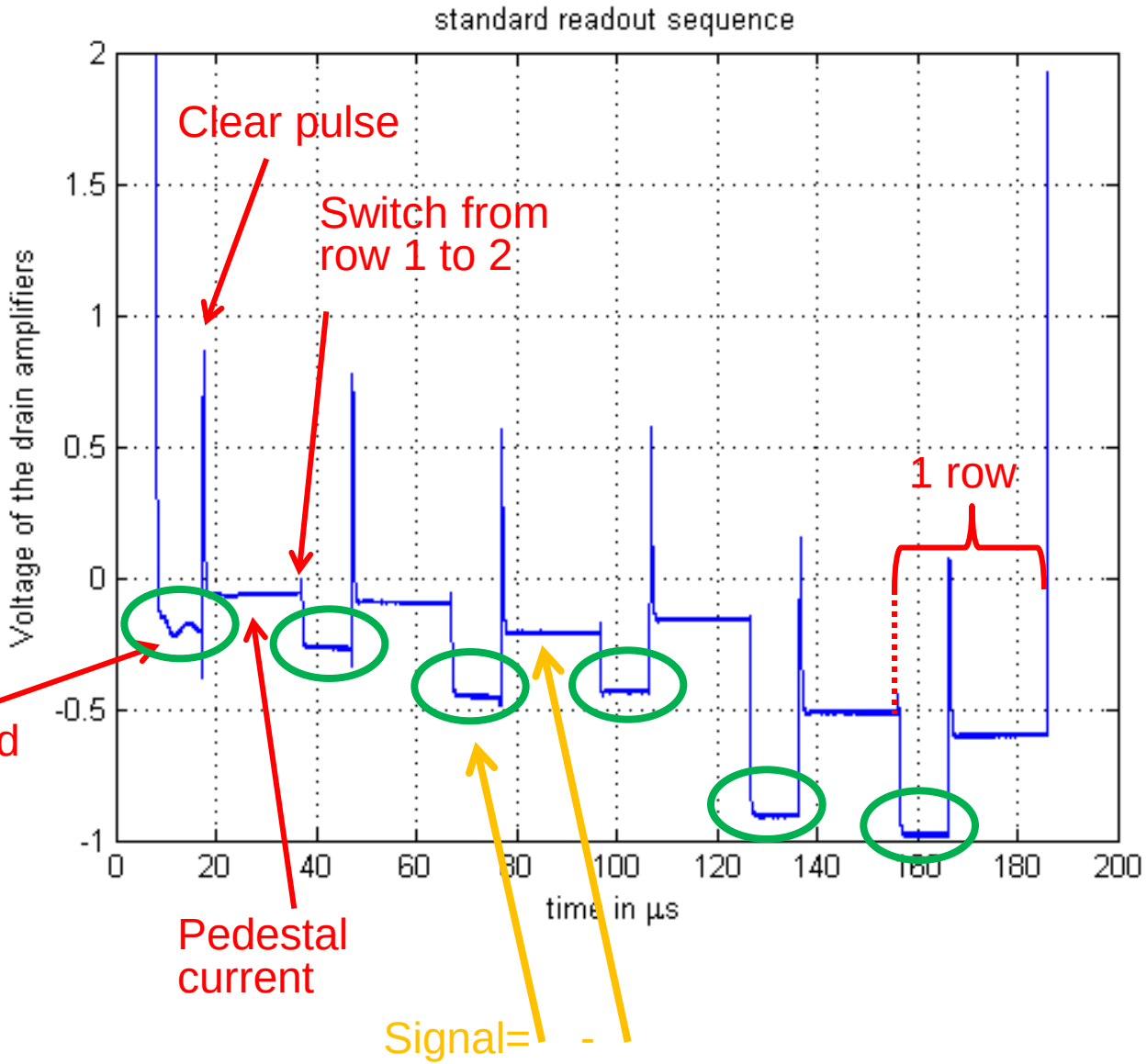
Signal of a single pixel (Gated-mode and normal operation)



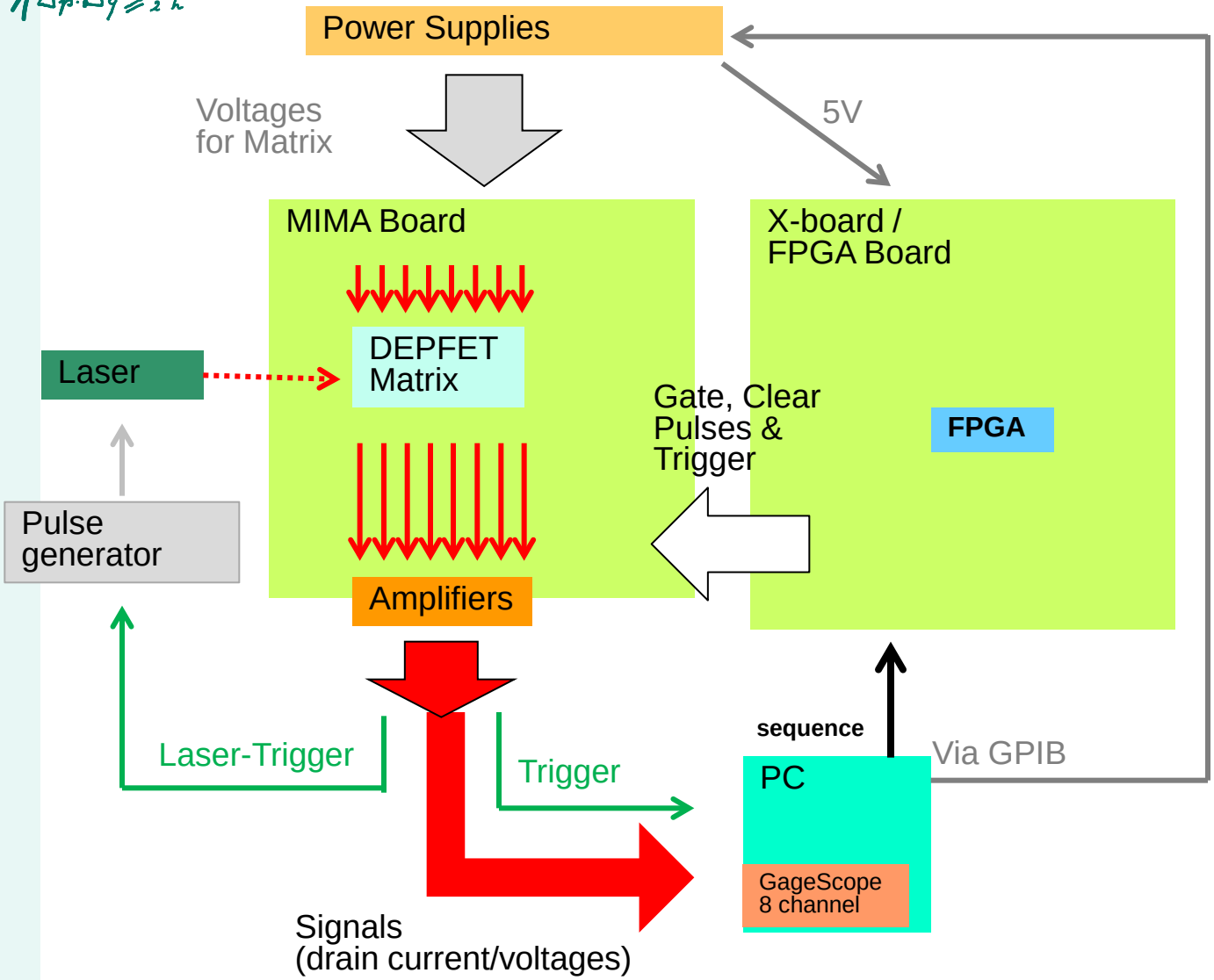
Standard Readout sequence (Rolling Shutter mode)



Read-out signal of a single column



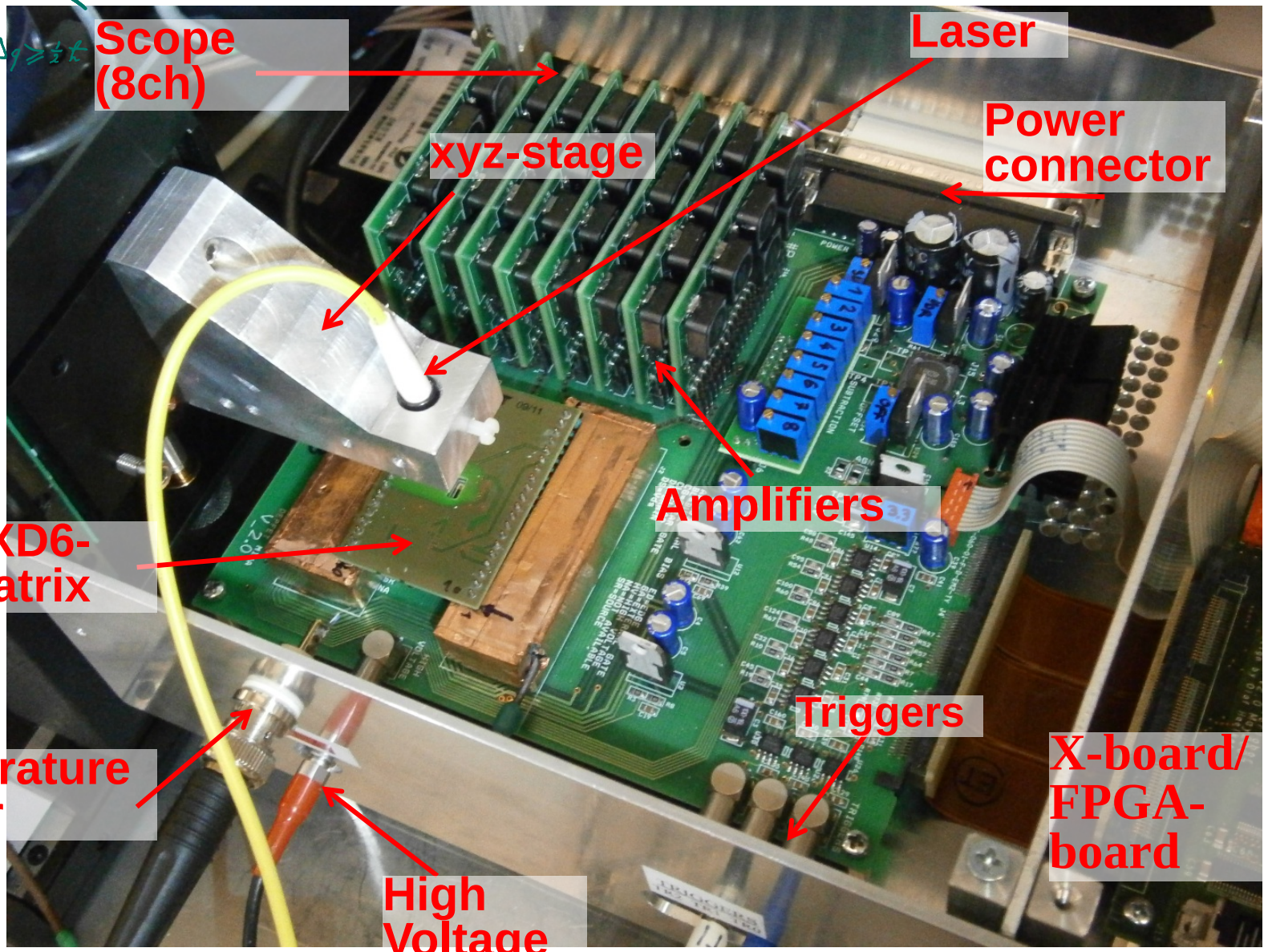
Schematic lab setup



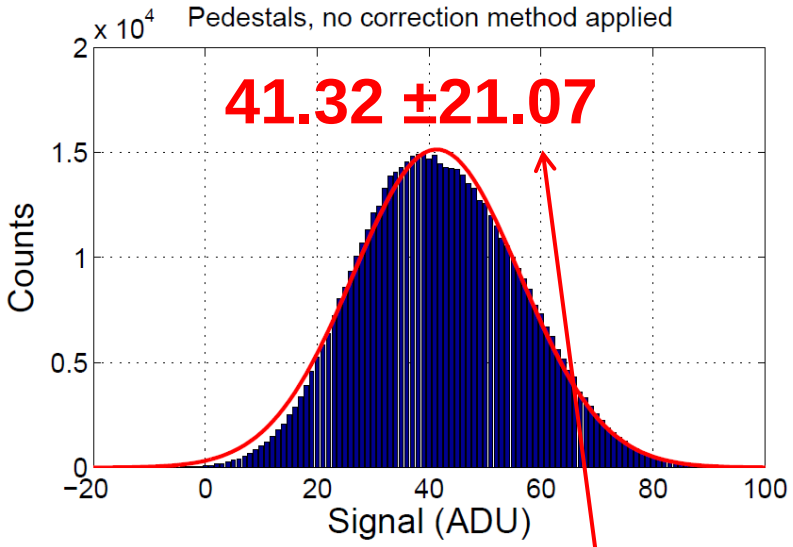
sequence

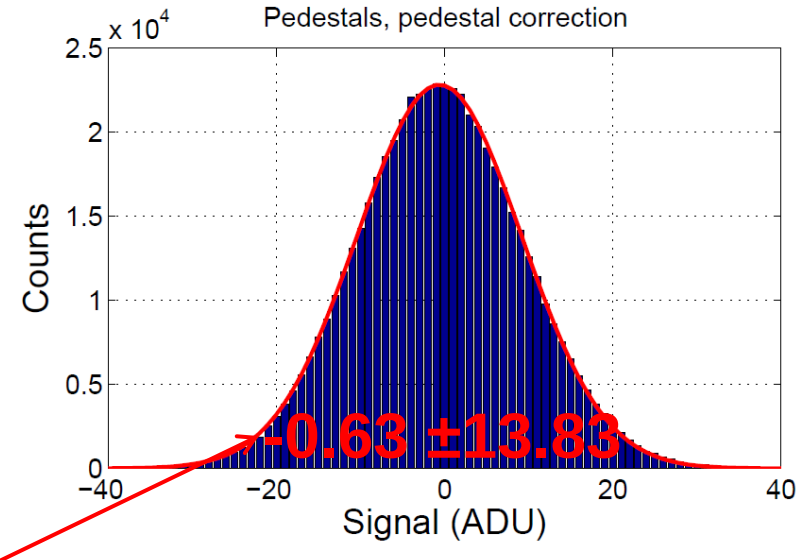
160	5	20	0	0	0	188
161	5	21	0	0	0	1023
162	5	22	0	0	0	275
163	5	23	1	0	0	33
164	5	24	0	0	0	1023
165	5	25	0	0	0	1023
166	5	26	0	0	0	553
167	5	27	0	1	1	0
168	6	0	0	0	0	0
169	6	1	0	0	0	1023
170	6	2	0	0	0	1023
171	6	3	0	0	0	1023

Laser impinging onto the DEPFET (detailed picture)



Pedestal measurements

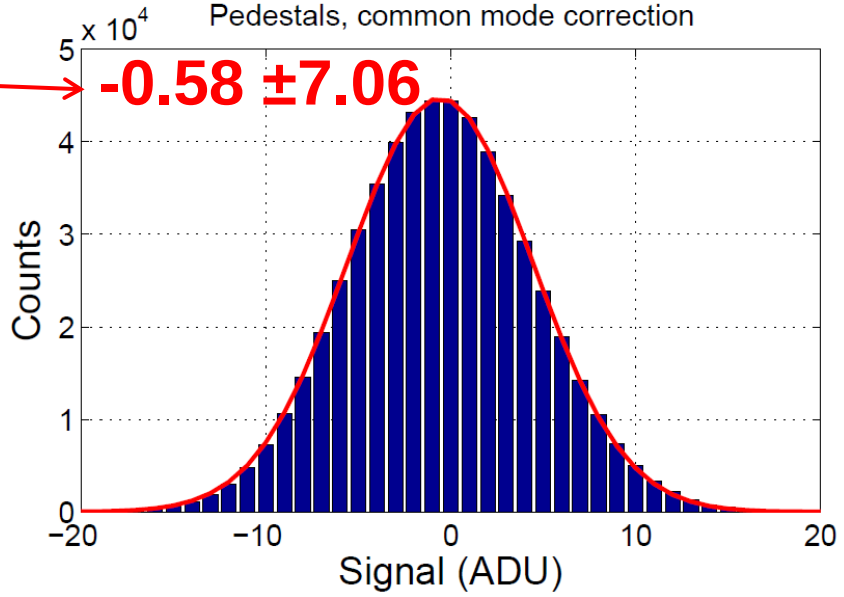




FWHM

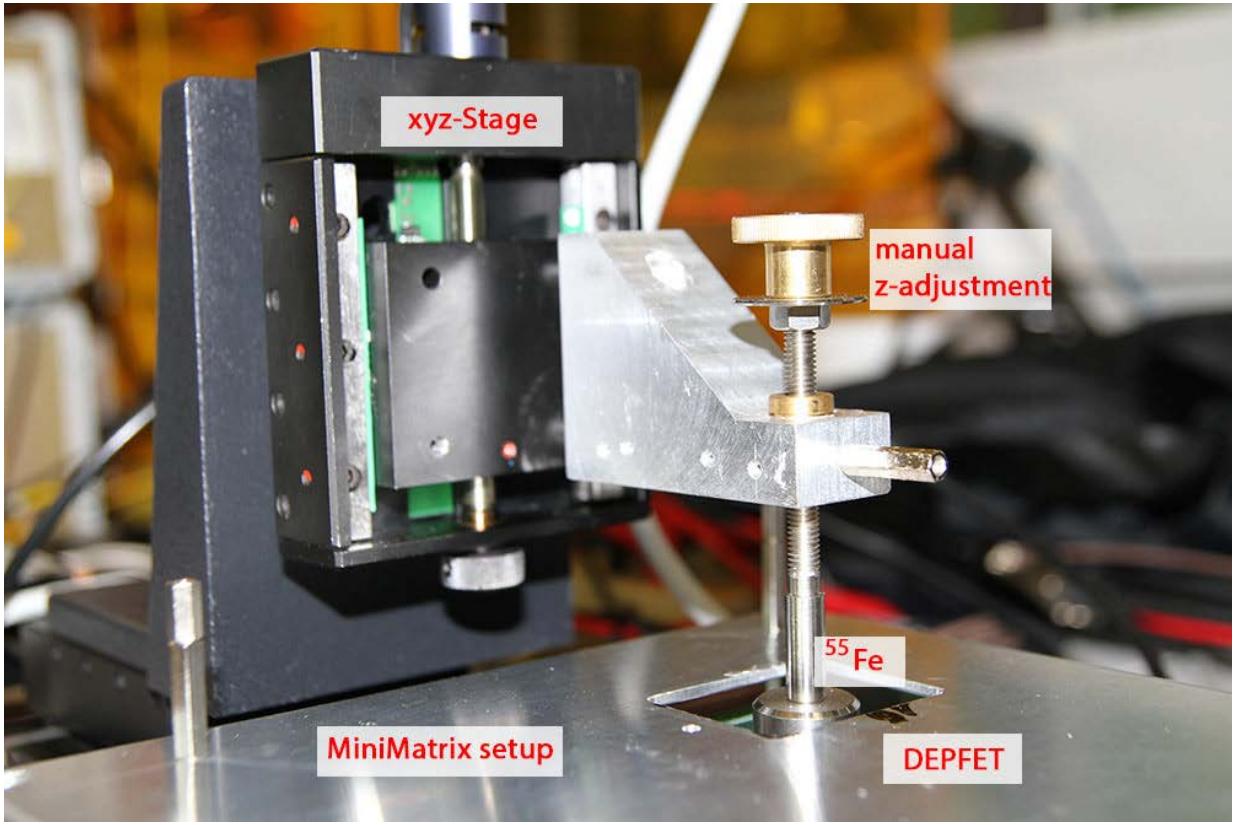
Common Mode

Correction (CM)

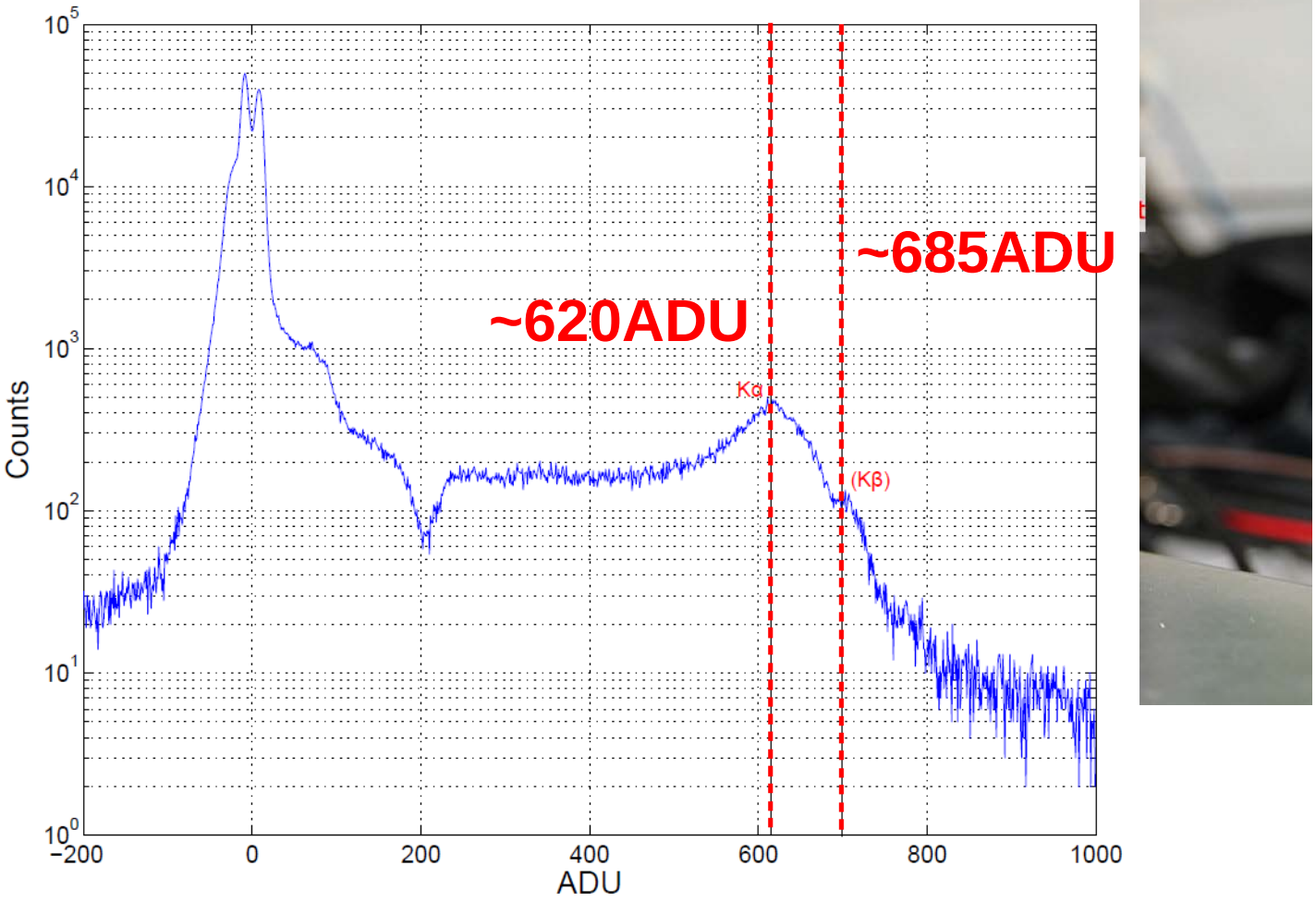


1ADU = 2.61 electrons

Calibration using Fe55 radioactive source



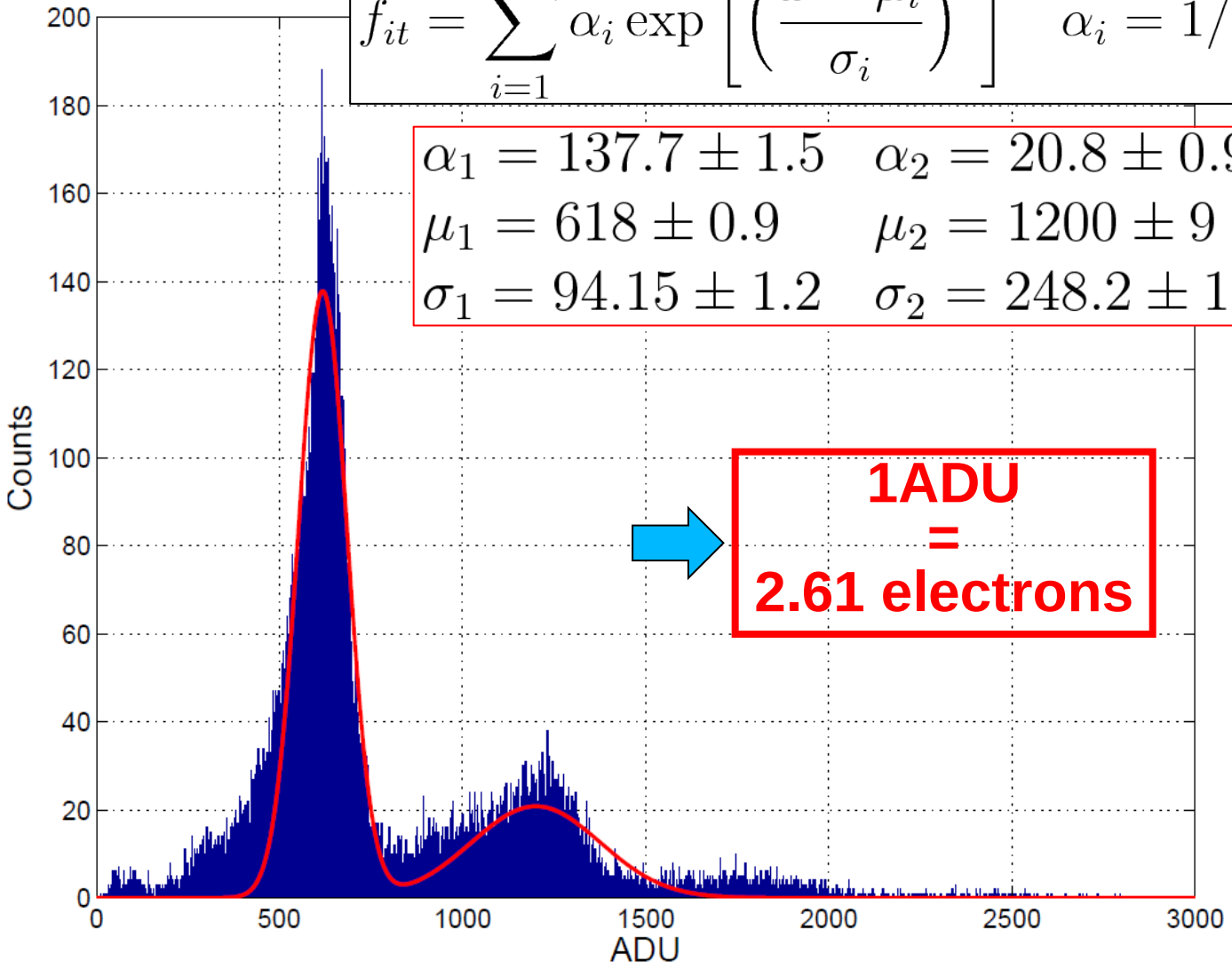
Calibration using Fe55 (without clustering)



Calibration using Fe55 (clustering)

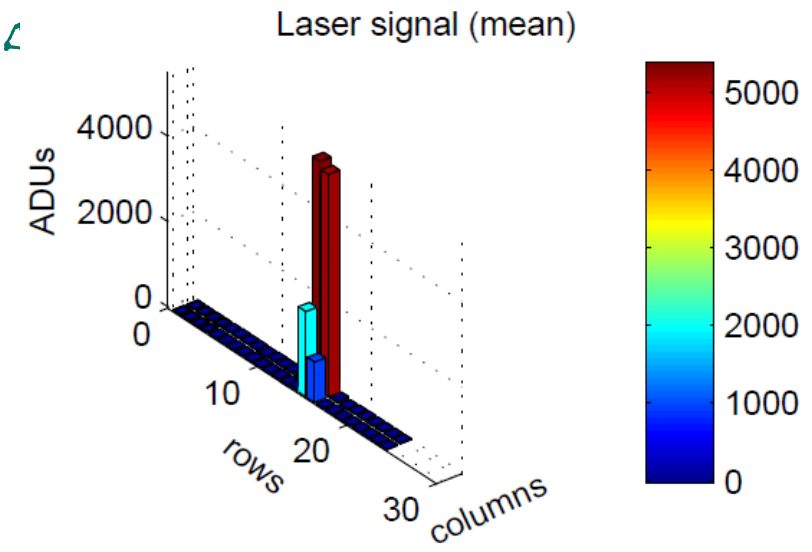
$$f_{it} = \sum_{i=1}^{2} \alpha_i \exp\left[\left(\frac{x-\mu_i}{\sigma_i}\right)^2\right] \qquad \alpha_i = 1/(\sigma_i\sqrt{2\pi})$$

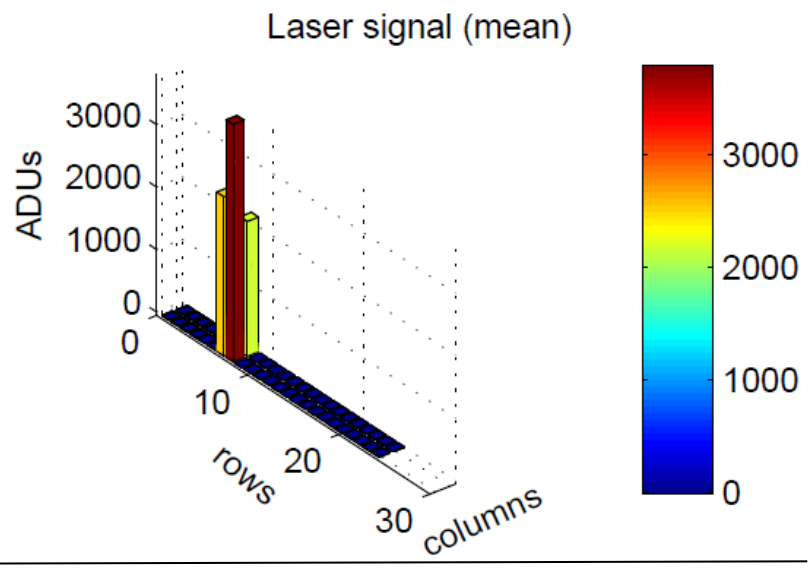
$$\alpha_1 = 137.7 \pm 1.5 \quad \alpha_2 = 20.8 \pm 0.93$$
$$\mu_1 = 618 \pm 0.9 \quad \mu_2 = 1200 \pm 9$$
$$\sigma_1 = 94.15 \pm 1.2 \quad \sigma_2 = 248.2 \pm 13.1$$

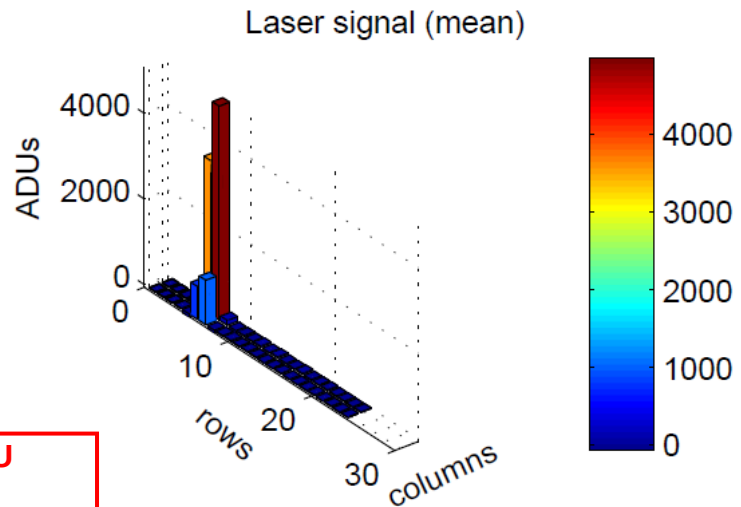


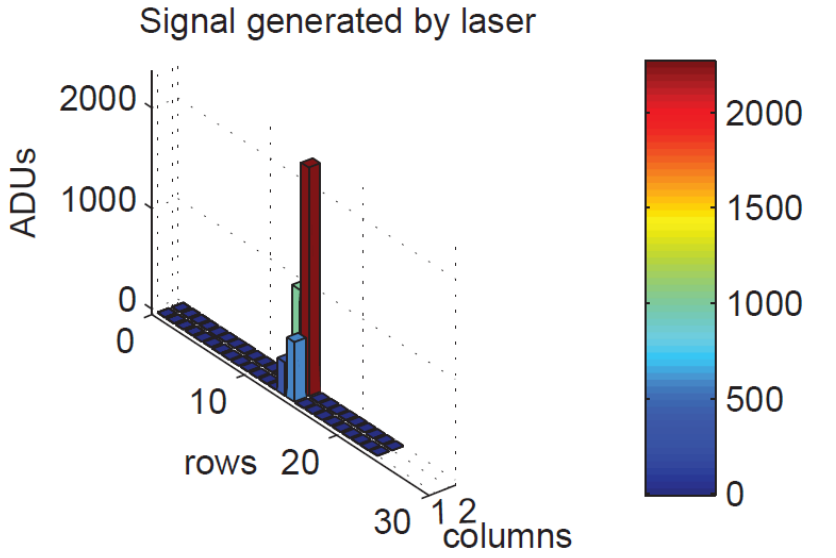
1ADU = 2.61 electrons

Laser impinging onto the DEPFET detector – signal



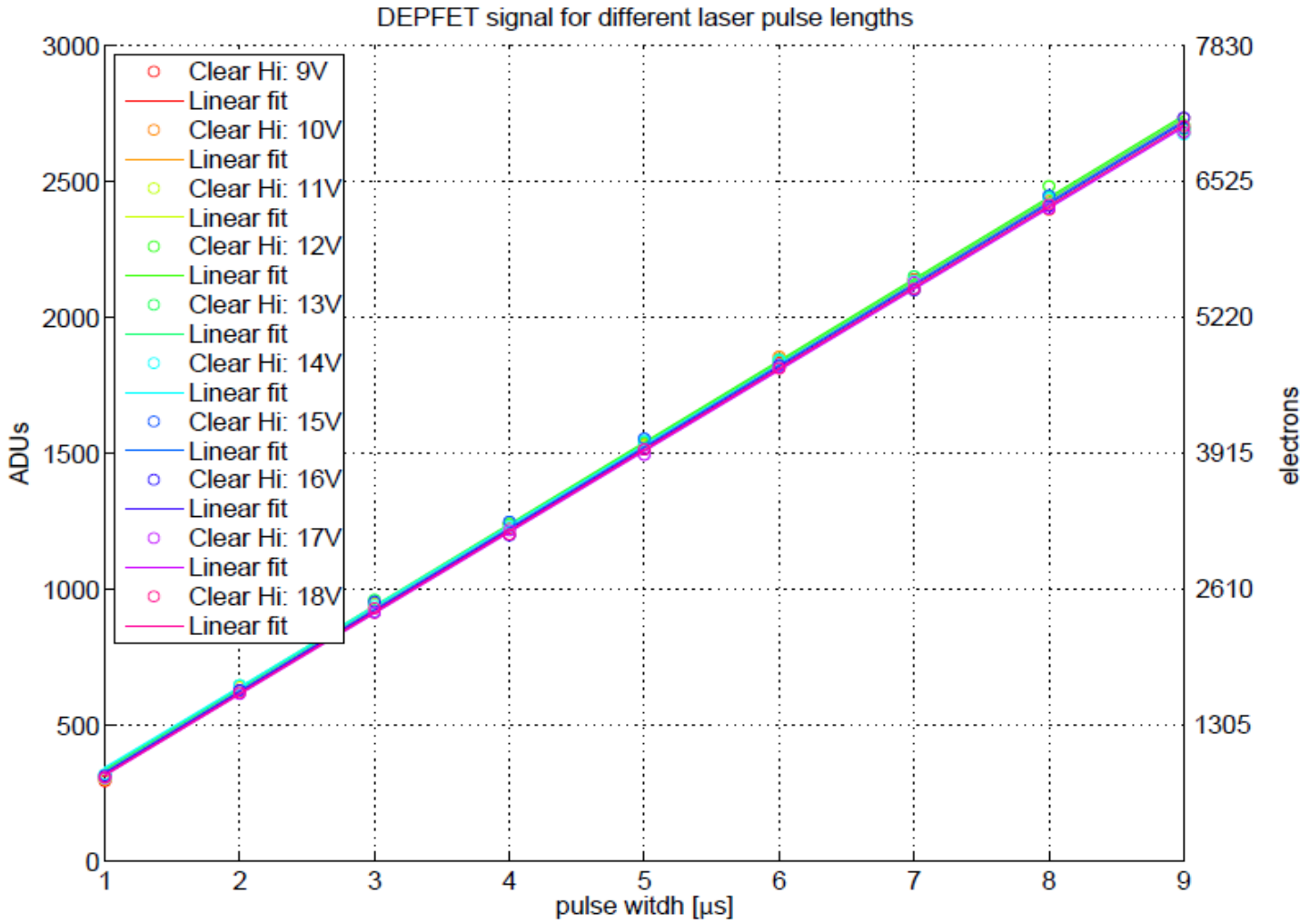




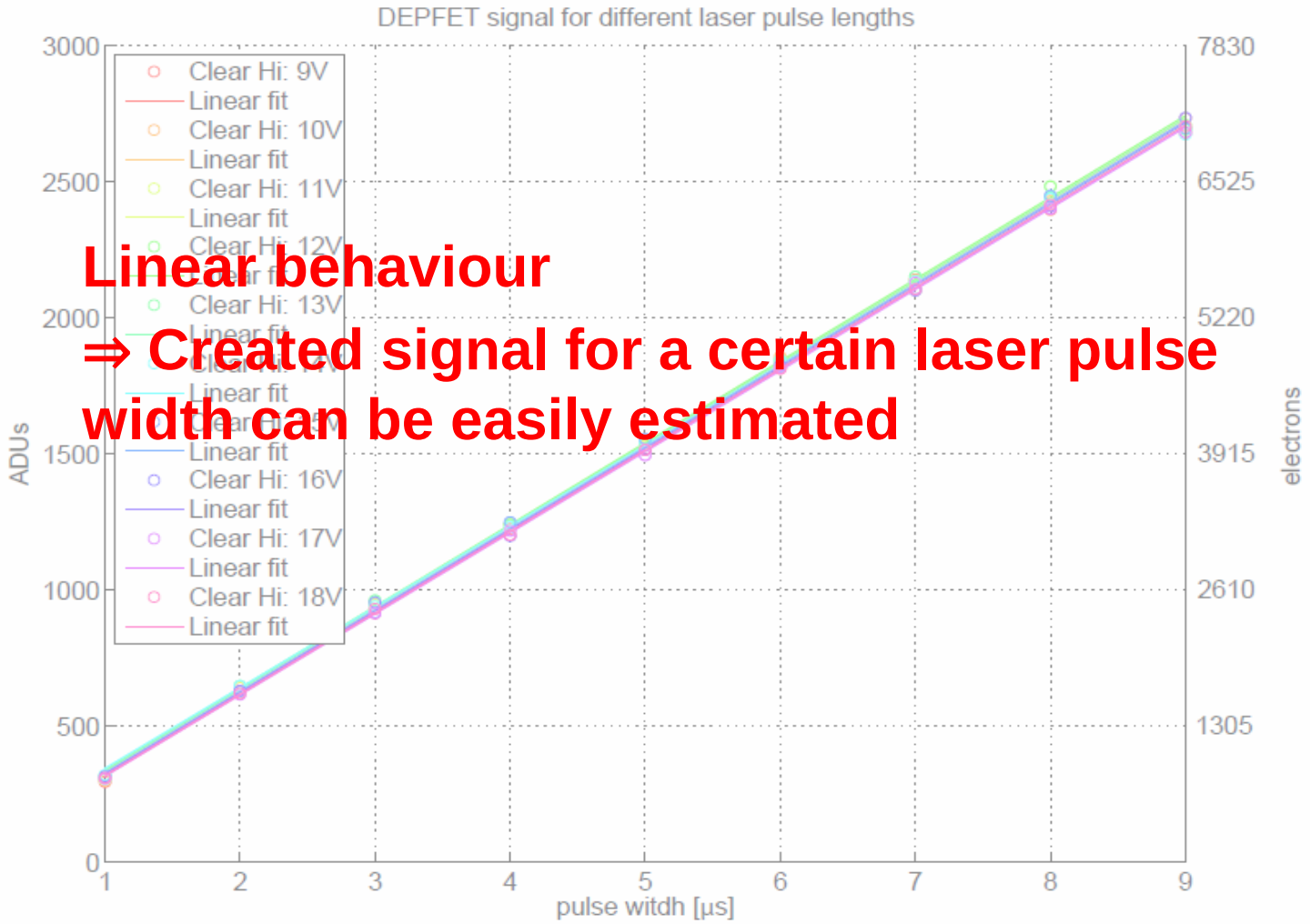


1ADU = 2.61 electrons

Measurement of signal generated by a laser



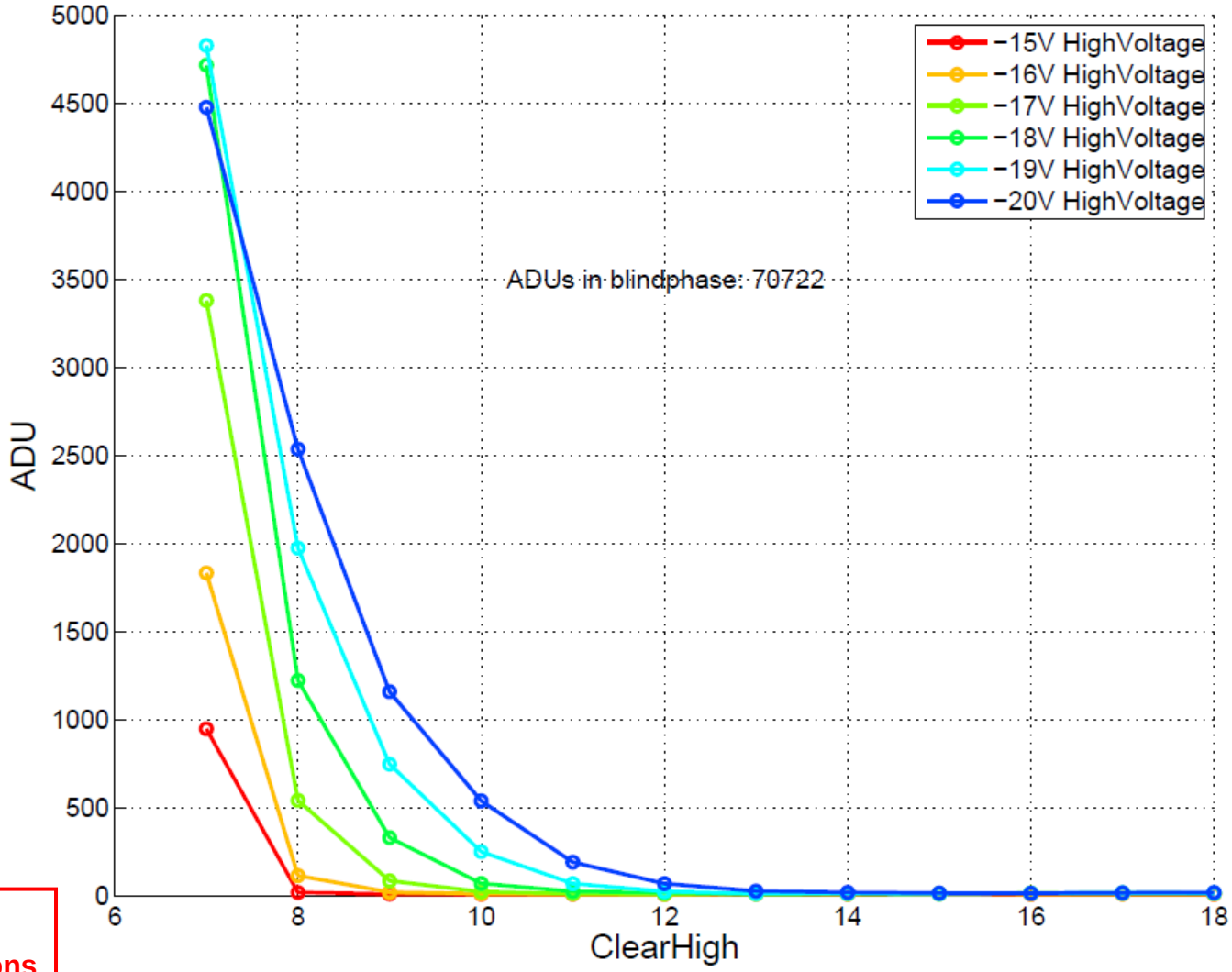
Measurement of signal generated by a laser



Linear behaviour

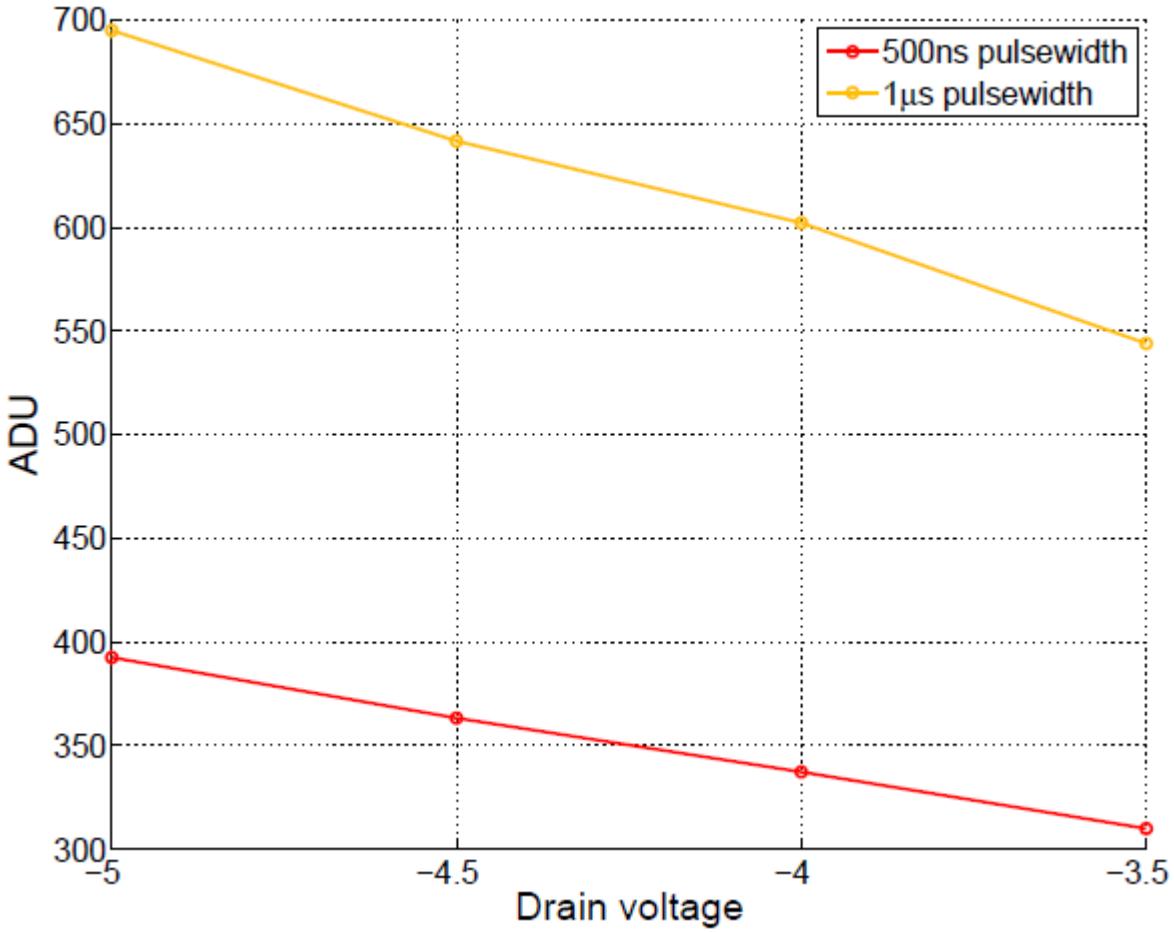
⇒ Created signal for a certain laser pulse width can be easily estimated

Generation of Junk Charge – High voltage dependence

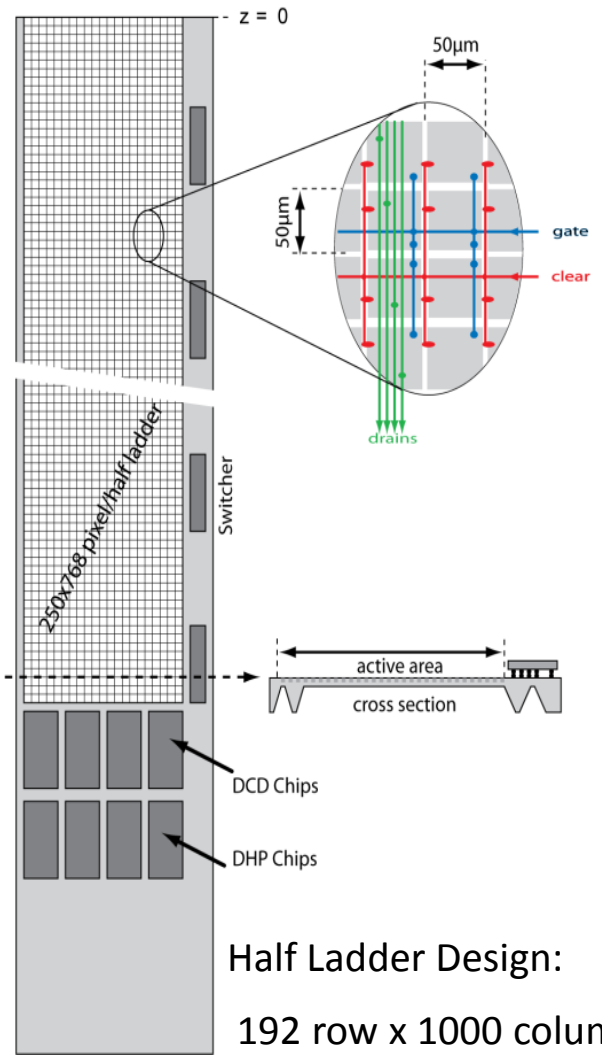


1ADU = 2.61 electrons

Impact of the signal with respect to the drain voltage



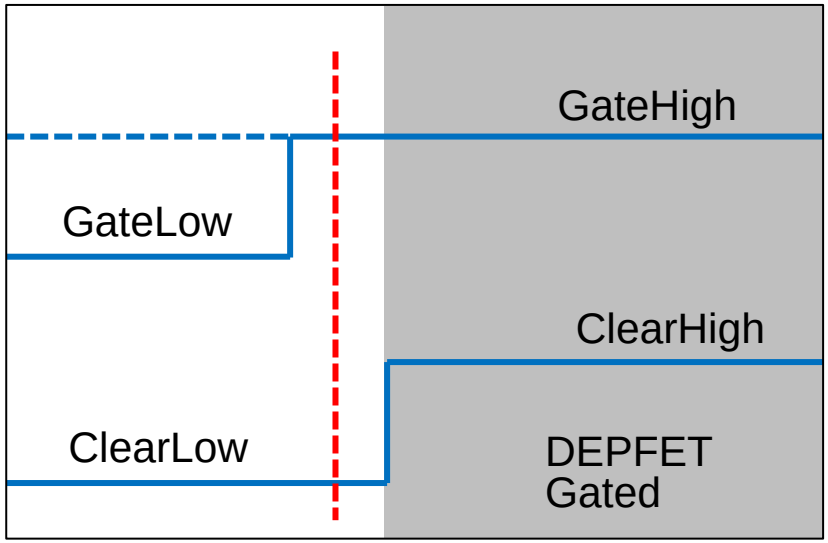
System Aspects – PXD Half Ladder



Half Ladder Design:

192 row x 1000 columns

Gated-Mode

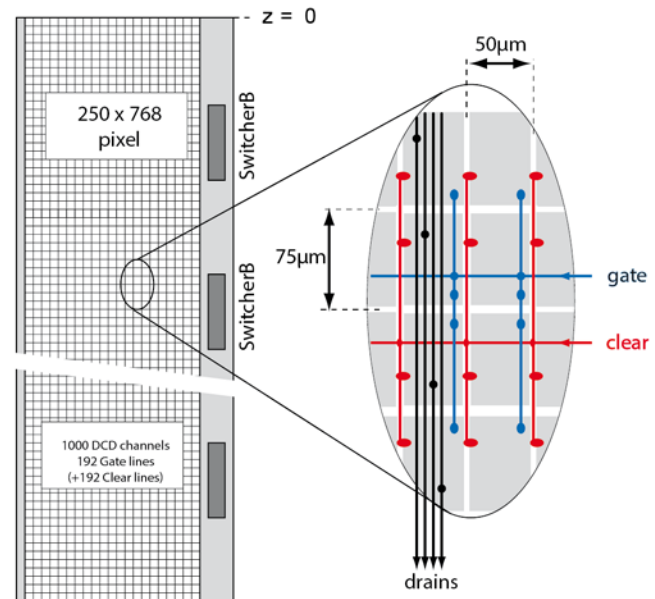


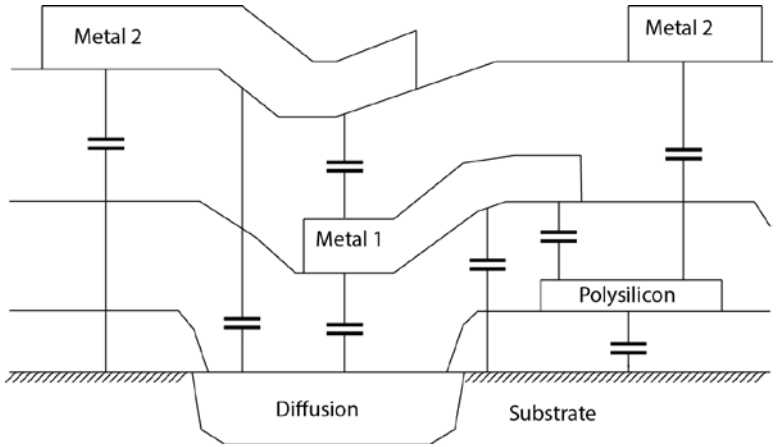
From Normal Read-Out to Gated-Mode (all rows)

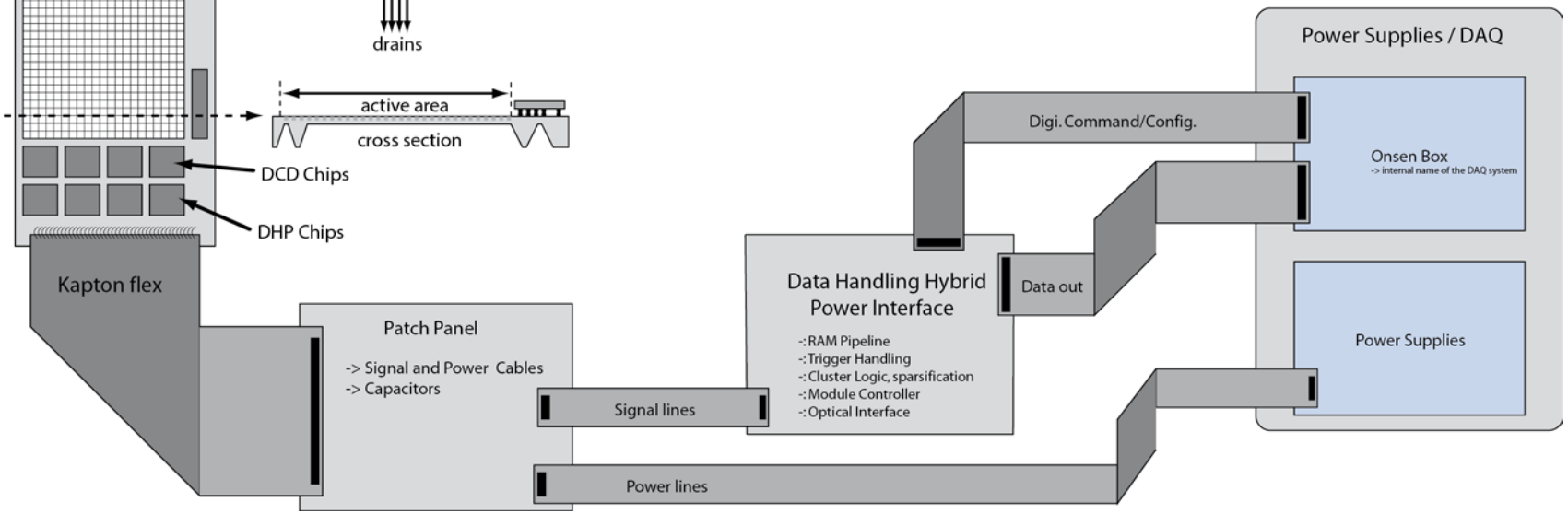
- GateHigh potential is applied to 191 rows → **must be applied for 1 additional row**
- ClearHigh is applied to 1 row → **must be applied to all 192 rows**

System Aspects – What are the obstacles?

- Parasitic Clear capacitance (~30nF) and resistivity of the supply lines



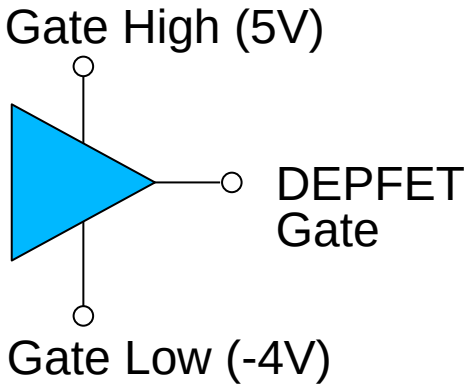


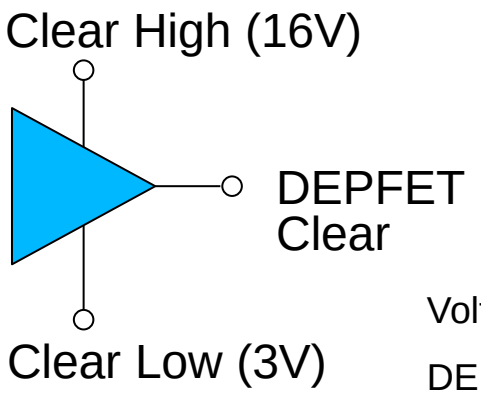


Principle of Gated-Mode

SwitcherB: Gate and Clear Channel

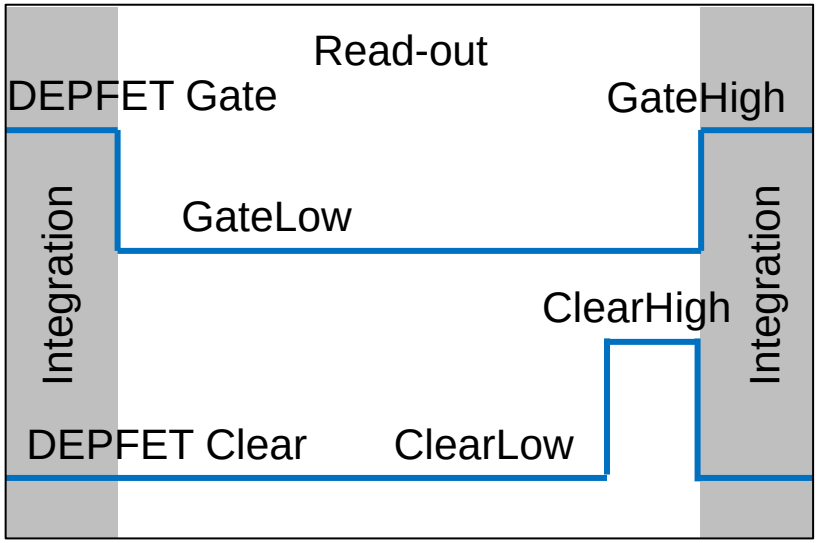
The terms GateOn and GateOff are also used. Since the DEPFET is a p-channel FET
GateOn = GateLow
GateOff = GateHigh





Voltages referred to DEPFET Source

Normal Operation



Gated-Mode