Probe Card System for DHP Chip Testing

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H. Krüger, Bonn University
Motivation

- PXD modules are sensitive to single-point-of-failure of the DHP
- Up to know very little statistics of the DHP yield (+ flip chip mounting to wirebond adapters with low yield only)
- Need to qualify ICs before flip-chip mounting
DHP Chip Probing Prerequisites

• What is needed:
  – Needle card for solder bump probing
  – Test bench for DHP environment
    • IO signals from test system (DHH like)
    • DCD input/output emulation
  – Test procedure to provide full coverage
  – Definition of cut parameters for chip classification

• Design is based on DHP 0.2
• DHPT 1.x will be pin compatible to DHP 0.2
DHP Chip Probe Test System

Power Supply

DHP test system
(XUPV5 FPGA Board)

Needle Card PCB

FPGA
DCD emulation
Sequencer r/b

Probe Needles

DHP

Probe Station

GPIB or USB

Infiniband

JTAG

Eth

DAC

GPIB or USB

Infiniband

JTAG

Eth
159 bumps need to be connected
Material: lead free, LTS
Pitch: 200µm (y), 180µm (x)
~110µm diameter
Connections:
- JTAG (4x LVDS)
- Timing (4x LVDS)
- Data Link (1x CML)
- Aux clock (2x LVDS)
- SWITCHER (4x LVDS)
- DCD out (8x 8 HSTL)
- DCD in (8x 2 CMOS)
- DCD timing (2x CMOS)
- DCD JTAG
- DCD_ref (analog)
- Power (8x VSS, 4x VDD, 2x VDD_CML)
- PLLxx2Fast
- FrameSync
- ResetB (CMOS)
- Analog IO test signals
- Bump coordinates in µm
- Origin in upper left corner
- No bump at location (0,0)
- Bumps with no needle connection shown in gray
DHP 0.2 Layout

Examples from vendor

Probecard in Cantilever-Bauweise (Beispiel Infineon Probecard)

Bild 1: Nadelspinne von oben gesehen

Bild 2: Nadelspinne von unten gesehen

Bild 3: Nadelspinne im Board/PCB
Debug Probe Card

- PCB with active components, will need some debugging
- Very sensitive with needles attached

⇒ Dedicated debug “Probe” Card
- (almost) same netlist as needle card PCB
- replace needle footprint with DHP 0.2 wire bond adapter

⇒ Debug PCB is ready and tested
- DHP communication ✔
- FPGA programming (DCD emulation, Switcher sequencer read-back) ✔
Needle Card PCB

Specs

• 6 layer PCB
• 3mm thick → mechanical stiffness

Status

– PCB Design & Production ✓
– Component mounting ✓
– Testing ✓
– Needle mounting
  • needs ~4 weeks (@ HTT)
Probe Station Setup

• Needle card fixture ✓
• We have diced chips only
  – put single chips on chuck (Ok for now)
  – “chess board” fixture with array of cavities for production testing → tbd
• External components:
  – Power supply ✓
  – DHP test system (FPGA board via Infiniband cables) ✓
  – extra JTAG for on board FPGA programming/readback, optional: can use JTAG from Infiniband connection ✓
Probe Card System Status

• Hardware components of the needle card test system
  – Debug probe card for HW verification and debugging ✓
  – Needle probe card: components mounted and tested, shipped for needle mounting end of January (takes ~4 weeks)
  – Mechanical fixture for probe station ✓

• Software
  – based on DHP test system from Mikhail (✓)
  – needs further extensions (for basic testing ok)
    • (more) systematic sequencer and DHP DAC output read-back
    • automation of test sequences
    • coverage...
    • definition of cut parameters
    • ...

• Planning
  – Start commissioning of the needle card system by end of Feb
  – First (rudimentary) tested DHP chips supposed to be available in March
DHP Chip Availability

• Only small number of DHP 0.2 chips left (~15)
• Next chip version (DHPT 1.0) available by mid 2013
• Need certain number of tested chips for E-MCM and PXD6 large matrix assemblies

Possible scenarios:

a) DHP has high yield, enough Ok tested die for E-MCM + PXD6 (very optimistic)
   ➔ no action needed

b) DHP yield not sufficient, need more chips (more likely)
   i) Buy remaining MPW chips from MOSIS (rather expensive)
   ii) Wait for DHPT 1.0 to become available (maybe too late)
   iii) Recover unsuccessful DHP 0.2 flip chip assemblies (quite a few)

➢ Recovery procedure
   • De-solder and clean DHP chips (Valencia ?)
   • Place new bumps (Heidelberg ?)