Options for Digitization and Data Compression

DAQ for CDEX-10 in Design

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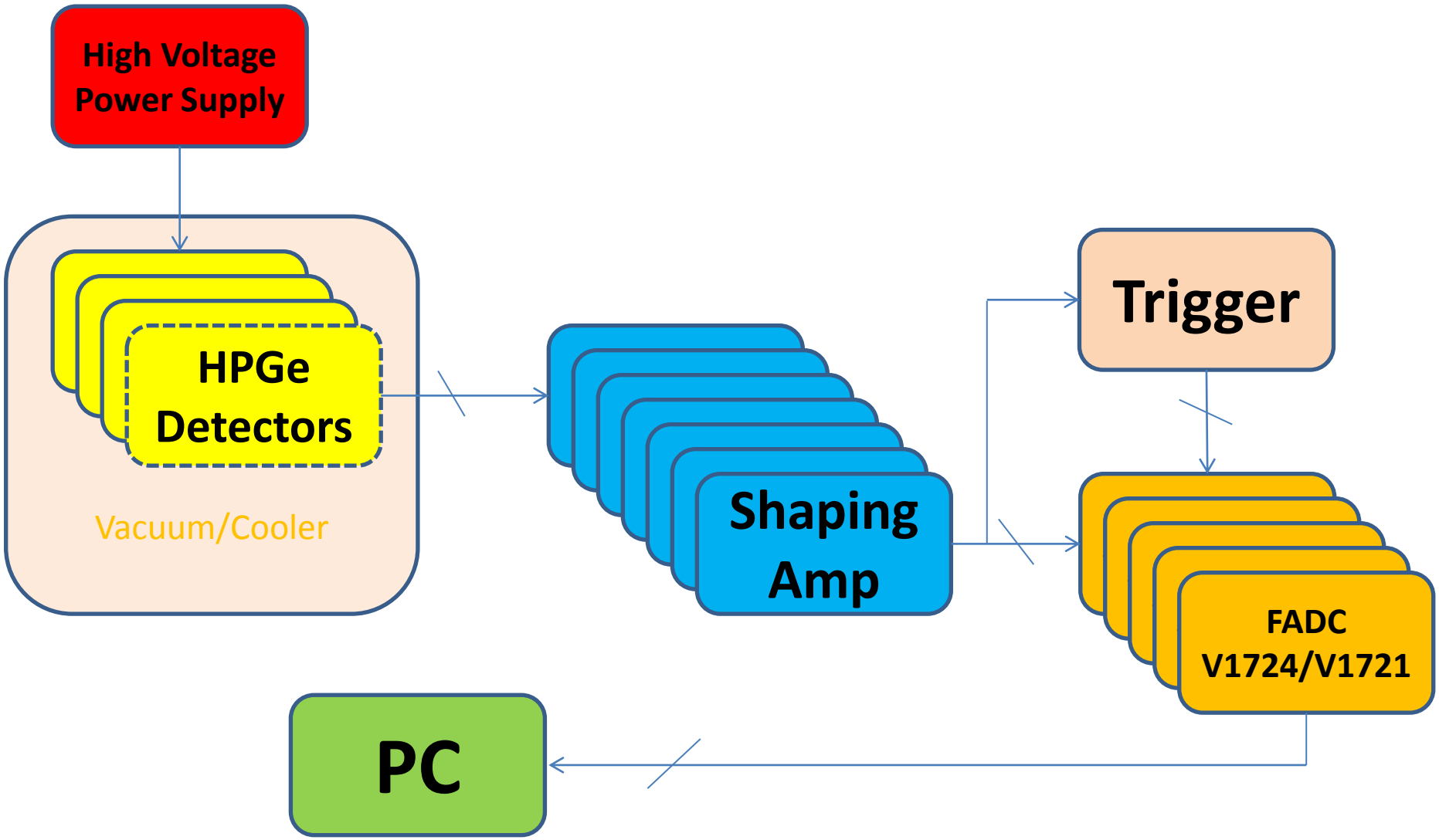
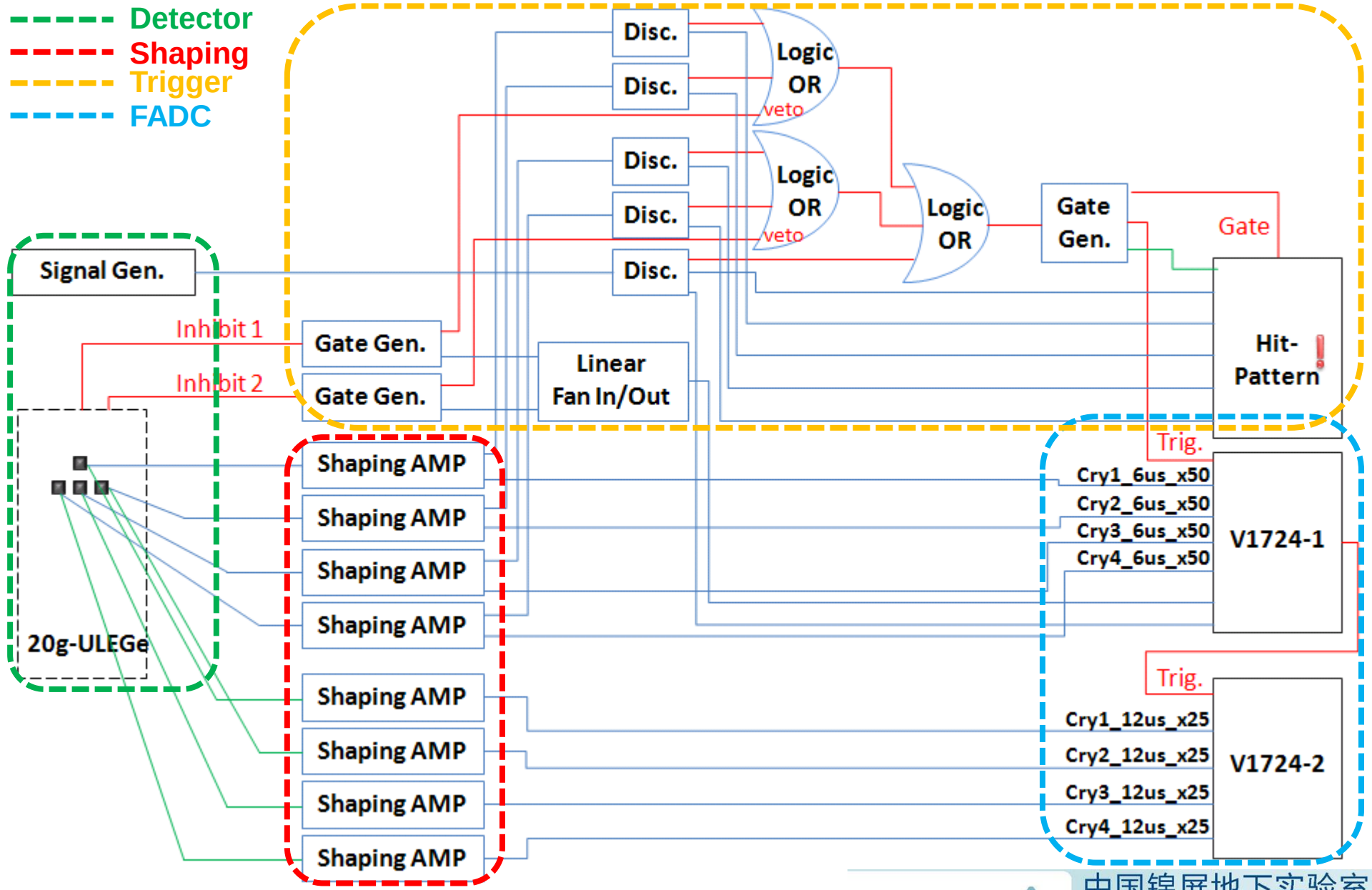
Outline

- What we need for next CDEX-10 project's electronics?
- Architecture for DAQ system, Shaping, FADC, Trigger, Clock distribution, DAQ
- Implement of Digitization and Data Compression in FPGA.

Electronics for 20g and 1Kg HPGe Detectors Now running in CJPL

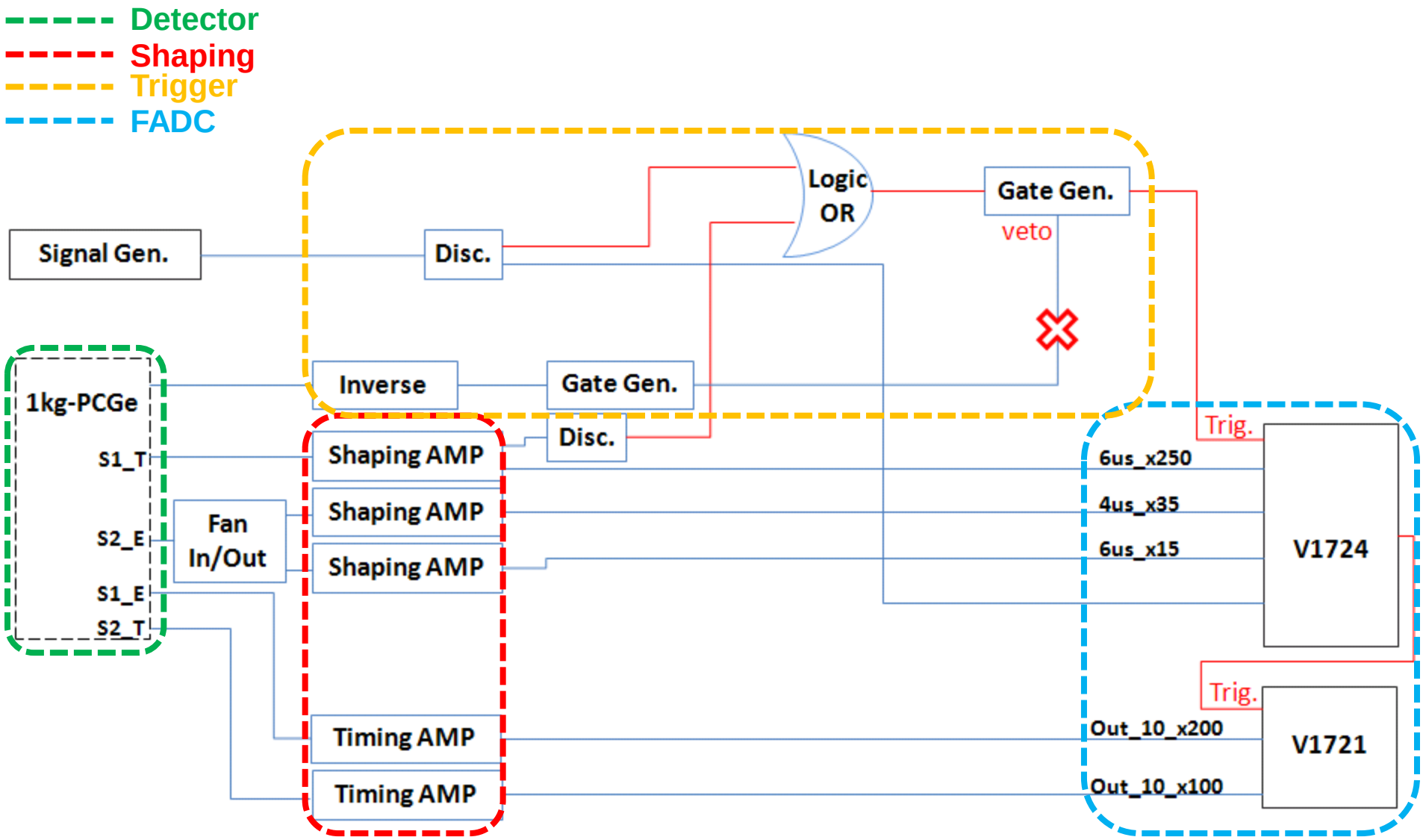


Schematic Diagram : 20g ULE Ge



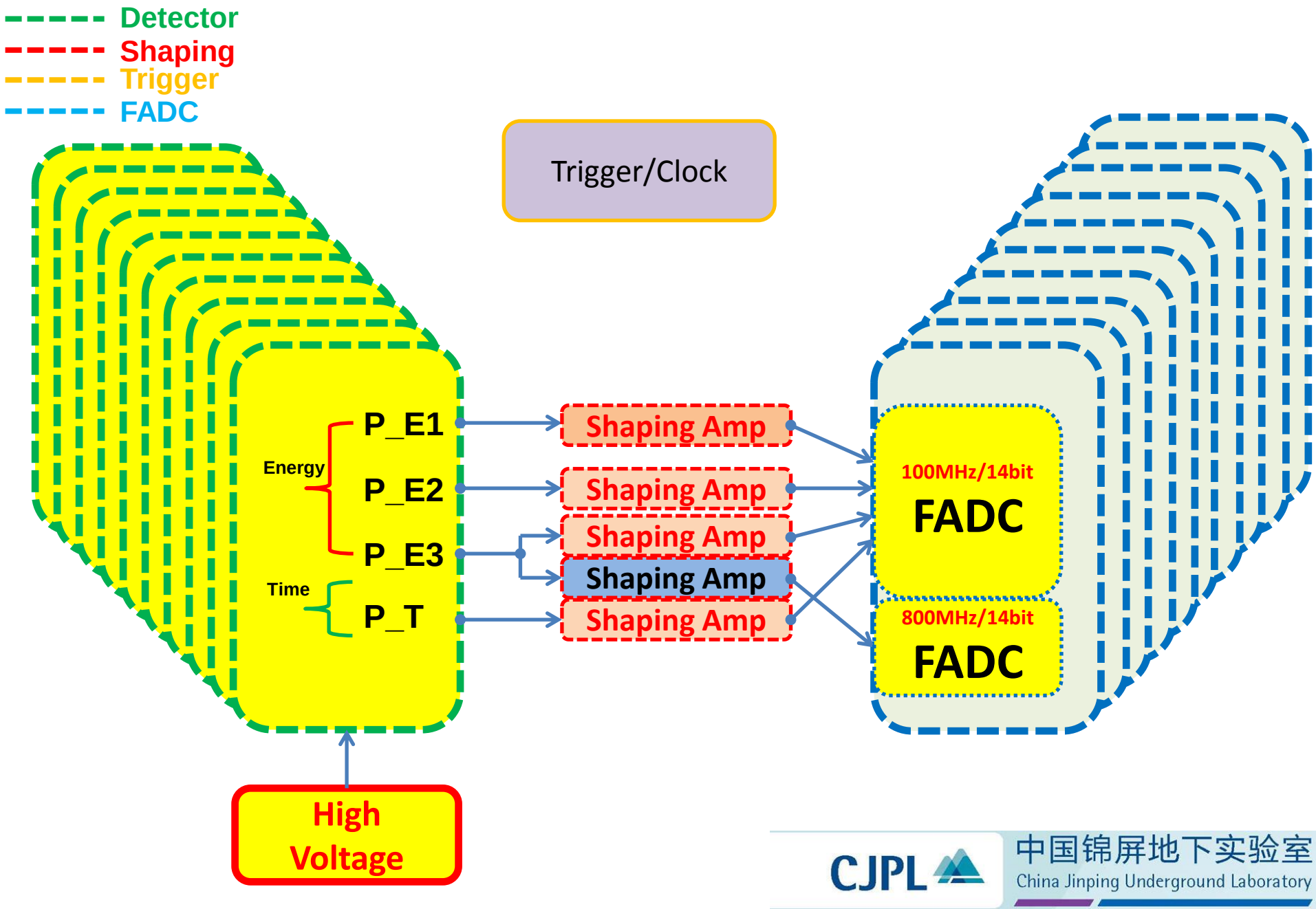
Picture from Wu Yucheng

Schematic Diagram : 1kg PPC Ge

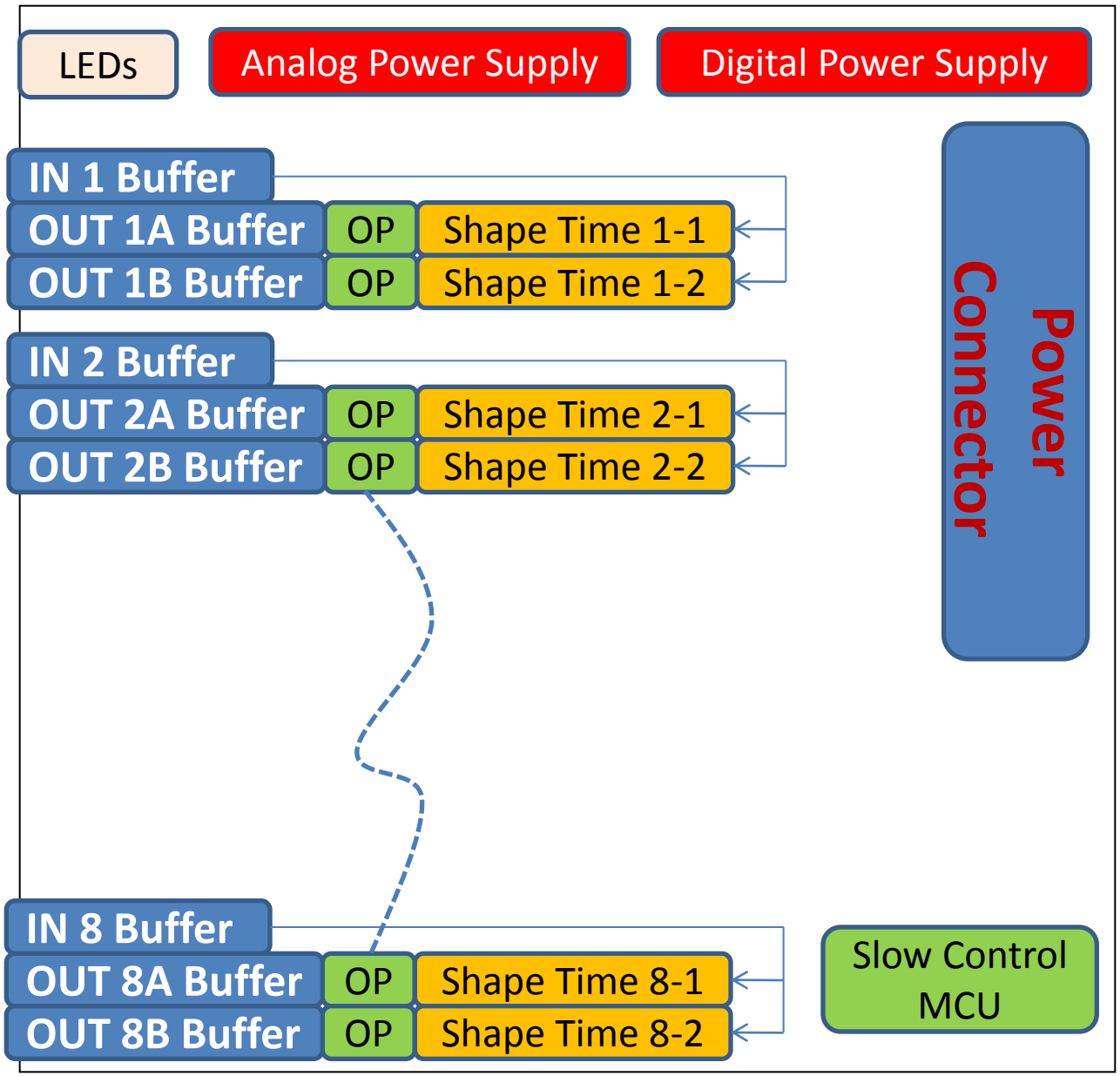


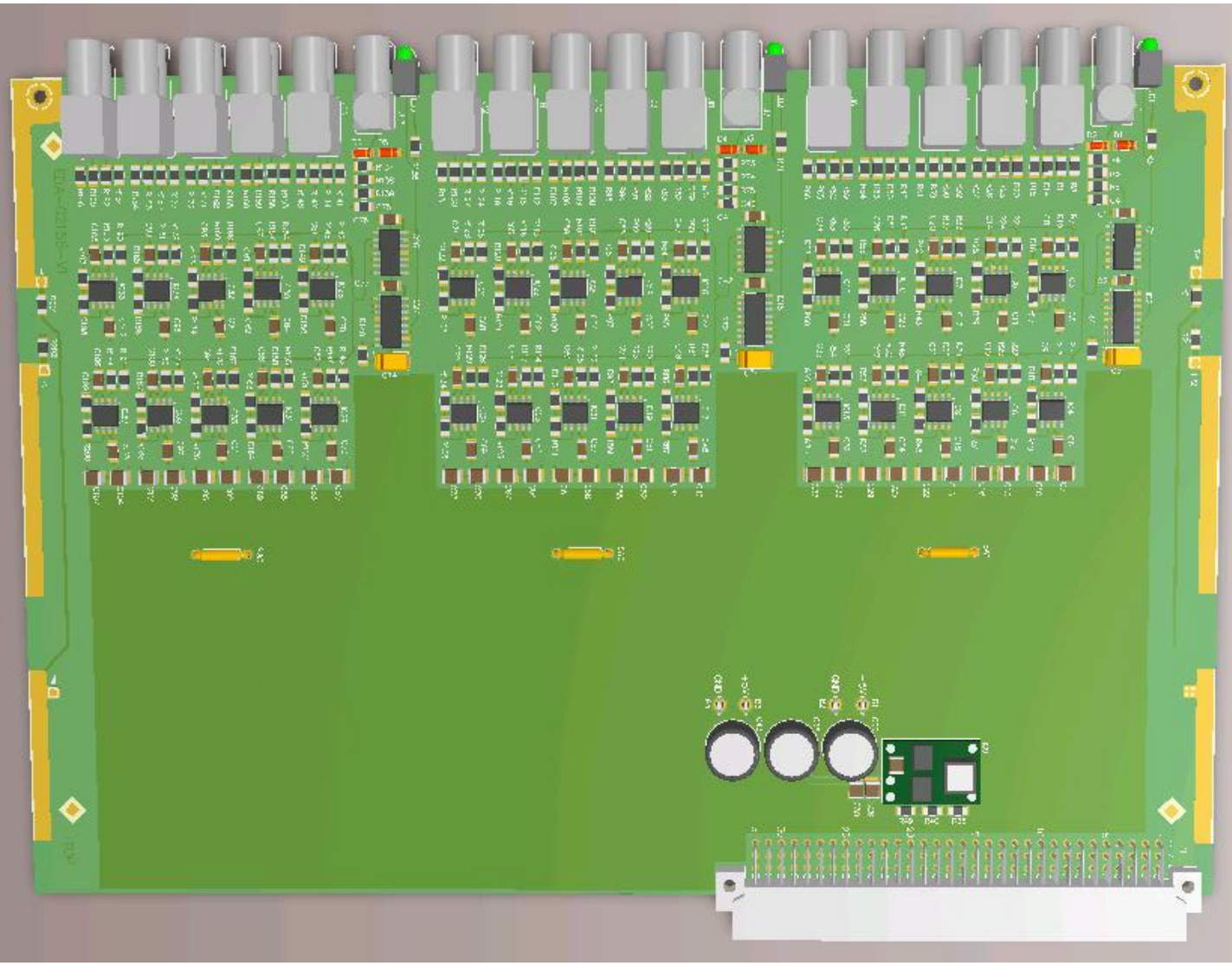
Picture from Wu Yucheng

Schematic Diagram in Future : 10kg PPC Ge



Shaping Amp Board

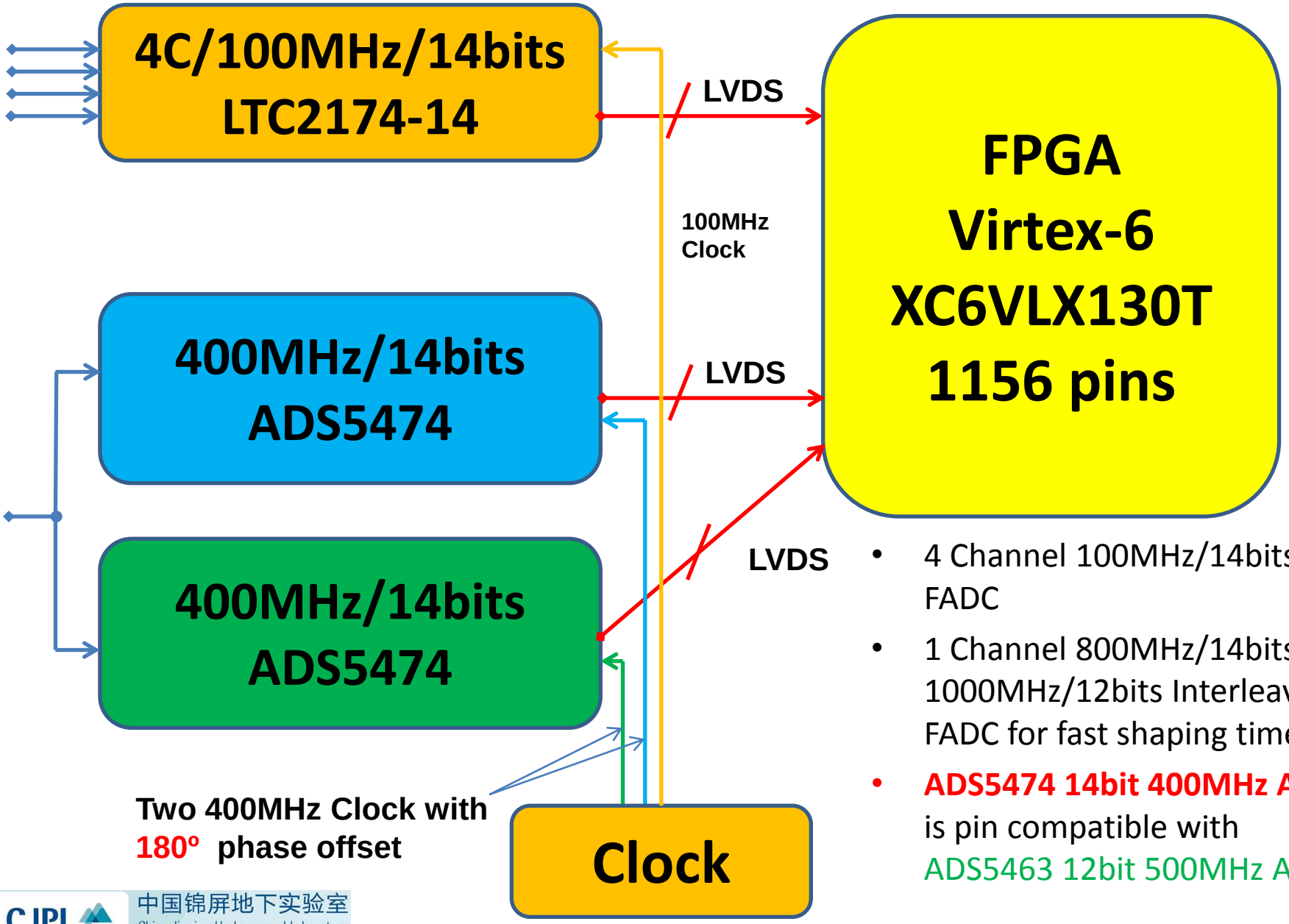




FADC

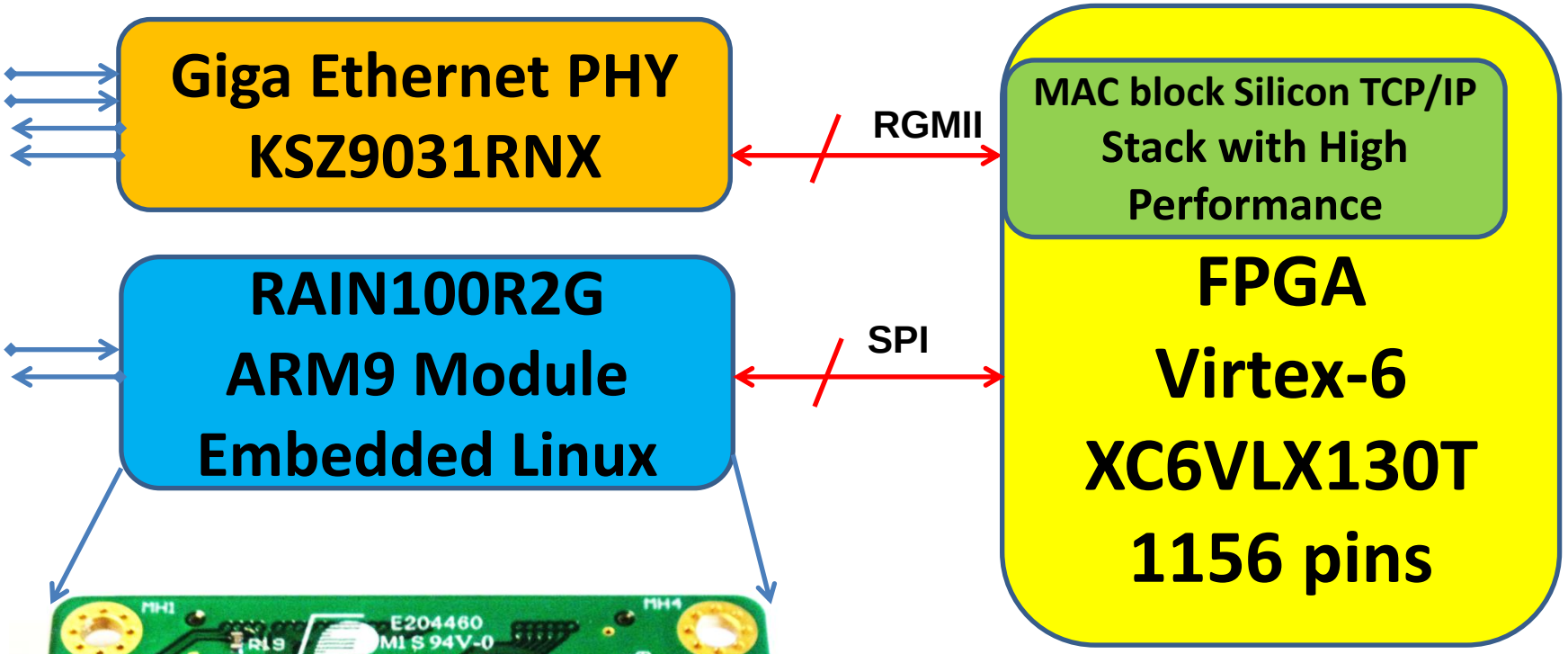
- 4 Channel 100MHz/14bits FADC
- 1 Channel 800MHz/14bits or 1000MHz/12bits Interleaved FADC for fast shaping time
- 1000Mbps Ethernet for readout
- 100Mbps Ethernet for slow control (Calibration, firmware update, status monitor, threshold setting ……)
- High speed interface for hit-sum
- Trigger and Clock interface

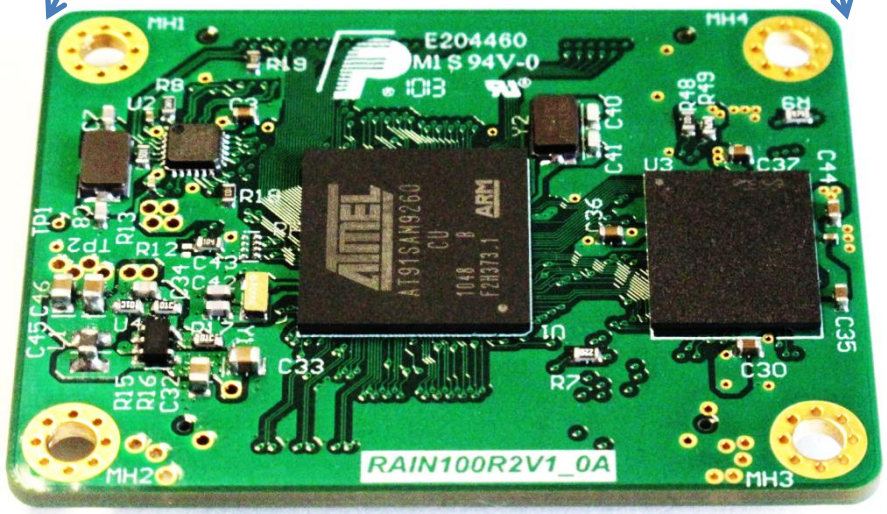
FADC Details part 1



- 4 Channel 100MHz/14bits FADC
- 1 Channel 800MHz/14bits or 1000MHz/12bits Interleaved FADC for fast shaping time
- **ADS5474 14bit 400MHz ADC** is pin compatible with ADS5463 12bit 500MHz ADC

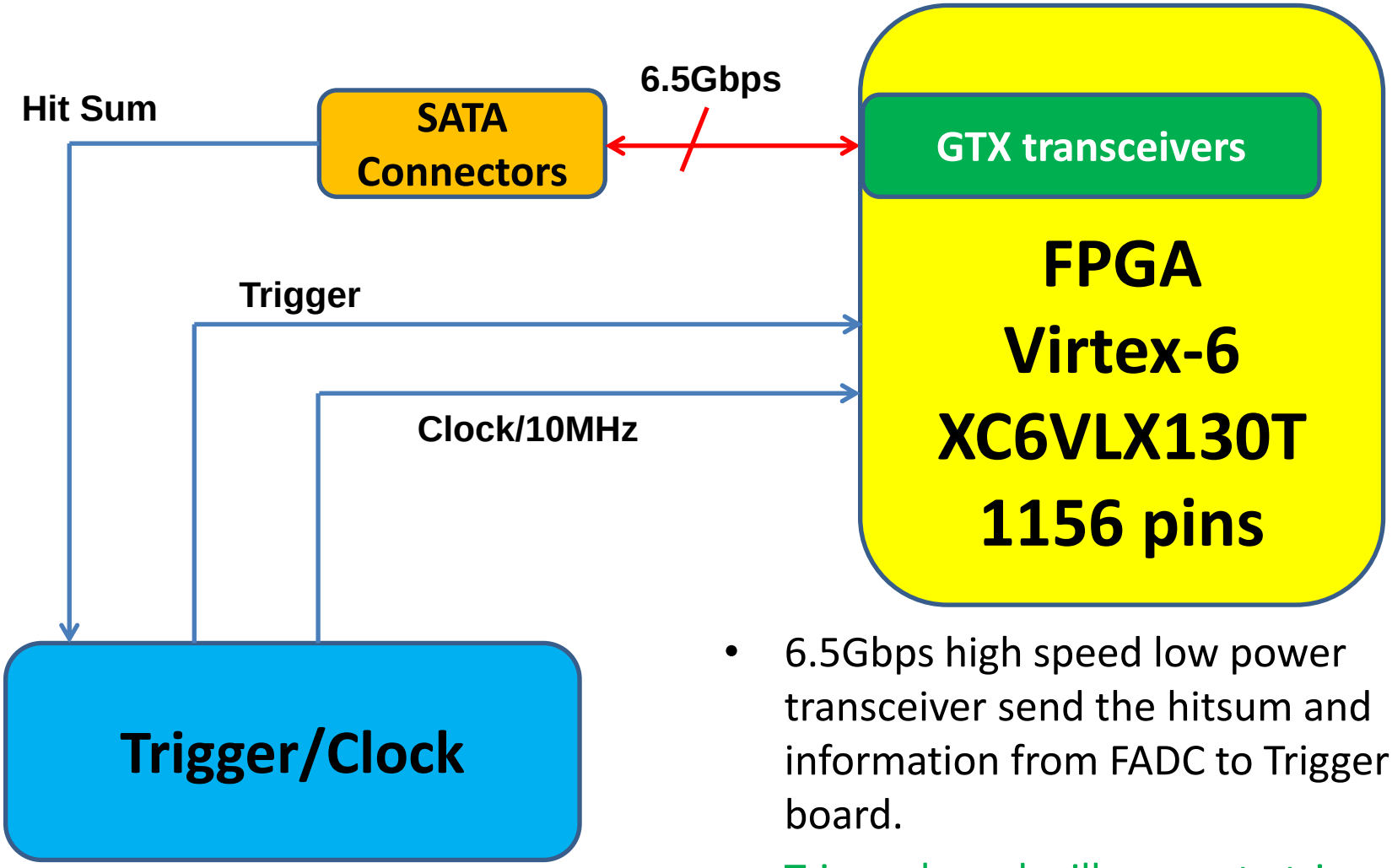
FADC Details part 2





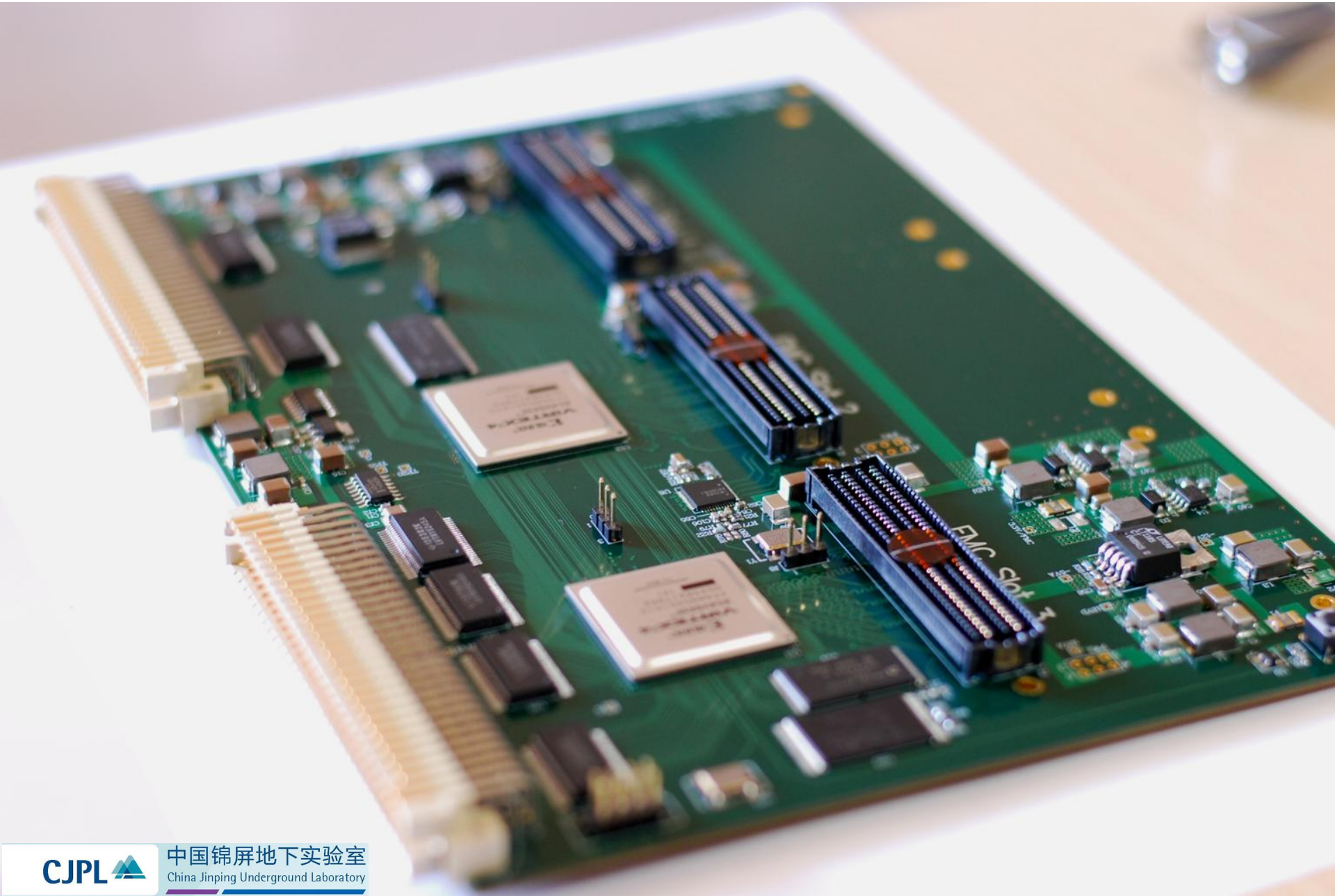
- 1 high speed 1000Mbps ethernet interface for readout
- 1 100Mbps ethernet interface for slow control, a RAIN100R2G ARM9 processor module is used
- Embedded Linux is running in RAIN100R2G, we can telnet to configure the FADC remotely

FADC Details part 3

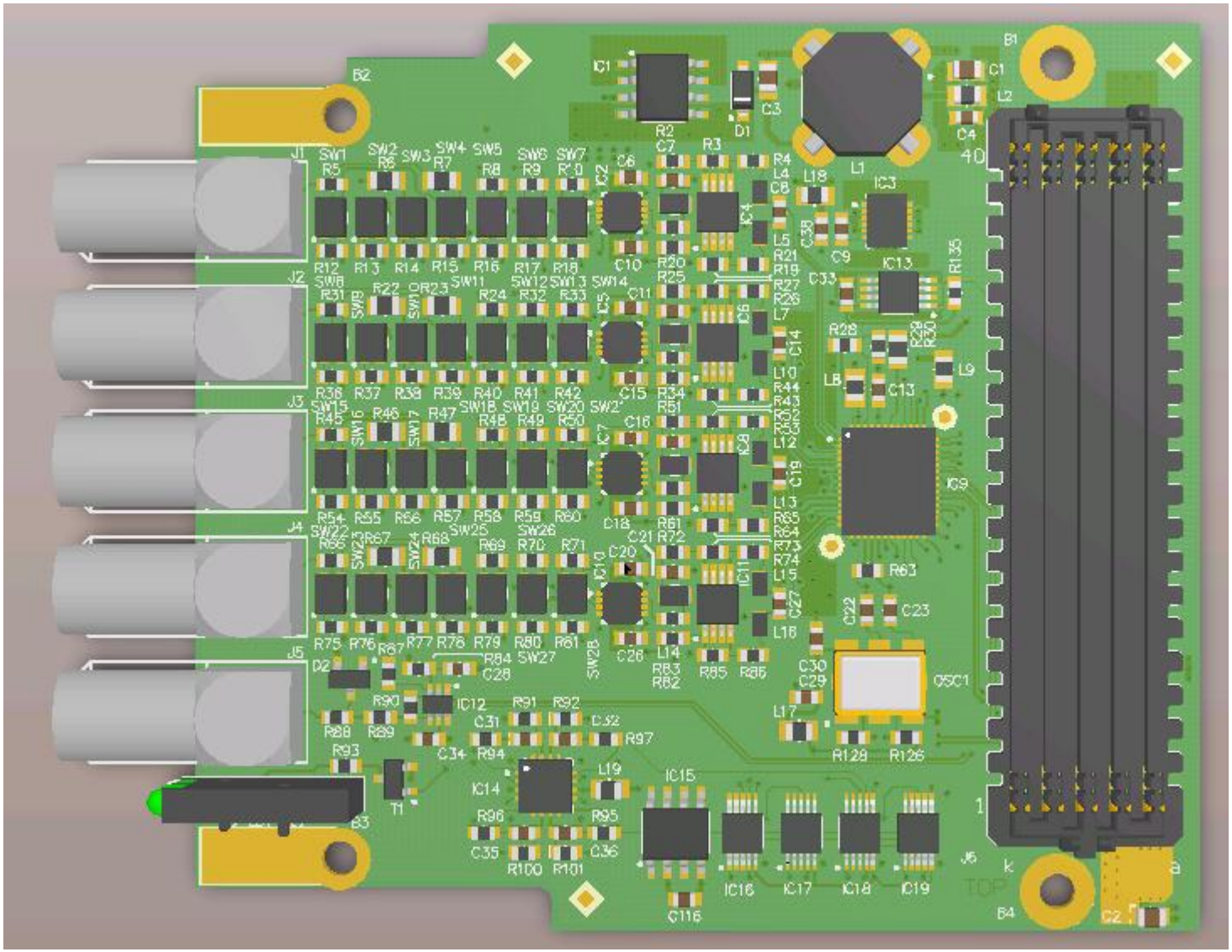


- 6.5Gbps high speed low power transceiver send the hitsum and information from FADC to Trigger board.
- Trigger board will generate trigger signal to FADC board
- Clock will be fan out to every FADC board.

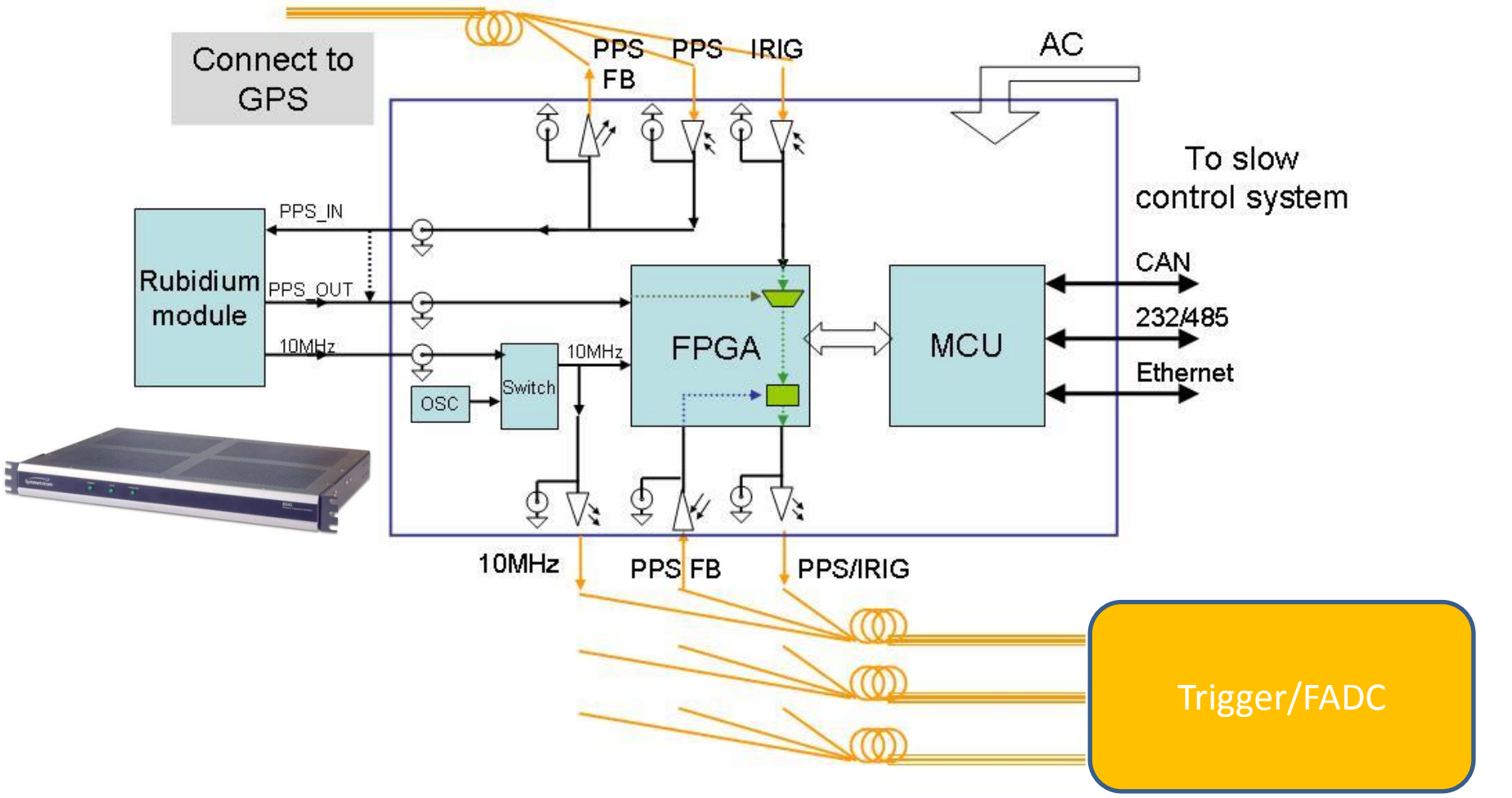
Prototype of FADC System



Prototype of 100MHz 14bits 4Channel FADC

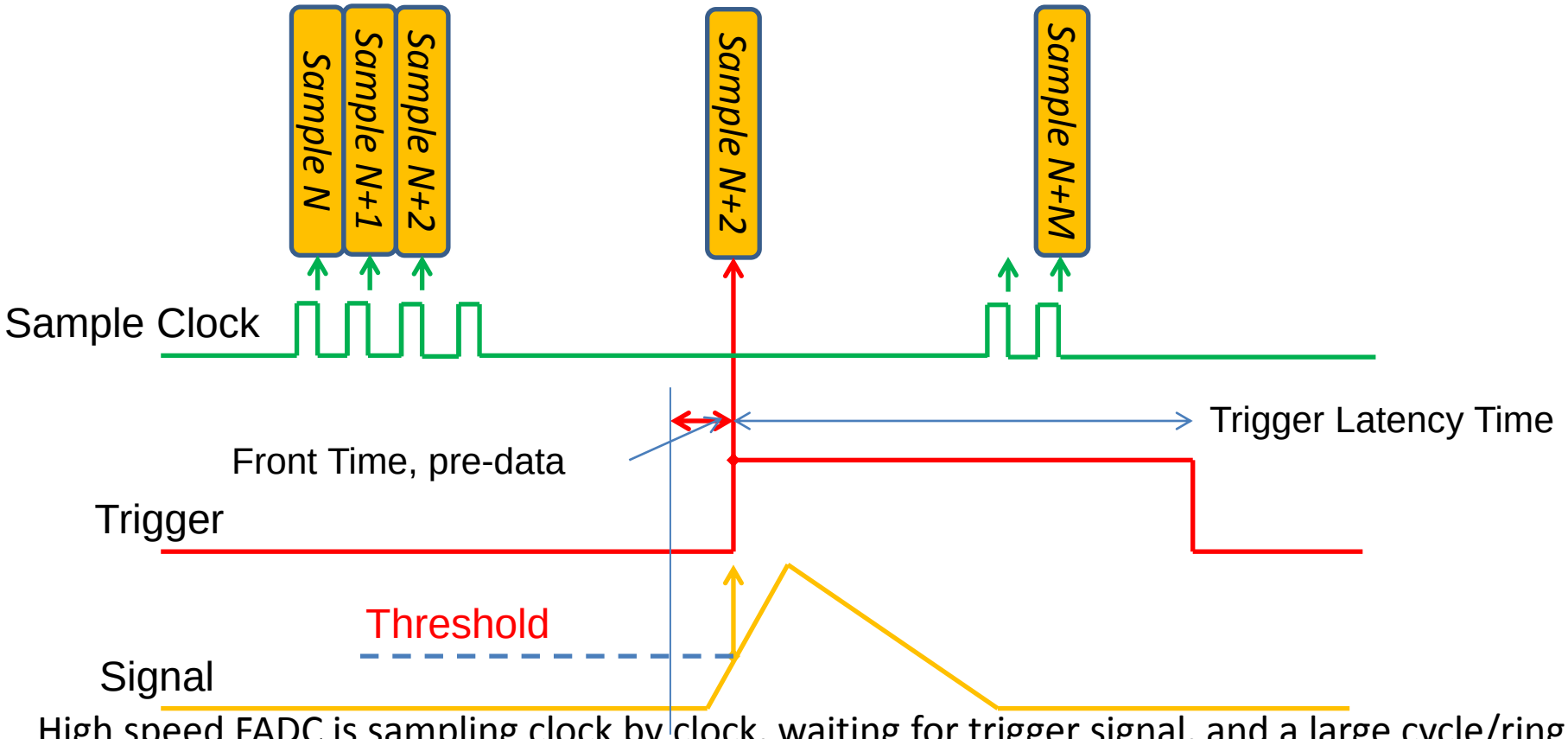


Clock



- **Rubidium clock system is used for 10MHz clock** Symmetricom 8040C
- **GPS to calibration absolute time PPS** Symmetricom XL-GPS

Digitization Implement in FPGA



- High speed FADC is sampling clock by clock, waiting for trigger signal, and a large cycle/ring buffer is used to store sample data
- Trigger will generated by trigger board, it collects all FADC board's hit sum information and judge if a trigger should be generated.
- FPGA also store the front pre-data into readout buffer
- The channels with all of data is lower than Threshold will be discarded
- The channels with small signal and most of data is lower than Threshold will be "ZERO" compressed. Where the readout bandwidth is lowered.

Thanks !

Loquat

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