

DHH Test Beam Report

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DHH Test Beam Report June 14th, 2013

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Test Beam Setup

Hardware Problems

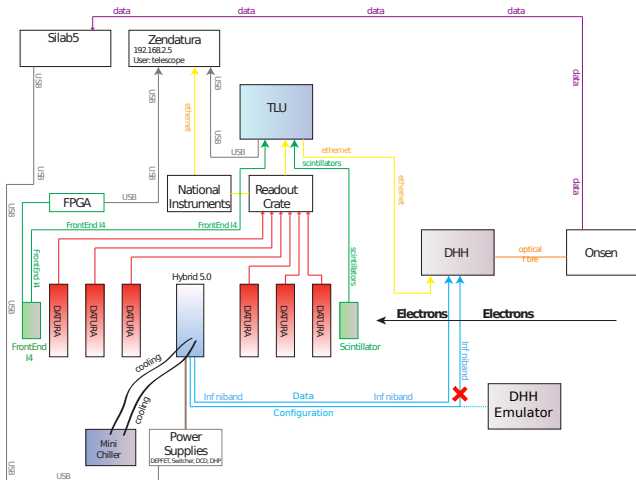
Firmware Problems

Slow Control

DHH System for EMCM Test



Experimental Setup



- in operation
10.05-12.05
- recorded approx.
2.5 Mio events
- mostly 8 DHP
frames per trigger
- DHP interface:
1.6 Gbps Aurora
- ONSen interface:
3.125 Gbps
Aurora



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- Broken Ethernet port on one of DHH card out of three taken to DESY
- Wrong deserializer clock for DHP
 - used 160 MHz instead of 152.652 MHz
 - correct clock was generated by programmable clock synthesizer, source of the DHP reference clock
- Problem with configuration of the clock synthesizer over I2C (probably not a hardware problem)
 - power cycle required to correct the bug
 - rare bug: only few times spotted before

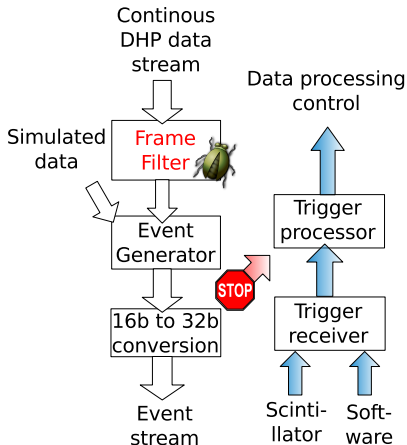
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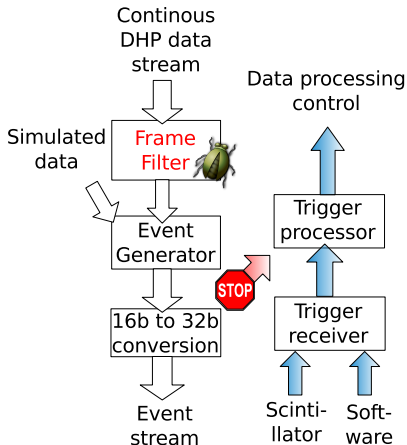
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Issues with Frame Filter

- Runs 254-273: double DHP frame headers hint at data loss
 - fixed in newer runs
- DHH header corruption if 1 clk cycle between DHP frames
 - can be fixed in offline software
 - firmware bug fixed



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Firmware Issues

- Last DHH firmware skips TLU triggers
 - will be investigated at HLL
- Wrong event size in some events
 - fixed in the frame generator module
- I2C master replaced with OpenCores.org implementation
 - no errors for a test over week-end
- Order of DHP words in 32b DHH words changed in newer firmware
- FPGA temperature measurements bug

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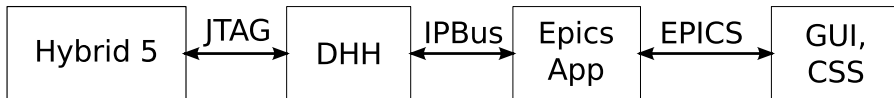
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Slow Control Scheme



- EPICS app as JTAG and IPBus driver
- IPBus: DHH control
- JTAG: DHP and DCDB control



Slow Control Issues

- DHP DCDB configuration issue
 - DCDB switch on/off via JTAG register works (power consumption increases)
 - data scrambled in full frame data
 - possible causes:
 - DHP-DCDB JTAG chain switched off if not used. Always on with DHH emulator
 - wrong configuration parameter
 - under investigation at the HLL

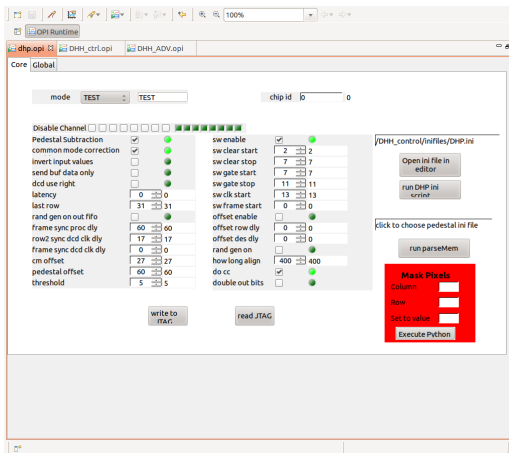


The screenshot shows the DHH GUI with the following sections:

- Runtime Status:**
 - ☒ DHP Channel up
 - ☒ DHP PLL locked
 - ☒ ONSEN Channel up
 - ☒ ONSEN PLL locked
- Control Buttons:**
 - Enable trigger (toggle switch)
 - Short RST
 - Read full frame
 - Long RST
- TLU Settings:**
 - Max bits: 32
 - TS2TUDEL: 0
 - TS2TADEL: 0
 - Clock slow down factor: 4
- DHP Trigger Settings:**
 - Trigger width: 4,096
 - Trigger delay: 0
 - FCk Length: 512
 - Timeout: 5,000
 - FCk strobe width: 5
 - Invert Trigger: ☐
- Statistics:**
 - DHP:**
 - DHP data counter: 1.07199004E8
 - DHP frame counter: 1451987
 - DHP data rate: 544,552 Bps
 - Trigger:**
 - Trigger counter: 265019
 - Trigger rate: 826
 - Missing triggers: 0
 - Missing trigger rate: 0
 - ONSEN:**
 - ONSEN data counter: 5.2399662E8
 - ONSEN frame counter: 1678632
 - ONSEN data rate: 1,250,416 Bps
 - Temperature: 228.12 C
- Other settings:**
 - RXEQMIX: 0
 - TCK Divider: 0
- Buttons:**
 - DCDB Settings
 - DHP Settings
 - DHH advanced

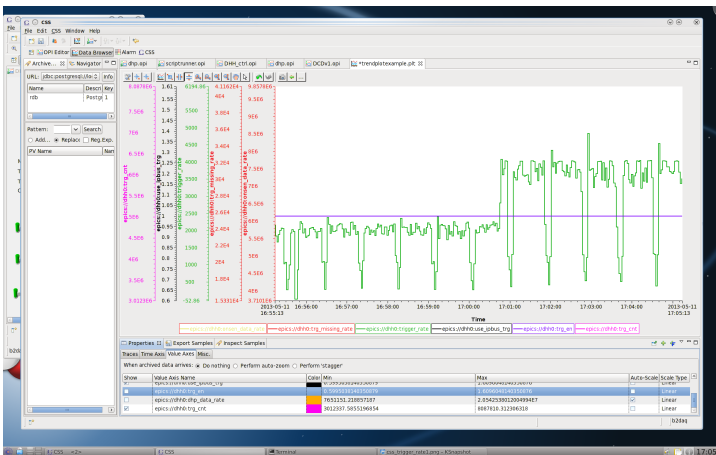


GUI Examples





GUI Examples



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DHH for Test Setups

- Data flow similar to the test beam firmware
- New: 4 DHP chips
 - round robin algorithm for read-out of the filtered frames
- Data read-out over IPBus
 - IPBus on the second ethernet interface
 - 10 Mbps on 100 Mbps network
 - data saved in ONSen format
- full frame read-out synchronous with trigger signal
- test JTAG on large chain



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Thank you!



Backup Slides



DHP Interface Timing Diagram



Technische Universität München

