



EMCM Substrate Testing

- Probe needle tests on ZMI-5 -

13. June 2013

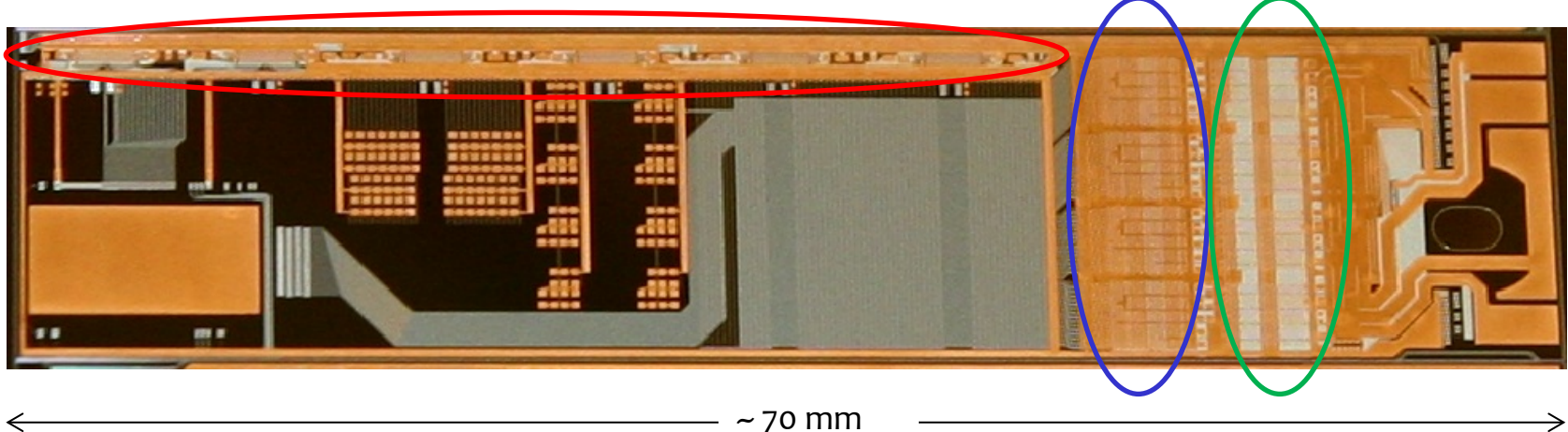
13th Int. DEPFET Workshop Ringberg 2013

Christian Koffmane for the HLL

● Electrical Multi-Chip Module – a reminder

- 3 metal layers on silicon substrate
- 2149 different electrical nets
- 4055 test pads (size down to $70\mu\text{m} \times 70\mu\text{m}$ and $50\mu\text{m} \times 100\mu\text{m}$)
- ~15k vias connecting the metal system in 3D (10k au1 to alu2, 5k alu2 to cu)
- Open and short test necessary before assembly of the ASICs
- Short test contains ~110k measurements per EMCM

Pads for control and read-out ASICs



● Iteration of EMCMs

Test-EMCM-1

- Produced on dedicated wafers (7 EMCMs per wafer, 3 wafer (+2 dummies))
- Results presented at B2GM March 2013 by Laci and summarized later in the session
 - All wafers show short to bulk – technological problem!

Test-ZMI-5

- 2 EMCMs per wafer – 6 wafers (+1 dummy)
- Slight design modification compared with Test-EMCM-1 (larger footprint of SWB decoupling capacitors)
- **Result of the Test-ZMI-5 EMCM testing will be presented now**

Test-EMCM-2

- Incorporates design changes learned from ZMI-5 (e.g. routing of SwitcherB control lines, fan-out of the DCDB analog inputs)
- Will be discussed in detail by Laci Andricek in the next talk

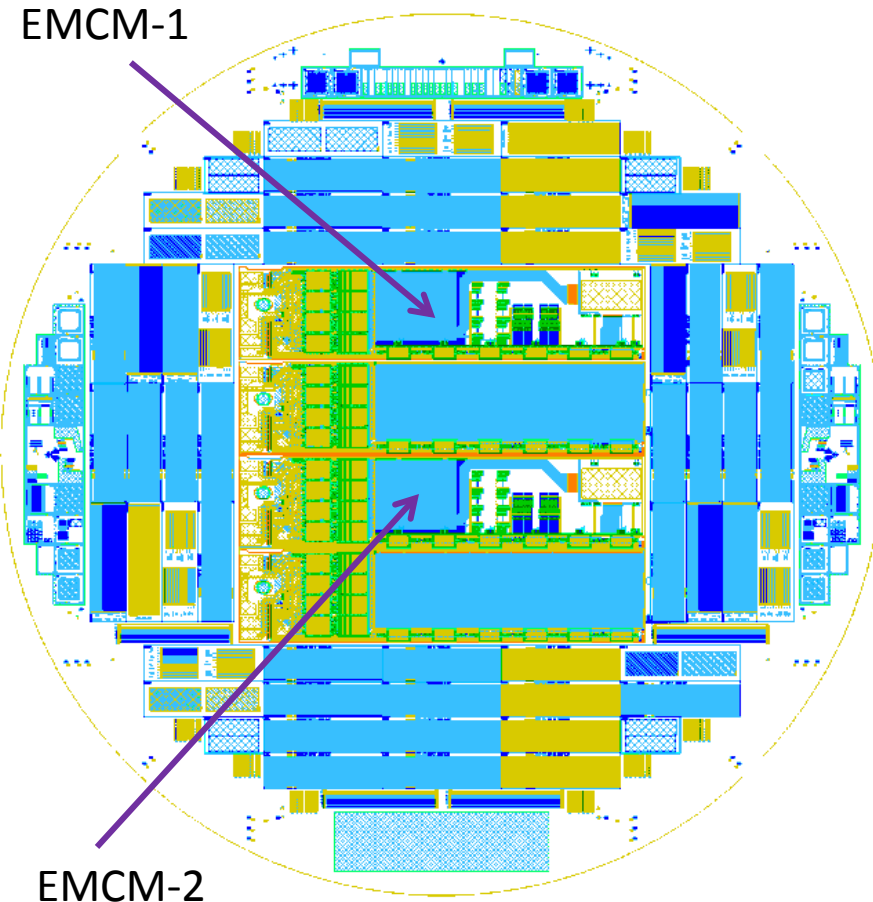
● Test-ZMI-5

- Goal of the project: optimize aluminum metal system (talk by Rainer Richter)
- 6 wafers with various inter-level dielectrics
- Many test structures + 2 EMCMs per Wafer

Wafer A1 – lithography test wafer

Wafer P1, P2, P3, P4, P6 showed good performance in the dedicated Alu1 – Alu2 test structures (EMCM end-of-stave was not tested before copper)

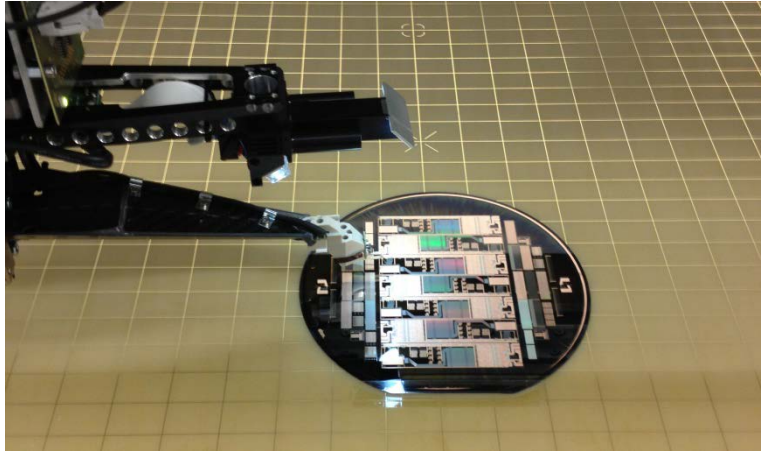
Wafer P5 had problems in the Alu metal system (therefore not tested)



● Test System Requirements

- High accuracy (several microns) and large working area (DUT 70mm x 16mm, wafer \varnothing 15cm)
 - Soft landing of the probe on Cu bump-bond pad and Alu wirebond pad
 - Software to generate a test program which checks for opens within one net and shorts of neighboring nets (3D)
- Cascade Automated Probe Head (PH510, PH600) which is often used in IC probing don't fulfill the requirements (mainly regarding the working area)
- Alternative: Test Equipment used in PCB and package industry
- We found the company **atg Luther & Maelzer (part of DOVER Corporation)** in Wertheim, Germany, which produces such test systems

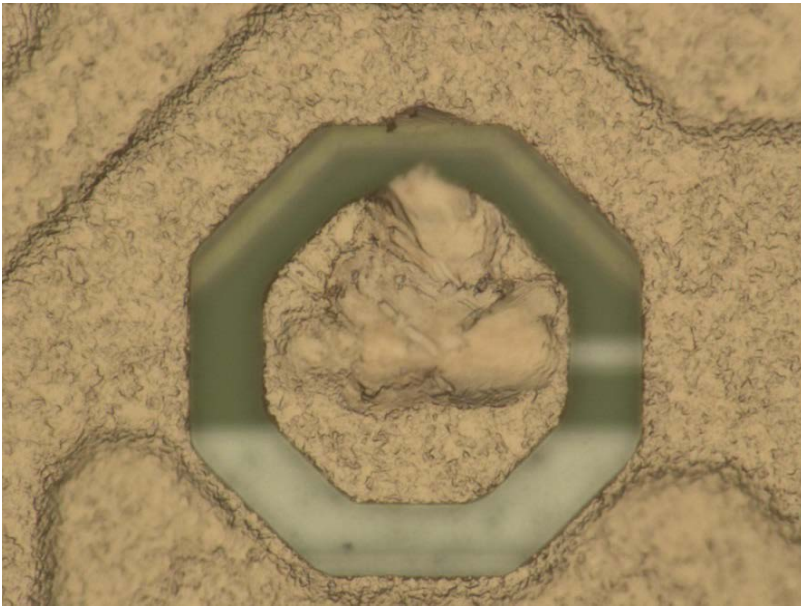
● Test of ZMI-5 Wafer at **atg Luther & Maelzer**



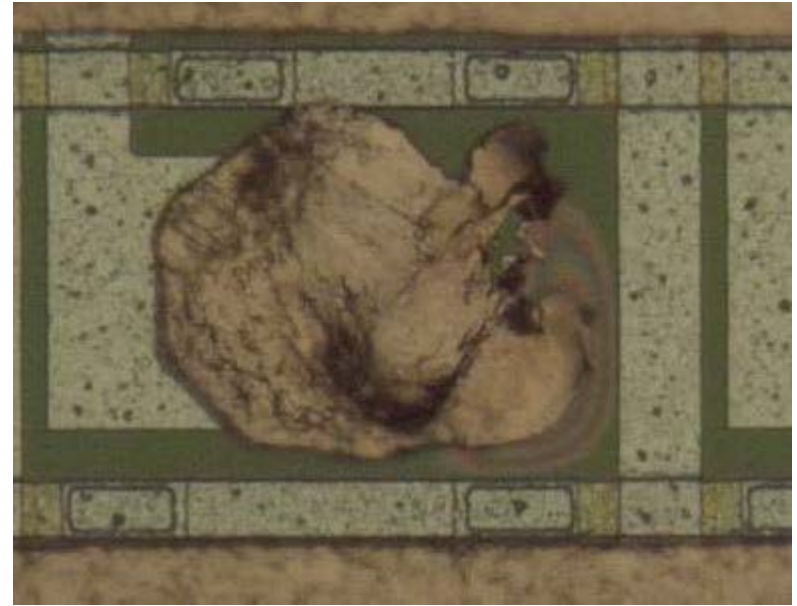
- **Wafers P1, P2, P4 and P6** measured in cw19 and cw20
- 4 test heads were installed during the test, probes with touch down detection used, test time for 2 x EMCs is 6h
- Test area 610 mm x 510 mm, Pad / Pitch = 36 μ m / 100 μ m
- Software to generate test program available (based on gerber file format)
- Test system at **atg Luther & Maelzer** placed in normal office space (no cleanroom, no temperature control)

● Alignment Accuracy & Stopping Speed

- Initial problems in cw19 in terms of accuracy and stopping speed of the probe
- Test of ZMI-5 Wafer A1 and P1



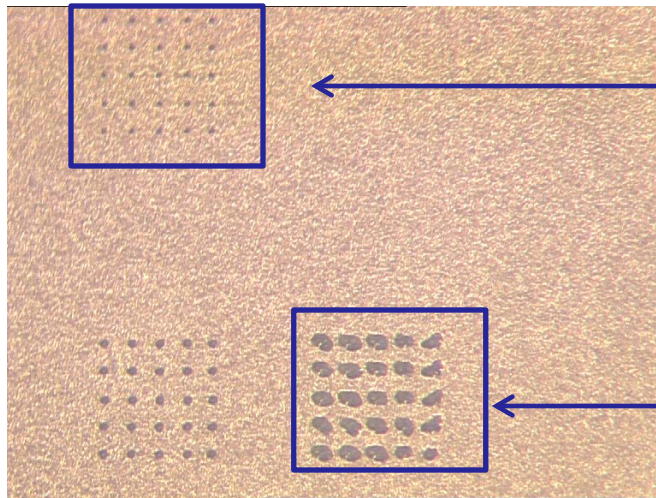
A7 machine has non optimal accuracy
Drifts due to the temperature changes



Non optimal stopping speed of the
probe heads & high number of touch
downs: up to 2k for individual pads

● Alignment Accuracy & Stopping Speed

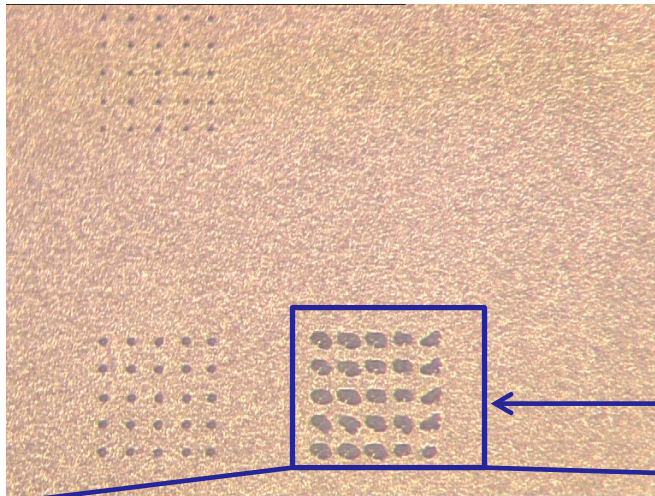
- Optimized speed of the probe heads (week20)
- Calibration of the A7 before each run
- Best results in terms of accuracy of the needle position during the night run (wafer P4)



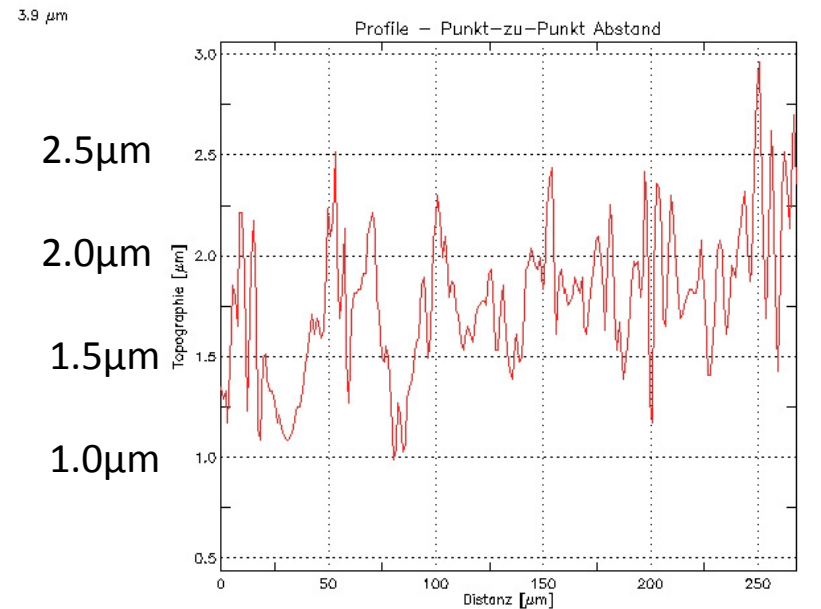
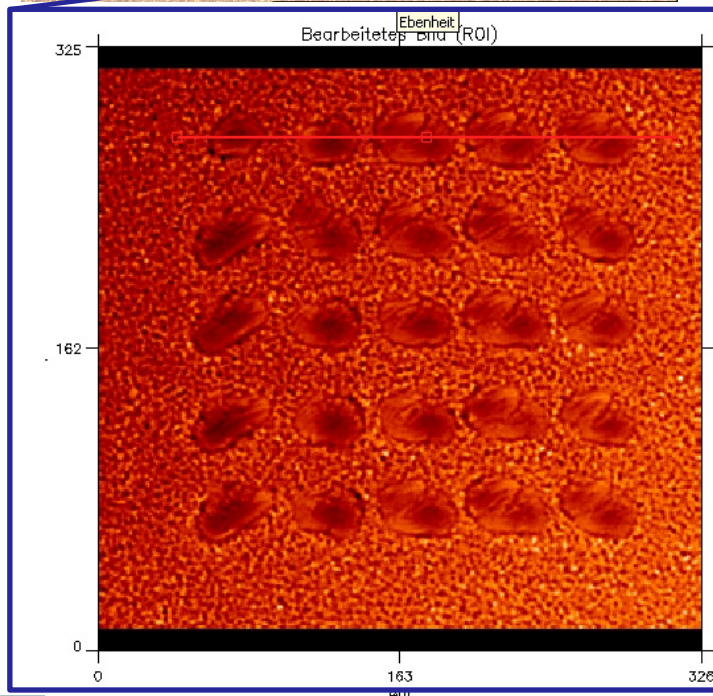
100 x touch down with optimized settings
(week 20)
(stroke, pressure and accuracy set to 5)

100 x touch down with non-optimized
settings from the first week (week19)

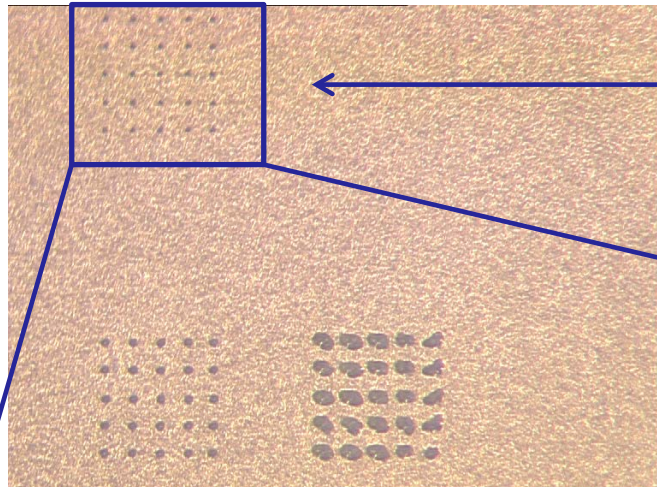
● Alignment Accuracy & Stopping Speed



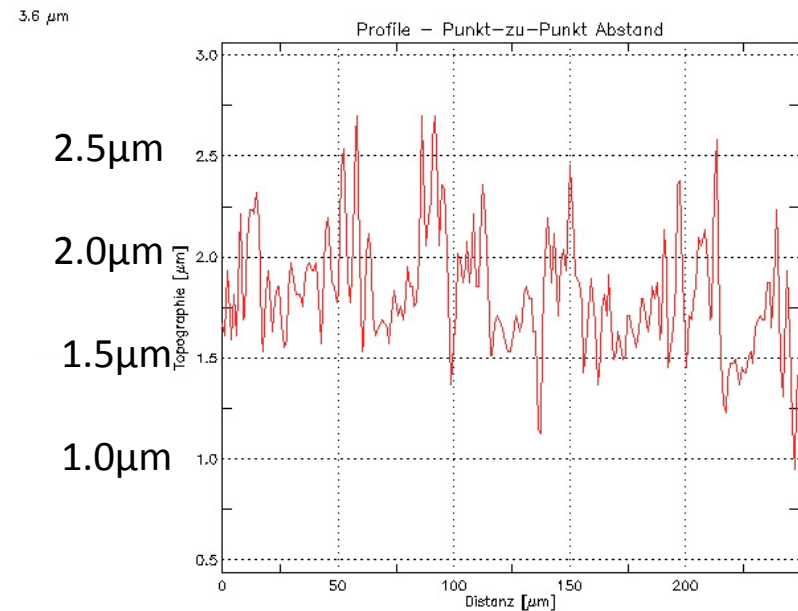
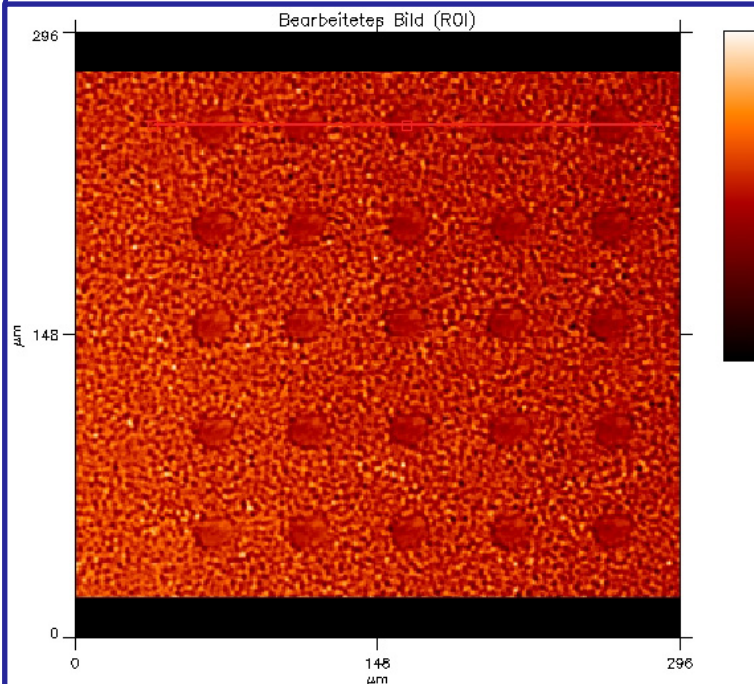
100 x touch down with non-optimized settings from the first week (week19)



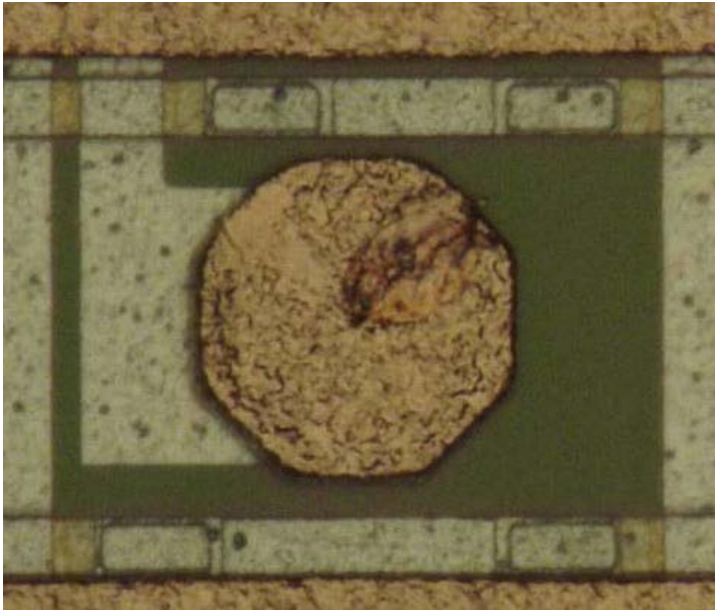
● Alignment Accuracy & Stopping Speed



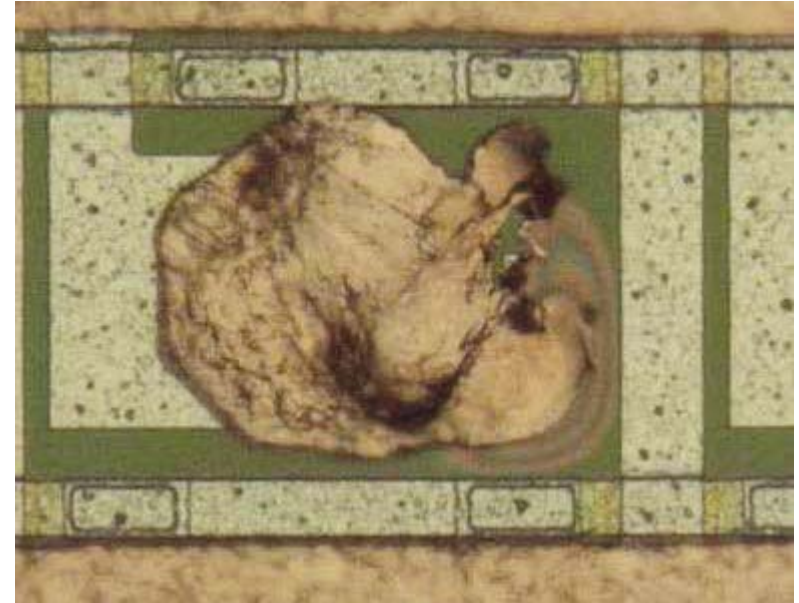
100 x touch down with optimized settings
(week 20)
(stroke, pressure and accuracy set to 5)



- SwitcherB Pads with High Touch Down Count



Improved stopping speed and better xy accuracy; number of touch downs ~2k too



Non optimal stopping speed of the probe heads & high number of touch downs: up to 2k for individual pads

● ZMI-5 EMCMs Electrical Failure Types

- 4 different failure types have been found on the ZMI-5 wafers
 - Opens
 - Low ohmic shorts (5Ω to $\sim 80\Omega$)
 - Mid ohmic shorts (in the $k\Omega$ range) - after cleaning all of these shorts disappeared
 - High ohmic shorts (in the $M\Omega$ range)

● Opens (discontinuities)

Wafer	Number of opens	Location of short
P1 – EMCM-1	23	SWB outputs, DEPFET to DCDB
P1 – EMCM-2	0	-
P2 – EMCM-1	0	-
P2 – EMCM-2	Not tested	
P4 – EMCM-1	0	-
P4 – EMCM-2	1	SWB output
P6 – EMCM-1	2	SWB output, DEPFET to DCDB
P6 – EMCM-2	2	DCDB (#2) output, DCDB(#4) input

- All opens showed up in connections which include vias from Alu2 to Copper placed just above of Alu1-to-Alu2 vias
- Suspicion: BCB (dielectric) still remaining between Alu2 and Copper
- Cross-section of wafer P1 in preparation

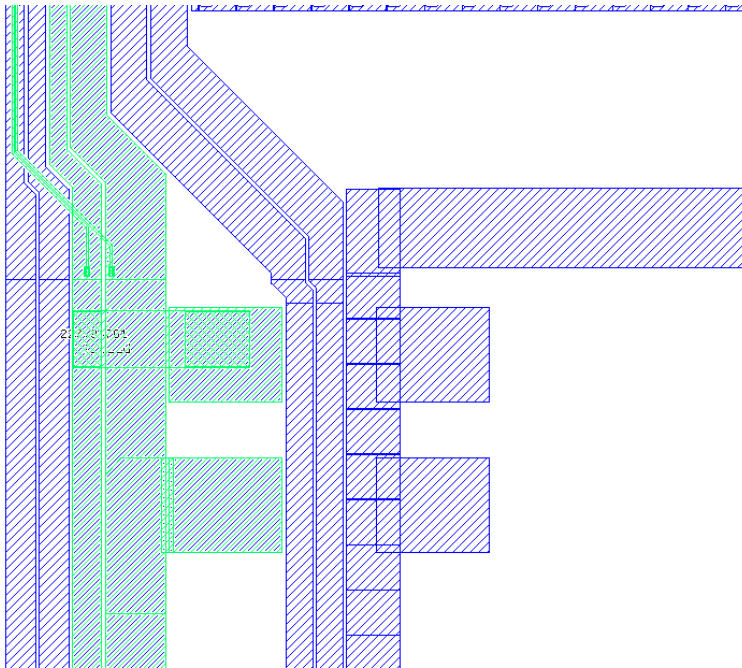
- Shorts – low ohmic shorts

Wafer	Number of shorts	Location of short
P1 – EMCM-1	15	SWB control lines
P1 – EMCM-2	Optical inspection	SWB control lines
P2 – EMCM-1	4	SWB control lines
P2 – EMCM-2	Optical inspection	SWB control lines
P4 – EMCM-1	0	-
P4 – EMCM-2	2	SWB control lines
P6 – EMCM-1	1	GateOn1 – GateOff
P6 – EMCM-2	0	-

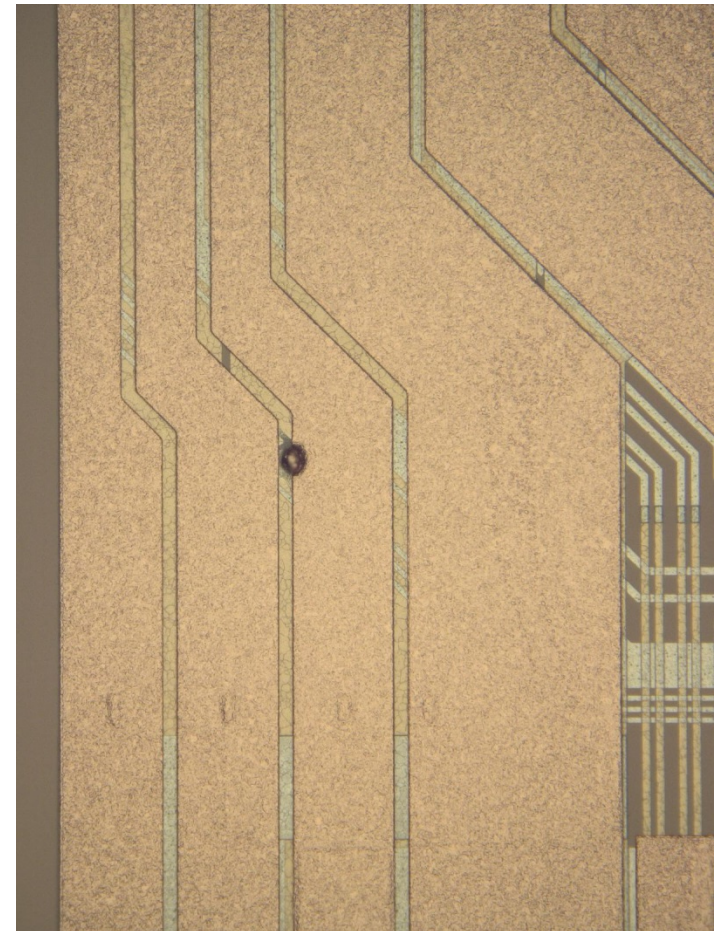
Wafer P3 showed the short in the SWB control lines in the optical inspection too and was not tested at **atg Luther & Maelzer**

● Wafer P6 – EMCM-1

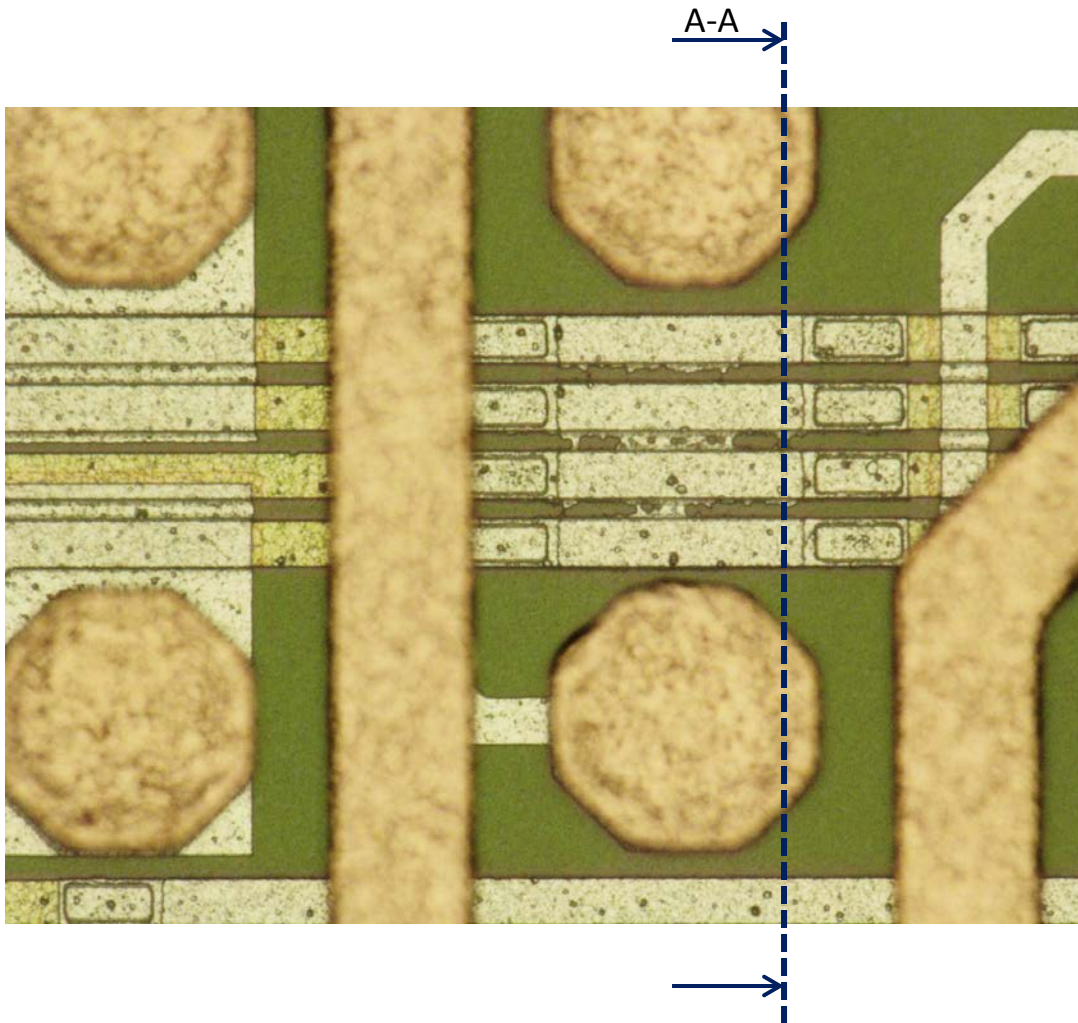
GateOn1 – GateOff short



Particle or below Cu?

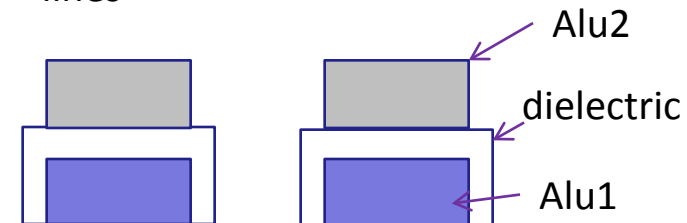


● Low Ohmic Short in the SWB Control Lines



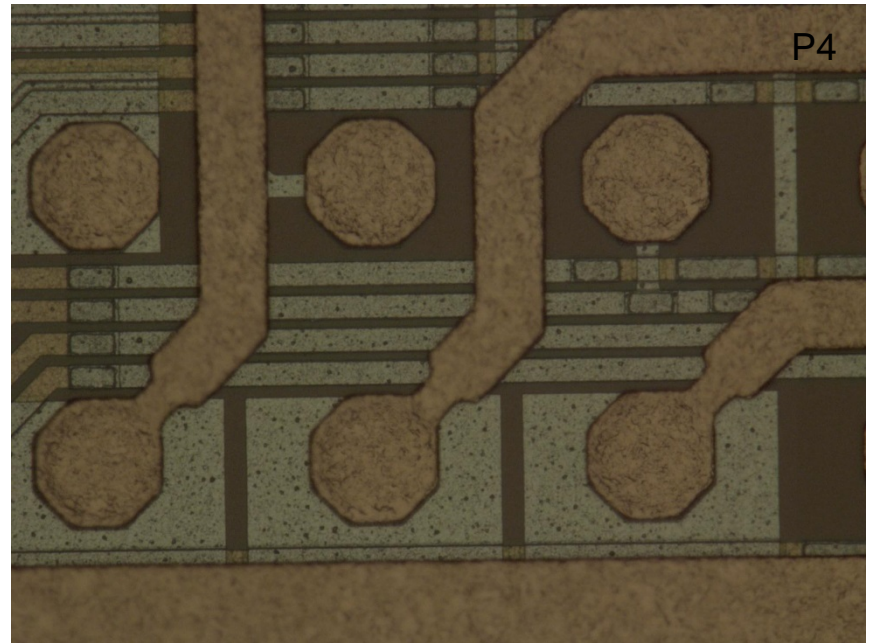
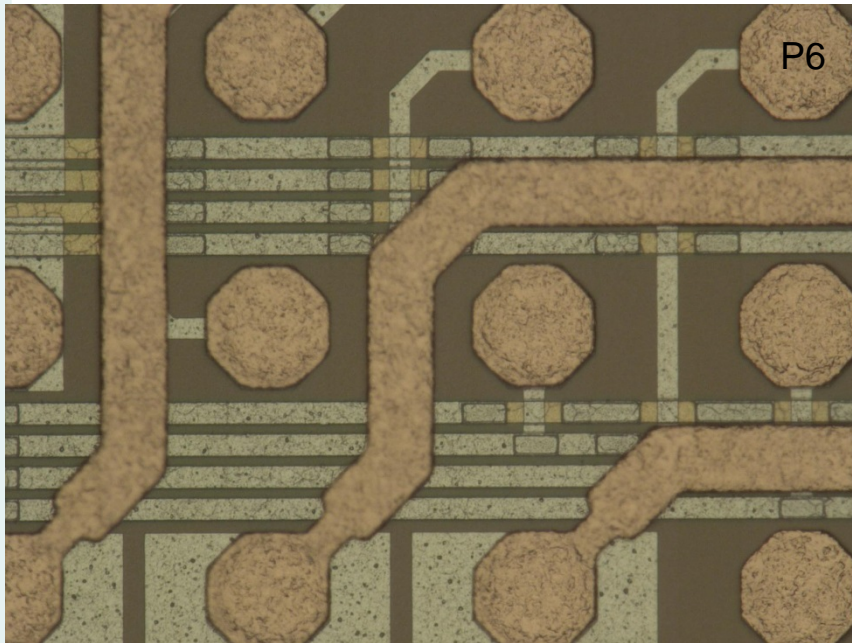
- Stack of Alu1 +Alu2 used to decrease resistance of the control lines of switchers had problems in production
- Differs from wafer to wafer

Schematic cut A-A of the Al1 +Al2 lines



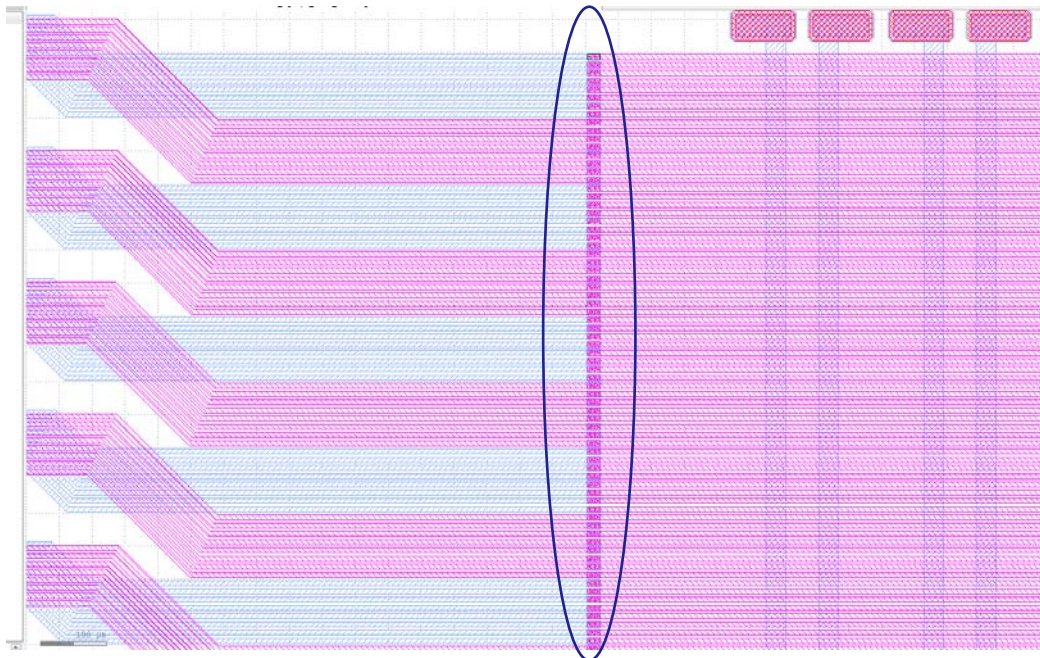
- Test-ZMI-5 Wafer P4 and P6

Optical inspection done on all wafers - this problem could not be identified of wafers P4 and P6 - still significant area under Cu



● High Ohmic Shorts

- Present on all tested wafers
- Test ZMI5 project had additional Polysilicon layer and Contact 1 mask to increase topology on Alu1-Alu2 test structures
- By mistake contact 2 openings (via Alu1-Alu2) were transferred into contact1 mask, resulting in connections of all drain lines to bulk



Since high ohmic material was used one can use these EMCs (in dark dynamic resistance of about $20\text{G}\Omega$ measured)

● Summary & Outlook

3 EMCMs can be used for further assembly

- Wafer P4 EMCM-1: no open, no low ohmic short
- Wafer P6 EMCM-1: 2 x opens, 1 x low ohmic short, still can be used for one set of ASICs (1xSWB, 1xDCDB, 1xDHP)
- Wafer P6 EMCM-2: 2 x opens, no low ohmic short, (opens in two DCDB-DHP channels)

Things improve in **Test-EMCM-2**

- change DEPFET drain line fanout (all lines of in Alu2, allowing the punch through contact to be placed below drain lines)
- change of layout of SWB control lines Alu2 above Alu1
- change of staggered vias or BCB development

Probe placement accuracy over time has to be improved → atg Luther & Maelzer will provide a S2 machine for testing of Test-EMCM-2 (better control of the z-axis, specified for smaller pads 10μm, and better stability over time and shorter test time)